

Focal Plane Technologies for LSST

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ABSTRACT

The baseline design for the Large Synoptic Survey Telescope (LSST) requires a detector mosaic of over 2 Gigapixels covering a 55 cm diameter focal plane with 0.2 arcsec sampling. The camera and detector package for this telescope will benefit greatly by utilizing advanced concepts not normally required for astronomical telescope instrumentation. For the detector assembly, these concepts include low-cost, back illuminated CMOS or CCDs detectors with integrated electronic modules, curved detectors which would allow fewer but larger individual sensors, small pixels which maintain high MTF and full well capacity, anti-blooming techniques, fully-butttable packaging, and near room temperature operation. The camera may require a low thermal conductance gas-filled dewar to reduce atmosphere loading on the window, interchangeable and compact optical filters, and a flexible internal shutter. In this paper we discuss these issues relating to LSST focal plane technology.

Keywords: CCDs, CMOS imagers, focal planes, telescopes

INTRODUCTION

The Large Synoptic Survey Telescope (LSST) is planned to be an 8.4 meter, 3 degree field of view survey telescope¹. The optimized 3-mirror Paul optical design places the camera within the beam affording little room for filter and shutter mechanisms. The requirement of 0.2 arcsec pixels for adequate sampling implies the need for a focal plane of over 2 billion, 10 micron pixels. Due to focal plane curvature, we expect to utilize more than 1,000 1500x1500 pixel sensors. New flat focal plane optical designs now exist which would require the same number of pixels but with fewer individual detectors. Such a project clearly requires careful optimization of the focal plane detectors, their mounting, and the required readout electronics. In this paper we discuss the LSST focal plane and the developmental efforts underway and planned that are required to realistically manufacture such a technologically challenging instrument. Others papers^{2,3} in these proceedings discuss more general instrument concepts.

Dewar

We show the proposed optical layout in Figure 1. The LSST dewar window is 1.3 m in diameter. If the dewar is to be evacuated, it will have an atmospheric load of approximately 14 tons. This would require the window to be much thicker than desired for optimal optical performance in order to remain rigid under such a force. This can be avoided by back filling the dewar with a low thermal conductivity gas such as Xenon. An outer can with filter and shutter mechanisms may be filled with dry nitrogen.

Cooling requirements are not severe for the detector mosaic. The criterion is that the dark rate be less than the sky photon rate in the darkest filters. We estimate that even for the U band filter photon rates will be $> 1.5 \text{ e}^-/\text{pixel}/\text{sec}$. With MPP CCDs or current CMOS devices, dark rates less than this can be achieved at a device temperature of -20 to -40 C. It follows that in the worst case of a 10 second exposure in a dark band a dark current plus read noise of $\approx 4 \text{ e}^-$ rms will be acceptable. At this

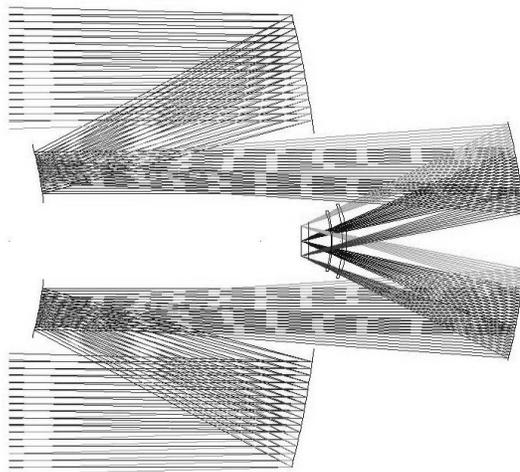


Figure 1. The optical layout of LSST, from reference 1. The focal plane dewar is contained within optical beam and must be minimized in size.

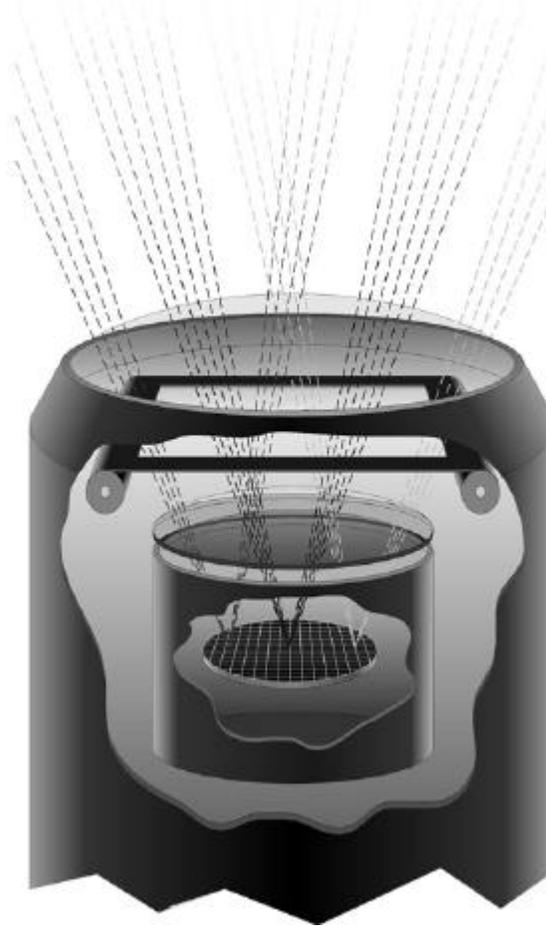


Figure 2. The Xenon filled inner dewar of the LSST camera protects the detector array. Outside this dewar is a dry nitrogen filled can housing the filter and shutter mechanisms.

and stability, safe detector assembly, maintenance access, and electrical I/O. It is likely the detectors will not be individually replaceable, but assembled in interchangeable *modules*. The size and design of such modules is not yet determined, but may consist of assemblies which are two devices wide and of arbitrary length such that all detector I/O is accessible by at least one edge. Alternatively, true 4-side butttable packaging developments are underway which bring out detector I/O underneath each module. In this case, the modules need only be a reasonable size for maintenance exchange. The cooled base plate on which the modules will be mounted presents thermal, electrical, and mechanical challenges. It must be mechanically stiff enough to have less than 3 microns gravity induced flexure. Its thermal conductance (area conductivity) must be sufficient to cool the modules while providing for voltage supply and digital data lines to the modules.

For the detectors themselves, we will examine several CCD and CMOS technologies. It is unlikely that the CMOS arrays developed for the commercial industrial and HDTV market will be of use for LSST due to their limited low light level performance. However, recent optical CMOS detectors hybridized to multiplexers promise self-shuttering, rapid readout, and high quantum efficiency. A further advantage of CMOS imagers is the much simpler interface compared to CCDs, which often includes integrated analog to digital conversion (A/D) and very low power dissipation. There are also several promising CCD technologies, but the back illuminated devices needed for this project must be fabricated at

temperature, the thermal losses due to the gas-filled dewar are acceptable. We show in Figure 2 a conceptual design of the dewar.

Shutter and filters

Since the camera is within the optical beam the cross section of the camera assembly is constrained, prohibiting conventional outboard filter changing and shutter mechanisms unless a cassette mechanism is used. Whether a shutter is even necessary depends on the nature of the detectors chosen for the mosaic. CMOS imagers can be self-shuttered via a rolling read or internal pixel structures. While CCDs have been developed in which a horizontal electric field can pinch off charge collection, this fails for red wavelengths where photons penetrate many tens of microns. A CCD focal plane will most likely require some type of shutter. Rolling (flexible) shutters, LCDs, and flip-type shutters will all be investigated. Lawrence Livermore National Laboratory has recently designed a rolling-type shutter which is capable of providing uniform exposures over the entire LSST focal plane.

The filter change mechanism is also a serious challenge. The science drivers require several bandpass exposures. Some science can settle for long filter change times, while other projects require that at least a few filters be available within minutes. Compact filter change/storage designs have been studied for the camera. In particular, a solution is now being studied in which up to four filters are stored in the outer chamber of the dewar. Developing a filter mechanism within the LSST mechanical constraints will be a major technological undertaking.

FOCAL PLANE TECHNOLOGIES

The 55 cm LSST focal plane will be populated with as many pixels as possible, each sampling 0.2 arcsec. The major issues which will be encountered when developing such a massive detector package include: thermal design, mechanical flatness

lower cost than previous generations. CCDs, particularly mass-produced small megapixel devices, have some attractive features for paving the LSST focal plane.

There are several factors leading to the need for relatively small individual detectors. A non-flat optical focal plane would accommodate flat devices smaller than about 2 cm per side. Semiconductor device yield decreases as area increases, driving reduced detector size. The readout time requirement, based on exposures as short as 10 seconds, is 2 seconds. With current or near-future amplifiers, low noise reads (5 electrons) of either CCDs or CMOS devices can be performed with correlated double sampling at individual amplifier rates of about 1 Mpix/sec. This leads to detectors of roughly 2 Mpix.

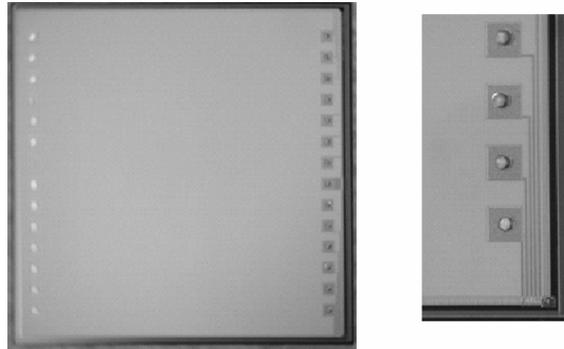


Figure 3. A fully buttable CCD imager built as a technology demonstration for a closely butted focal plane such as LSST. The bond pads are on top of the pixels. Gold bumps have been applied to the pads, as seen on the right, for hybridization before back illumination processing.

As a way to minimize the gaps between the individual modules and sensors, we are presently exploring detector packaging techniques which will allow the use of 4-side buttable devices using semiconductor industry standard packaging technologies. This development would limit the inter-device gaps to the non-imaging silicon of each detector, which is dominated by clock busses, amplifiers, and, most significantly, I/O bonding pads. With the recent industry wide trend toward smaller I/O structures, 50 micron bond pads are possible. In Figure 3 we show an experimental CCD we have custom fabricated with the bond pads on top of the pixels, allowing for edge gaps as small as 100 microns⁴. An LSST fill factor of over 95% can be obtained with such techniques.

There are several optical detector technologies which have been developed in the past few years which are available for making integrated detector/electronics modules. Our goal is that each module contains the clocking and readout electronics, including correlated double sampling and A/D, and that the detector exhibit high quantum efficiency over the range 0.3 - 1 micron, 4-side edge buttability, and low noise. Self shuttering capability is important but not absolutely required. We describe below the most likely possibilities for the required sensor technology.

Back illuminated CCDs

Because of the requirement for high QE, we consider only back illuminated devices. State-of-the-art large format CCDs are now 4kx4k pixels, 60 mm per side^{5,6}. Such devices are expensive, however, and relatively slow to read out through the limited number of amplifiers typically found on scientific grade devices. If the focal plane is curved, the large area detectors would also need to be bent to match focal plane curvature. While industrial vision CCDs now can now be obtained with 128 or more amplifiers, large number of smaller CCDs actually presents a better solution for reasons previously discussed.

The CCDs could be flip chip bonded to an active hybridization device containing clocking and signal processing, as shown in Figure 4. Several variations of this theme are possible, including hybridizing to intermediate ceramic supports, attaching application specific integrated circuits (ASICs) or integrated video and driver components to the underside substrate, or using isolated vias in active circuitry itself. The development of a custom LSST ASIC, for example, presents a very compact means of obtaining a digital focal plane. The ASIC could contain the same level of circuitry now found on active pixel CMOS imagers, including a correlated double sampler (CDS), a timing generator and clock drivers, and fiber optic interface. The development cost of such a custom device is prohibitive for many projects, but

would be a very small fraction of the focal plane cost for LSST and could lead to very significant mechanical, electrical, power, and thermal savings. Alternatively, these individual functions might be obtained from a few integrated components which can be bump bonded or surface mount attached to the detector module or intermediate I/O routes within the dewar.

A significant issue for CCDs is the control of charge blooming from bright stars. Deep wells, anti-blooming measures and the use of many smaller devices will all be important control measures. Considerable progress has been made in recent years to improve the full well capacity of smaller pixel devices. It is reasonable to expect over 200,000 electrons full well capacity for 10 micron pixels as 160,000 electrons has been demonstrated for 8x8 micron pixels⁷.

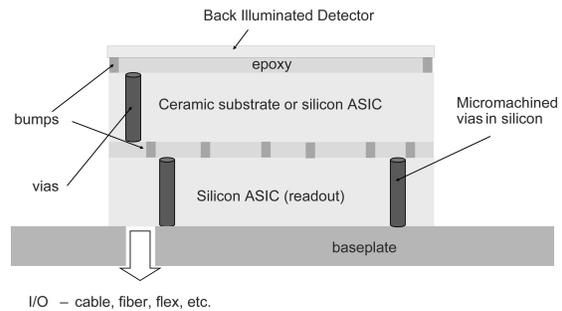


Figure 4. A schematic view of a possible LSST detector, integrating the imaging sensor and the readout electronics.

In a CCD focal plane, anti-blooming capabilities (which often reduce full well) may be incorporated. Alternatively, anti-blooming clocking schemes may be used during integrations. To avoid excessive data loss from blooming due to the brightest stars in the field, a large number of smaller format devices will again be preferred.

Other sensor technology to be studied includes hybrid CCD imaging arrays with CMOS readouts. These structures are produced by bump bonding the equivalent of an array of CCD columns onto a CMOS readout with one “readout pixel” per CCD column. Such Hybrid Imaging Technology (HIT) is being pursued at JPL and may prove advantageous for LSST due to the high fill factor and inherently integrated electronics.

Backside processing of over 1000 CCDs is a daunting and potentially expensive task for any one project. Methods to reduce cost have been under study at the University of Arizona Imaging Technology Laboratory for the past few years. While certainly a very large number of devices are required for this project, the CCDs themselves could be manufactured today. The DC shorts yield of several fabrication lines is now over 50%. If 50% of these unshorted thick CCDs are of astronomical quality, a mature lot run will yield about 25% useable devices from 150 mm silicon wafers at a modern facility. Assuming a conservative 50% thinning and packaging yield, the final thinned device yield would be about 10% of the starting lot. This would then require about ≈200 wafers to be fabricated with 50 devices per wafer, after one or

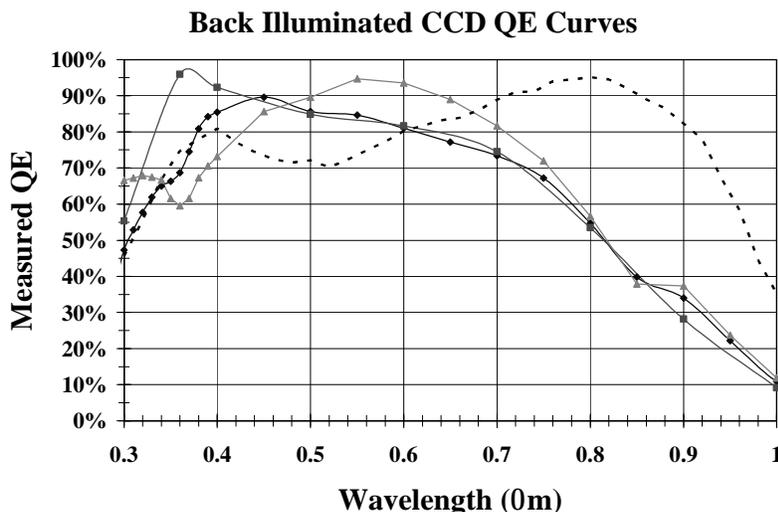


Figure 5. The measured QE of several back illuminated CCDs. The dashed line represents a red-enhanced device from MIT Lincoln Labs while the others are from four separate manufacturers but processed at the University of Arizona. The differences in the QE are due to variations in device thickness (because of epitaxial layer differences) as well as to the applied antireflection coatings.

two engineering and test lots. DC and AC (imaging) wafer probing will allow rapid feedback to the fabricator on device quality and yield. This fabrication project is of the same order as several previous space-based CCD development efforts. As a demonstration of typical CCD performance, we show in Figure 5 the measured QE of several CCDs from various manufacturers. The enhanced red QE from the MIT/LL device represents a nearly ideal LSST QE curve. The CCDs shown in the figure from the U of A were hybridized to an inactive silicon substrate, but in a manner consistent with LSST focal plane requirements. Replacing the substrate with an ASIC or ceramic carrier on which CDS and clock drivers have been attached is a relatively straightforward modification of the existing process.

Monolithic CMOS imagers

An alternative focal plane to traditional CCDs is an array of CMOS imagers. These silicon detectors are rapidly replacing CCDs in the low-end consumer markets, and much progress has been made toward reducing their inherent noise sources. Less than ten electron readout at 200 kHz seems likely in the near future. The tremendous advantage of a CMOS array for LSST would be the great reduction in the electronics needed to control the focal plane. CMOS imagers essentially need only a single low voltage DC power source and input clocking patterns to produce a video output stream.

There have been huge advances in this area in the past two years, motivated by the HDTV imager market. Cost is low and noise performance is improving rapidly. The major problem is the non-filled area due to the need for 3-4 transistors within each pixel. Additional transistors may be required for self-shuttering ability. We note that with modern design rules continuously shrinking, the fill factor naturally improves over time because the pixel area needed for transistors is reduced. Custom CMOS device exists today with fill factors as high as 80%. Another issue is the relatively low QE in the near-IR, due to thin epitaxial silicon often used for CMOS devices. For a custom runs of devices, as would most likely be required for LSST, this is not a significant issue since the starting silicon material may be specified. In this case, near-IR QE would be similar to CCDs, except for fill factor.

Back illuminated monolithic CMOS devices are also an option to be studied. These devices are being successfully thinned at the University of Arizona. We have successfully thinned CMOS imagers built using p-on-p+ silicon and are developing processes to thin n-type and bulk p-type silicon devices. Backside processing allows the same high broadband QE as CCDs. 100% fill-factor can potentially be obtained if internal doping implants are made to direct photogenerated electrons to the photodiodes. Several manufacturers are currently experimenting with this processing. We are optimistic that considerable resources will be applied to backside enhancement processes for CMOS devices not only for higher QE, but for the potential to achieve very high radiation tolerance due to the reduced silicon cross-section. Such technology developments, funded by the military and industrial vendors, will surely benefit astronomical devices.

Hybrid CMOS imagers

Hybrid CMOS imagers, in which a detector is bump bonded to a multiplexer/ASIC, have been developed for IR and remote sensing applications and are now a mature technology. Recently, 2Kx2K versions have been developed for the IR and versions for visible applications are available^{8,9}. As an example, Rockwell Scientific has announced their Hybrid Visible Silicon Imager (HyVis) which consists of an AR coated, 100% fill-factor silicon detector hybridized to a CMOS multiplexer readout. Pixel sizes are currently 18 microns or larger and the readout circuitry is the HAWAII2 MUX used for IR astronomical applications (<http://www.rockwellscientific.com/imaging/hyvisi>).

This hybrid CMOS technology is now advanced to the state that it appears to be competitive with CCDs for an application such as LSST. Silicon detector material can be processed for very high and stable QE and then bump bonded to the CMOS readout. New amplifier designs have reached just a few electrons read noise by increasing the node sensitivity using modern design rules. 16-bit ADC's exist which are much smaller than the area of the LSST detector, allowing for the inclusion of on-chip CDS circuits. Custom readouts for the required detector which include ADC, CDS, and all drivers can reasonably be expected based on this technology.

SUMMARY

It is clear there are many options for LSST detectors. Both CCD and CMOS technologies have advantages and limitations. Because of the large scale of this project, and the relatively long lead time available, it is critical to study the possibilities of customizing the sensors in ways not previously attempted for ground-based astronomical projects. The design and development of custom CMOS imagers and ASICs, for example, would often seem too expensive for previous single projects. Developing new manufacturing techniques for large quantities of smaller backside CCDs may

also prove cost effective. An important first step is a careful specification of the detector requirements, as determined by science requirements. A first attempt at this is shown in Table 1. None of these required device characteristics are unattainable today; they are only not available all in one detector. Over the next few years the sensor development effort for LSST will study and push for the development of the technologies which will enable the desired LSST focal plane imagers to be available when needed.

Table 1. Preliminary LSST Detector/Module Specifications

Specification	Value
Array format	1500 x 1500 – 4096 x 4096
Pixel size	11 ± 2 microns
Read rate	≤ 2 seconds
Data/driver format	DC input, 16-bit digital serial data output with CDS
CTE (if CCD)	≥ 0.99999
Noise	$\leq 7 e^-$ rms, $< 30 e^-$ fixed pattern
Full well	$\geq 100,000 e^-$ at non-linearity onset
Non-linearity	$< 5\%$ from $100 e^-$ to full well
Flatness deviation	≤ 3 microns p-p @ operating temp of $-40c$
Parallelism	≤ 3 microns (image surface to package backside)
Packaging	4-side buttable
Minimum QE	60% @ 400 nm, 80% @ 600 nm, 70% @ 800 nm
Photo Response Non-Uniformity	$\leq 5\%$ p-p (relative) measured over entire device, (50x50 pixel blocks, 50 nm bandpass)
QE stability	$\leq 1.0\%$ p-p (relative) over 1 hour, $\leq 2.0\%$ p-p (relative) over 1 month
Dark signal	$\leq 2 e^-$ /pixel/sec ($-40C$)
Dark Signal Non-Uniformity	$\leq 5\%$ p-p
Interference fringing	$\leq 5\%$ @ 800 nm, $\leq 20\%$ @ 900 nm, $\leq 50\%$ @ 1000 nm, (p-p, 10 nm bandpass)
Number of bright pixels	≤ 1000 ($\geq 10x$ mean dark current)
Number of dark pixels	≤ 1000 ($\leq 80\%$ mean QE)
Number of traps	≤ 10 ($\geq 200 e^-$ trapped)
Number of bad columns	≤ 5 (bright, dark, or trapped over ≥ 10 pixels)
Operating temperature	-40 to $-30 C$
Storage temperature range	$-55 C$ to $+135C$
Temperature cycling	$-55 C$ to $+30 C$, 150 cycles over lifetime

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