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Technology of large focal planes of CCDs

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ABSTRACT

e2v technologies has demonstrated capability in the supply of state-of-the-art CCDs for large area scientific focal planes. We discuss technical developments and lessons learnt from the manufacture and supply of large-format CCDs. Several large mosaics have now been built or are under construction using e2v sensors - these include CFHT Megacam, ESO VST, SAO Megacam, Kepler, and GAIA. Design, assembly and operational issues are presented.

Keywords: CCD, focal plane, alignment, power dissipation

1. INTRODUCTION

CCDs have been widely used for ground-based astronomy for over two decades, and within the last decade we have seen many focal plane mosaics being put into use. Some particularly large (30 to 40-chip) arrays are now in use or under construction on the ground. The technology developments needed for these instruments have been developed further for space-based instruments, and several large focal planes of CCDs are now in construction. Here we shall show how the technology has evolved, give examples of specific features, and discuss construction and use of large focal planes.

2. PACKAGE DESIGN

2.1 INTRODUCTION

There are many ways to package silicon depending on the application, ranging from simple ceramic packs to complex metal/ceramic hybrids and others. Ceramic is often a simple and economical default, but has relatively poor dimensional control, which is often a disadvantage for precision focal planes where flatness or accurate alignment is required. On the other hand metal packages, such as Invar, can be accurately machined and are quite well expansion-matched to silicon but have a higher mass. Several newer generation materials are in development for lightweight optics/focal planes, and some of these can be useful as CCD carriers. Recently techniques for processing Silicon Carbide have improved so that it is practical to use this for lightweight precision package and focal plane assemblies. It has many advantages, which include- good expansion match to silicon, low density, high strength, and good thermal conductivity. We believe that the GAIA CCDs will be the first to use this material, in association with a SiC instrument structure[1].

We will discuss a few techniques for achieving precision packages and assemblies. Although it is not appropriate here to describe all of our design, assembly, and measurement capability we shall present examples that illustrate applications that are demanding either in quantity or quality of focal plane.

Single chip applications usually pose least difficulties, and a simple package style often suffices; here we list a few examples- ceramic for simplicity and economy, ceramic with metal base for improved flatness, metal base with ceramic & PGA connections, metal base with flexi-circuit connections.

2.2 PRECISION PACKAGES

Devices such as the e2v CCD44-82 and CCD42-90 have been considered a standard design for at least 5 years, with a large number of installed devices in ground-based instruments. The features included in these packages are:

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- Stable, thermal expansion matched material: Annealed Invar 36
- Very flat mounting surface, bonded with very thin epoxy layer.
- Shims to control the package thickness and tilt.
- Precision location pins to allow close butting without risk to adjacent CCD.
- Foolproof loading system for assembly and service of close packed arrays[2].
- Transportation containers form part of loading system.
- Integral PGA connector and custom ZIF socket allows minimal footprint for efficient close butted mosaics.

2.3 ASSEMBLY AND ALIGNMENT

The use of large CCDs in close-butted mosaics poses particular problems during the assembly stages, since these are valuable and fragile units. Careful schemes have to be evolved in order to facilitate safe assembly

The figure below indicates one stage of the process of inserting a chip in between two others; the alignment and guide pins prevent it from making contact with the others during insertion. The diagram here shows the chip out-of-position, and unable to be fully inserted, and unable to touch adjacent chips. When correctly aligned it can be inserted fully.

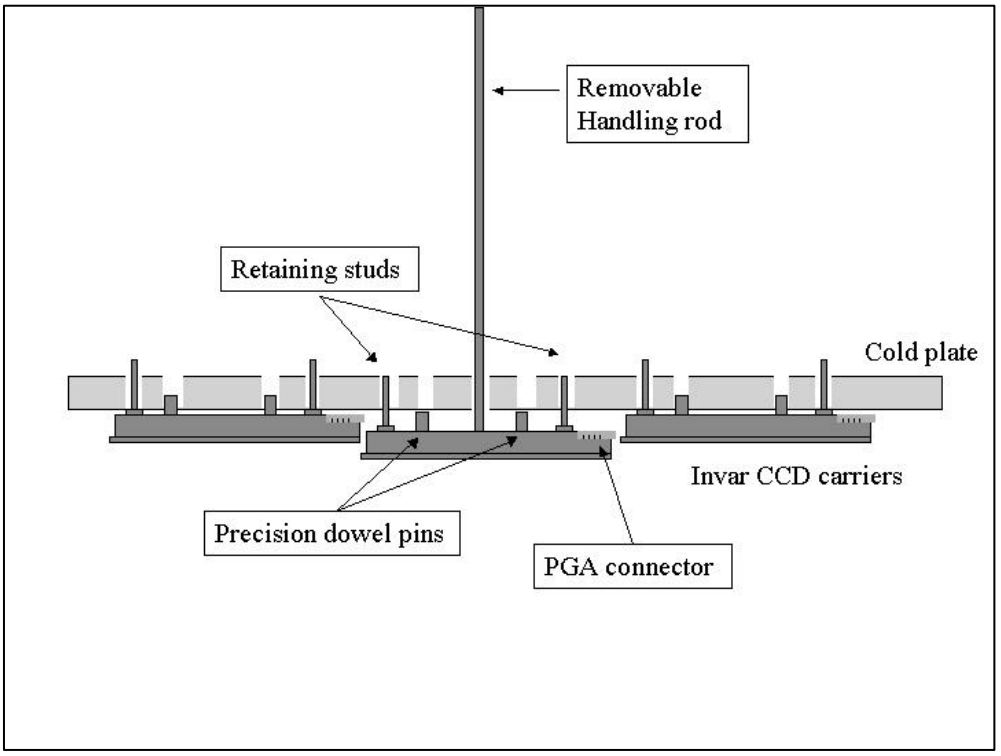

Figure 1. CCD insertion.

With careful choice of materials such packages are suitable for space applications; in fact a variant of the CCD42-80 sensor has been built in this package style for the European COROT mission.

An example of use in a large focal plane is the 40-chip CFHT mosaic, which is now operational on that telescope. This style of package has been used for mosaics with a 'dead-reckoning' assembly onto a precision baseplate, where sub-pixel alignment is not required. High stability is nevertheless achieved. A focal plane flatness of order 10 μm can be achieved, when CCDs are mounted on a suitable base plate, with no adjustment.

For higher accuracy we have mounted this type of device (CCD44-82) into a purpose-made cold-plate, and adjusted the device position prior to final clamping to the plate. In this case, for the SALT programme, we achieved sub-pixel rotational (6 µm in 60 mm) and lateral (1 µm) relative alignment between a pair of devices by manipulating one device in slotted holes relative to a fixed device. The maximum deviation of focal plane position was +/- 4 µm from a reference plane. See later figure also. This procedure would be limited to a small number of devices in practice.

With precision measurement equipment we are able to determine absolute focal plane positions in assembled mosaic plates. An example is the LBT plate (see later for picture); in this case we measured the surface profiles at an early stage of mock-up assembly, so that the chips were very far from being in the same plane. The figure below indicates measured profiles; we can measure surface planes of assembled chips to an accuracy ~ 1 µm at present.

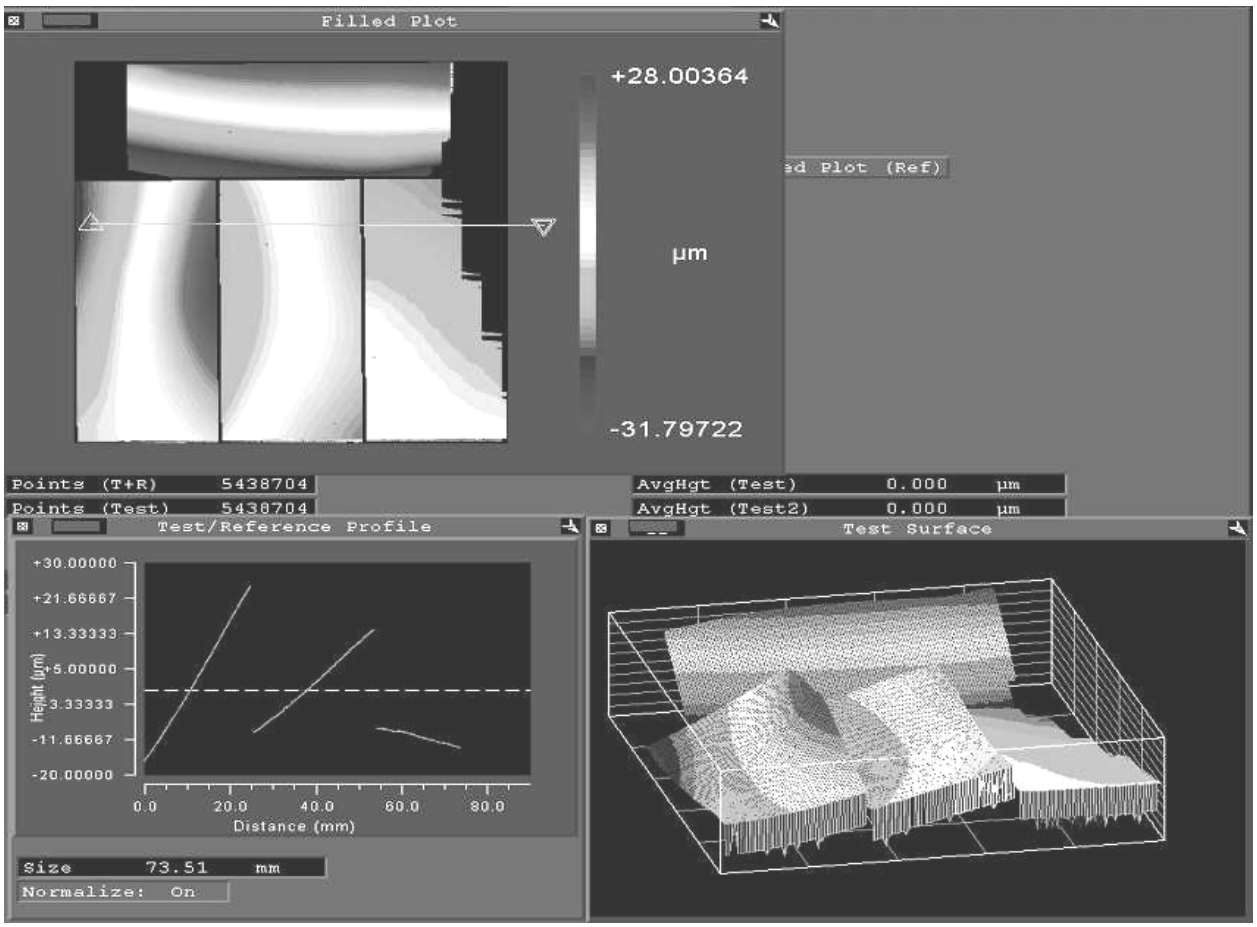

Fig 2. Example of flatness measurements of a non-aligned 4-chip mosaic.

If sub-pixel precision of relative location between many devices is needed then the device package needs specific development. For example, it is possible to locate each silicon die onto a precision metal carrier so that high order subsequent adjustment is not needed. Location of image area to edge of the silicon die, and alignment of die edge to package edge is possible with an accuracy of order 5 µm. This can facilitate extended precision co-alignments, which are required for extended TDI instruments such as the proposed DIVA mission. Extended strips of chips could be mounted onto a sub-carrier plate, by careful manipulation of each one against a reference edge, prior to adhesive bonding. The sub-carrier units (of say 5-10 chips in a line) would then be built up into larger arrays, as needed- with a degree of mechanical adjustment between each one.

Later sections give examples of various package types.

2.4 MATERIALS FOR CRYOGENIC AND VACUUM USE

Careful selection of materials allows reliable use in vacuum cryogenic conditions. Materials are selected from NASA list (reference publication 1124), and if it is necessary to use alternate materials then these are characterised for low outgassing (TML <1%, CVCM <0.1%). We utilise a small range of adhesives that have been tested and selected for appropriate properties - e.g. electrical insulation between silicon & metal, or electrical conductivity (in some cases), good thermal conductivity, good expansion matching, appropriate viscosity and curing time, etc. In many cases a trade-off may be necessary between the available properties.

3. POWER DISSIPATION

For space applications power (and weight) are always important considerations and so we will briefly review here the main components of power dissipation.

3.1 CLOCKING DISSIPATION

During operation the voltage swing of the clock gates causes power dissipation due to resistive impedance losses. This is given by the standard formula - $P = C * V^2 * f$.
The capacitance (C) is the total capacitance of all clock phases that are being driven at frequency (f), with an amplitude (V). Note that the power is a quadratic function of voltage swing.

Clock gates will have a characteristic time constant, T= RC. This is determined by capacitance and resistive impedance on-chip, and it determines the maximum frequency of operation. If the clocks are being driven at a frequency f (with period t= 1/f) such that $f << f_{max}$, then most of the dissipation will occur in the clock drive circuitry, and on-chip dissipation is P= 2T/t.

See also Graeve & Dereniak[3] for a discussion of power dissipation.

3.2 OUTPUT AMPLIFIER POWER

This is generally a static DC dissipation, which depends on voltage applied, and current drawn from the output stages. With two on-chip stages, common on most e2v current designs, the second stage usually dominates since the first stage draws much less current. The first-stage load is internal to the CCD (and not included in this discussion), and the second-stage load is off-chip. P=V * I, where V = drain voltage supply, I = load current. This second-stage load is usually local to the CCD, and therefore included in this calculation. If the load is more distant then the local dissipation reduces to P= Vds * I, where Vds = drain-source voltage drop on-chip (and is typically ~ 4V).

3.3 RADIATION TRANSFER

Large CCDs, and large focal plane assemblies, offer a significant surface area for radiative transfer; this is rarely negligible in cryogenic systems. The usual radiation transfer laws apply, although estimating the degree of transfer is often best done empirically. CCDs surfaces with AR coatings may have low emissivity at visible wavelengths, which increases at longer wavelengths. For a CCD (of area A) at cryogenic temperatures (e.g. –100C), and exchanging radiation directly with an ambient temperature environment (e.g. through a vacuum window), then the power transferred is $P_R = A * Q$, where $Q \sim 40$ mW cm^{-2}. The reduced emissivity of the CCD surface, and cryogenic radiation shielding would normally reduce this, but the potential magnitude of the effect can be seen.

3.4 AN EXAMPLE OF A POWER DISSIPATION CALCULATION

We will give some typical calculations for an e2v CCD42-40 full-frame backthinned, non-inverted 2048*2048 pixel array. This example refers to a ‘staring mode’ windowed readout. Similar calculations would apply to other devices, although the relative power dissipation components may change.

Parallel clocking
Parallel clock bus impedance (for each phase) ~ 30 ohm, Capacitance ~ 60nF, hence T= RC ~ 2 µS.
A parallel clock frequency of f= 100 kHz (t = 10 µS) is chosen for maximum speed. 10V clock swings are used.
On-chip power dissipation, $P_p = (2T/t) * C * V^{2} * f$ ~ 250 mW per phase.

In this example, the device integrates signal for 100 mS (T_{int}), followed by a windowed readout sequence which lasts for ~100mS. Total time between readout cycles is therefore T_T ~ 200mS. The time spent for parallel clocking, T_p = 2048 * 10 µS ~ 20 mS.
With allowance for the duty cycle, and including all three phases, the total parallel clock dissipation on-chip is -
$P_1 = (T_p/T_T) * 3 * P_p$ = 75 mW

Serial clocking
Serial clock bus impedance ~30 ohm, capacitance ~ 300pF, hence T ~ 10 nS.
A serial clock frequency of f= 1 MHz is used.
On-chip power dissipation, $Ps \sim (2T/t) * C * V^{2} * f$ ~ 0.6 mW per phase.

In this example, the device only reads 50 rows in a windowed readout. The serial clocks are active throughout the readout time, which lasts for T= 50 * 2048 * 1 us ~ 100 mS.
With allowance for the duty cycle, and including all three phases, the total serial clock dissipation on-chip is -
$P_2 = (T_s/T_T) * 3 * P_s$ = 1 mW

In continuous high rate readouts, such as TDI modes, it is common for serial clock dissipation to dominate over parallel clock dissipation.

Output circuit power
The device operates typically with a 30V drain supply, and 5 mA load current.
$P_3 = V * I$ ~150 mW per output., using a local load resistor.
If two outputs were used then this figure would double. It is assumed that the inactive output is powered down.

Radiation loading
Chip area (image area only is counted here, not package) A ~ 7.4 $cm^{2.}$ Assuming 10% transfer with ambient, radiative power transfer
P_4 ~ 0.1 * 7.4 * 46 mW = 35 mW

Hence, in this example, total power dissipation is $P = P_1 + P_2 + P_3 + P_4$ = 260 mW

3.5 POWER REDUCTION TECHNIQUES

Most e2v CCDs are constructed with serial registers that have a larger signal capacity than the parallel phases. For example, in the case of the widely used CCD44-82 sensor the serial pixel capacity is approximately a factor of four to five times larger. This is necessary if on-chip binning is used with large signals. However, if this excess capacity is not needed then adequate serial transfer efficiency can be obtained at lower clock amplitudes. For example reducing the amplitude from 10V to 7V would half the power consumption of the serial clocking. In some cases this could allow lower consumption drive circuits to be used also, further reducing total power dissipation.

CCDs are traditionally made with a 'standard' thickness of gate dielectric; this generally requires 10-12V clock amplitudes for adequate internal fields and charge movement. It is possible to manufacture devices with a thinner gate dielectric, which allows effective operation at lower applied clock amplitudes (e.g. ~ 7V). This can significantly reduce clock dissipation, with perhaps only a small impact on manufacturing yield - due to an increased probability of gate-to-substrate short circuits. The probability of a fatal defect increases with device area, so the advantages of this process may be harder to achieve on large arrays. As discussed above, the possibility exists of operating with an even lower clock voltage in some cases.

It is possible to minimise output circuit power dissipation by reducing drain voltage supply levels during inactive periods. This requires additional control circuit flexibility, and a degree of settling time before readout commences. If an off-chip load is used remote from the sensor then the on-chip dissipation is reduced.

4. DEVICE OPERATION

4.1 OPERATING VOLTAGES

Semiconductor devices, such as CCDs, are traditionally stable in operation. Furthermore, with careful manufacture the various operational parameters (i.e. drive voltages) may also be very repeatable from one device to another- not only within one manufacturing batch, but from batch to batch. This considerably aids system integration for space instruments, which may have limited adjustment flexibility. It also facilitates the operation of large mosaics, where common drive electronics would be applied for multiple sensors.

On every batch we routinely monitor the ϕ_{th0} parameter, which is the channel potential with gate set at substrate potential; this represents the difference between externally applied gate voltage and internal buried channel potential. This, together with output transistor gate characteristics and similar parameters, are used to define optimum operating settings for the CCDs. Because of the stability of these parameters, it is usual for most devices to operate with a common (default) set of operating conditions. However, optimisation may be done according to the batch parameters, which will generally define how all devices from one batch should operate best. Optimum performance is obtained by using the appropriate parameters specific for each chip.

4.2 RADIATION DAMAGE

CCDs, like most semiconductors, suffer damage in radiation environments such as exists in most space missions. This is well documented elsewhere, and is not discussed in detail here. However, one particular performance parameter (charge transfer efficiency, CTE) degrades with known consequences on efficiency of science missions. Some specific design improvements can offer amelioration techniques that deserve attention in the context of space telescope focal planes. Radiation damage is well known to cause reduced charge transfer efficiency due to silicon lattice damage resulting in trapping sites. This usually results in loss of signal, particularly when small events are of interest. At high signal levels the traps fill up readily, and CTE degradation is less troublesome.

One technique is the use of a supplementary buried channel (or 'notch'). This reduces the volume of silicon through which small signals will pass, thus reducing the probability of interaction with radiation-induced traps.

These traps may become filled with charge, which is then held for a characteristic time before being released. At low temperatures this de-trapping time constant may be sufficiently long that many transfers may occur whilst the traps are ineffective (already filled).

It is possible to use an optical illumination pre-flash or post-flash to provide extra signal exposure over the whole frame, as a means of filling traps. However, this invariably introduces associated Poisson noise to the exposed signal.

The technique of using a controlled injection of charge may be used to fill such traps, and allow better operation at low signal levels. A controllable injection structure to allow injection of rows of charge when required was first used by e2v for the XMM-Newton EPIC CCD22 sensors. More recent implementations have included the CCD43 sensor (HST WFC3), the CCD90 (Kepler mission), and the ESA GAIA CCDs.

Various injection options could be used, ranging from a single row, to one row in 50, up to injection at every row- depending on the numbers of traps (and their time constants). Injected rows would typically have ~ 10,000 e- signal levels (or more), with an expected corresponding Poisson noise of say 100 e-. This extra noise would normally limit the use of this technique to situations where radiation damage is high, or where signal levels are high. However recent measurements[4] suggest that the noise on this charge is lower than expected, and so charge injection on all rows may be possible.

For TDI (or continuous)-mode readouts an occasional injected row may interspersed with other image rows. In this case these periodic injected rows would keep traps filled, and other rows should not suffer the effects of the traps.

The injection structure needs careful design to provide adequate column-to-column uniformity, and to provide controlled and repeatable injection levels. For some applications, a large signal level (perhaps approaching full well) may be desired; in other cases, such as WFC3, a lower level may be wanted (e.g. 10,000 e- or less). The control of the injection process presents a challenge to the chip designer if a wide dynamic range is required.

Other design and manufacturing techniques are used by e2v to minimise other effects of radiation exposure, but are not discussed in this paper.

The figure below shows the architecture of the WFC3 sensor, as an example of a device with an injection structure.

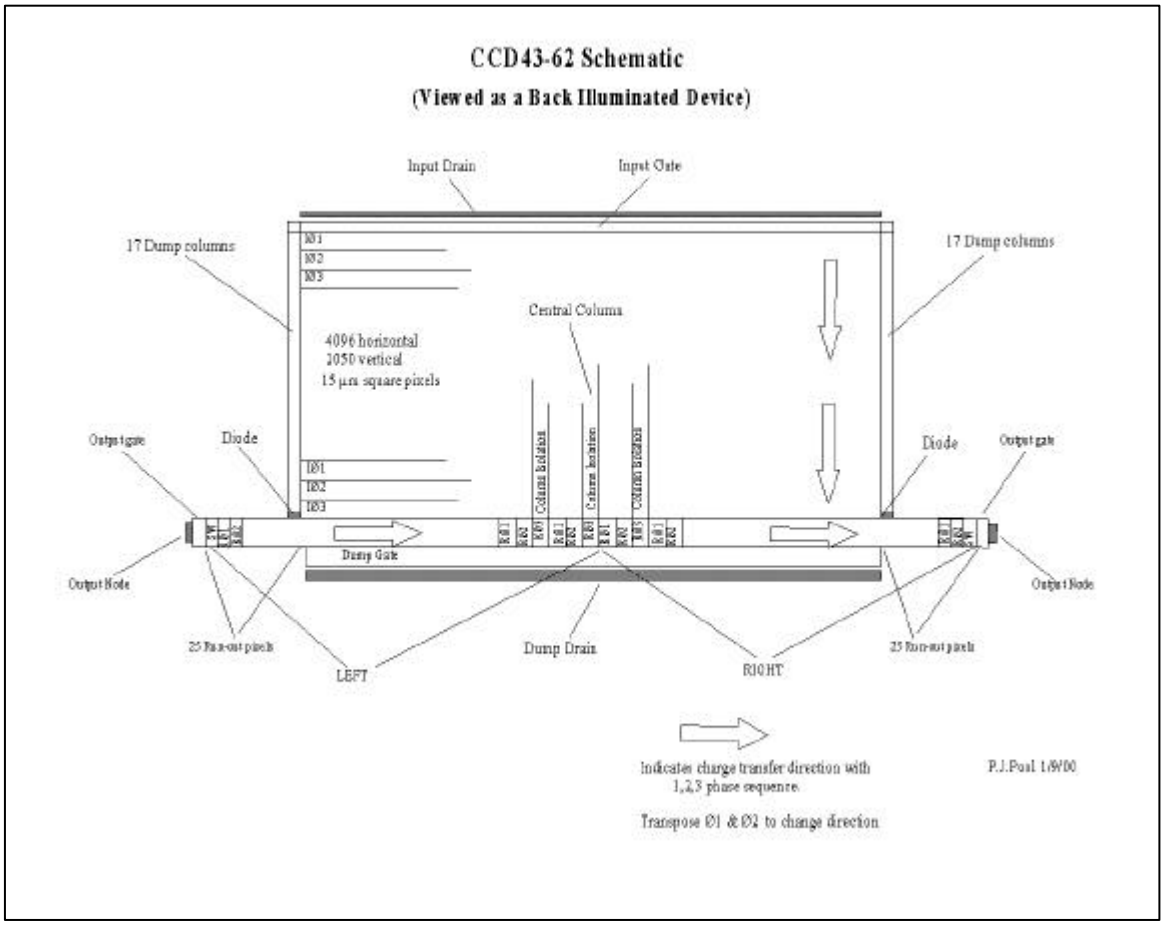

Figure 3. CCD43 architecture

5. EXAMPLES OF GROUND-BASED CCD MOSAICS

In recent years e2v have supplied CCDs for a variety of ground-based instruments of progressively increasing focal plane size. The figures below show some small and large focal planes, all of which utilise the ccd42-90 or ccd44-82 sensor. Both of these use a minimum footprint package of similar design, with integral PGA connector and custom ZIF connector for maximum buttability.

The Large Binocular Telescope (LBT) will use a set of four devices in a 'red' and 'blue' imaging camera [5]. The South African Large Telescope will use a set of two devices in its first-light SALTICAM instrument [6]. The Canada France Hawaii (CFHT) Megacam [7] uses 36 science devices in a large imaging mosaic, which was commissioned earlier in 2003. The European Southern Observatory VST [8] and Smithsonian Astrophysical Observatory MMT [9] instruments will also use similar sized sets of close-packed CCDs in their focal planes. Examples of such small and large mosaics are given in the figures below.

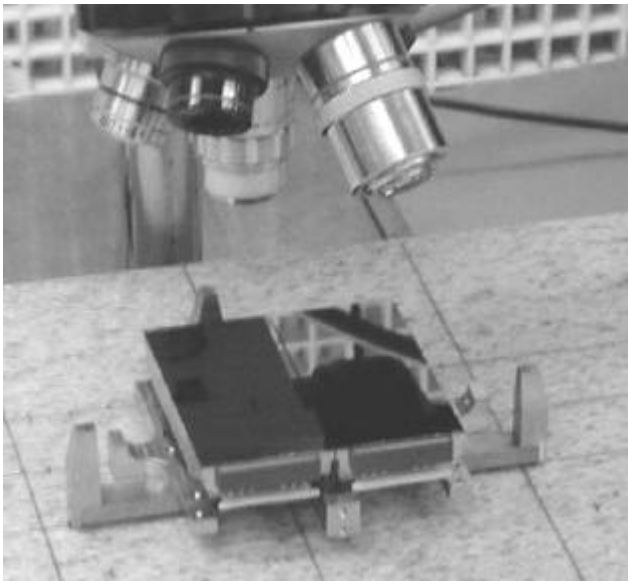

Figure 4. SALTICAM 2-chip assembly

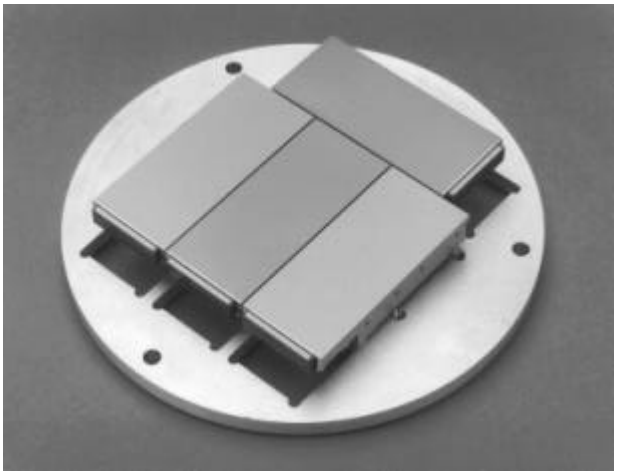

Figure 5. LBT baseplate (mock-up assembly only)

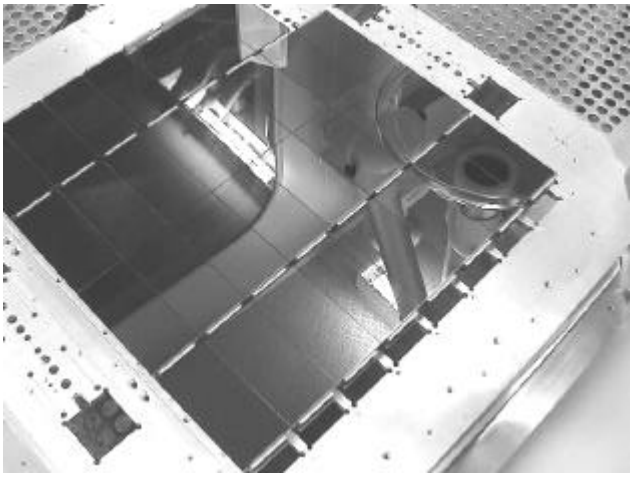

Figure 6. ESO VST Omegacam mosaic

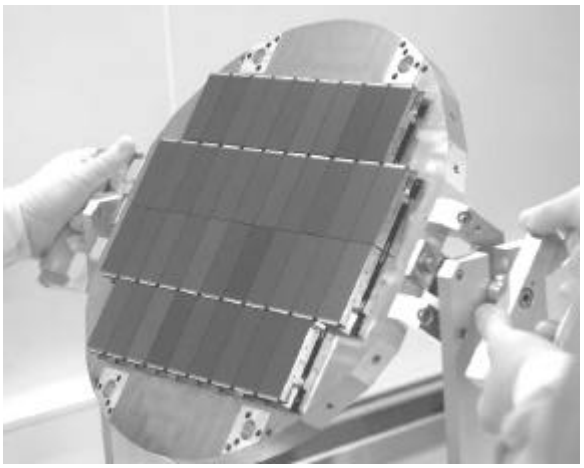

Figure 7. CFHT Megacam mosaic

Both of the last two examples shown do not use complex adjustment facilities, but rely on the precision CCD package and precision cold plate in order to achieve high accuracy focal planes.

6. EXAMPLES OF CCDS FOR SPACE APPLICATIONS

The use of CCDs for space applications has been widespread for many years; a large number have been used in space. Here we will exclude star-trackers and remote-sensing CCDs and only present examples of array applications for science instruments. For most space programmes the integration of sensors onto a focal plane has been done by the instrument builder; e2v generally designs a custom sensor and a custom package to match scientific specifications and focal plane integration requirements. We will indicate some of the primary science applications of e2v sensors for a variety of existing and forthcoming missions (listed alphabetically not chronologically):

- Planned ESA/CNES Corot CCD42-80. A pair of frame-transfer sensors.[10]
- Diva. Array of 25 CCD42-20 sensors planned. See paper in this conference.[11]
- Planned ESA Eddington mission. Four sets of six CCD42-C0 sensors proposed.[12]
- ESA GAIA mission. Large set (>200 TBD)- ASM, AF, BBP, MBP, & RVS CCDs.[13]
- HiRISE. Fourteen CCD89 sensors planned.[14]
- NASA Kepler mission. CCD90 in production. 42 CCDs planned for focal plane.[15]
- NASA HST WFC3. Pair of CCD43 sensors.[16]
- XMM-Newton. Two sets of seven CCD22 sensors (EPIC) and two sets of nine CCD15 sensors (RGS).[17]

The figures below illustrate a few examples of large-area e2v CCDs for science applications in space.

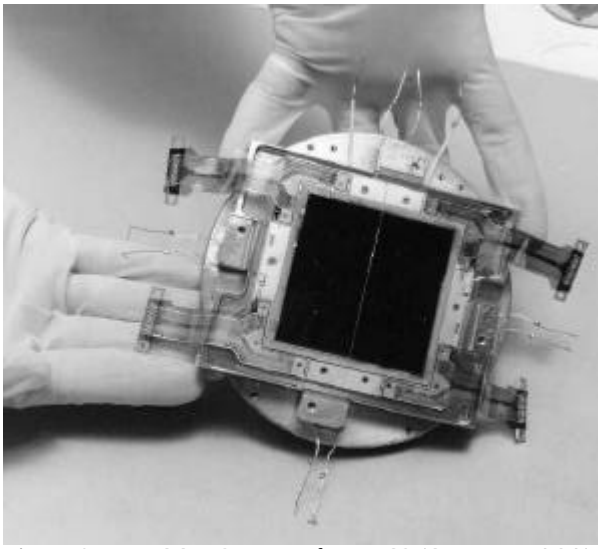

Figure 8. Two CCD43 sensors for WFC3 (Courtesy NASA)

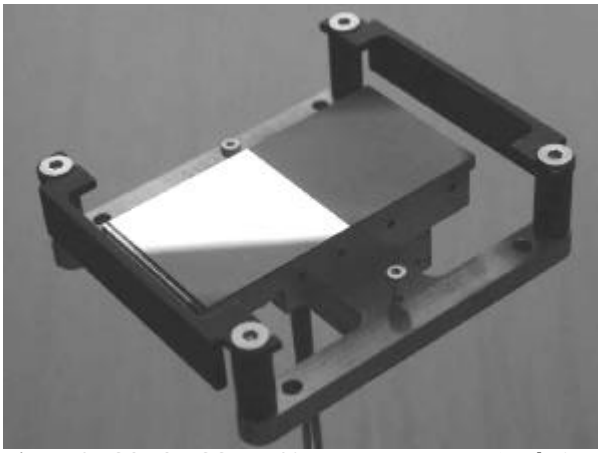

Figure 9. COROT CCD42-80 sensor on transport 'spider'.

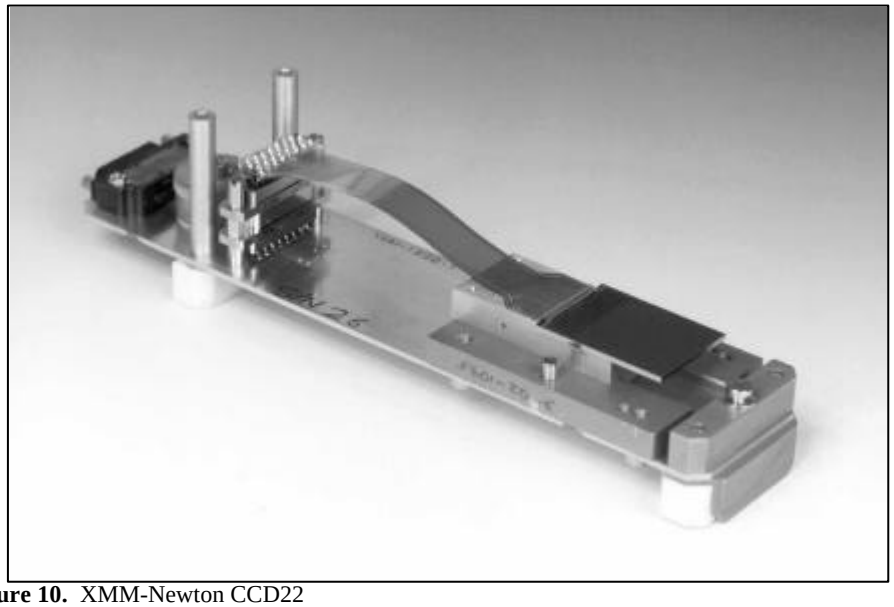

Figure 10. XMM-Newton CCD22

7. THE L3VISION SENSORS

The recently developed e2v L3 sensors are proving to have many useful applications in science, commercial, and defence applications. Because of the high level of interest expressed in these new sensor types we will give a status report and indicate ongoing developments.

7.1 CHRONOLOGY AND DEVICE LIST

L3Vision sensors include an internal gain register to allow sub-electron noise readout from an otherwise traditional CCD imager[18]. The technology has evolved over the last four years or so, and several sensors have been developed, or are in development. Some ground-based observatories have acquired and operated some of these sensors, whose applications are still being explored, taking advantage of the novel performance levels which allow very low light level sensitivity. The table below indicates the device types that are available currently.

Table 1. List of L3Vision CCD types

Device	Format (pixels)	Applications	Date
CCD65 FI	576 * 288, 20 * 30 um (625 line)	TV imaging, surveillance	Available since mid-2001
CCD60 FI	128 * 128, 24 * 24 um	High frame rate imaging	Available since 4Q 2001
CCD60 BI	Back-illuminated version	Wavefront sensing, low level	Available since 4Q 2002
CCD87 FI	512 * 512, 16 * 16 um	Scientific imaging	Available since mid-2002
CCD97 BI	Upgraded BI version of CCD87	Low level scientific imaging	Available in 3Q 2003
CCD79	1024 * 1024, 13 * 13	Scientific imaging	Samples tested in 2003
CCD95 FI	768 * 288, 15 * 30 (625 line)	Higher resolution TV imaging	Available in 4Q 2003

The technology can be applied to any CCD format, and larger format L3 sensors are being planned; custom formats are possible. Based on the body of knowledge gained from the chips made so far the yield, cost and performance issues are mainly understood, which should allow us to make further developments of format from a good baseline. However, experience of using the devices in the real world is limited and so the full characteristics and limitations are still being explored[19] (for example readout noise and signal/noise, and effects of low-level clock-induced charge). The L3 sensors have been used for acquisition, guiding, and wavefront sensing as well as for diffraction limited imaging using their low-

noise properties for selected exposures ('lucky astronomy')[20]. There is a commercial interest in higher frame-rate operation, and planned developments in this direction should be valuable for wavefront sensing as well as 'lucky astronomy'.

In addition to the sensor development, e2v have been supplying camera systems. These have initially been of analogue form, for the ccd65 primarily and also the ccd60. A new digital camera is in the final stages of development, and will initially be used for ccd95 operation, followed closely by ccd60 and ccd97 use (2Q 2004). Again, experience of the use of cameras in operational situations is growing and cameras are beginning to be used in a variety of sectors - including defence, commercial and scientific applications.

7.2 SPACE USE AND RADIATION SENSITIVITY

For space applications one important consideration is the sensitivity of this new technology to the radiation environment. Although the device is too new for us to have acquired much relevant experience, some evaluation work has been undertaken[21],[22]. One concern has been the sensitivity of the high-gain region to radiation damage; however this only occupies a small fraction of the total area so the effect of radiation damage is lessened. The results of these studies show that the performance of these electron-multiplying CCDs following irradiation is sufficiently promising to merit the consideration of this technology for use within radiation environments.

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