

# The 40 CCDs of the MegaCam wide-field camera: design and first tests of the front-end electronics.

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## ABSTRACT

MegaCam is the new wide-field imaging camera currently being built for the new prime focus of the 3.6m Canada-France-Hawaii Telescope. Among all the challenges imposed by the ambitious specifications of MegaCam, there is the CCD Controller. We chose to realize a new highly integrated CCD Controller and to implement some other original solutions. This paper presents the solutions we retained.

**Keywords:** CCD, CCD Mosaic, CCD Controller, CCD Electronics.

## 1. INTRODUCTION

MegaCam is the next generation wide-field imaging camera that will be used at the prime focus of the Canada-France-Hawaii Telescope. It is based on a mosaic of 40 2Kx4.5K backthinned CCDs. The whole project was presented at the previous SPIE Kona meeting<sup>1</sup>, as well at ESO's last 'CCD Workshop'<sup>2</sup> and also in this present SPIE meeting<sup>3</sup>. The main characteristics of the instruments are summarized in table 1:

Total FOV	$\Phi$ 1.4 °	Focal plane size	313 x 261 mm
Pixel FOV	0.18 " x 0.18 "	Pixel size	13.5 $\mu$ m x 13.5 $\mu$ m
Number of CCDs	40	CCD type	EEV 4290
Array size	20K x 18K	CCD size	2K x 4.5K
Mosaic filling factor	93 %	Number of CCD amplifiers	2 (split register)
Spectral range	350 - 1000 nm	Minimum exposure time	1 second
Operating temperature	150 K	Readout time	20 seconds
		Readout noise	<10 e-

**Table 1.** Main characteristics of the MegaCam mosaic CCD mosaic

## 2. SOME CHALLENGES IN A LARGE CCD MOSAIC CONTROLLER

Thanks to the experience got with the development of EROS1<sup>4</sup> (16 buttable CCDs) and EROS2<sup>5</sup> (2 x 8 buttable CCDs mounted on a 1m telescope) instruments, running in La Silla Observatory, we were aware of the distinctive features of such large CCD mosaic Controller compared to simpler systems.

Let's analyse the example of only one EROS2 camera: we designed the Controller as an assembly of boards for individual CCDs. This provided a high modularity of the system, with possibilities of control of any mosaic made of any number of any type of CCD... On the other side, this implies the presence of 3 crates (1 for Control + 2 for Readout) located near the cryovessel with another one (Power) put down on the telescope base, and 36 cables (inside and outside of the cryovessel) plus 3 additional cables (for power) and 2 optical fibers (as link with the acquisition buffer). After 4 years of use, the few problems we have seen came from the connectics.

The boards thermal dissipation was 100W + additional 100W due to linear power supply, i.e. 25W per CCD. An extrapolation to MegaCam would give 40 x 25W = 1KW... (at the primary focus, and only for the CCD electronics). The linear power supply was questionable too: its low yield gave a high dissipation, so a good reason to move it away from the telescope. Then, it imposed long and big cables running on the telescope, giving poor regulation and noise performances, a pity for a linear power supply. Similar cables in MegaCam, due to the CFH Telescope dimension, should be more than 50m long.

Inside the cryovessel, there were small cards (1 per CCD) with no preamplifiers but low-pass filters and some flat cables and twisted pairs; not a good point for outgassing rate. In MegaCam, many of the 40 CCDs are in the center of the mosaic, so not easily connectable, and moreover, due to the large window, the cryogenics need to be more powerful and thus quite cumbersome. Twelve hermetic connectors were arranged all around the cryovessel. In MegaCam, there are almost 2000 wires to pass through the cryovessel. That makes enough problems to look for another solution ...

Concerning the digital part, there are two main difficulties. Its first role is to act as a sequencer to control the charges transfer in the CCDs and to organize various signals like AD conversion start. In the case of a large CCD mosaic with multi-outputs devices, this role can be simple (all CCDs operated in broadcast) or very complex (individual sequencing, windowing or binning modes, etc...). Moreover, the noise performance specifications imposes to keep signals as synchronous as possible. A single local sequencer thus seems preferable. Its second role is to read the AD Converters (80 in MegaCam) and to transfer the data to the acquisition buffer. And the data have to be re-arranged or descrambled before storing in memory. Of course it is possible to share the job between some CPUs in parallel, but as always, it is preferable to minimize the number of CPUs. Finally, the amount of data is quite enormous (800MB per image in MegaCam), thus requires high performance digital part and high rate transfer media.

Our conclusion is that a modular approach is OK up to 8-16 CCDs. Beyond that, an integrated design is needed or at least can strongly simplify the system. Concerning the digital part, it is preferable to design with the most powerful components (CPU, links) in order to minimize again the system.

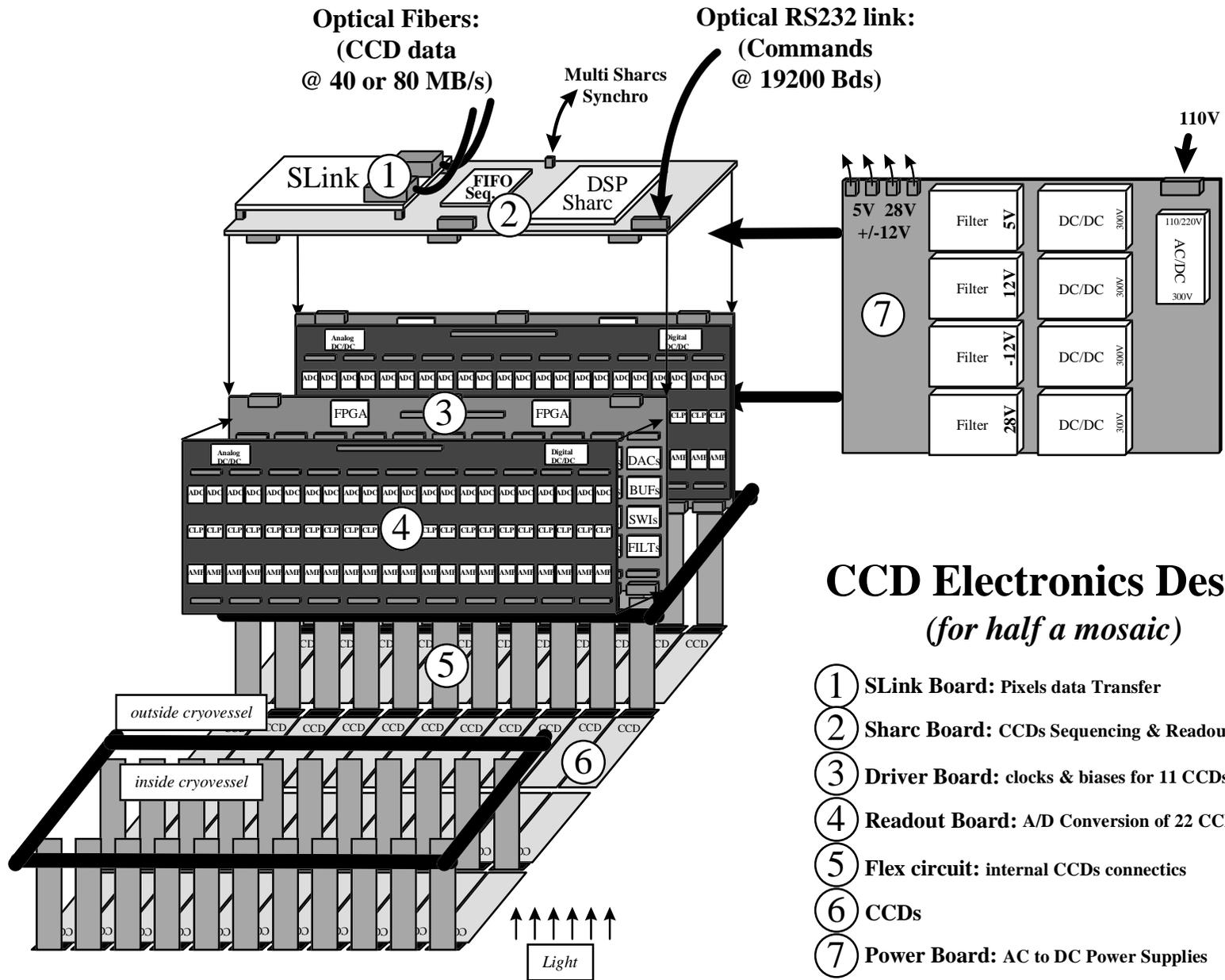
### **3. THE MEGACAM DESIGN CHOICES**

The MegaCam specifications were so far than those for usual telescope instruments, that they imposed to redesign the CCDs electronics starting from scratch. The location of MegaCam at the primary focus (at the inner top of the Canada France Hawaii Telescope) imposes minimal dimensions, heat dissipation and weight and asks for maintenance operations as simple as possible. And obviously, there was always the usual specification like a faster readout (20s max) with less noise (10e- max) but with 40 CCDs and 80 readout channels in this case...

Our natural first idea was to split the Controller in different parts in order to let only at the primary focus the most essential close functions and to move away all the others parts. We chose exactly the opposite approach ! We chose to design a very high integrated Controller and put it as close as possible of the CCDs (see figure 1).

This high integration allows to group all common functions like sequencer, voltage reference, I/O interface, glue logic, etc... thus to minimize dimensions, weight and dissipation. We are foreseeing only 2 crates of about 32x30x10cm, 10Kg and 100W each (power supply and mechanics included) and only 4 types of custom boards. The system is simpler, thus any development/maintenance too (we think that simplicity is the only true solution for maintenance rather than complex and powerful diagnosis system, or universal Controller, for examples). Thanks to the 'natural architecture', where the boards are plugged directly on the rear face of the cryovessel, connectics is minimum inside the cryovessel (only 15cm flex circuits), and quasi-inexistent outside of it. This improves strongly reliability. Moreover, all signals wires lengths are minimized and kept inside the metal crates, giving a system naturally less sensitive to pick-up noise. Finally, the high integration is helpful to achieve a reasonable cost. The main constraint is to tie the boards width to the CCDs pitch i.e. to implement all CCD channels in 3cm wide printed circuit strip. And the farthest boards will have two unused channels since the mosaic is not square. All boards are designed to manage 11 CCDs and/or 22 readout channels.

Figure 1. MegaCam CCD Controller 3D View (mechanics not represented)



## CCD Electronics Design (for half a mosaic)

- ① SLink Board: Pixels data Transfer
- ② Sharc Board: CCDs Sequencing & Readout
- ③ Driver Board: clocks & biases for 11 CCDs
- ④ Readout Board: A/D Conversion of 22 CCDs signals
- ⑤ Flex circuit: internal CCDs connectics
- ⑥ CCDs
- ⑦ Power Board: AC to DC Power Supplies

#### 4. SOME ORIGINAL CHARACTERISTICS

We integrated the usual requirements like CCDs biases and clocks levels controlled by DA Converters. The Controller is designed to fit first with the Marconi Applied Technologies (ex-EEV) CCD4290 device<sup>6</sup> but is not limited to this particular device. We also added some original characteristics:

##### 4.1 CCDs voltages generation and check

CCDs biases and clocks levels are controlled by DA Converters and DC amplifiers (more than 1100 independent signals to generate), and are checked back by special AD Converter. For each CCD, up to 12 independent bias voltages and 16 clocks can be generated. All voltage ranges are first limited by amplifiers power supply rails, then defined by an additional system (see table 2) controlled by potentiometers (common to 11 CCDs). The final accurate value is setup by the user via software and 8bits DA Converters. This avoids overvoltage on CCD pins due to user, software or transfer errors. The CCDs voltages are all written into DACs then enabled to rise on CCDs pins following a single user command. That avoids high differential gap during initialization. Moreover, the CCDs voltages are disabled directly by the 'Power Board' in case of power failure even before the real drop of power voltages. The CCDs voltages are finally low-pass filtered at the level of the output connectors (15cm to the CCDs).

The user can ask for a check of CCDs voltages. A network of multiplexors and a 12bits AD Converter measures each CCD voltage one by one and directly on the CCDs pins (there is only the Flex circuit between probe and pin); then the SHARC compares the measured values with the instructions. The clocks levels voltages (high and low levels) are measured in two steps, so the system is also able to detect any problem in the analog switches. The CCDs thermistors are also measured in the same way. Finally, a voltage reference is tied to the input multiplexors. The user can ask for an auto-calibration of the check channels (muxes and ADC) and then the generation channels (DACs and amplifiers).

No power buffer is needed to generate the clocks, even for the  $A\Phi$  signals (parallel shift). Capacitors in front of the analog switches are big enough to provide the current peaks at rate up to 10Khz. The board dissipation and dimensions remain then reasonable (all resources for one CCD fit in 3x15cm board surface). Some clocks levels are common to some CCD clocks (example  $R\Phi1L$ ,  $R\Phi1R$ ,  $R\Phi2L$  and  $R\Phi2R$  have the same high and low levels, see table below) but there is no grouping between two CCDs. Clocks timing is generated either by the SHARC or by a dedicated synchronous FIFO tied to the same master clock. They just have to output 32 bits patterns at 40MHz rate. Each bit controls one CCD clock and some extra bits define CCDs selection. So, it is possible to send different sequences of clocks patterns to any CCDs and to touch any single clock of any CCD.

Possible range (V)	EEV name	Typical value (V)	Adjustable allowed range (V)	Possible range (V)	EEV name	Typical value (V)	Adjustable allowed range (V)	Notes:
0/+26	ODL ODR	22.5 22.5	16/26	-10/+10	$A\Phi1$ $A\Phi2$ $A\Phi3$ FT1	-9.5/0.5	-10/0 & 0/10	
0/+26	RDL RDR	9.5 9.5	6/16	-10/+10	FT2 FT3	-9.5/0.5	-10/0 & 0/10	FT not used in MegaCam
0/+26	DDL DDR	15 15	10/20	-10/+10	$R\Phi1L$ $R\Phi1R$ $R\Phi2L$ $R\Phi2R$	-8.5/1.5	-10/0 & 0/10	
-10/+10	OG1L OG1R	-6.5 -6.5	-8/2	-10/+10	$R\Phi3$ SWL SWR	-8.5/1.5	-10/0 & 0/10	
-10/+10	OG2L OG2R	-5.5 -5.5	-8/2	-10/+10	$\Phi RL$ $\Phi RR$	-9.5/2.5	-10/0 & 0/10	
				-10/+10	DG	-8.5/1.5	-10/0 & 0/10	

Table 2. MegaCam CCD Controller: CCD signals SetUp (VSS = 0V)



### 4.3 Simple Readout Chain

The 'Readout Board' is plugged on the 'Driver Board' as a mezzanine. In order to fit 22 CCD readout channels on a 32x18cm board, the schematic is kept quite simple. Base line management and Correlated Double Sampling operation are made by clamping to the ground. Differential mode up to the 16 bits AD Converter (LTC1604) helps to minimize any ground loop effect. Thanks to the EEV CCD4290 capability to compensate its output offset, no offset adjustment is needed. Only one gain will be available.

### 4.4 The SHARC large I/O capabilities and power

We chose to manage the Controller resources by inserting locally one of the more powerful DSP available in the market, the SHARC 21060 from Analog Devices (see figure 3). Its speed (25ns instructions) allows to read 40 CCD channels tied to its parallel port in less than 3µs while in the same time, two of the link ports with associated DMA are able to transfer previous pixel data at 80MB/s. Moreover, two 3 wires serial ports are useful to setup the large number of DACs used to control the CCD voltages. The large I/O capabilities of the SHARC and its local implantation help to reduce the digital part of the Controller. The SHARC code may be downloaded from either acquisition buffer or from local prom or from other SHARC.

The MegaCam CCD Controller contains two SHARCs (one per crate). An interrupt mechanism is used to synchronize them with less than 25ns jitter. They can also exchange data via the four additional 40MB/s link ports, if needed. It is always possible to freeze all signals (except master clock, but including link ports) during critical time, for example when pixel 'sample & hold' signal occurs.

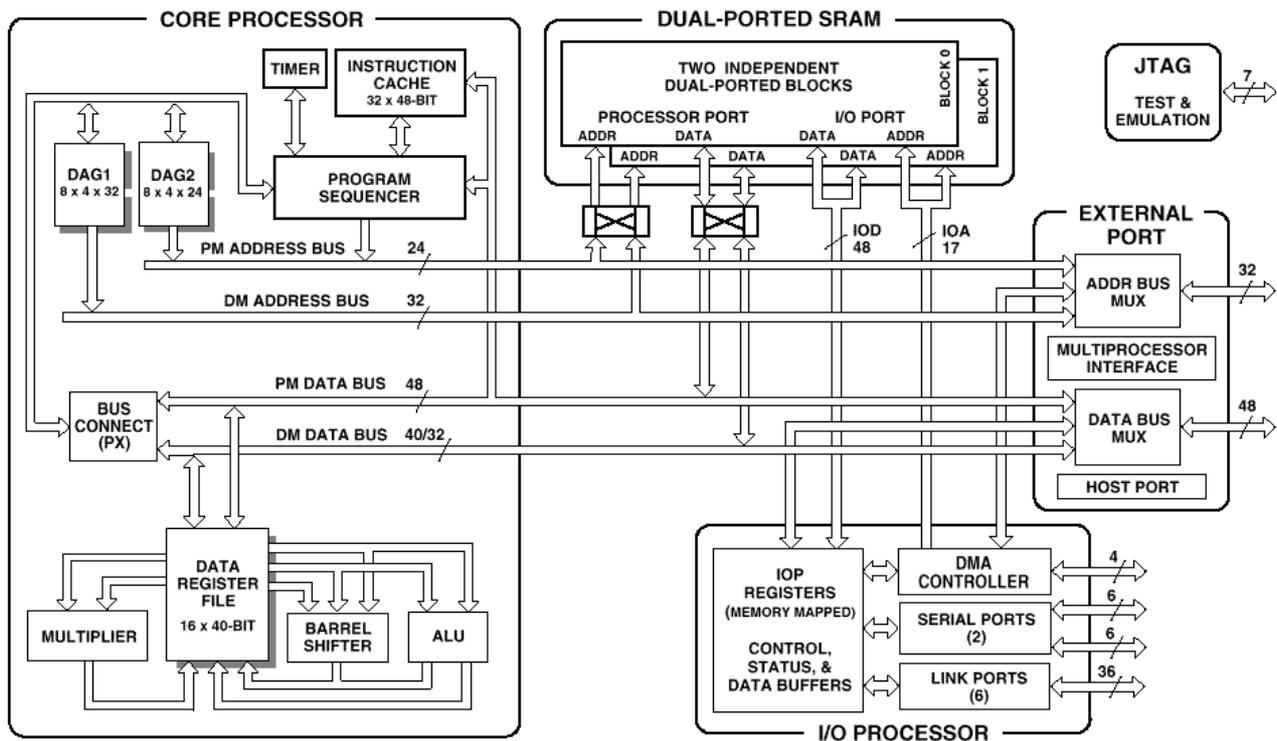


Figure 3. SHARC 21060 Block Diagram

#### 4.5 In situ descrambling

The large internal double port memory of the SHARC (512KB) allows to store 2 rows of all its corresponding 20 CCDs. The SHARC reads the pixels and computes in real time its address in memory. Then it can store the pixels at the right places, building a descrambled super-row made of 40 CCD half rows (see figure 4). In the same time, the link ports transfer the previous descrambled super-row stored in memory, to the outside world. All the following data treatments and transfers become then more efficient since the data blocks contain only consecutive pixels. However, this is only a partial descrambling since the rows of all CCDs remain interleaved. The complete descrambling is achieved in the acquisition buffer.

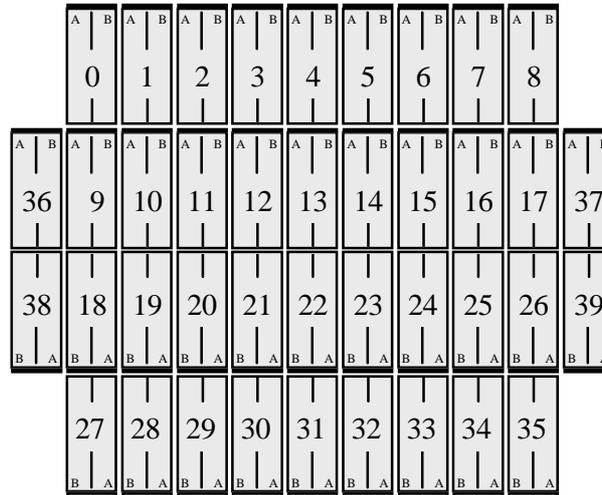


Figure 4. MegaCam CCD Controller: the mosaic readout configuration (2 amplifiers per CCD)

#### 4.6 Various readout & sequencing modes

As in most of CCD Controllers, we chose to implement locally a DSP to do the sequencing, rather to use only a remote sequencer (i.e. at the other side of the optical fibers). It imposes of course to manage the reset, boot and commands procedures but the system remains simple. There is no need for a second high rate optical link (from acquisition buffer to Controller) and a complex synchronization system.

A special FIFO with retransmit function is dedicated to sequence the CCDs in normal readout mode. The SHARC has just to fill it once with the 'shift 1 pixel' sequence patterns and to give it the start signal at the beginning of each pixel cycle.

The EEV CCD4290 has two outputs left and right, and can be used in 3 modes: all pixels shifted to the left output, all pixels shifted to the right output, half image shifted to the left output and second half image shifted to the right output. In a large mosaic, there is no problem to select any desired output, but on the other hand some cases of sequencing can be difficult to manage; for example, if one wants to use some devices with only left output and other ones with right output, one needs to send different sequences (with some change on register clocks) to the both group. It is not easy to design a mosaic Controller which allows to change the outputs configuration without intervening on the hardware. The solution retained uses extra bits (in the sequence patterns), each extra bit controlling one device. It is necessary to write alternative patterns for left devices and patterns for right devices (25ns delay only).

Two readout strategies are available:

1. all the CCDs are read (by any one or two amplifiers) simultaneously and in similar manner. The special Fifo sequences the CCDs in broadcast while the SHARC reads the pixel data. This is the normal fast readout mode.
2. special readout modes like sampling, binning, windowing are defined. The SHARC manages alone the full operation. It allows any readout mode, even in case of individual CCD sequencing (different window sizes for example).

#### 4.7 High rate pixel data transfer with commercial boards and compatibility to PCI bus

Contrary to usual CCD Controllers, no complex boards have been developed to transfer pixel data on optical fibers to the outside. We use the SLink<sup>7</sup>, developed in CERN (European Organisation for Nuclear Research); it is a commercial optical link composed of two CMC cards (see figure 5).

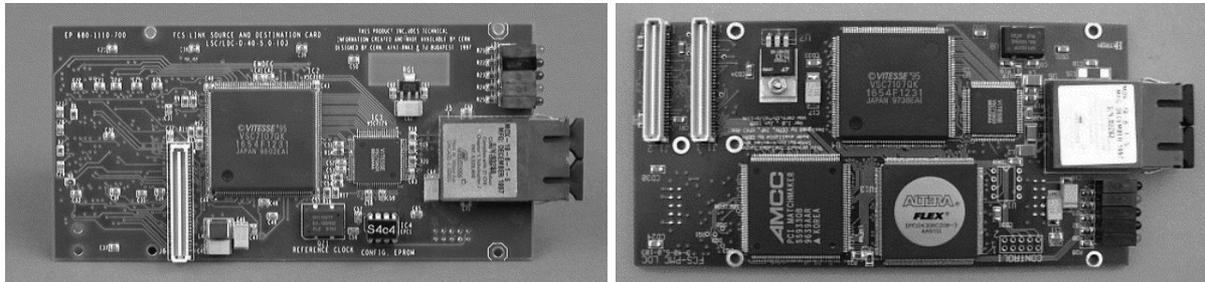


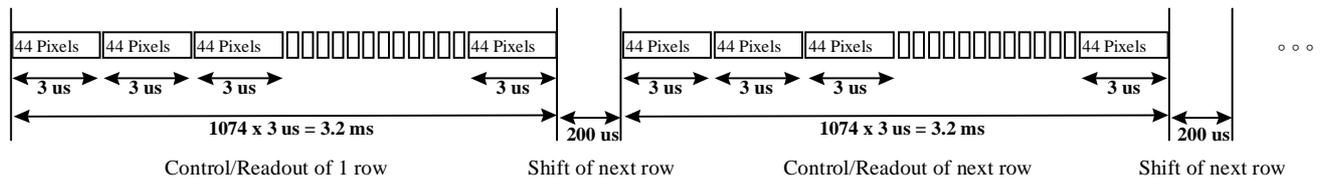
Figure 5. SLink Source and Destination cards

The SLink emitter is easy to implement in a custom Controller since it is seen only as a 32bits synchronous Fifo. SLink can transfer continuous data flow at speed of 100MB/s. In MegaCam, it is in fact limited to 80MB/s (see figure 6) by SHARC 21060 link ports (note that is no more true with the next SHARC 21160 device).

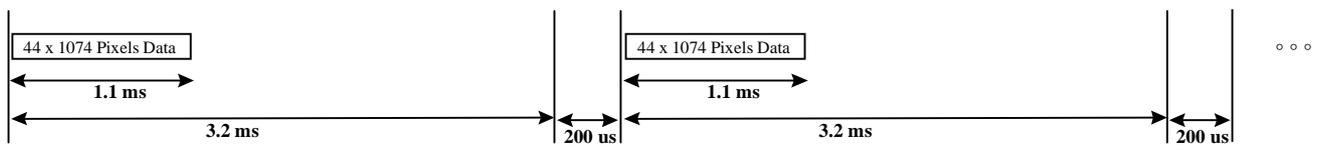
The SLink receiver is directly PCI compatible, thus can be inserted in many powerful computers. That makes the Controller output 'standard' and not tied to a particular acquisition buffer.

A VxWorks software driver has been written for MegaCam. It consists essentially to initialize the SLink and the DMA in the receiver side at each end of packet. The data are transferred in 1074 pixels packets without use of the available control words. The 4 slow rate return lines are not used, since a second link is present for slow control.

#### CCDs Outputs to Sharc: data rate ~ 30MB/s (22 CCDs w/ 2 outputs & 3 us ADCs conversion time)



#### Sharc to SLink: data rate = 80MB/s (via two Sharc Link)



#### Two concurrent SLinks to Memory Buffer: data rate = 133MB/s (limited by PCI)

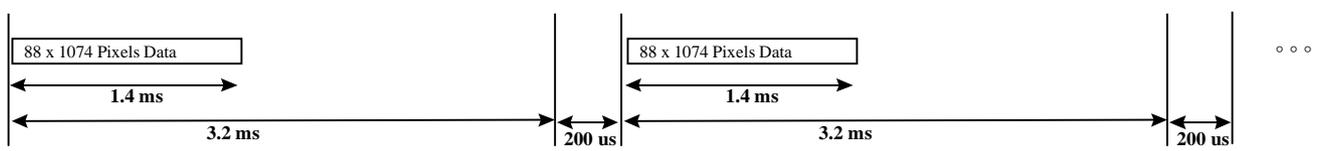


Figure 6. MegaCam CCD Controller: example of data transfer timing from CCDs to memory

Here are the conclusions of the transfer tests we made: first, the transfer rate is limited at the source by SHARC links. It can be too strongly reduced at the receiver side i.e. in the acquisition buffer (see figure 7) depending on the PCI activity and on the performances of the various bridges between SLink DMA and memory. In MegaCam we plan to plug the SLink and memory cards on an PCI expander board in order to isolate them from the CPU board PCI bus (and so from all inevitable requests like system requests, ethernet requests, etc...). Moreover, a particular attention is needed to reduce the CPU time to re-initialize DMA at each end of packet. As there is only a very small FIFO in the receiver side, a dedicated signal is sent back to the emitter to force it to wait for the current receiver initialization. That is possible in the SHARC with no effect on the CCD readout or sequencing timing because the transfer via the link ports is fast enough and asynchronous with the readout. We plan to increase the FIFO size to make the system more insensitive to such delays.

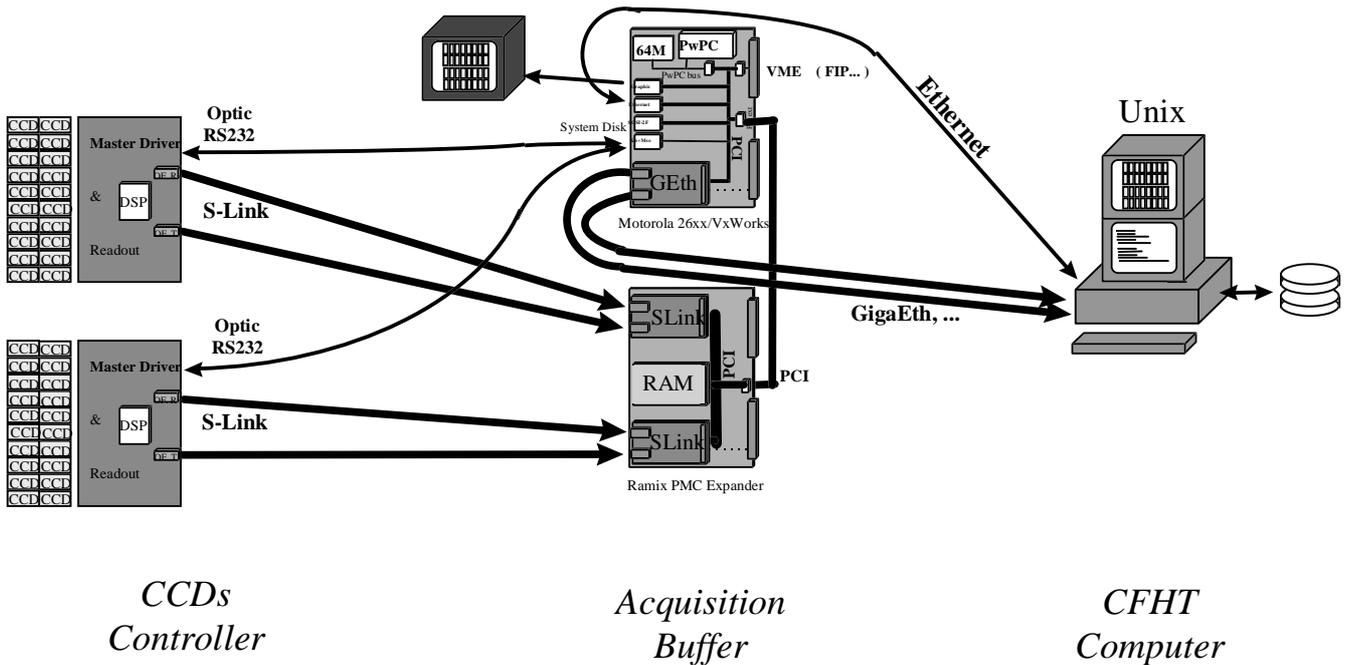


Figure 7. MegaCam CCD Controller Links to an Acquisition buffer (example)

Two SLinks will be used in MegaCam. Some possible architectures for the acquisition buffer are under test.

#### 4.8 Second link for slow control with simple software tools

The Controller is also tied to the acquisition buffer via a serial RS232 data link. When mounted in the telescope, a commercial RS232 to optical fiber adapter auto-powered module (see figure 8) provides electrical isolation and required length. During maintenance and development in lab, a simple serial cable is sufficient. The Controller can then be connected anywhere to a PC for an easy maintenance. One uses a simple software from Analog Devices to communicate with the SHARC. One doesn't need the whole acquisition system for maintenance or further development.

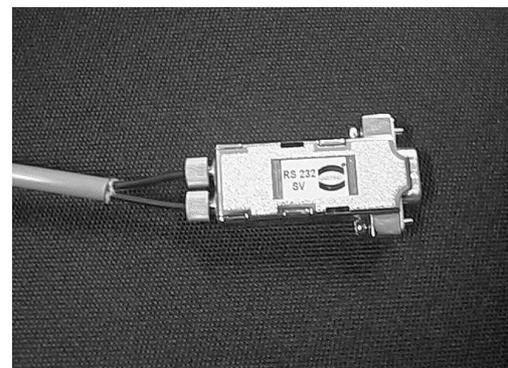
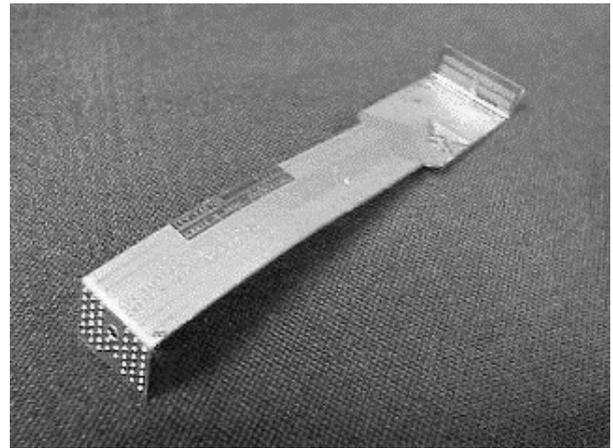


Figure 8. Slow Control Link (optical auto-powered RS232)

#### 4.9 No electronics inside the cryovessel

This is best to avoid outgassing, to simplify camera mounting and also to facilitate development and maintenance since one has access to all the electronics. There is no disadvantage because the Controller boards are directly plugged on the cryovessel. The distance between CCDs and drivers or preamplifiers is less than 20cm. The internal check system can also measure the voltages directly on CCD pins (in two steps for clocks). That allows also easy failure diagnosis.

A folded kapton flex circuit (see figure 9) connects each CCD to the hermetic connector. It allows to route easily all CCD signals from the EEV ZIF connector (new version) to a SAMTEC SMD socket. This is a 4 layers flex circuit. An internal ground layer protects the biases and clocks layers but is connected to only one side to avoid too much thermal loss. The additional layer contains a larger ground wire. We evaluate the thermal loss due to the 40 flex circuits to less than 4.6W i.e. only 12% of the total cryovessel losses.

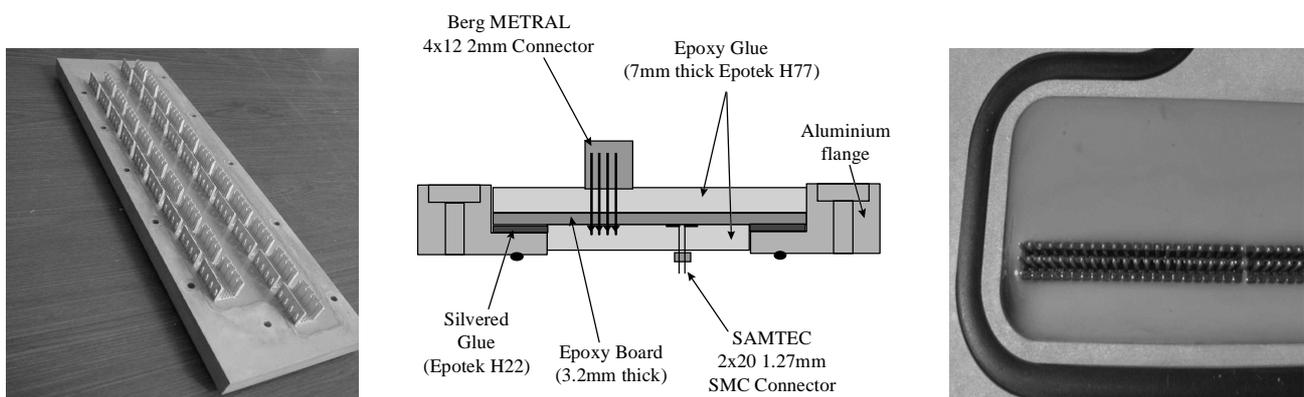


**Figure 9.** MegaCam CCD Controller: CCD Kapton Flex Circuit (ZIF connector is missing)

#### 4.10 Custom hermetic connectors

About 2000 wires have to go from the CCDs inside the cryovessel to the boards outside it. As we wanted to plug directly the Controller boards on the cryovessel rear face, we have looked for rectangular connectors, more reliable and smaller than classical hermetic SubD connectors. Hermetic microD connector with ceramic isolator were suitable but much too expensive (equal to the budget of the whole Controller...). We decided to develop a special technique (see figure 10) to build our own hermetic connectors at a reasonable cost. The main idea was to avoid direct pass through both faces. Thus we built a 3.2mm printed circuit board accommodating 20 4x12 pins Metral connectors on a face and 20 2x20 pins Samtec strips on the other face, both connector types tied by printed wires. This board is then inserted in a metal flange and 'drowned' with epoxy. This system allows to choose independently the most suitable connector in both side (big ones on board side, small ones on flex circuit side), to place them exactly where needed and moreover provides better EMC protection thanks to a ground plane.

This kind of connectics has been successfully used for 2 years in our dedicated CCD testbench cryovessel (2 CCDs only). The leak factor is less than  $10E-9$  mb.l/s.



**Figure 10.** MegaCam CCD Controller Hermetic Connector Prototype (external view, principle and internal view)

#### 4.11 Local DC/DC power supply

We have demonstrated the possibility to use such power supply technology in a low noise acquisition system like a CCD Controller since we have been using it successfully for 2 years in our dedicated CCD testbench. DC/DC modules followed by filter modules give less than 10mV p-p ripple and noise. In addition to simplicity of use, this technology has many advantages. The efficiency is very high (>80%) and the minimal size allows to integrate the power supply inside the Controller (see figure 1). There is no more long and big cables to install along the telescope, only a main power cable. The AC/DC input module is automatically compatible 110V/220V, which is useful when the instrument is made in Europe and installed in Hawaii. One of the 'Power board' can provide up to +5V/20A, +12V/8A, -12V/8A and +28V/3.5A i.e. a total of 400W. Each module is thermally protected but we put an additional thermistor to shut down power in case of too high temperature in the crates. A special signal is asserted some few ms before power failure. We use it to switch off properly all CCDs voltages before power down.

#### 4.12 Multi-fibers bundle

Each optical link needs 2 optical fibers. The total is then 8 fibers (two SLink x 2 + two RS232 x 2). To improve reliability and facilitate mounting and dismounting of MegaCam, the 8 optical fibers are grouped together in only one bundle, including multi-fibers connectors (see figure 11). The whole Controller is then tied to the telescope by only one optical fiber bundle (and one 110V cable). A second bundle will be available on the dome floor for the setup of MegaCam before use on the telescope. Each connector is guaranteed to have less than 0.3dB optical loss and thus doesn't put too much strain on optical budget. The 8 optical fibers forms a strong cable. The only requirement is, as usual, to protect the fibers terminals against dust, oil, etc... by screwing on the cable a dedicated cap when unused.

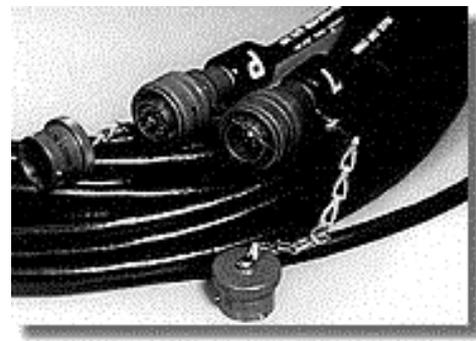


Figure 11. MegaCam CCD Controller Multi-Fibers Bundle (made by Glenair)

#### 4.13 Cooling by conduction and glycol

The whole Controller (for 40 CCDs) should dissipate about 200W at the primary focus. This is not the major part in the heat dissipation budget of MegaCam but these 200W have to be removed too. Two aluminium plates (from AAVID) cooled by glycol will be fixed to each side of the Controller crate (see figure 12). The heat of the electronics boards will be conducted to the so cooled crate aluminium walls by a 2mm special thermo-conductive gel sheet (from BergQuist) hugging the boards thickness mismatches. There is no need for any fan or hole then the crates will be totally insensitive to humidity or dust.

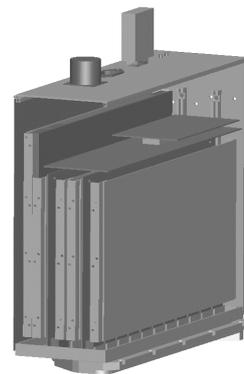
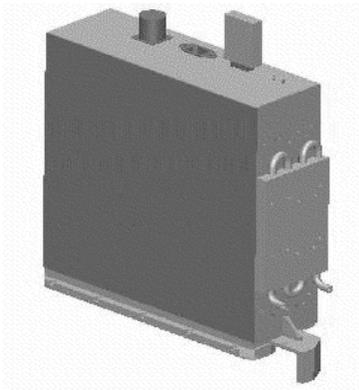


Figure 12. MegaCam CCD Controller cooled Crate (2 crates needed for the whole mosaic)

## 5. PRESENT DEVELOPMENT STATUS AND CONCLUSIONS

However the development of the MegaCam CCD Controller is not complete yet. Prototypes of all boards (except the 'Readout Board') have been built and tested in lab. Both slow and high rate optical links have been implemented (software included). A first version of the SHARC low level software is running. A test of the Controller with 2 CCDs is planned in spring and summer 2000. The final integration will take place by the end of 2000.

Thanks to high integration, the MegaCam CCD Controller found its place very close to the detectors without any conflict with other parts of the camera (cryogenic pulse tube, filter juke box, shutter, etc...). It will not put much strain on weight, dimension and dissipation budgets too. It will be at the same time the biggest CCD Controller of the world and one of the most simple.

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