Integrated Circuit Front Ends for Nuclear Pulse Processing

2010 IEEE Nuclear Science Symposium & Medical Imaging Conference

Short Course Schedule

8:30 a.m.	Welcome – Paul O'Connor
8:40 a.m.	Detector Signal Processing (Part I) – Veljko Radeka
10:00 a.m.	Break
10:20 a.m.	Detector Signal Processing (Part II) – Veljko Radeka
11:00 a.m.	Semiconductor Technology for Integrated Circuit Front Ends (Part I) – J. Oliver
12:00 p.m.	Lunch
1:10 p.m.	Semiconductor Technology for Integrated Circuit Front Ends (Part II) – J. Oliver
2:00 p.m.	Analog Circuit Design (Part I) – Paul O'Connor
3:00 p.m.	Break
3:15 p.m.	Analog Circuit Design (Part II) – Paul O'Connor
4:15 p.m.	Design Examples – all
5:15 p.m.	Discussion period

DETECTOR SIGNAL PROCESSING

Veljko Radeka - radeka@bnl.gov

1.Signal Formation and Ramo's Theorem

2. Noise Generation Mechanisms

- Generation of noise spectra
- Random telegraph Noise (RTS) and 1/f noise

3.Equivalent Noise Charge (ENC) Calculation

- ENC calculation in time and frequency domains
- Simple ENC calculation for series and parallel noise
- ENC Calculation for *1/f* noise
- 1/f noise parameters and noise corner frequency for *1/f* vs. white noise

4.Signal Processing, i.e., "filtering" or "pulse shaping“

- Weighting function of the whole detector readout system
- Correlated and uncorrelated sampling
- Optimum weighting functions

5. Charge Amplifier Configuration

Transfer of charge from detector to amplifier

6. Timing Measurements

Anti-walk techniques

7. Total Fluctuations on a Capacitance and Charge Measurement Sensitivity

"kTC noise" and correlated sampling

8. Noise from Dielectrics

9. References on Signal Processing for Radiation Detectors

Appendix

A.1 Noise calculation: Time domain and Frequency domain
A.2 Parallel Noise in devices with Avalanche Gain
A.3 Noise Figure and Noise Temperature
A.4 Noise in Resistors at Different Temperatures and "Electronic Cooling" by Feedback
A.5 Zero-crossing statistics of noise
A.6 Autocorrelation function as a diagnostic tool
A.7 Pileup effects *vs* shaping

1. Signal Formation and Ramo's Theorem

Induced Current and Charge

S. Ramo, Proc. IRE, 27(1939) 584
(and W. Shockley)

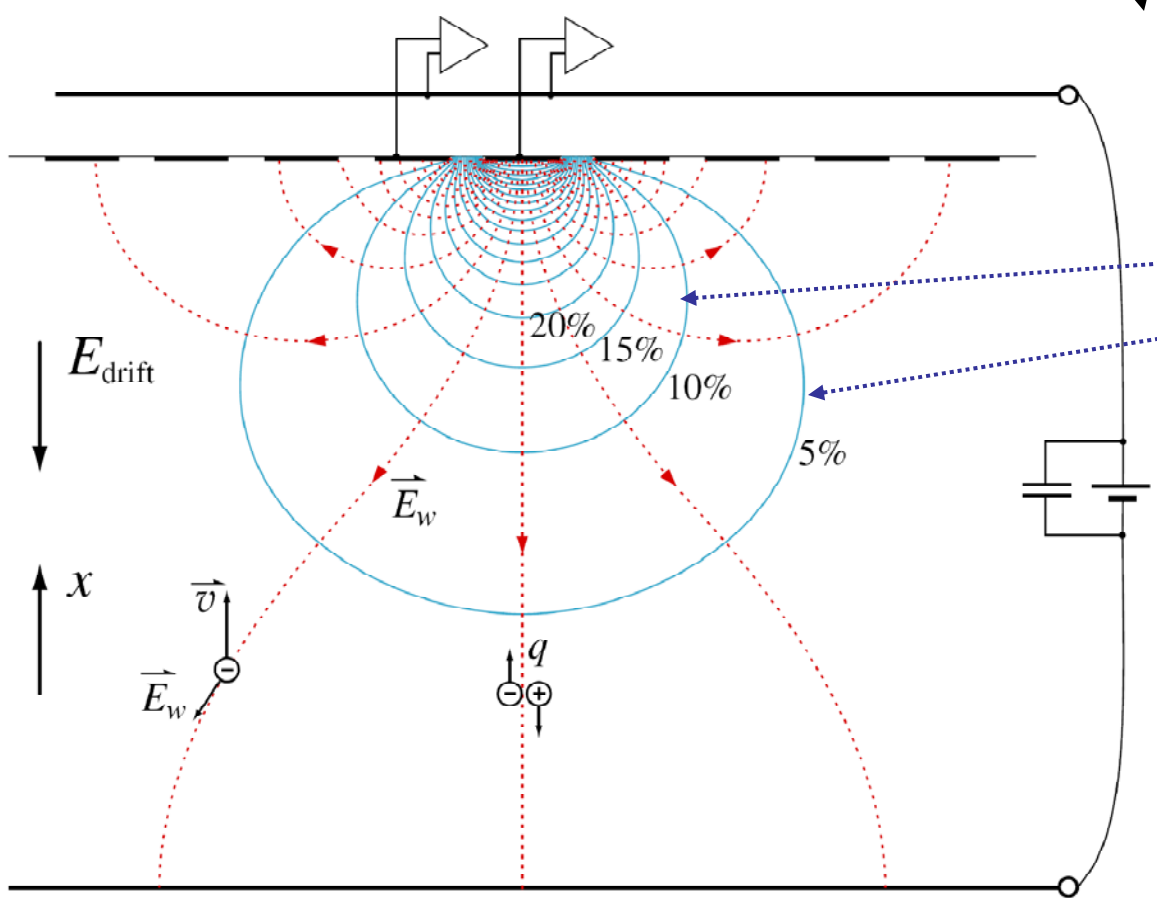
Weighting field

$$i = -q\vec{E}_w \times \vec{v}$$

$$v = dx/dt$$

$$Q_s = \int i dt = +q\int \vec{E}_w d\vec{x}$$

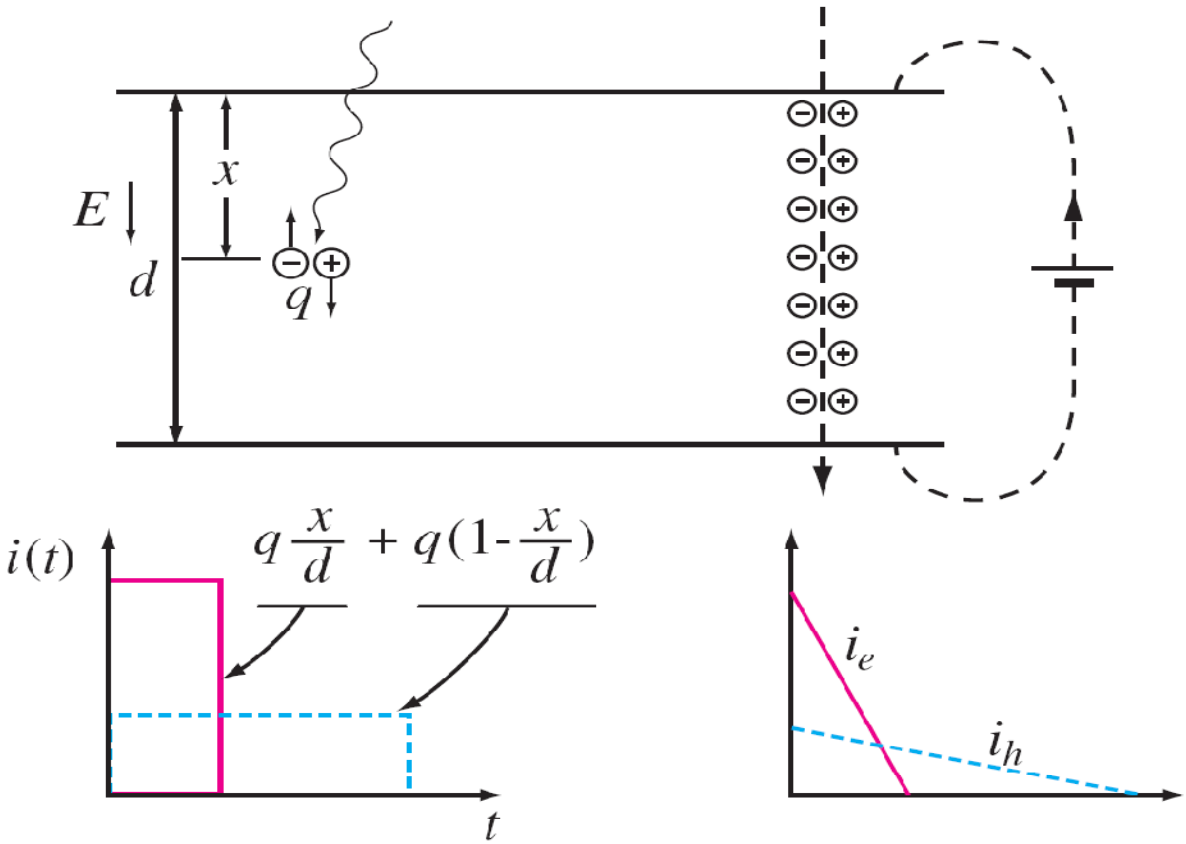
$$Q_s(1,2) = q(V_{w2} - V_{w1})$$



Weighting potentials

4

The Simplest Case: Induced Currents in Continuous Planar Electrodes for Localized and Extended Ionization in Semiconductor, Gas and Liquid Detectors



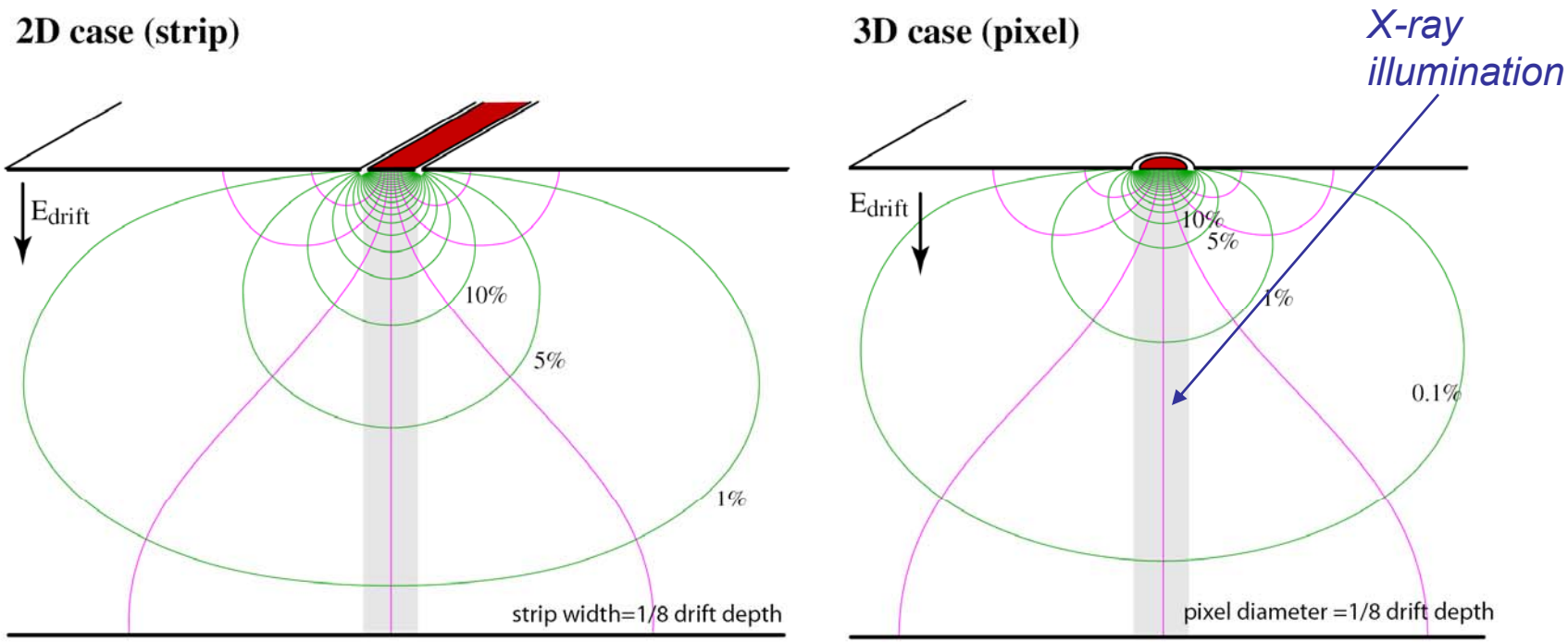
$$E_w = \frac{1}{d}$$

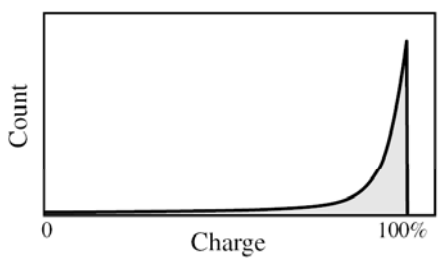
Carrier drift velocity

$$i = q \cdot \frac{v}{d} = \frac{q}{t_d}$$

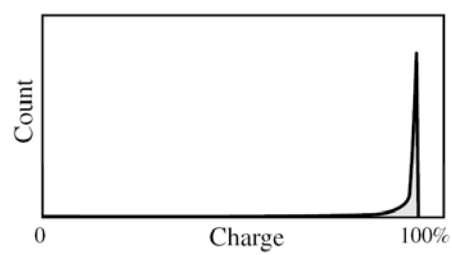
Carrier transit time

Weighting Potential and Pulse Height Distribution for Strips vs Pixels





Comparison of their theoretical induced charge pulse height distributions. Assuming an ionization event creates a point charge, and the absorption probability is constant along the depth.



2. Noise mechanisms

A Model for Generation of Noise Spectra

$$h(t) \overset{F}{\Leftrightarrow} H(j\omega)$$

Random sequence of impulses

White noise with 1st order band limit (relaxation process)

$$\frac{1}{\tau} e^{-\frac{t}{\tau}} \Leftrightarrow \frac{1}{1 + j\omega\tau}$$

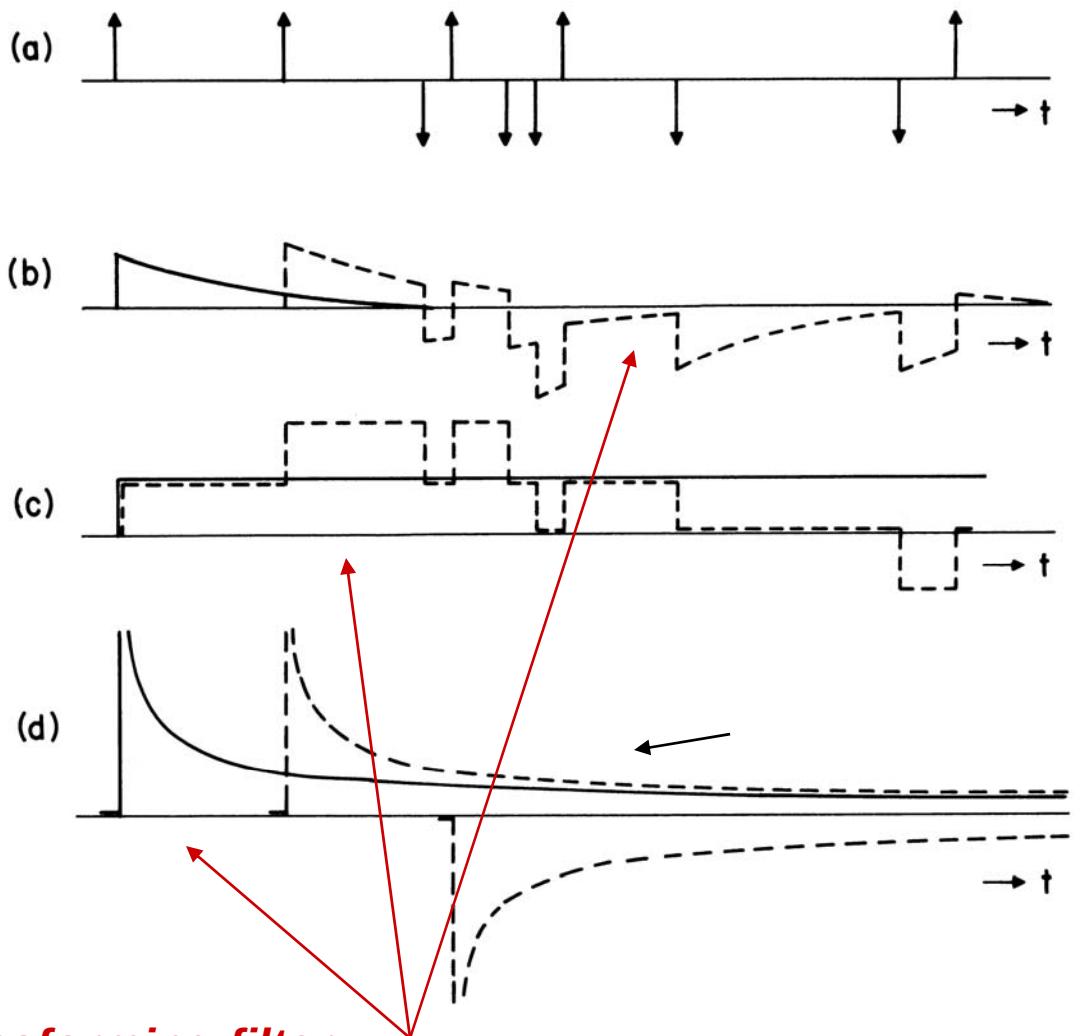
1/f ^{2} noise

(random walk)

$$U(t) \Leftrightarrow 1/j\omega$$

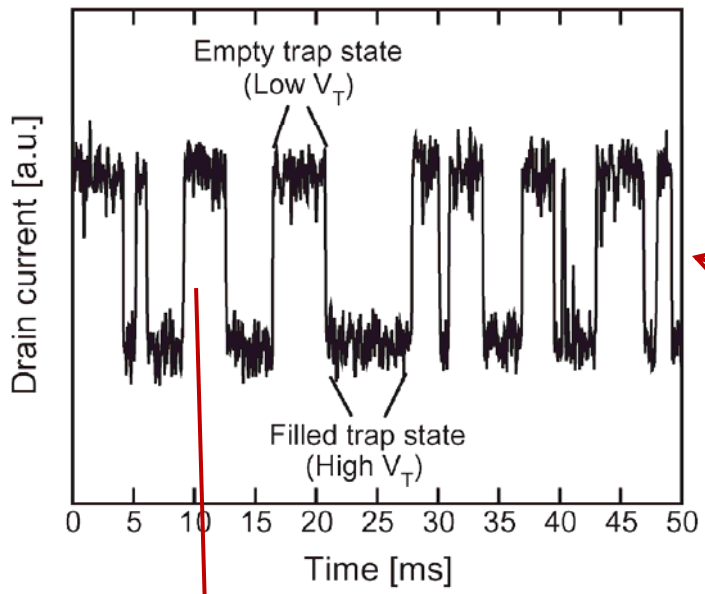
1/f noise

$$U(t)/t^{1/2} \Leftrightarrow 1/(j\omega)^{1/2}$$

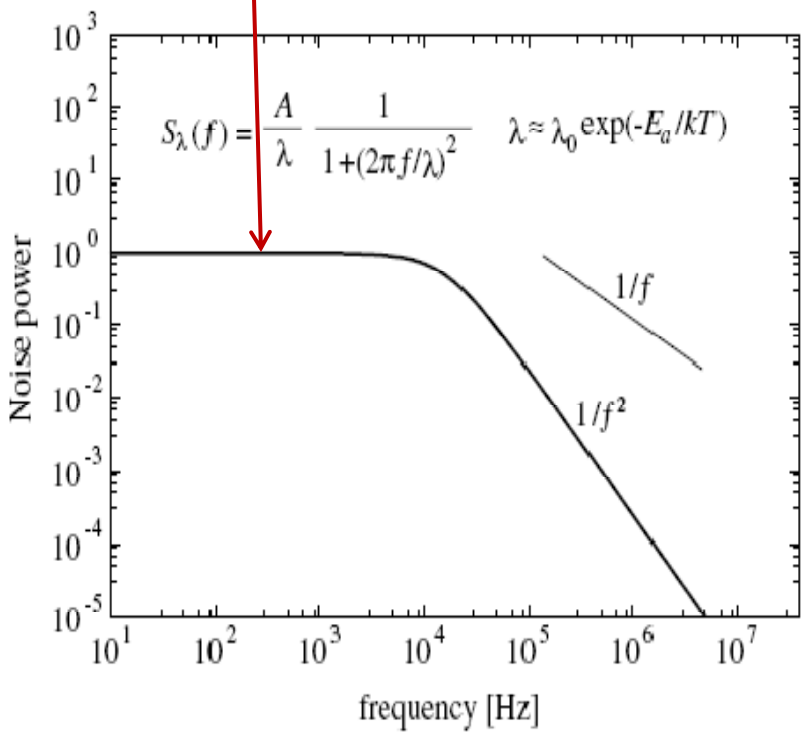


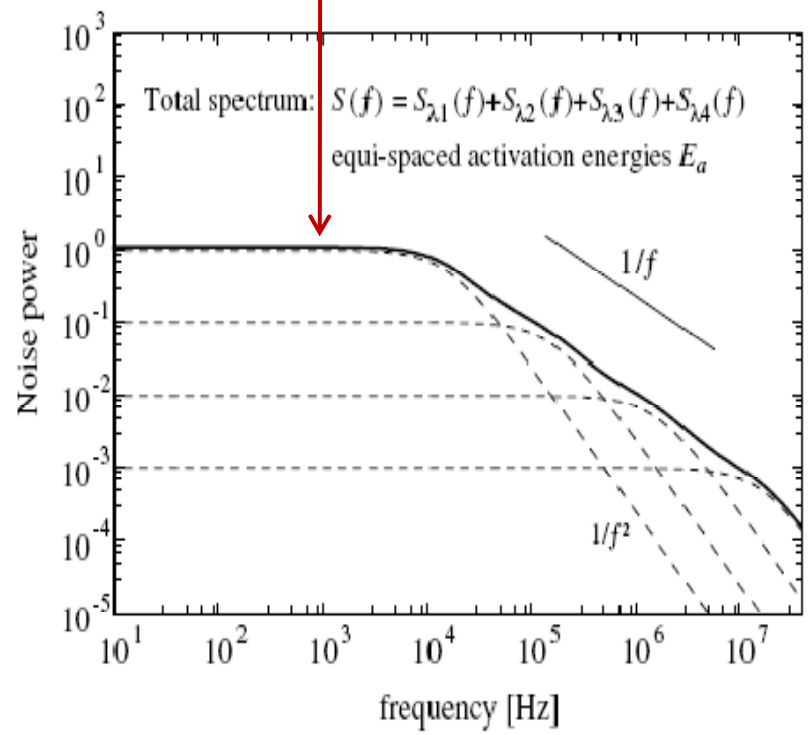
White noise × ***transforming filter***=

Low frequency Noise: Trapping Noise – from RTS (Random Telegraph Noise to 1/f Noise

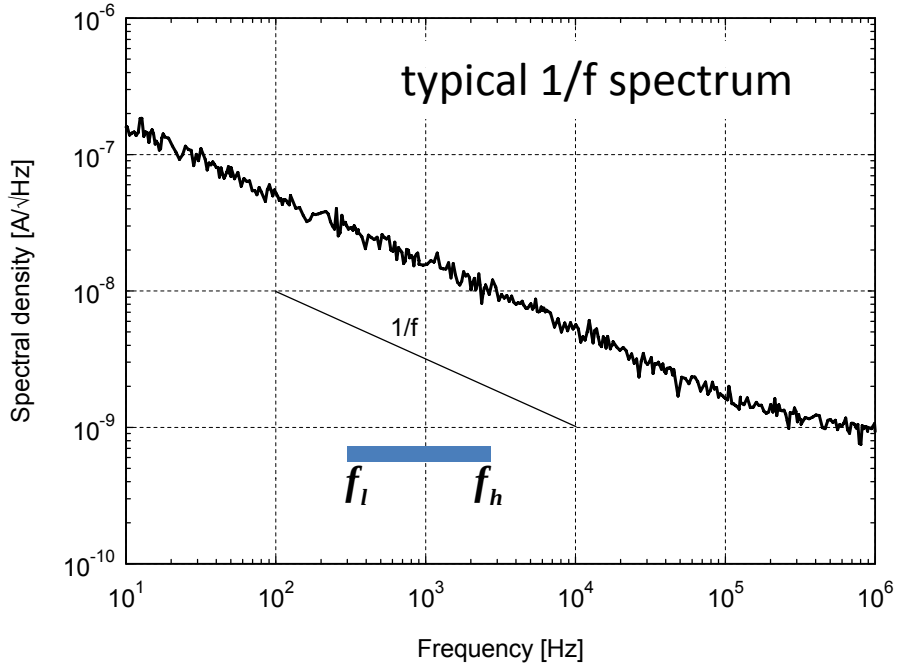


- Single trap → Lorentzian spectrum
- Distribution of traps → 1/f spectrum





“Self-similarity” of 1/|*f*| Noise (scaling invariance)



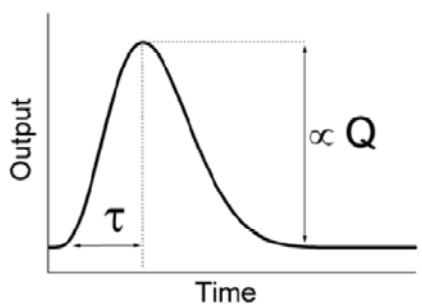
$$\sigma(f_l, f_h) \propto \left(\ln \frac{f_h}{f_l}\right)^{1/2} \quad rms$$

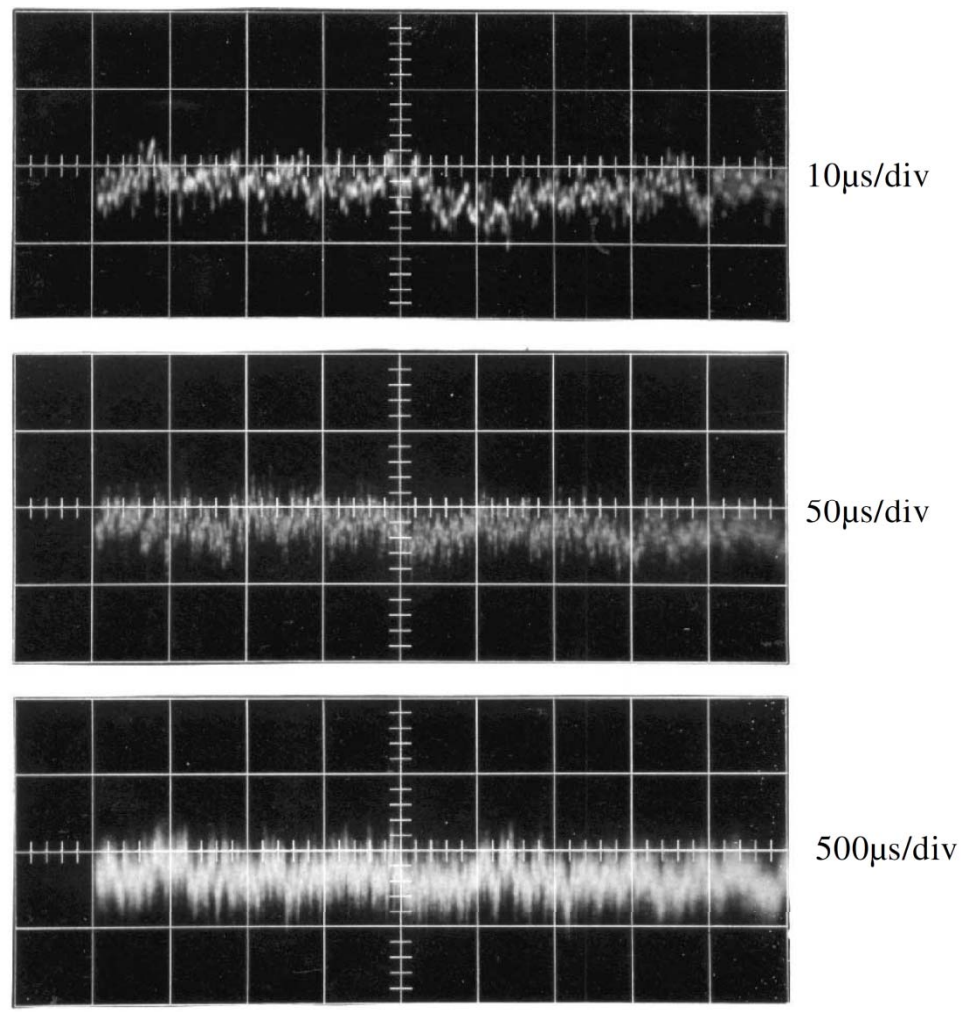
Variance (noise power):

$$\sigma(f_l, f_h)^2 = \int_{f_l}^{f_h} \frac{A_f}{f} df = A_f \ \ln \frac{f_h}{f_l}$$

$\sigma(f_l, f_h)$ constant for same ratio f_h/f_l

i.e., independent of shaping (peaking time) $\boldsymbol{\tau}$

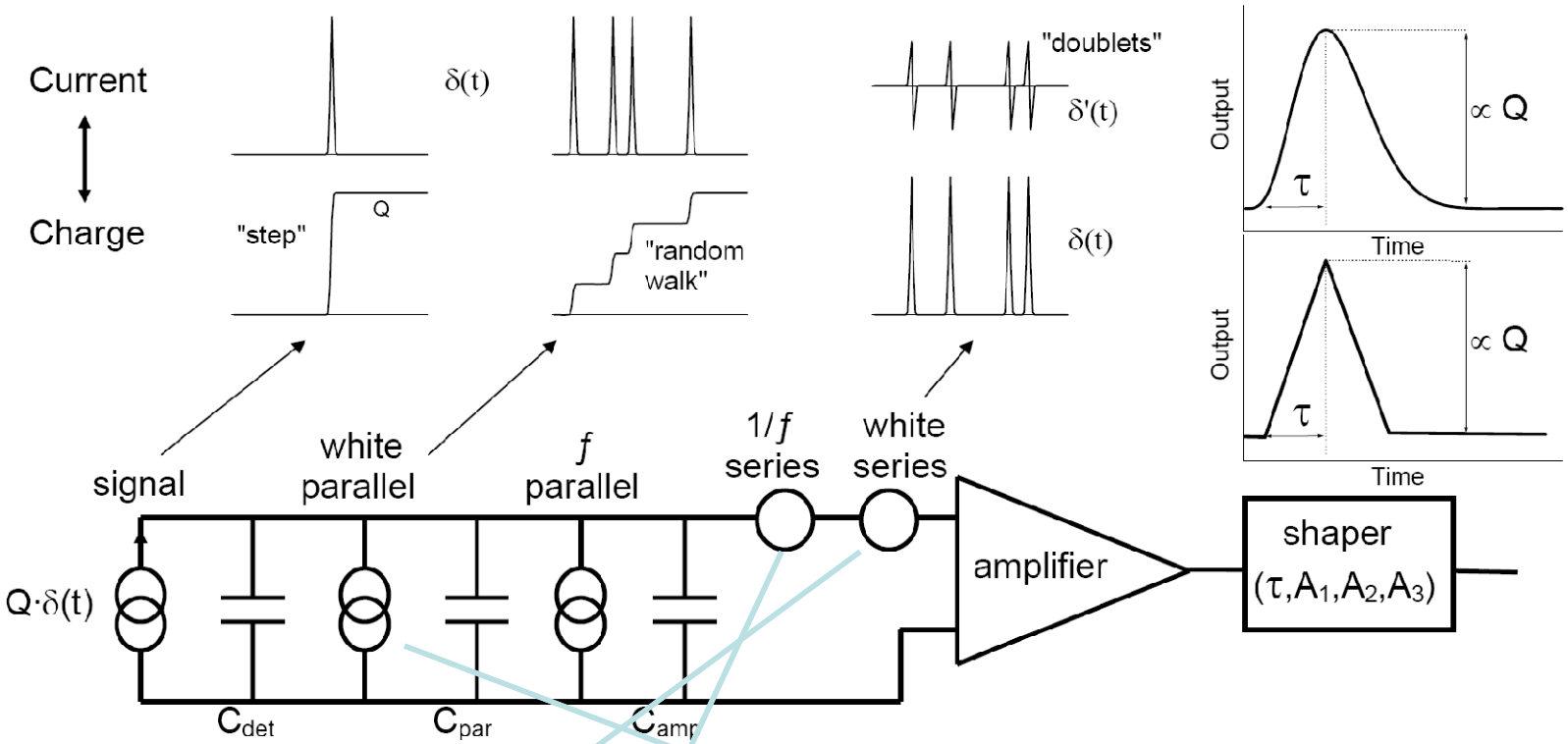




1/|*f*| noise — different time scales

3. Equivalent noise charge (ENC) calculation

Noise Sources and Spectral Densities in Charge Amplifiers



$$v_n^2 = e_n^2 + \frac{2\pi A_f}{\omega} + 2q_e I_0 \frac{1}{C_{in}\omega^2}$$

$$i_{neq}^2 = v_n^2 \omega^2 C_{in}^2 = \omega^2 C_{in}^2 e_n^2 + 2\pi C_{in}^2 A_f \omega + 2qI_0$$

Noise spectral density:

Voltage: $e_n \left[nV/Hz^{1/2} \right]$

Current: $I_0 \left[fA, pA, nA, \ldots \right]$

Equivalent Noise Charge (ENC) – Integrals and Coefficients A1, A2, A3

$$ENC^2 = \frac{1}{2\pi}\int_0^{\infty} i_{neq}^2 \left|H(\omega)\right|^2 d\omega = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left(\tfrac{1}{2}\right) i_{neq}^2 \left|H(\omega)\right|^2 d\omega$$

$$ENC^2 = \tfrac{1}{2} e_n^2 C_{in}^2 I_1 + \pi C_{in}^2 A_f I_2 + q I_0 I_3 = \tfrac{1}{2} e_n^2 C_{in}^2 \frac{A_1}{\tau} + \pi C_{in}^2 A_f A_2 + q I_0 A_3 \tau$$

$$I_1 = \int_{-\infty}^{\infty} \left[w'(t)\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|H(j\omega)\right|^2 \omega^2 d\omega = \frac{A_1}{\tau}$$

Series white

$$I_2 = \int_{-\infty}^{\infty} \left[w^{(1/2)}\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|H(j\omega)\right|^2 \omega\, d\omega = A_2$$

1/f

$$I_3 = \int_{-\infty}^{\infty} \left[w(t)\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|H(j\omega)\right|^2 d\omega = A_3 \tau$$

Parallel white

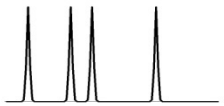
Time domain (weighting function)

Frequency domain (transfer function)

ENC Calculation in Time domain: *Weighting Function Role*

$\delta'(t)\ C_{in}$ white "series" noise

$$ENC_S^2 = \frac{1}{2}\overline{e_n^2}\ C_{in}^2 \overbrace{\int [w'(t)]^2 dt}^{I_1}$$



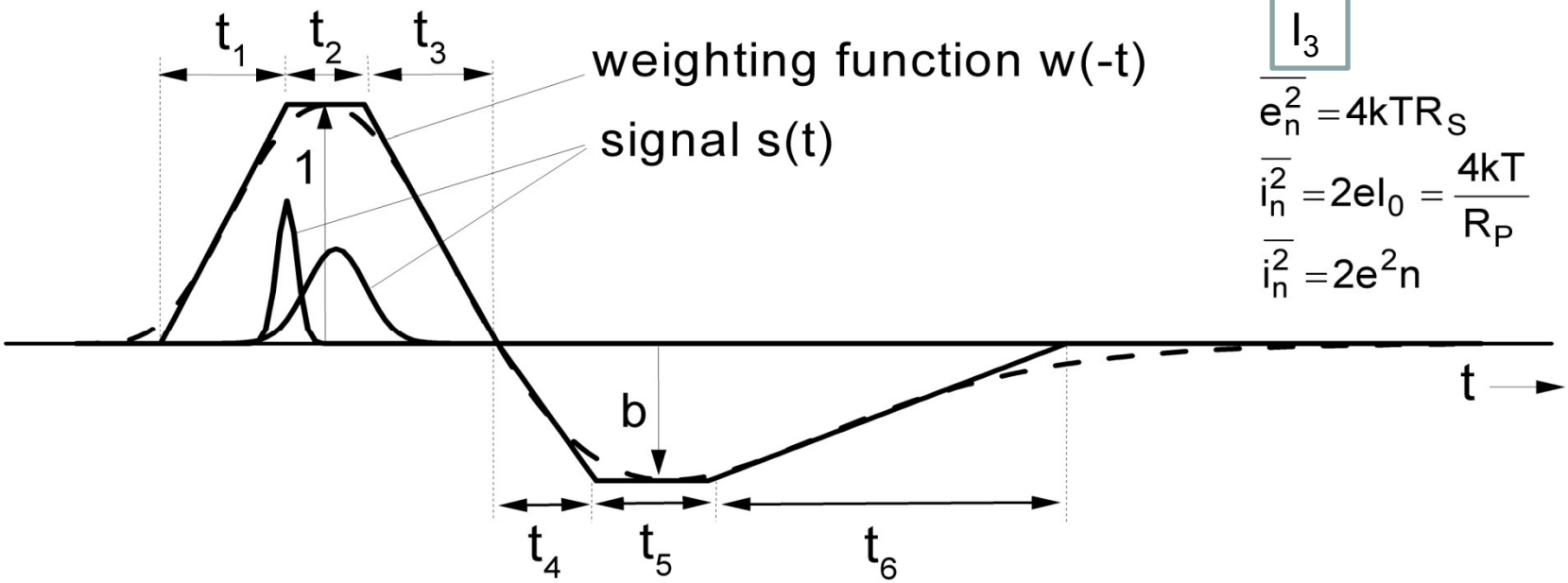
$\delta(t)$ white "parallel" noise

$$ENC_P^2 = \frac{1}{2}\overline{i_n^2} \underbrace{\int [w(t)]^2 dt}_{\boxed{I_3}}$$

$$\overline{e_n^2} = 4kTR_S$$

$$\overline{i_n^2} = 2eI_0 = \frac{4kT}{R_P}$$

$$\overline{i_n^2} = 2e^2 n$$



$$I_1 = \frac{1}{t_1} + 0 + \frac{1}{t_3} + b^2\frac{1}{t_4} + 0 + b^2\frac{1}{t_6}$$

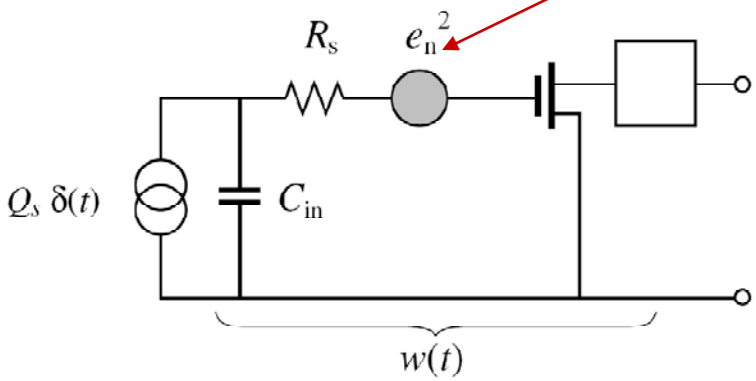
$$\boxed{I_3} = \frac{t_1}{3} + t_2 + \frac{t_3}{3} + b^2\frac{t_4}{3} + b^2 t_5 + b^2\frac{t_6}{3}$$

ENC Calculation in Time Domain

V.R., Ann. Rev. 1988
R. Wilson, Phil. Mag., 1950

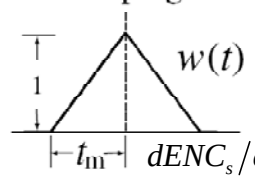
Simple ENC Calculation for ***Series*** White Noise

$$ENC_s^2 = \tfrac{1}{2}\, 4kTR_s C_{in} \bullet I_1$$



$$A_1 = I_1 t_m = 2$$

Shaping:



$$dENC_s / dC_{in} = e_n / t_m^{1/2} \quad [\ ]$$

$$I_1 = \int_{-\infty}^{\infty} w'^2(t)dt = 2/t_m$$

(for 5th order semi-gaussian $I_1 = 2.2$)

$$ENC_s = e_n C_{in} / t_m^{1/2}$$

Noise slope:

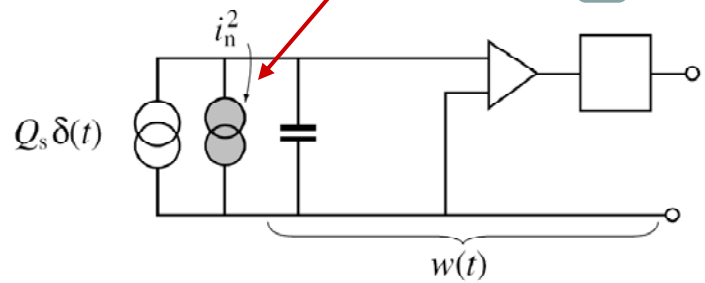
$e_n = 1\ \text{nV/Hz}^{1/2}$
$C_{in} = 1\ \text{pF}$
$t_m = 1\ \mu\text{s}$

$\rightarrow ENC_s \approx 6$ rms e $\rightarrow \Delta ENC_s / \Delta C_{in}$

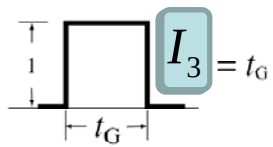
e_n = series noise (voltage) spectral density [V/Hz$^{1/2}$]
$e_n C_{in}$ = series noise (charge) spectral density [e/Hz$^{1/2}$]

Simple ENC Calculation for ***Parallel*** White Noise

$$ENC_p^2 = \tfrac{1}{2}\, \underbrace{2\, eI_o}_{i_n^2} \bullet I_3 \qquad I_3 = \int_{-\infty}^{\infty} w^2(t)\,dt$$



1. Assume a gated integrator for $w(t)$:



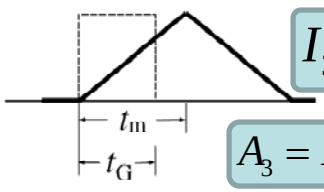
$I_3 = t_G$

$$ENC_p = (eI_o t_G)^{1/2} = (e^2 n t_G)^{1/2} = e(n t_G)^{1/2} = e\, n_G^{1/2}$$

$$ENC_p / e = n_G^{1/2} \quad \text{[rms e]}$$

1 nA in 1μs → $n_G = 6250$ e, $ENC_p = 79$ rms e

2. Triangular weighting function (similar to semi-gaussian)



$I_3 = \frac{2}{3} t_m$

$A_3 = I_3 / t_m = 2/3$

$$ENC_p / e = (2nt_m/3)^{1/2}$$

equal ENC_p for: $t_G = 2t_m/3$

3. Resistor noise = shot noise: $4kT/R_p = 2\, eI_o$

for $R_p I_o = 50$ mV at 293K

Calculation of ENC for 1/f Noise

From slides 12, 13:

$$ENC_f^2 = \pi C_{in}^2 A_f A_2$$

$$A_2 = \int_{-\infty}^{\infty} \left[w^{(1/2)}(t) \right]^2 dt$$

($w^{(1/2)}$=fractional order derivative)

It can be shown that:

$$A_2 \le (A_1 A_3)^{(1/2)}$$

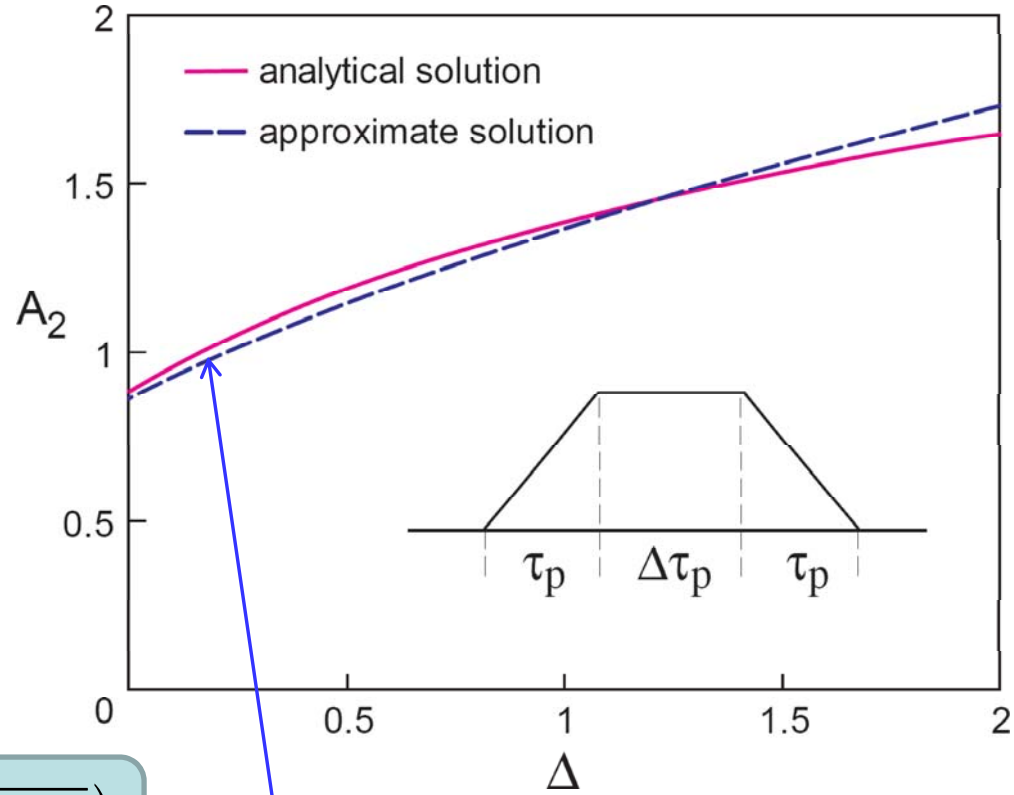
An approximation for practical purposes (*ENC_f to 10%):*

$$A_2 \approx 0.75 (A_1 A_3)^{1/2}$$

$$ENC_f^2 = \pi C_{in}^2 A_f A_2 \approx \pi C_{in}^2 A_f \left(0.75 \sqrt{A_1 A_3} \right)$$

Transistor technology constant (~independent of transistor size) :

$$K_f = A_f C_{gs} \qquad \left[(V^2)(As/V) \right] = [VAs] = [Joule]$$



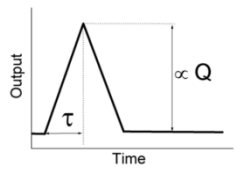
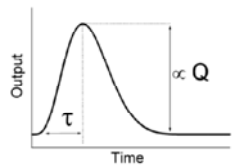
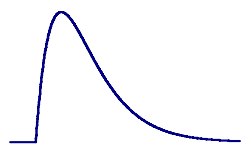
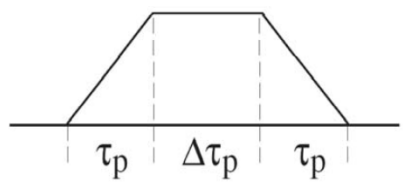
Trapezoidal weighting function (e.g., dual slope integrator):

$$A_1 = 2$$

$$A_3 = \left(\Delta + 2/3 \right)$$

$$A_2 \approx 0.75 \left[2 \left(\Delta + 2/3 \right) \right]^{1/2}$$

Weighting Function Noise Coefficients

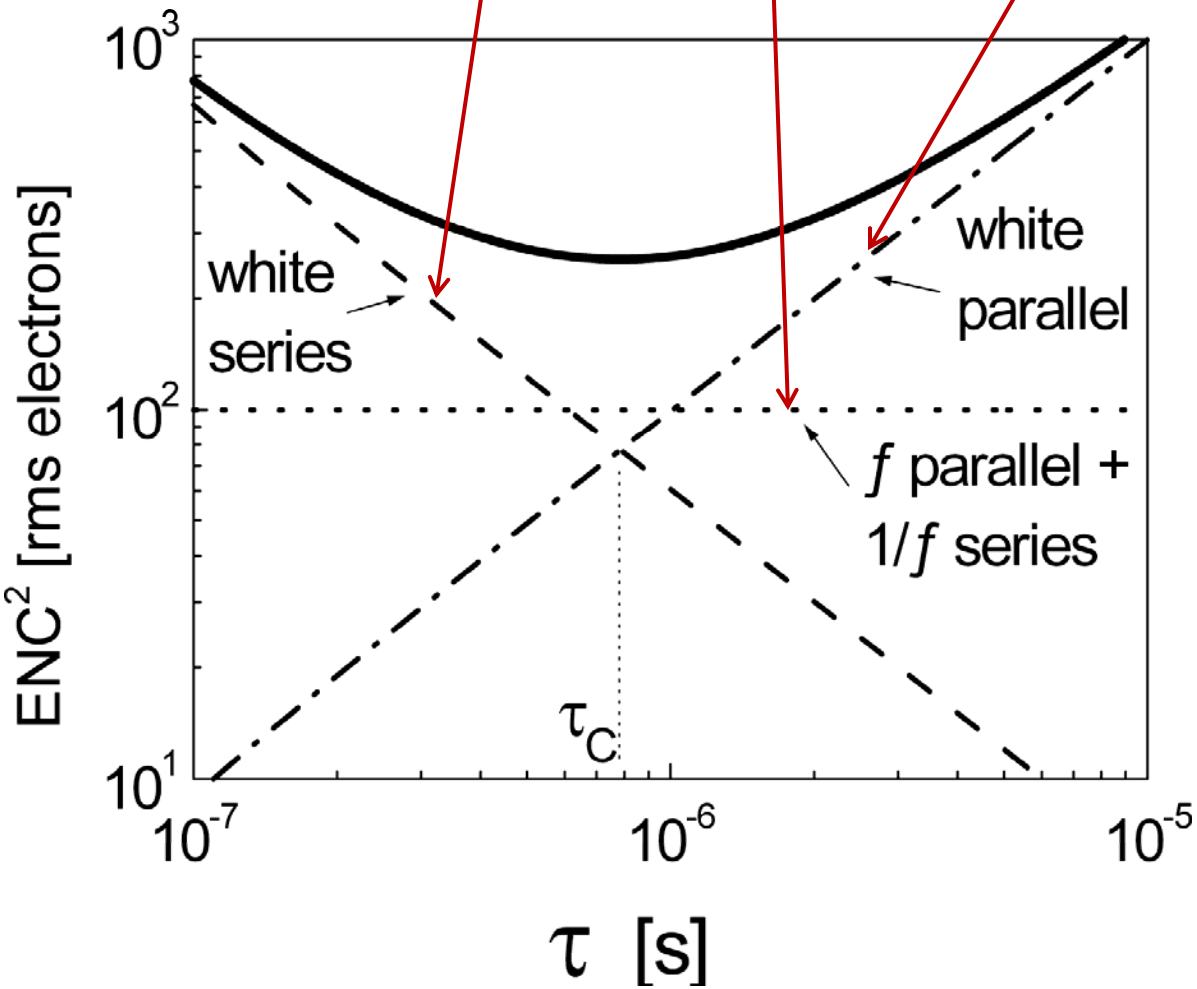
Weighting function	Series white A_1	Parallel white A_3	Series *1/f* $A_{2(calc)}$	Series 1/f $A_{2(approx)} \approx 0.75(A_1A_3)^{1/2}$
triangle 	2	2/3	0.88	.87
semi-gaussian 4th order 	2.04	0.90	1.04	1.01
CR-RC 	1.85	1.85	1.18	1.39
trapezoidal Δ=1 	2	1.67	1.38	1.37

$$ENC^2 = \tfrac{1}{2} e_n^2 C_{in}^2 \frac{A_1}{\tau} + \pi C_{in}^2 A_f A_2 + q I_0 A_3 \tau$$

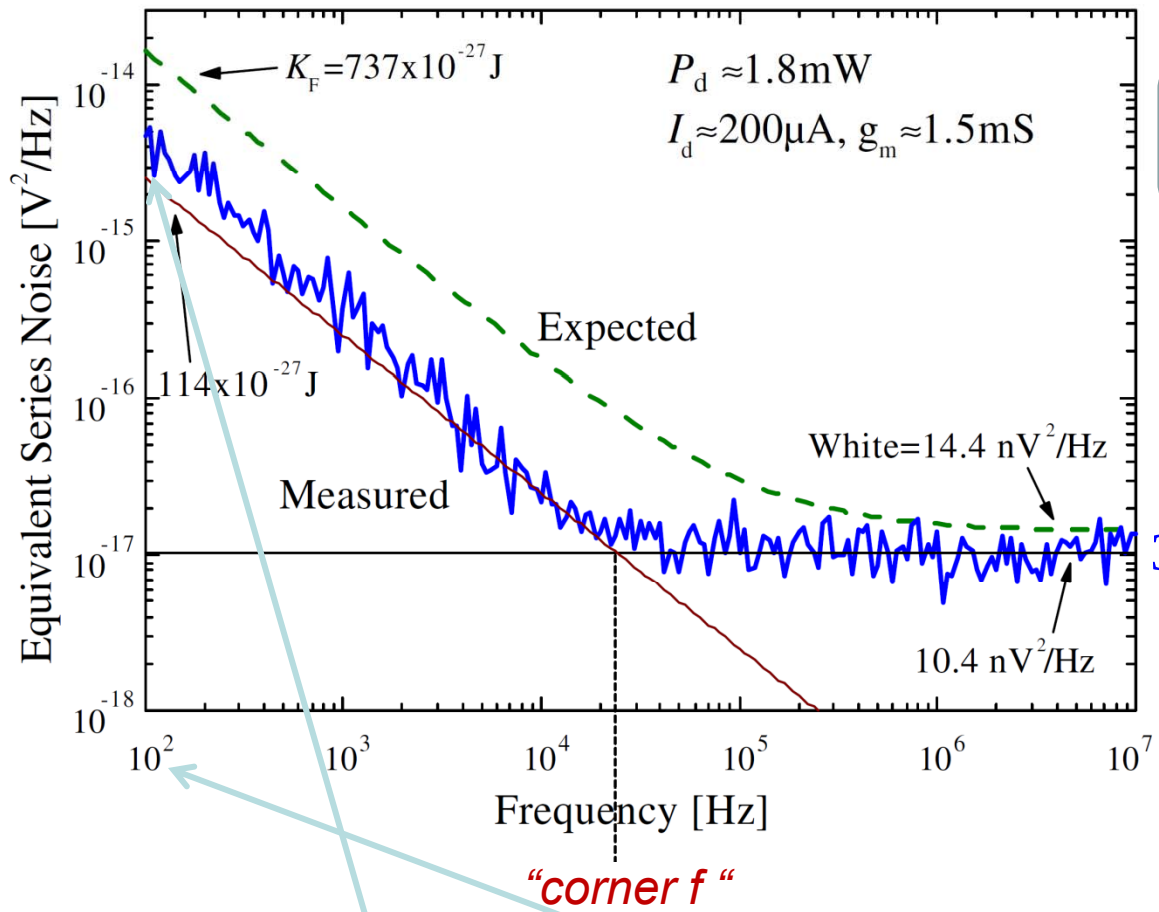
ENC vs shaping (peaking time):

$$ENC^2 \approx \frac{e_n^2 C_{in}^2}{\tau} + \pi C_{in}^2 A_f + qI_0 \tau$$

(Semigaussian 4th order)



1/f Noise parameters: *corner frequency, "technology constant" K_f and "measurement constant" A_f*



"corner f "

Measure:

$$\frac{K_f}{C_{ox}WLf} = \frac{A_f}{f} = v_n^2 \quad \left[(rms\,volts)^2\right]$$

$$K_f = (C_{ox}WL)A_f \left[joules\right]$$

$3nV/Hz^{1/2}$

$$e_n^2 = \gamma 4kT/g_m \;;\gamma \simeq 2/3$$

$$K_{fN} \sim 10K_{fP}$$

$$K_{fN} \sim 10^{-25}\,J$$

$$K_{fJFET} \sim 10^{-27}\,J$$

$$A_f = v_n^2 f \approx (3x10^{-15-}V^2/Hz)\cdot(10^2\,Hz) = 3x10^{-13}V^2$$

Low-frequency noise in CMOS: slope and dependence on L

(Adapted from: G. De Geronimo and P. O'Connor, Ref. 39)

$$S_f = \frac{K_f}{C_{ox}\mathbf{WL}f}$$

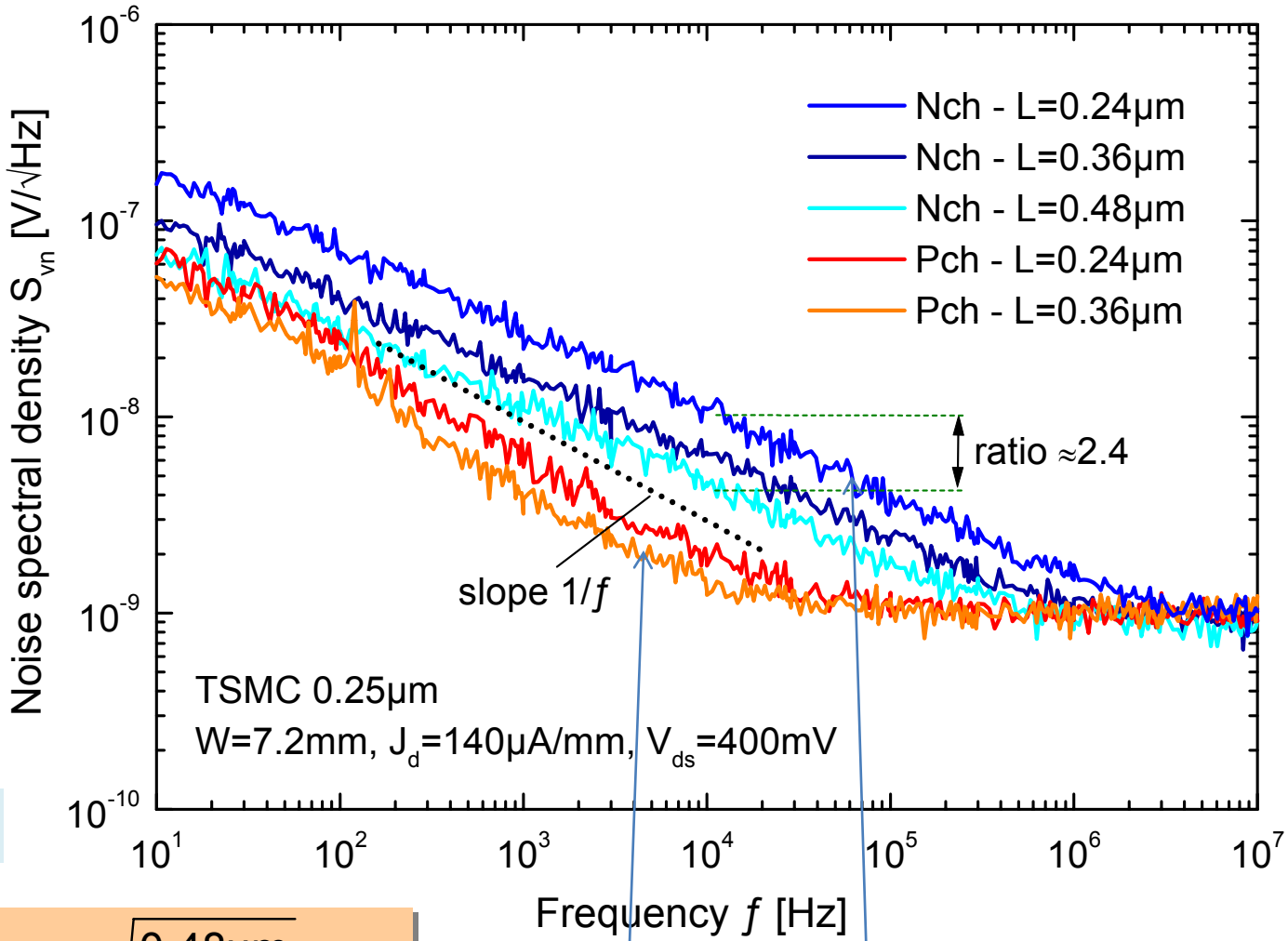
↓

$$S_f = \frac{K_f(\mathbf{L})}{C_{ox}\mathbf{WL}f^{\alpha_f}}$$

TSMC 0.25µm

measured :

$0.85 < a_f < 1.08$



$5\times10^{-25} < K_f < 2.7\times10^{-24}$

$$\text{ratio} \approx 2.4 \quad >> \quad \approx \sqrt{\frac{0.48\mu m}{0.24\mu m}} \approx 1.4$$

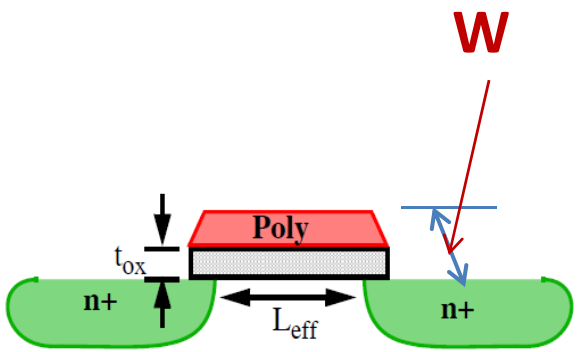
What do different transistors have in common?
-- *Fluctuations associated with the gain mechanism*

Intrinsic (white) noise, although from a different mechanism for each device type, can be expressed by the transconductance in terms of the equivalent noise resistance,

$$R_{neq} = \gamma / g_m$$

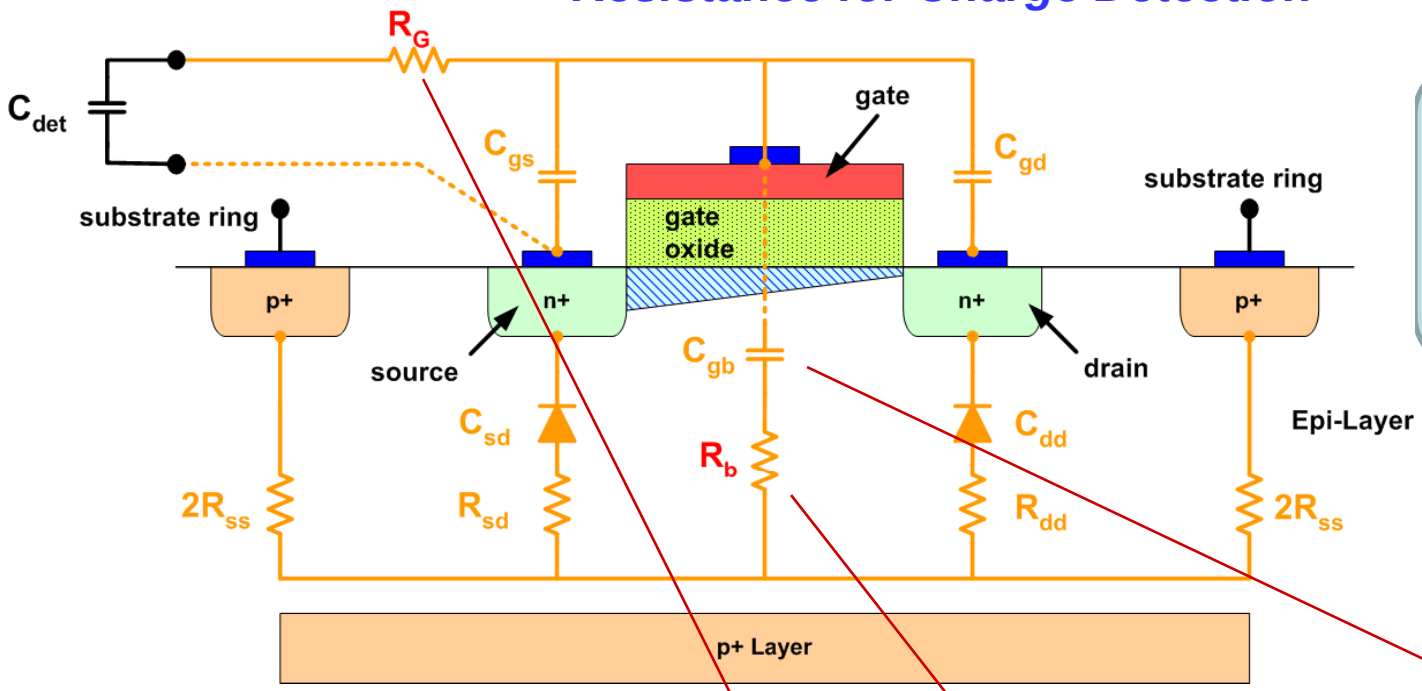
$\gamma - values:$

BJT	1/2
JFET	2/3
CMOS (strong inv..)	2/3
CMOS (weak inv.)	1/2
CMOS <~180nm	>2/3



Noise (voltage) spectral density: $$e_n^2 = 4kT \frac{\gamma}{g_m}$$

Additional (white) noise sources in MOSFETs: and Equivalent Series Noise Resistance for Charge Detection



"Intrinsic" channel noise:

$$e_n^2 = 4kTR_n\,;\; R_n = \gamma / g_{ms}$$

$$\gamma \geq 2/3 \text{ for FETs}$$

$$\gamma = 1/2 \text{ for BJTs}$$

$$\frac{R_{eq}}{\gamma / g_{ms}} = 1 + \frac{\delta}{5\gamma}\left(\frac{C_{gs}}{C_{in}}\right)^2 + \frac{1}{\gamma}\left(R_g g_{ms}\right) + \left(R_b g_{mb}\right)\frac{g_{mb}}{g_{ms}} + \frac{1}{\gamma}\left(R_b g_{ms}\right)\left(\frac{C_{gb}}{C_{in}}\right)^2$$

Gate induced

«1

Intrinsic channel noise

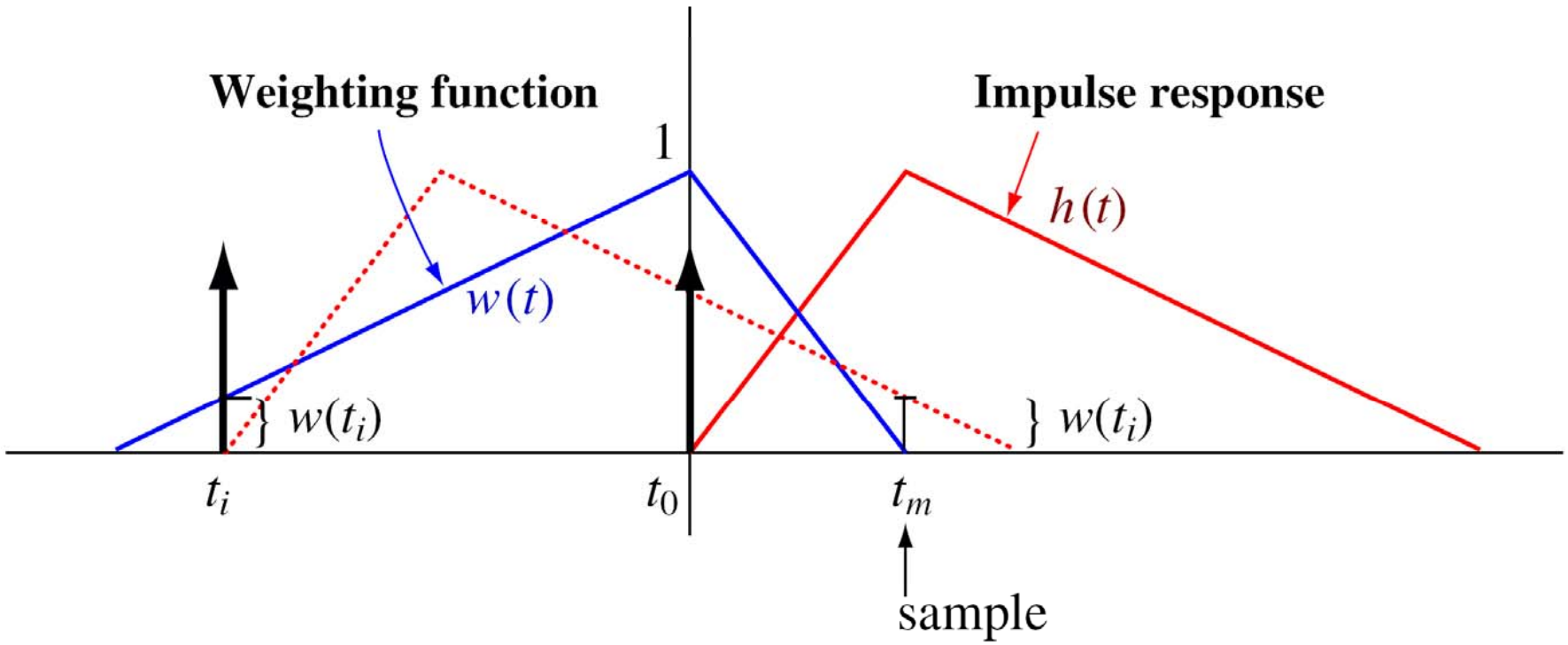
Gate resistance

Substrate resistance

Induced into gate (shielded by the inversion layer!?)

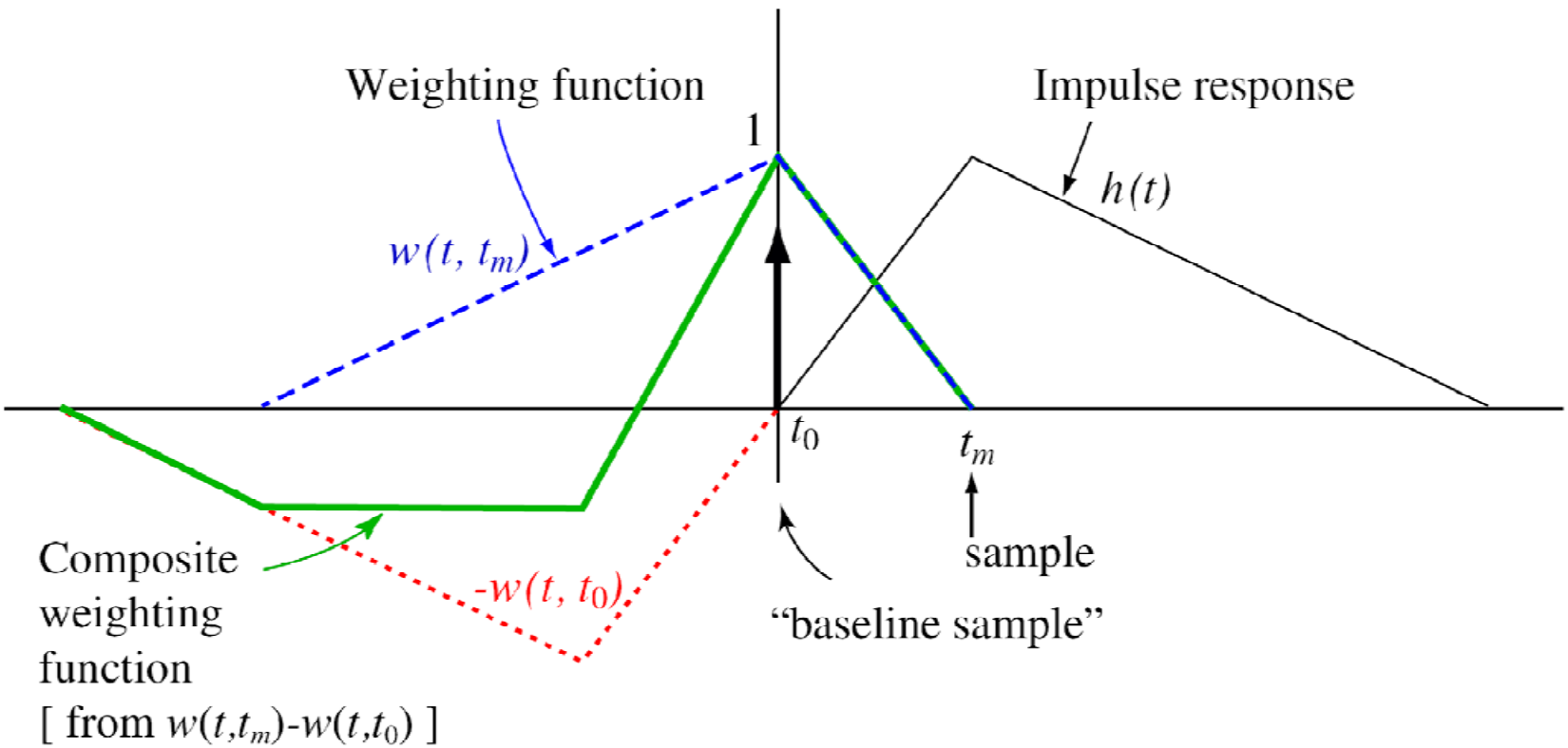
4. Signal processing, i.e., “filtering” or “pulse shaping”

Weighting Function



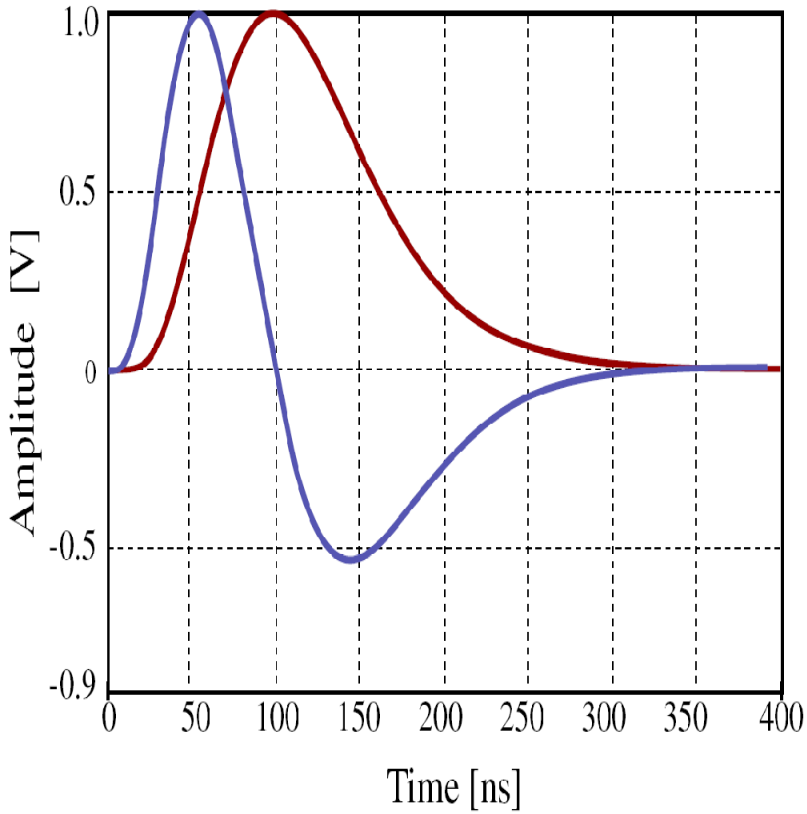
∴ Each sample carries a memory of the past events determined by the impulse response of the system preceding the sampler.

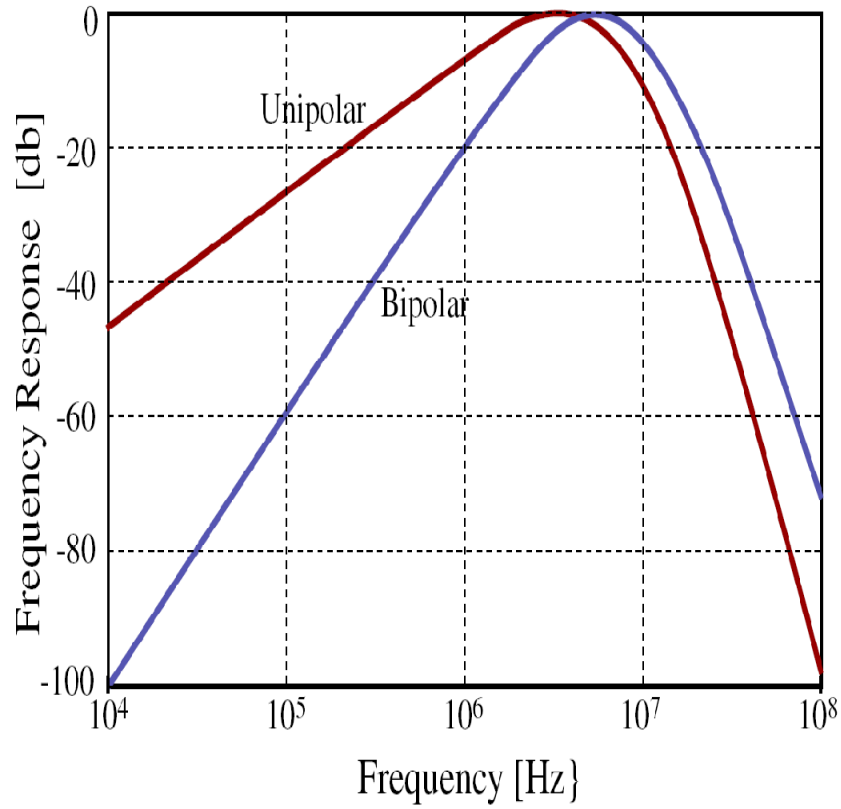
Composite Weighting Function for Correlated Double Sampling



∴ Each sample carries a memory of the past events determined by the impulse response of the system preceding the sampler.

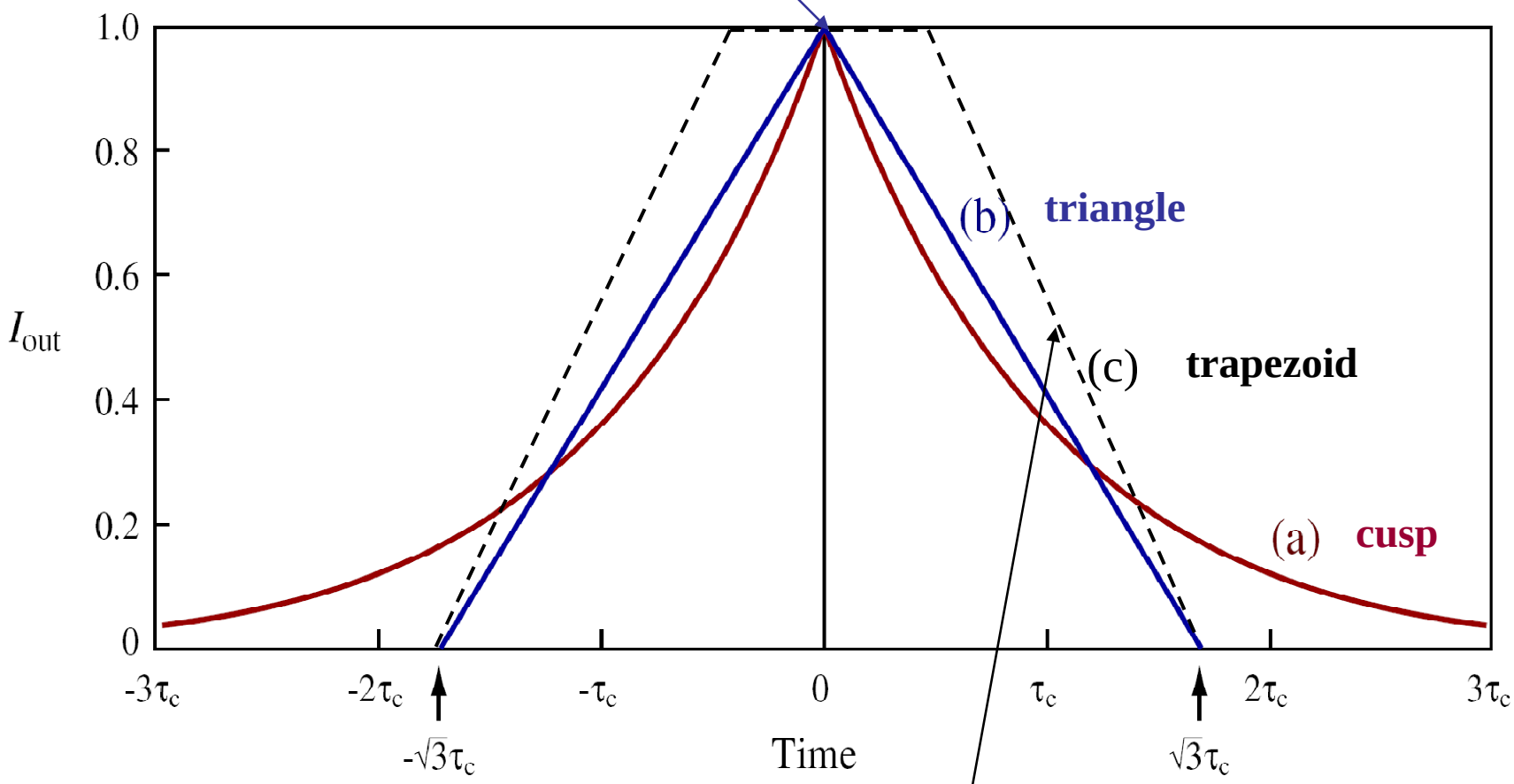
Transfer Functions in Time and Frequency Domains





Optimum Filter for Amplitude Measurement

(delta function signal current)

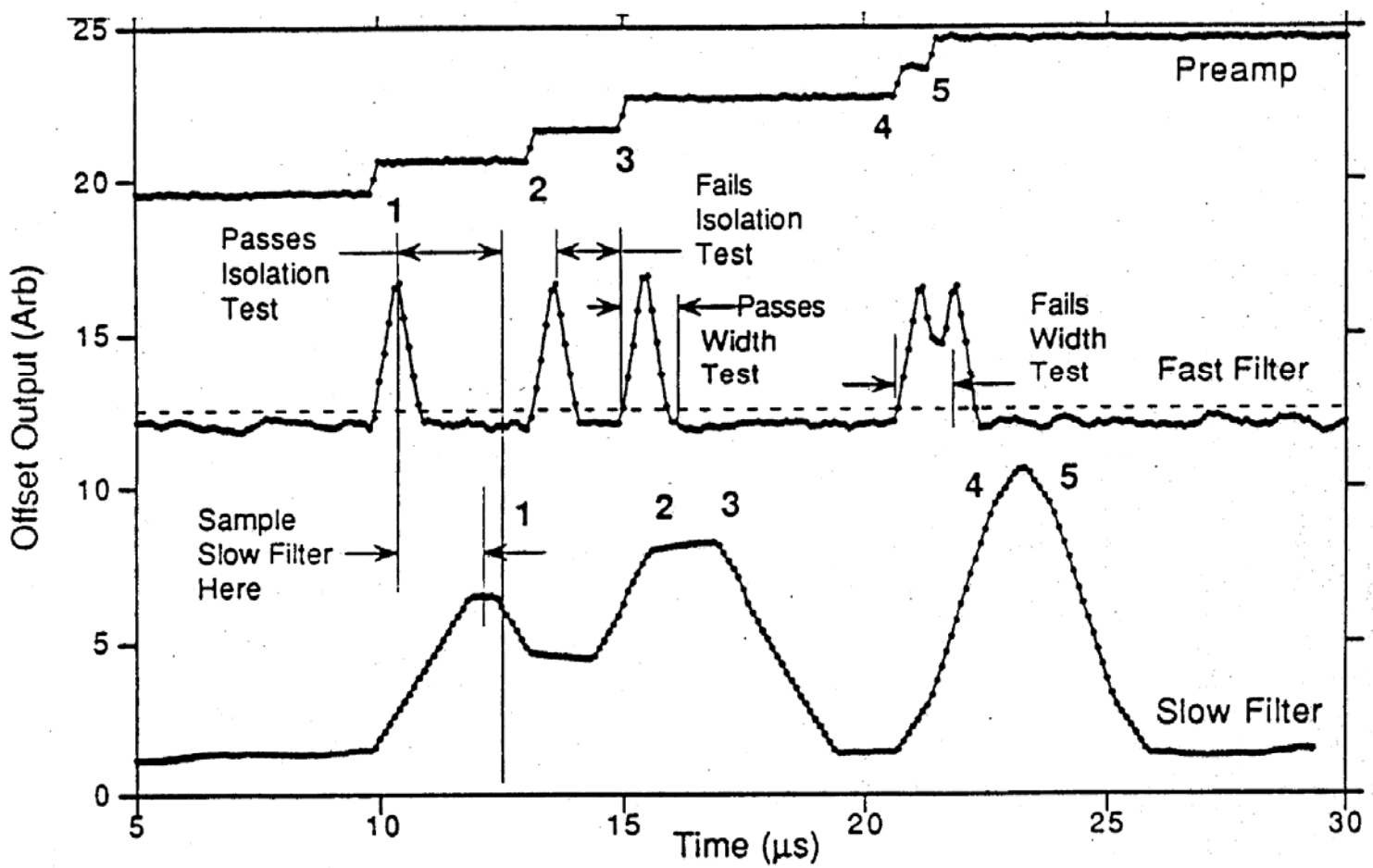


τ_c= noise corner time constant

Trapezoid w(t) for reduced ballistic deficit with finite width signal current

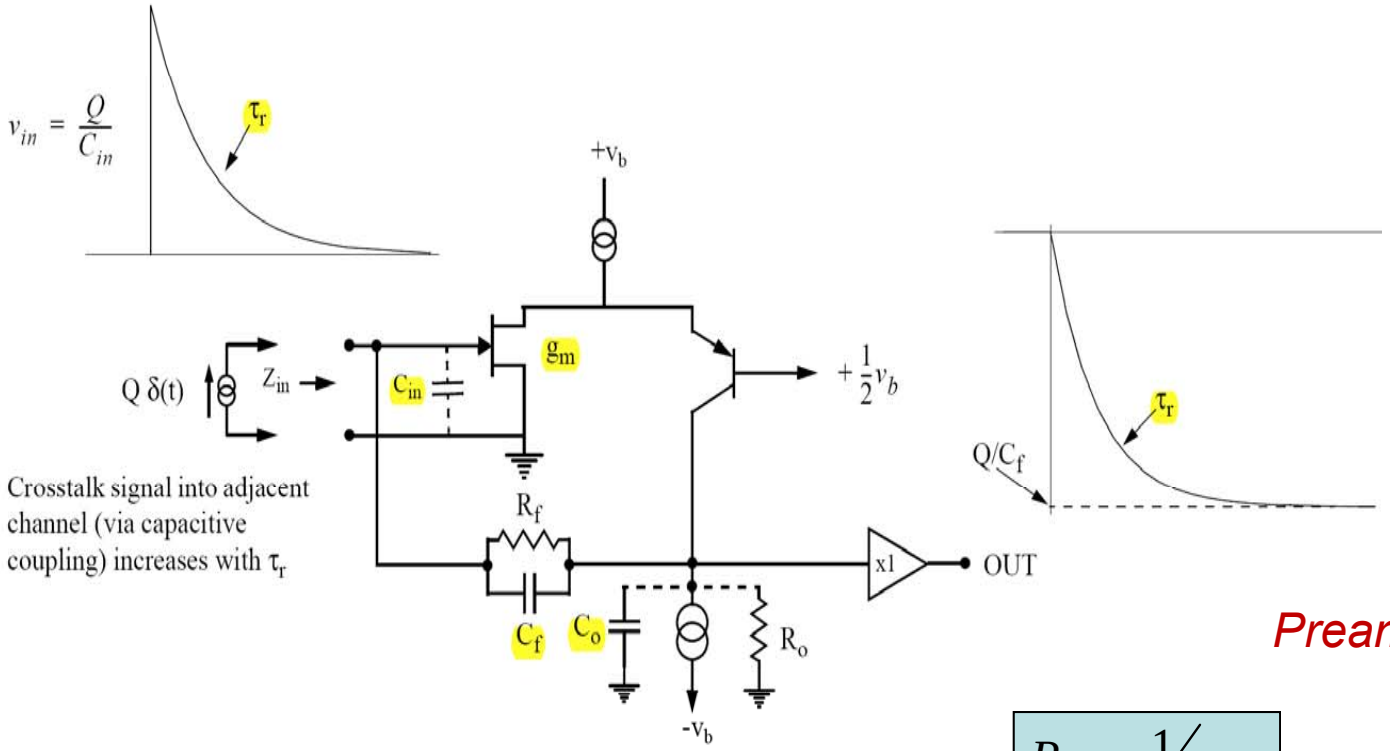
Trapezoidal Weighting Functions
by
Digital (***Uncorrelated***) Signal Processing

From: X-ray Instrumentation Associates,
App. Note 970323-1



5. Charge amplifier configuration and charge transfer from detector to amplifier

Basic Feedback Preamplifier Configuration



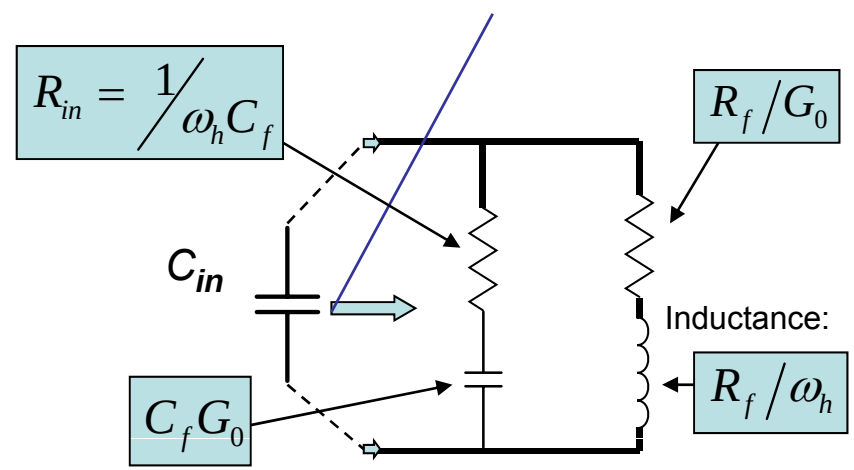
$$G_o = g_m R_o$$

$$\omega_h = g_m / C_o \qquad R_{in} = \frac{C_o}{g_m C_f}$$

$$\omega_L = \frac{1}{C_o R_o} \qquad \tau_r = C_{in} R_{in} = \frac{C_{in}}{C_f\,\omega_h} = \frac{1}{g_m} \cdot \frac{C_{in} C_0}{C_f}$$

Rise t.c.

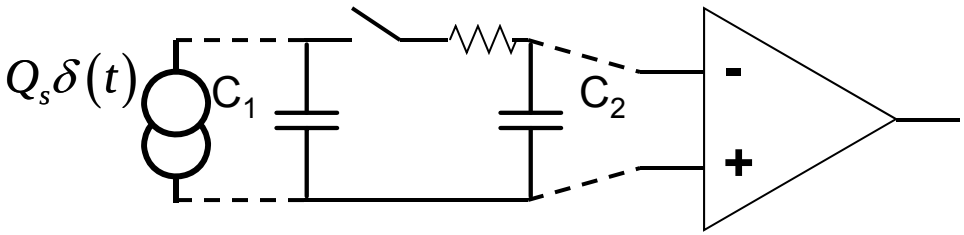
Preamp input eq. circuit



Aperiodic response for $\rightarrow$ $R_f \geq 2 \frac{1}{\omega_h C_f} \cdot \frac{C_{in}}{C_f}$

Charge Transfer from Detector to Amplifier

Transfer by *conduction*:

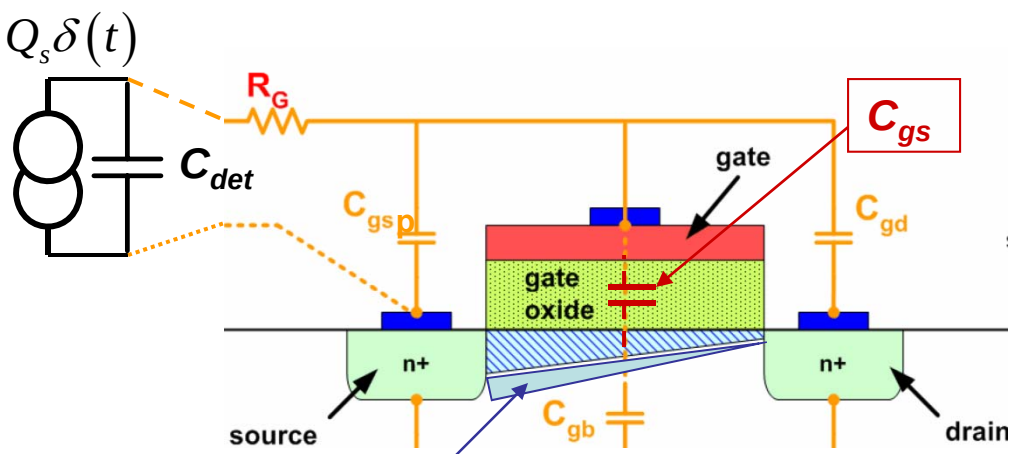


$$Switch\ closed: Q_1 = Q_s \frac{C_1}{C_1 + C_2}; Q_2 = Q_s \frac{C_2}{C_1 + C_2}$$

Q_s *is distributed as the ratio of capacitances*

The lowest noise for an electronic amplifier that could be achieved under ideal circumstances:

$$ENC_{s\,opt} \cong 2\sqrt{2}\sqrt{k_B T C_{gs}}\sqrt{\tau_e / t_m}$$



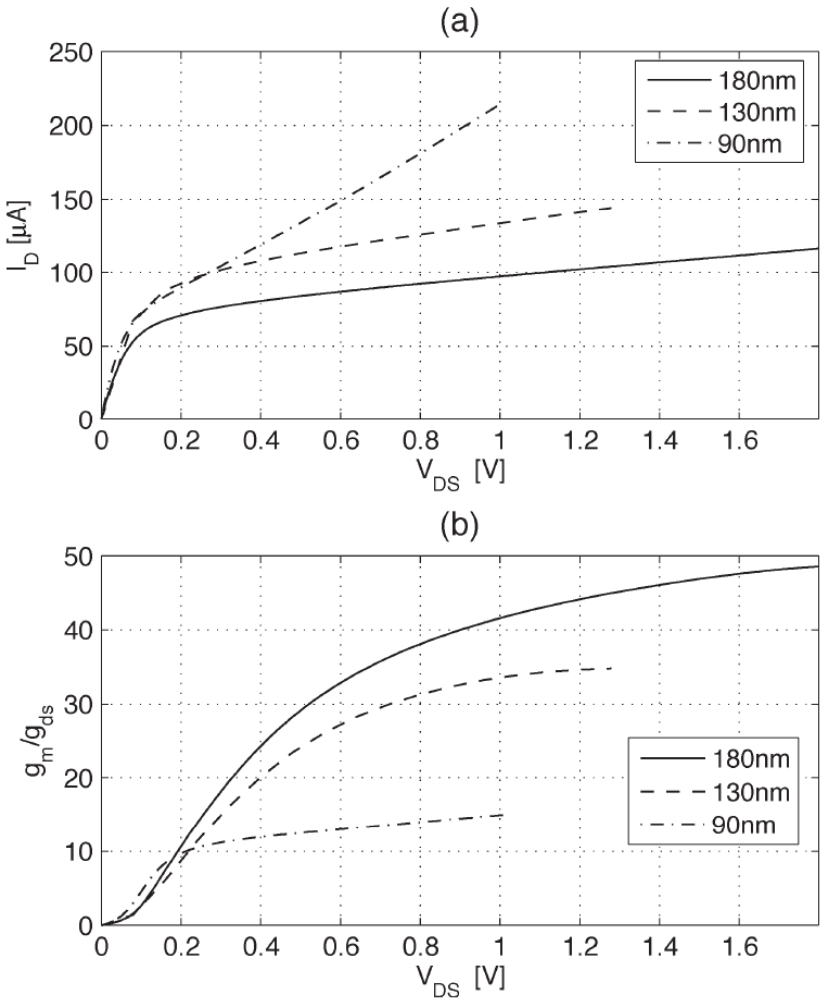
$$C_{gs}\ vs\ C_{det}\ matching\ needed!$$

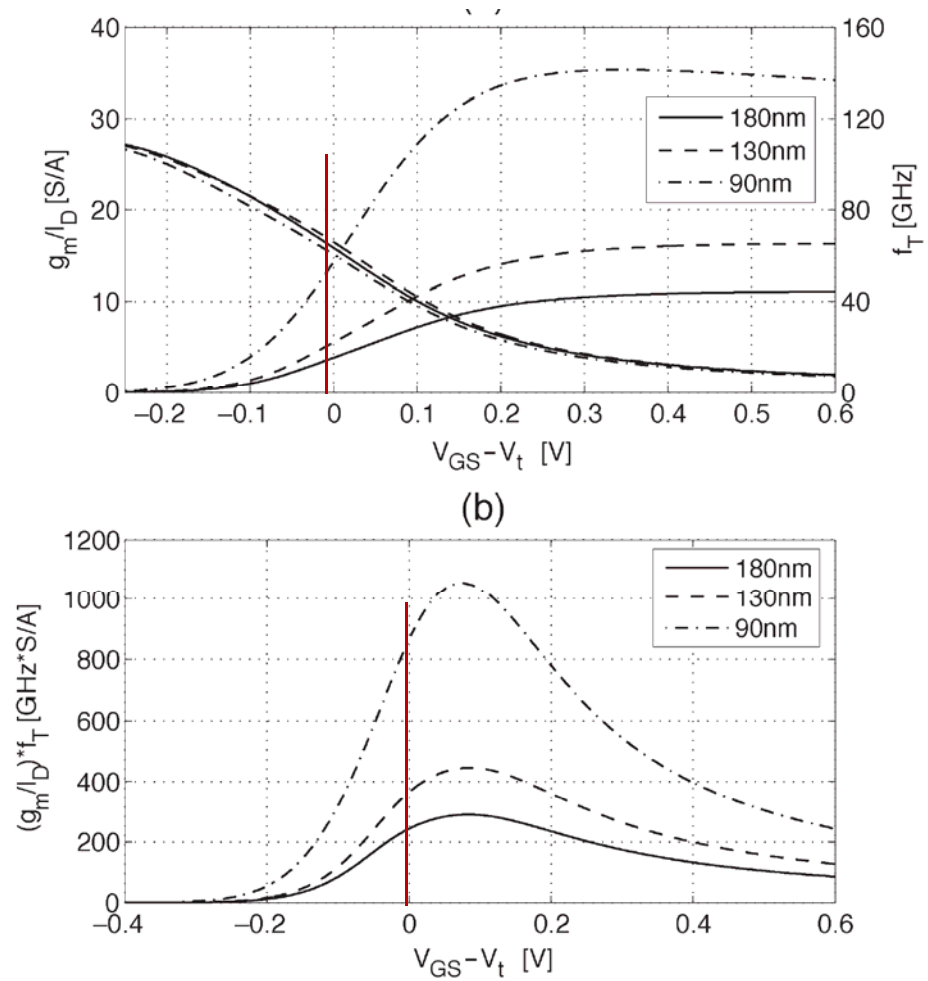
"useful" charge: $\Delta Q_c = Q_s \Big/ \left[1 + \left(C_{det} + C_{gsp} + C_{ds}\right)/C_{gs}\right]$

τ_e = *electron transit time through the channel*

$$\Delta Q_c / \Delta I_d = \tau_e = C_{gs}\Delta V_{gs} / \Delta I_d = C / g_m \rightarrow C_{gs} = g_m \tau_e$$

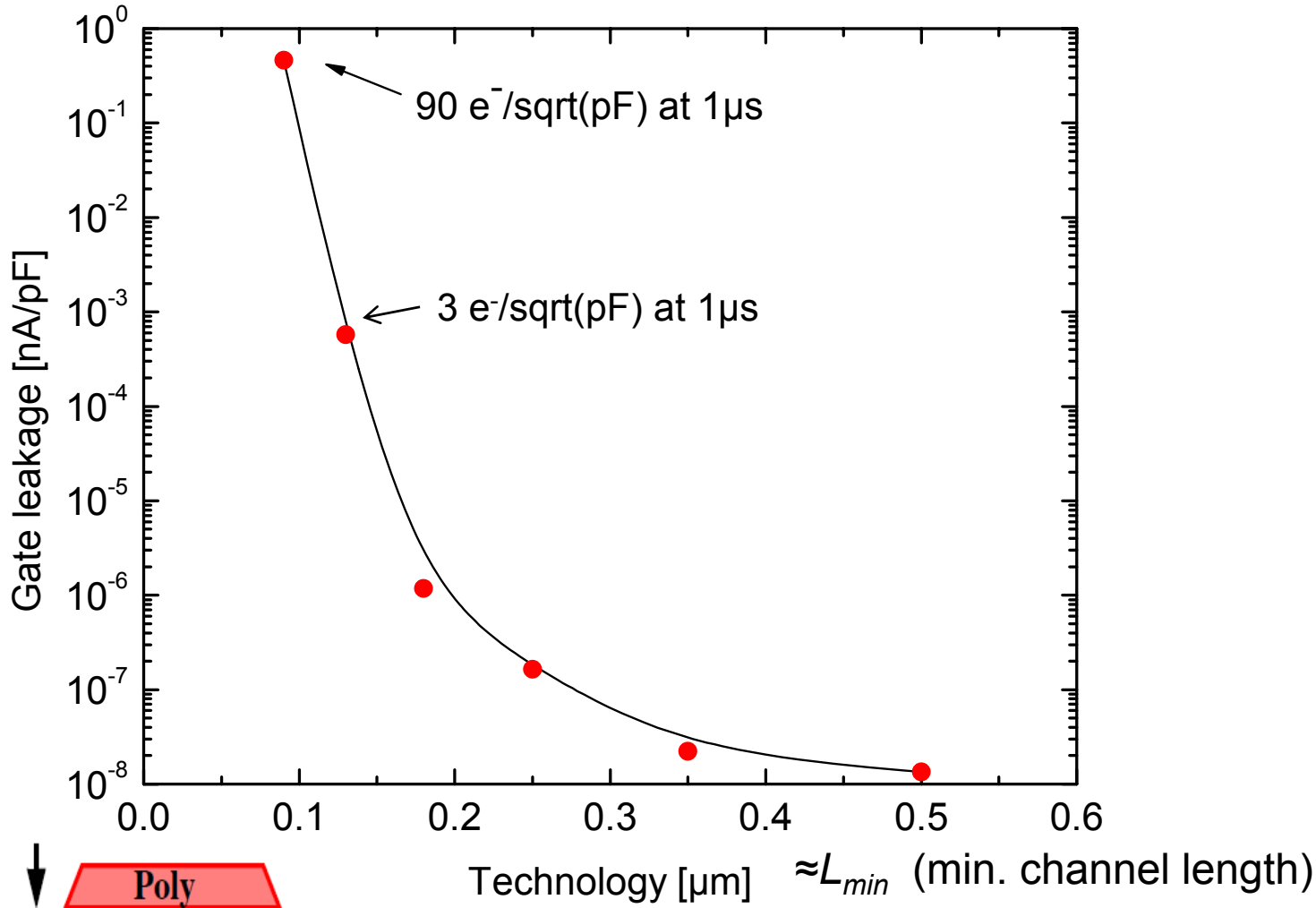
Optimization of speed, gain and power in CMOS

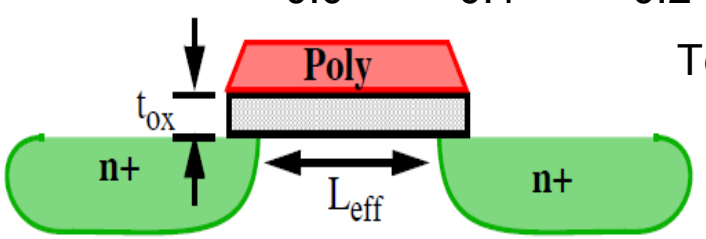




From: B. Murmann et al.

Eq. Noise Charge (ENC) due to gate tunneling current (parallel noise)



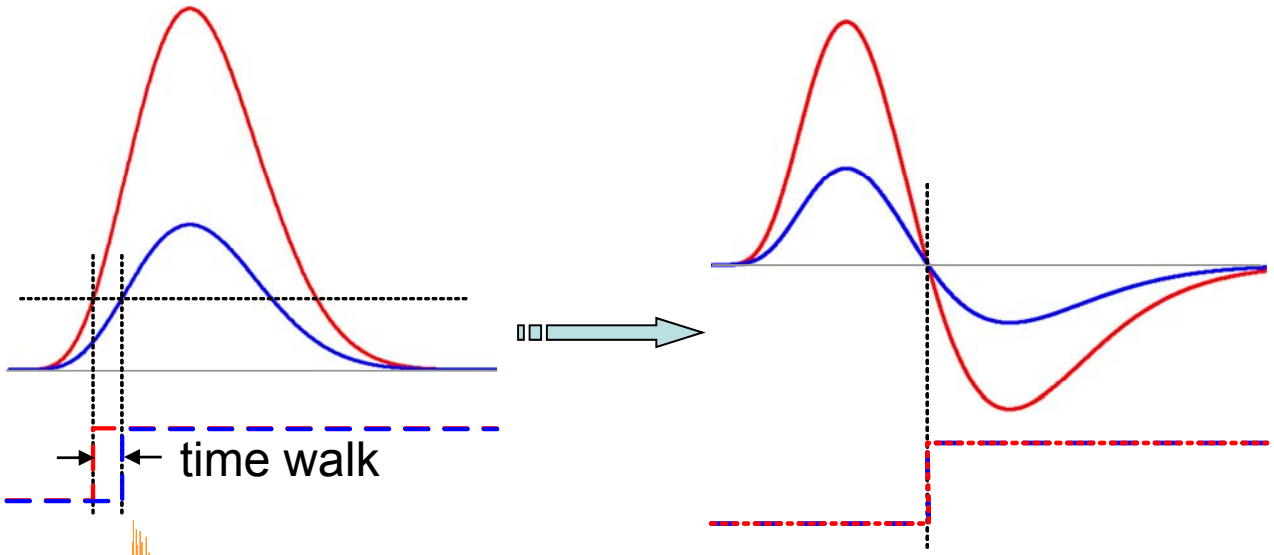


Gate oxide thickness: $t_{ox} \approx L_{min}/50$

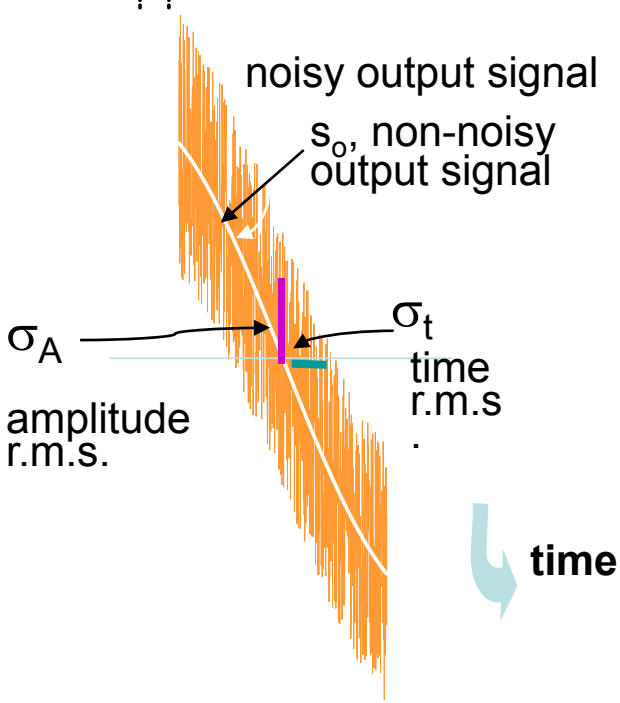
6. Timing measurements

Time Measurements

We want to measure the arrival time of the signal pulse



as time information we choose the 0-crossing time of the output signal



- for simplicity we fix the 0-crossing time in t=0
- From the ratio of amplitude and time fluctuations:

$$\frac{\sigma_A}{\sigma_t} = \left(\frac{ds_o}{dt}\right)_{t=0} \quad \Rightarrow \quad \boxed{\sigma_t^2 = \frac{\sigma_A^2}{\left(\frac{ds_0}{dt}\right)_{t=0}^2}}$$

time resolution improves as the slope at the 0-crossing increases

Adapted from: C. Guazzoni

Constant Fraction Timing of *Variable Shape Signals*

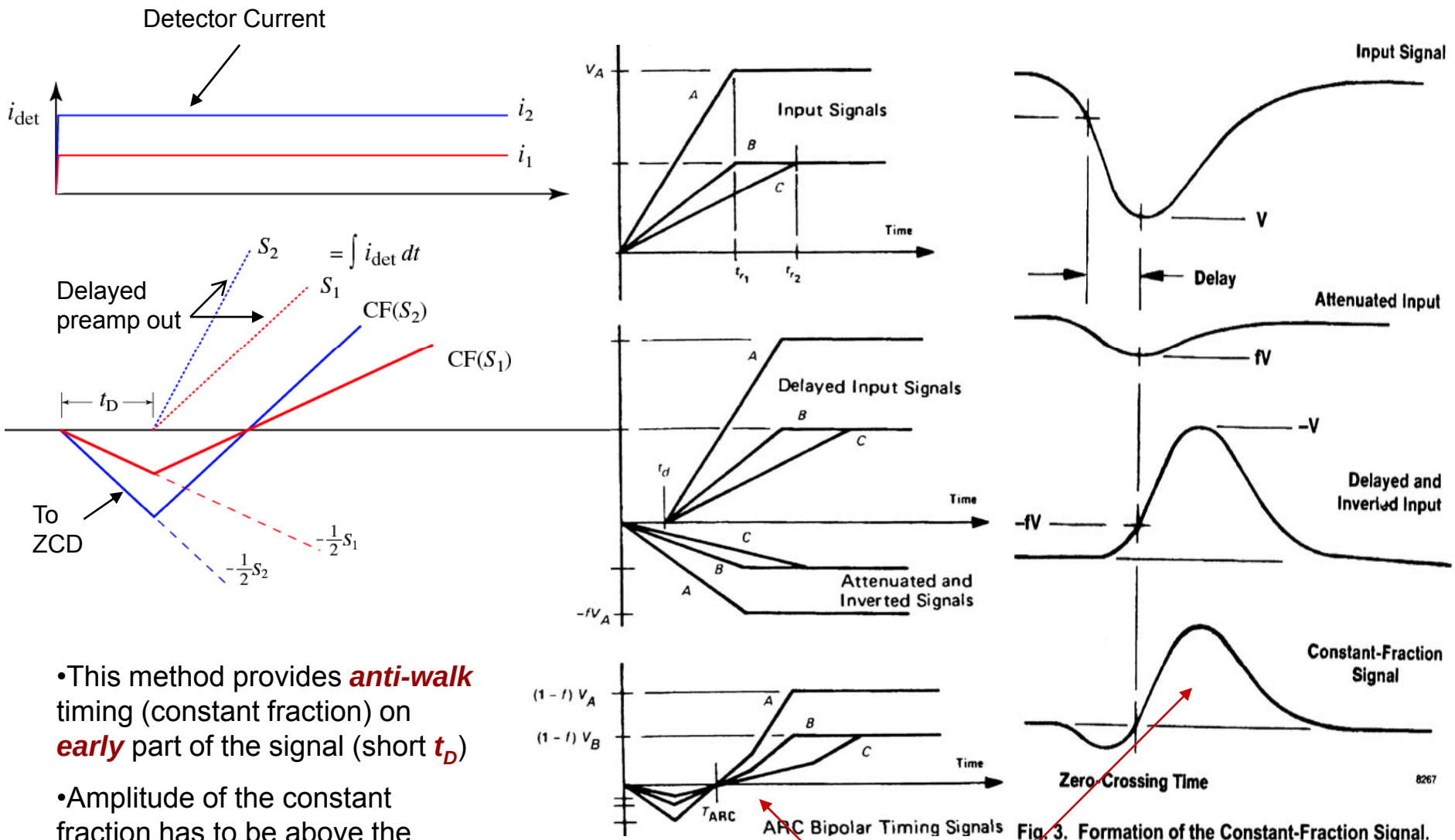


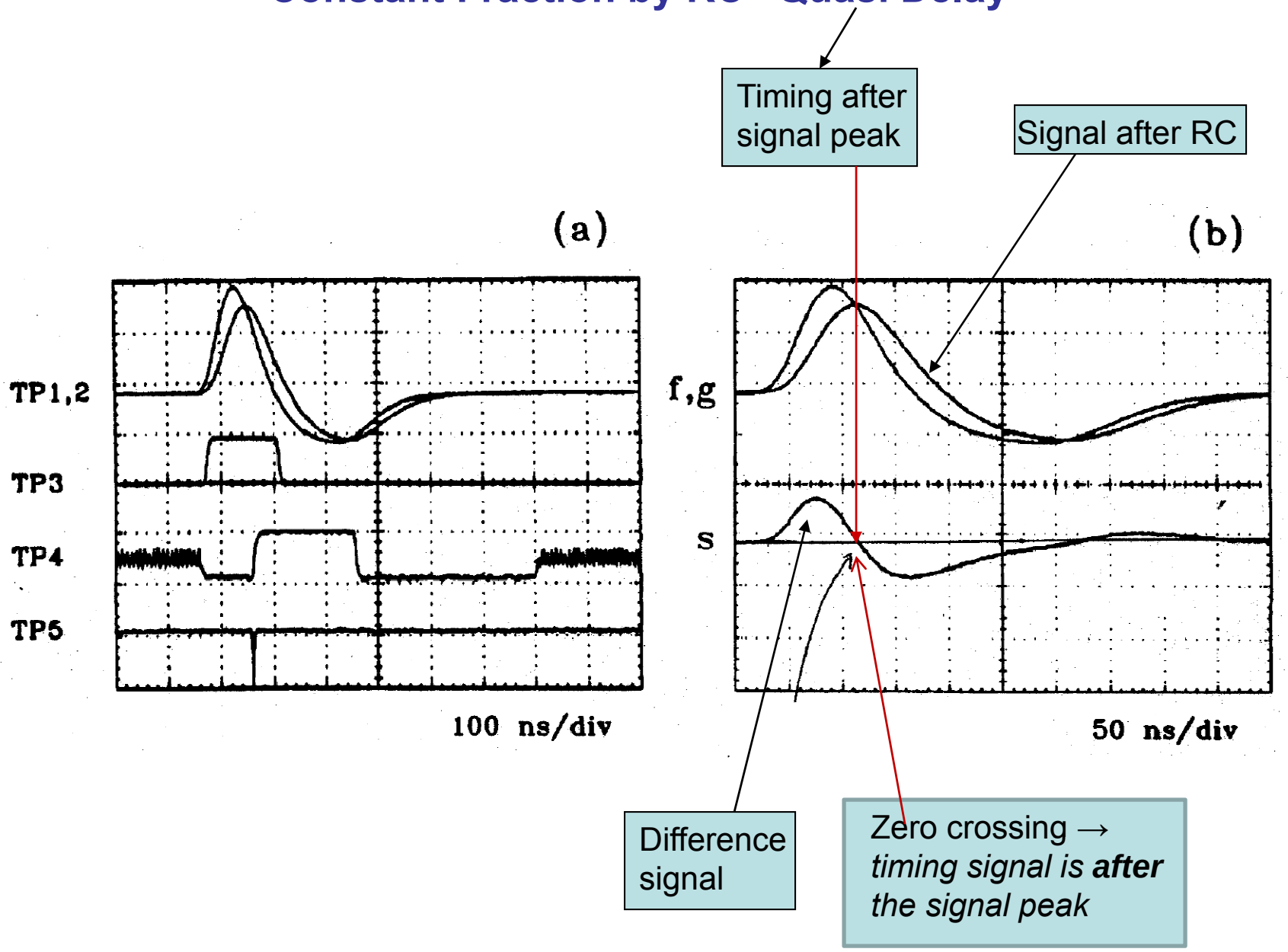
Fig. 3. Formation of the Constant-Fraction Signal.

- This method provides ***anti-walk*** timing (constant fraction) on ***early*** part of the signal (short t_D)
- Amplitude of the constant fraction has to be above the noise.

Constant fraction signal

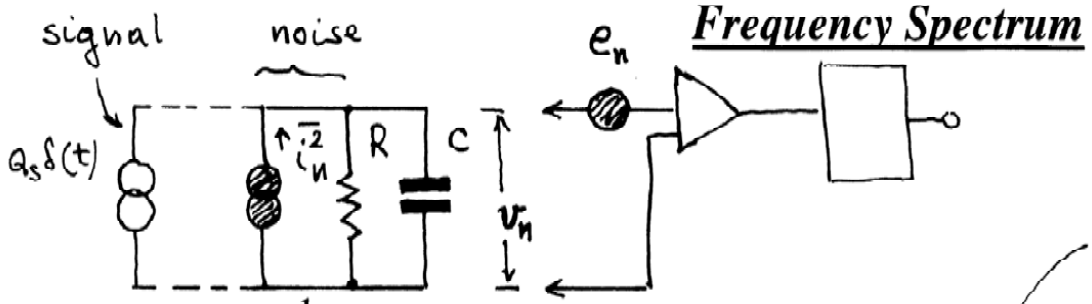
(From: Ortec)

Constant Fraction by RC "Quasi Delay"

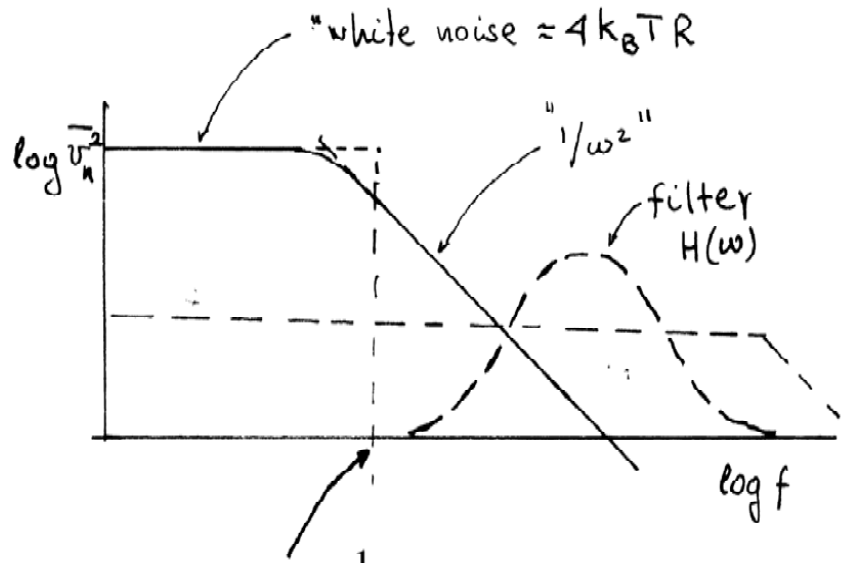


7. Fluctuations on a capacitance and charge measurement sensitivity - kTC noise

Thermal Noise, Total Fluctuation without band-limiting: *kTC noise*



Frequency Spectrum



$$Y = \frac{1}{R} + j\omega C$$

$$\overline{i_n^2} = 4k_BT/R$$

$$\overline{v_n^2} = \overline{i_n^2}\left|Y^{-1}(\omega)\right|^2 = 4k_BTR\frac{1}{1+(\omega CR)^2}$$

Total fluctuation:

$$\sigma_v^2 = \int_o^\infty \overline{v_n^2}df = \frac{k_BT}{C}$$

$$\sigma_q^2 = k_BTC$$

"independent of R"

Eq. bandwidth $f_h = \dfrac{1}{4RC}$

According to equipartion theorem $(1/2)k_BT$ for each degree of freedom →

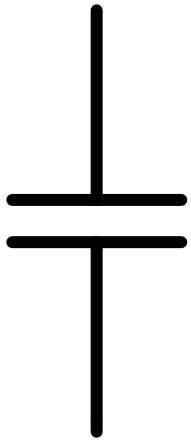
$$(1/2)k_BT = (1/2)\sigma_q^2/C = (1/2)C\sigma_v^2$$

independent of R

1. C=1pF, R=1GΩ — RC = 1ms, f_h = 250 Hz
2. C=100fF, R=10kΩ — RC=1ns, f_h = 250 MHz

Charge and Voltage *Total Fluctuations* on Capacitance

Capacitance: $C\ [F]$	***Charge fluctuation:*** $(kTC)^{1/2}/q_e\ [rms\ e]$	***Voltage fluctuation:*** $(kT/C)^{1/2}\ [V]$
1a	**0.4**	**64m**
10a	1.26	20m
100a	4	6.4m
1f	**1.26x10**	**2.0m**
10f	4.0x10	0.64m
100f	1.26×10^2	0.20m
1p	**4.0×10^2**	**64μ**
10p	1.26×10^3	20μ
100p	4×10^3	6.4μ



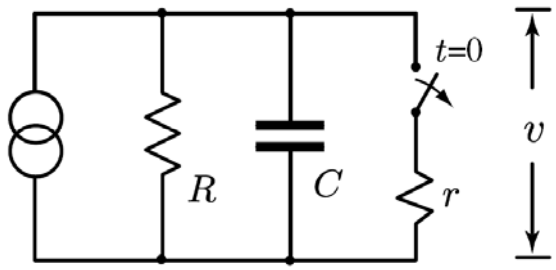
Dynamic range:

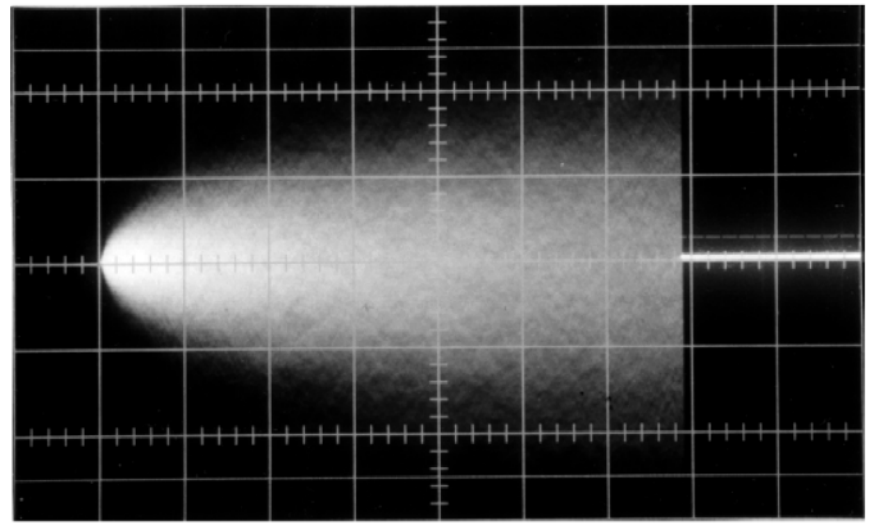
$$500mV/5\sigma \approx 500$$

ENC (if no filtering):
≈126 rms e

Transient Build-up of Noise: ***kTC noise vs time***

$$\overline{i_n^2} = 4k_BT/R$$



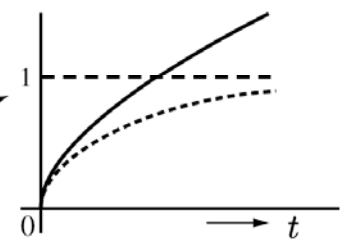


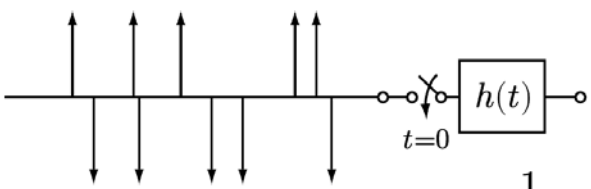
Campbell:

$$\sigma_v^2 = \frac{1}{2}\,\overline{i_n^2}\int_0^t h^2(u)du = \frac{k_BT}{C}(1-e^{-2t/\tau})$$

$$\underline{\sigma_v/(k_BT/C)^{1/2}} = \underline{(1-e^{-2t/\tau})^{1/2}}$$

$$\frac{\sigma\,(t)}{(k_BT/C)^{1/2}}$$





$$h(t) = \frac{1}{C}\,e^{-t/\tau}$$

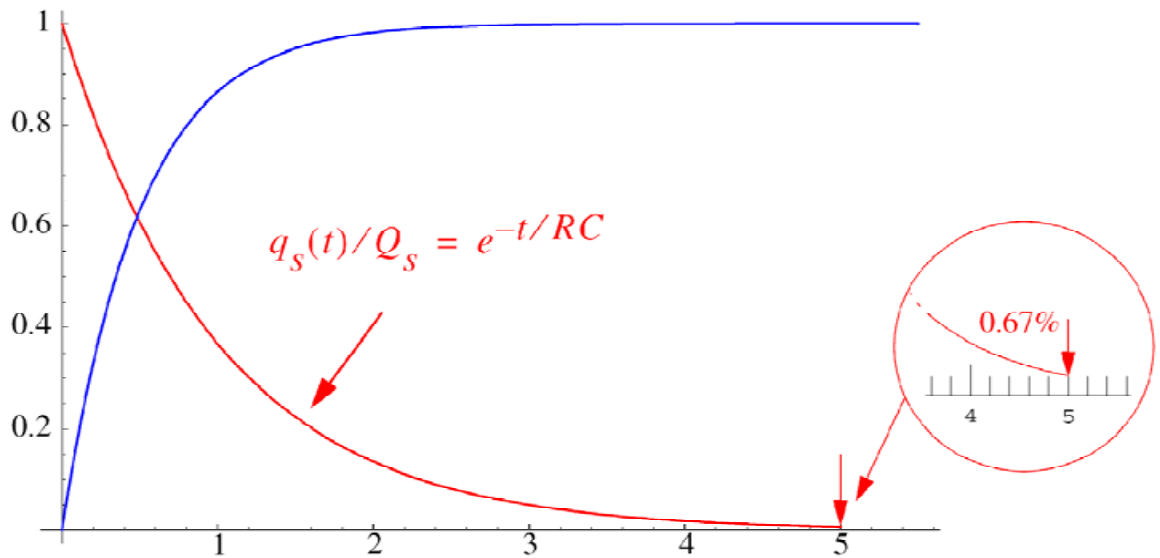
For $t/\tau \ll 1$: $\sigma_v^2 \propto t$ (random walk)

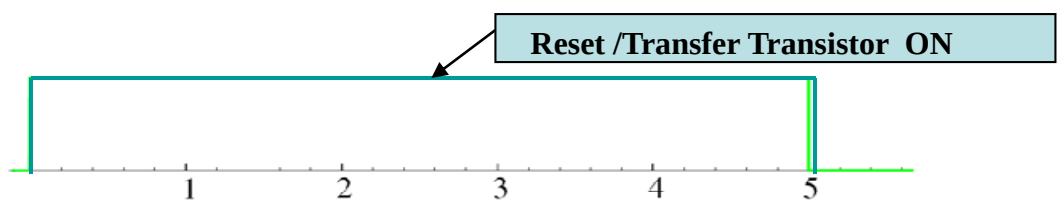
$$\sigma_v \approx (k_BT/C)^{1/2}\cdot(2\frac{t}{\tau})^{1/2}$$

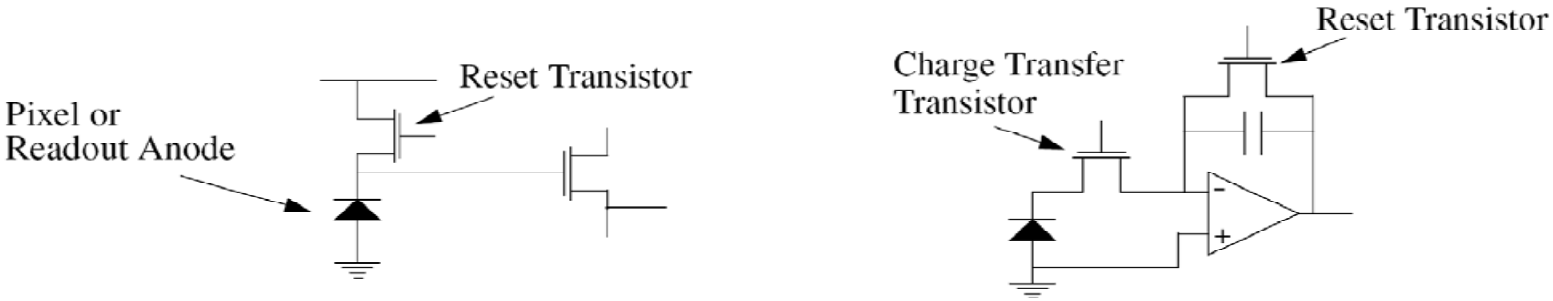
For $\left.\begin{array}{l}\tau = RC = 1\text{s},\\ t \quad\quad\quad = 1\mu\text{s}\end{array}\right\}$ $\sigma_v/(k_BT/C)^{1/2} \approx$ 4.5%

Pixel Reset, or Charge Transfer and kTC Noise vs Time

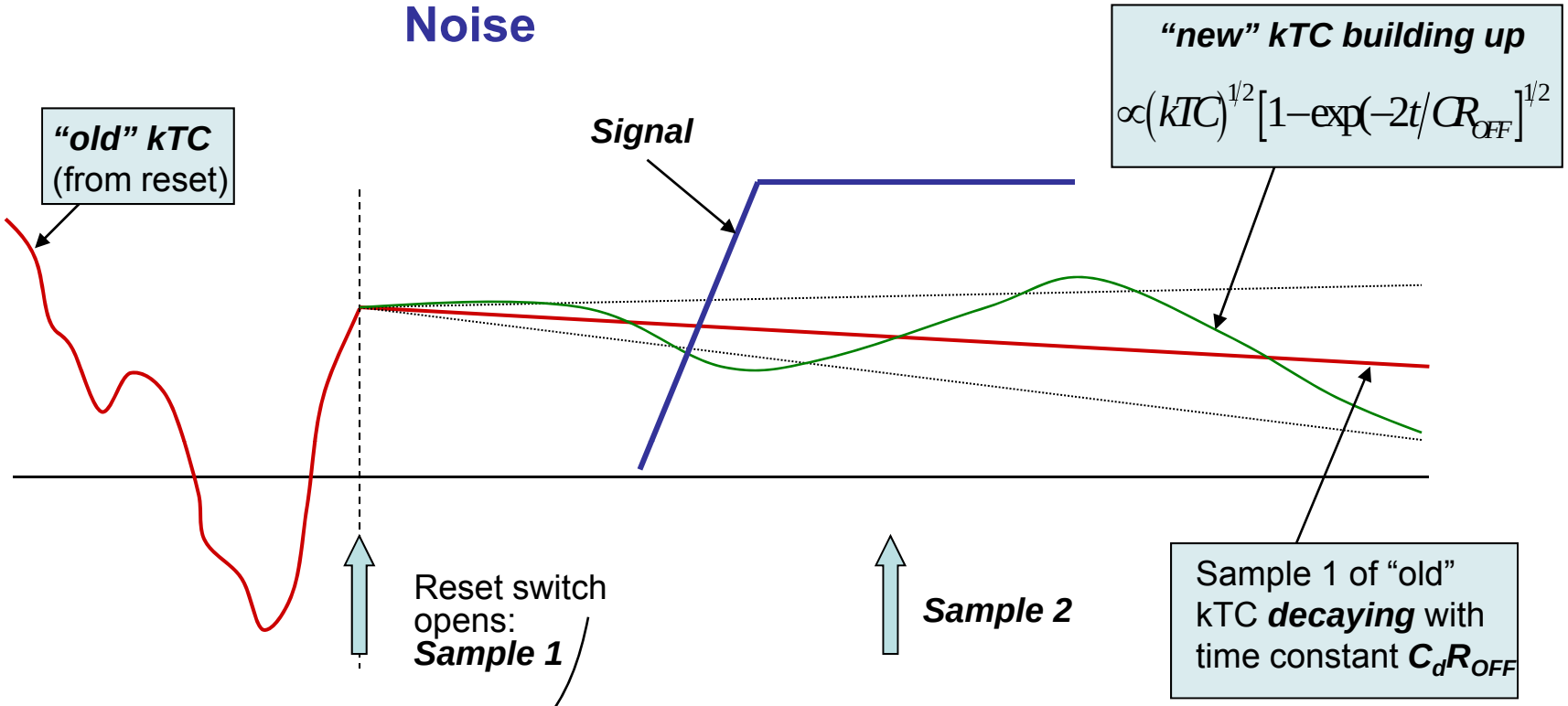
$$\sigma_q/(kTC)^{1/2} = (1 - e^{-2t/RC})^{1/2}$$

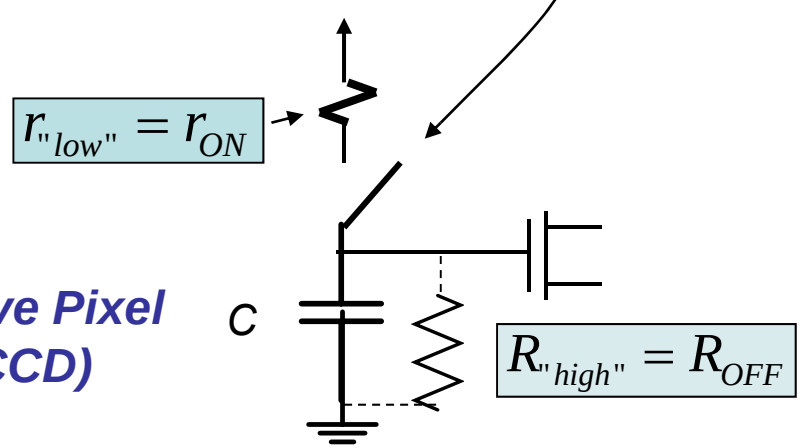






Correlated Double Sampling (CDS) and *kTC* Noise





Active Pixel (or CCD)

$$R_{OFF} / r_{ON} \sim 10^6 - 10^{11}$$

Example:

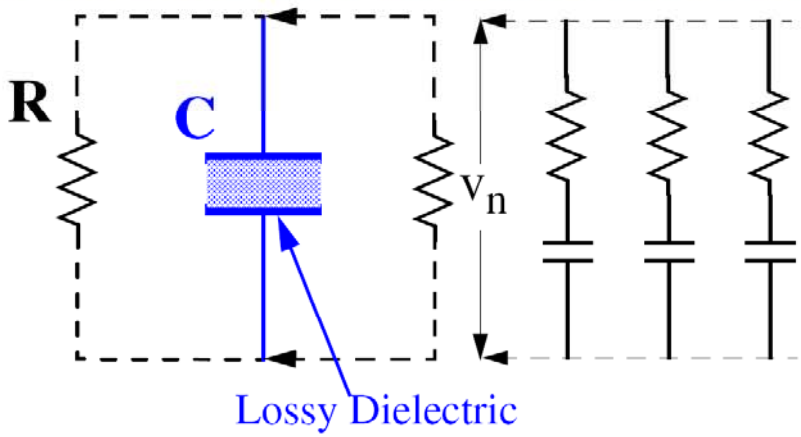
$C \sim 20$ fF

$r_{ON} \sim 10^3$ ohms $\quad r_{ON}C \sim 20$ ps

$R_{OFF} \sim 10^{13}$ ohms $\quad R_{OFF}C = 0.2$ s

8. Noise from Dielectrics

Lossy Dielectrics and Complex Networks



$$\varepsilon = \varepsilon' + j\varepsilon'' = \varepsilon'\left(1 + j\frac{\varepsilon''}{\varepsilon'}\right)$$

$$\frac{\varepsilon''}{\varepsilon'} = D = \frac{1}{Q} = \frac{g(\omega)}{\omega C}$$

From the Fluctuation-Dissipation Theorem: $\overline{v_n^2} = 4k_B T D \frac{1}{\omega C}$; $\overline{q_n^2} = 4k_B T C \frac{D}{\omega}$

For charge measurement (ns to ms range) $ENC_D \approx k_B T C(2.4D)$

For C = 1 pF at T = 293 K

$\sigma_q = (k_B\, T\, C)^{1/2} = 400$ e rms

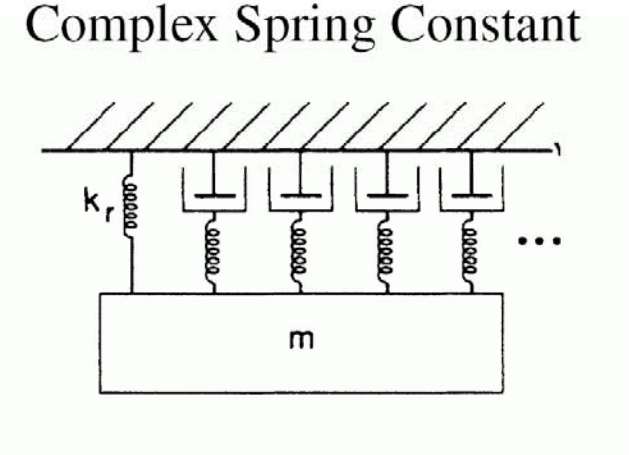
$ENC_a < 5$ e (with an optimized amplifier)

Dielectric Noise Contribution:

$D \approx 5\times10^{-5}$, $ENC_D \approx 4$ e rms

$D \approx 2\times10^{-2}$, $ENC_D \approx 86$ e rms (G10 circuit board)

Complex Spring Constant



$k = k_r(1 + j\varphi)$

k_r = "relaxed" spring constant

$f = 1/Q \approx 10^{-4} - 10^{-8}$

$$v_n^2(\omega) = 4k_B T \frac{R(1 + CDR\omega)}{C^2R^2\omega^2 + (1 + CDR\omega)}$$

$$\sigma_v^2 = \int_0^{f_h} v_n^2(f)\, df \cong \frac{k_B T\left(\pi + \frac{D^2}{\pi R C f_h(1+D^2)} + Log(4\pi^2R^2C^2[1+D^2])\right)}{\pi C(1+D^2)} + \frac{2k_B T Log(f_h)}{\pi C(1+D^2)}$$

$$\sigma_v^2 \approx \frac{k_B T}{C}$$

9. Literature

REFERENCES ON SIGNAL PROCESSING FOR RADIATION DETECTORS

1. S. Ramo; Proc. IRE, 27(1939) 584.
2. E. Gatti, G. Padovini, and V. Radeka; *Signal Evaluation in Multielectrode Radiation Detectors by Means of a Time Dependent Weighting Vector;* NIM 193 (1982) 651.
3. R. Wilson; *Noise in Ionization Chamber Pulse Amplifiers;* Philosophical Magazine, Ser. 7, Vol. xli, p. 66, Jan. (1950).
4. E. Baldinger and W. Franzen; *Advances in Electronics and Electron Physics;* 3 Academic Press, New York, (1956) 256.
5. V. Radeka; *Optimum Signal Processing for Pulse Amplitude Spectrometry in the Presence of High-Rate Effects and Noise;* IEEE Trans. Nucl. Sci. NS-15 (1968) 455.
6. M. Konrad; *Detector Pulse Shaping for High Resolution Spectroscopy;* IEEE Trans. Nucl. Sci. NS-15, No. 1 (1968) 268.
7. V. Radeka; *State of the Art of Low Noise Amplifiers for Semiconductor Radiation Detectors;* Proc. Int'l. Symposium on Nuclear Electronics, Versailles, 1968, Vol. 1 : 1 (1968).
8. V. Radeka; *Field Effect Transistors for Charge Amplifiers;* IEEE Trans. Nucl. Sci. NS-20, 182 (1973).
9. V. Radeka; *Trapezoidal Filtering of Signals from Large Germanium Detectors at High Rates;* Nucl. Instrum. & Meth. 99 (1972) 535.
10. V. Radeka; *1/| f | Noise in Physical Measurements;* IEEE Trans. Nucl. Sci. NS-16 (1969) 17.
11. V. Radeka; *Signal, Noise, and Resolution in Position-Sensitive Detectors;* IEEE Trans. Nucl. Sci. NS-21, No. 1 (1974) 51.
12. W. J. Willis and V. Radeka; *Liquid Argon Ionization Chambers as Total Absorption Detectors;* Nucl. Instrum. & Meth. 120 (1974) 221.
13. V. Radeka and R. A. Boie; *Centroid Finding Method for Position Sensitive Detectors;* Nucl. Instrum. & Meth. 178 (1980) 543.
14. F. S. Goulding, D. A. Landis, and N. W. Madden; IEEE Trans. Nucl. Sci. NS-30, 301 (1983).
15. V. Radeka; *Semiconductor Position Sensitive Detectors;* NIM 226 (1984) 209.

16. E. Gatti and P. F. Manfredi; *Processing the Signals from Solid-State Detectors in Elementary Particle Physics;* Rivista de Nuovo Cimento, Vol. 9, N. 1 (1986).
17. V. Radeka; *Low-Noise Techniques in Detectors;* Ann. Rev. Nucl. Part. Sci. 38 (1988) 217.
18. V. Radeka, et al.; *Monolithic Preamplifier Employing Epitaxial n-Channel JFETs;* Nucl. Instrum. & Meth. in Physics Research A326 (1993) 77.
19. Valentin T. Jordanov and Glenn F. Knoll; *Digital Synthesis of Pulse Shapes in Real Time for High Resolution Radiation Spectroscopy;* Nucl. Instrum. & Meth. in Physics Research A345 (1994) 337.
20. G. C. Smith, et al.; *High Rate, High Resolution, Two-Dimensional Gas Proportional Detectors for X-ray Synchrotron Radiation Experiments;* Nucl. Instrum. & Meth. in Physics Research A323 (1992) 78.
21. G. Bencze, et al.; *Position and Timing Resolution in Interpolating Cathode Strip Chambers in a Test Beam;* Nucl. Instrum. & Meth. A357 (1995) 40.
22. O. Benary, et al.; *Liquid Ionization Calorimetry with Time-Sampled Singals;* Nucl. Instrum. & Meth. in Physics Research A349 (1994) 367.
23. B. T. Turko and R. C. Smith; Conf. Record of the 1991 IEEE Nucl. Sci. Symp., (1991) 711.
24. O. Benary, et al.; *Precision Timing with Liquid Ionization Calorimeters;* Nucl. Instrum. & Meth. in Physics Research A332 (1993) 78.
25. G. Bertuccio and A. Pullia; *An HEMT Input Charge Preamplifier for Nanoseconds Signal Processing Time;* IEEE Trans. Nucl. Sci. Vol. 42, No. 2, April (1995) 66.
26. Suharli Tedja, et al.; *A CMOS Low-Noise and Low-Power Charge Sampling Integrated Circuit for Capacitive Detector/Sensor Interfaces;* IEEE J. Solid State Circuits, Vol. 30, No. 2, February (1995) 110.
27. P. O'Connor, et al.; *Ultra Low Noise CMOS Preamplifier-Shaper For X-ray Spectroscopy;* Nucl. Instrum. & Meth. A409 (1998) 315.
28. V. Radeka; *Shielding and Grounding in Large Detectors;* Proc. 4th Workshop on Electronics for LHC Experiments, CERN/LHCC/98-36, p. 14.
29. R. Isobe, et al.; *Improvements in Throughput of an Analog Triangular Pulse Shaper;* JEOL Engineering Co., Application Note.

30. G. De Geronimo, P. O'Connor, V. Radeka, and B. Yu; *Front-End Electronics for Imaging Detectors;* Nucl. Instrum. & Meth. A471 (2001) 192-199.
31. Paul O'Connor and Gianluigi De Geronimo; *Prospects for Charge Sensitive Amplifiers in Scaled CMOS;* Nucl. Instrum. & Meth. A480 (2002) 713-725.
32. Rahul Sarpeskhar, Tobias Delbrück, and Carver A. Mead; *White Noise in MOS Transistors and Resistors;* IEEE Journal of Circuits and Devices 10, 23 (1993).
33. Hui Tian, Boyd Fowler, and Abbas El Gamal; *Analysis of Temporal Noise in CMOS Photodiode Active Pixel Sensor;* IEEE Journal of Solid-State Circuits 36, 92 (2001).
34. Carver Mead; *Analog VLSI and Neural Systems;* Addison-Wesley Publishing Company, (1989).
35. R. P. Kraft, et al.; *Soft X-ray Spectroscopy with Sub-Electron Readnoise Charge-Coupled Devices;* Nucl. Instrum. & Meth. A361, 372 (1995).
36. Chiara Guazzoni; *Fundamentals of Pulse Processing and Noise Filtering in Radiation Detectors;* 9th European Symposium on Semiconductor Detectors, Schloss Elmau, June 23-27 (2002); **http://www.elet.polimi.it/people/guazzoni.**
37. L. L. Lewyn, et al., *Analog Circuit Design in Nanoscale CMOS Technologies*, Proc. IEEE, 97, No. 10, (2009) 11687.
38. B. Murmann et al., *Impact of Scaling on Analog Performance and Associated Modeling Needs*, IEEE Trans. on Electron Devices, 53, No. 9, (2006) 2160.
39. G. De Geronimo, and P. O'Connor, *MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers*, IEEE Trans. Nucl. Sci., Vol. 52, No. 6 (2005) 3223.

Appendix

A. 1
Noise Calculation: Time Domain and Frequency Domain

- For <u>time invariant</u> systems impulse response <u>h(t)</u> and weighting function <u>w(t)</u> are interchangeable for noise calculations.

From Parseval's theorem, noise variance can be expressed as:

$$\sigma^2 = \bar{n}\, q^2 \int_{-\infty}^{\infty} h^2(t)dt = 2\,\bar{n}\, q^2 \int_{0}^{\infty} |H(\omega)|^2\, df$$

Campbell's theorem

Also: $\sigma^2 = W_o \int_{0}^{\infty} |H(\omega)|^2\, df$

Thus noise spectral density: $W_o = 2\,\bar{n}\, q^2 = 2q_eI_o$ for shot noise
(similarly $W_o = 4kT/R$ for thermal noise)

<u>Parallel noise integral</u>:

I_2 $$\overline{ENC_p^{\,2}} = \tfrac{1}{2} W_{op} \int_{-\infty}^{\infty} h^2(t)dt = W_{op} \int_{0}^{\infty} |H(\omega)|^2 df$$

parallel noise (current) spectral density = W_{op}

<u>Series noise integral</u>:

I_1 $$\overline{ENC_s^{\,2}} = \tfrac{1}{2} W_{os}\, C_{in}^{\,2} \int_{-\infty}^{\infty} h'^2(t)dt = W_{os}C_{in}^{\,2} \int_{0}^{\infty} \omega^2 |H(\omega)|^2\, df$$

series noise (voltage) spectral density, $W_{os} = \overline{e_n^{\,2}} = 4kTR_s$

(since $\int_{-\infty}^{\infty} h'^2(t)dt = 2\int_{0}^{\infty} \omega^2 |H(\omega)|^2\, df$)

- For <u>time variant</u> systems, noise is calculated using <u>weighting function</u> and time domain relations.

A.2 Parallel Noise due to ***Dark Current*** in Devices with ***Avalanche Gain***

Parallel noise (from Campbell's theorem):

$$ENC_p^2 = nq^2 \int_{-\infty}^{\infty} w^2(t)dt = nq^2 t_G$$

$$nq^2 = q(nq) = qI_o$$

n = rate of charge impulses

t_G = equivalent integration time

- Devices ***without avalanche gain***: $\boldsymbol{q = e}$ = electron charge
- Devices ***with avalanche gain*** M : $\boldsymbol{q = Me}$ = charge in each impulse in Poisson sequence

Parallel noise due to dark current in avalanche photo-diodes:

$$ENC_p^2 = n(Me)^2 t_G$$

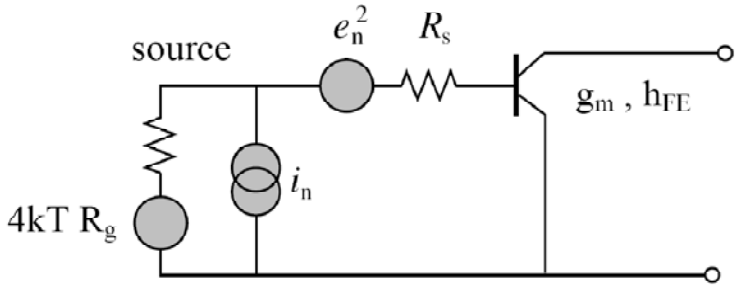
$$ENC_p^2 = I_o M \cdot e\, t_G$$

Avalanche gain magnifies the noise (ENC_p) by $\boldsymbol{M^{1/2}}$ compared to the shot noise from a current I_o ,

i.e., the noise due to ***avalanche dark current*** $\boldsymbol{I_o}$ equals the noise due to single electron current $\boldsymbol{MI_o}$.

(Surface leakage current noise is not subject to avalanche gain.)

A3. Noise Figure vs Noise Voltage, Noise Current and Noise Temperature



$R_s = 1/2g_m + r_{bb'}$
$i_n^2 = 2\ eI_b = 2e\ \ I_c/h_{FE}$

$NF = 10 \log_{10} [(\text{source} + \text{ampl.})/\text{source}]$

$NF = 10 \log_{10} [1+(e_n^2 + i_n^2 R_g^2)/4kTR_g]$

For $i_n^2 R_g^2 << e_n^2$, i.e., $R_g = 50$:

$\underline{NF = 10 \log_{10} [1 + R_s/R_g]}$ $= 10 \log_{10} [1 + T_n/T]$ [db]

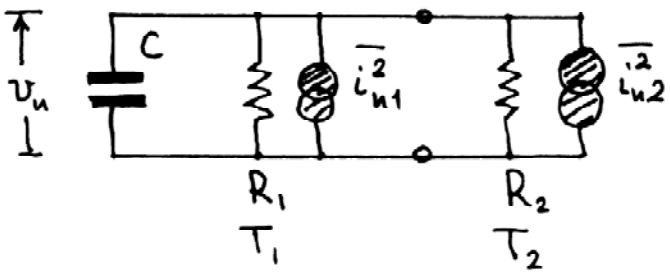
T_n = ampl. noise temperature

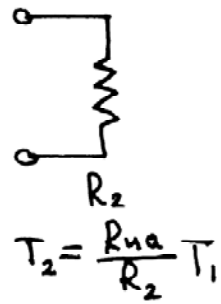
$R_s T = R_g T_n \rightarrow T_n/T = R_s/R_g$

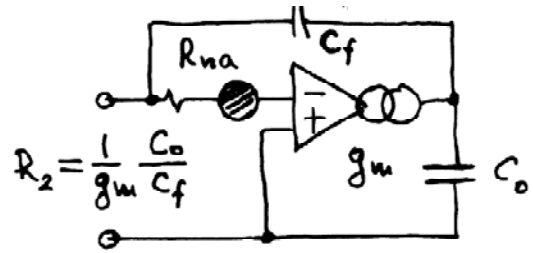
NF [db]	R_s [ ]	e_n[nV/Hz$^{1/2}$]	T_n[K]
3	50	0.91	293
2	29	0.71	170
1	13	0.47	76
0.5	6	0.32	35

<u>ENC</u> from <u>e_n</u> , <u>i_n</u> (with $C_D + C_A$ and t_m)

A4. Noise in Resistors at Different Temperatures and "Electronic Cooling" by Feedback







Total fluctuation (all frequencies):

$$\sigma_v^2 = \frac{k_B}{C} \cdot R_1 \| R_2 \left(\frac{T_1}{R_1} + \frac{T_2}{R_2} \right)$$

1. for $T_1 = T_2 \rightarrow \sigma_v^2 = \frac{k_B T_1}{C}$

2. if $T_2 = 0 \rightarrow \sigma_v^2 = \frac{k_B T_1}{C} \cdot \frac{1}{1 + R_1 / R_2}$

With feedback (cooled) damping:

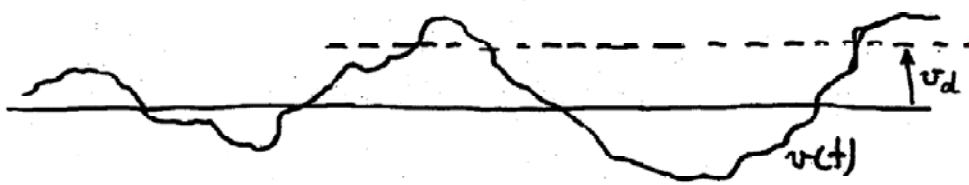
$$\sigma_v^2 = \frac{k_B T_1}{C} \cdot \frac{1}{1 + R_1 / R_2} \left(1 + \frac{R_{na} R_1}{R_2^2} \right)$$

σ_v min for $R_2 = (R_1 R_{na})^{1/2}$

$$\rightarrow \sigma_v^2 = \frac{kT_1}{C} \cdot \frac{2}{1 + (R_1 / R_{na})^{1/2}}$$

$$\left.\begin{array}{l} R_1 = 10^6 \Omega \\ R_{na} = 100 \Omega \end{array}\right\} \begin{array}{l} R_2 = 10^4 \Omega \\ \sigma_v^2 \cong \frac{k_B T_1}{C} \cdot \frac{1}{50} \end{array}$$

A5. Zero-Crossing Statistics of Noise



Discriminator threshold

$W(\omega) =$ spectral density

$K(\tau) =$ autocorrelation function

$\sigma = [K(0)]^{1/2} =$ rms noise

Rate of ***positive*** zero crossings:

$$n_{zc+} = \frac{1}{2\pi}\left[-\frac{K''(0)}{K(0)}\right]^{\frac{1}{2}} = \frac{1}{2\pi}\left[\frac{\int_0^\infty \omega^2 W(\omega)d\omega}{\int_0^\infty W(\omega)d\omega}\right]^{\frac{1}{2}}$$

Rate of positive level crossings:

$$n(v_d)_+ = n_{zc+} \cdot \exp\left[-v_d^2 \big/ 2K(0)\right]$$

Example: 2nd order high frequency cutoff (2 RC integrations)

Solution:

$$n_{zc+} = \frac{1}{2\pi(\tau_1\tau_2)^{1/2}}$$

For: $\tau_1 = \tau_2 = 50ns; 1\mu s$

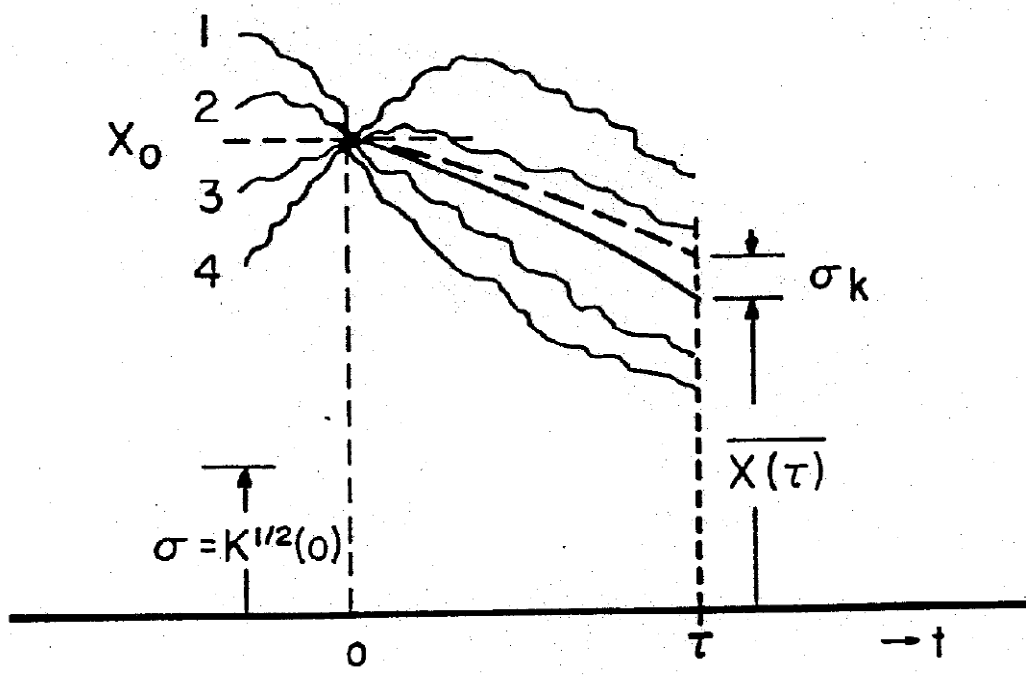
$n_{zc+} = 3MHz; 150kHz$

Threshold crossing rate:

$v_d/\sigma \Rightarrow$	$n(v_d)_+/n_{zc+}$
2	1.4×10^{-1}
3	1.1×10^{-2}
4	3.3×10^{-4}
5	4×10^{-6}

J.S. Bendat, Principles and Applications of Random Noise Theory, J. Wiley&Sons, 1958,p. 125

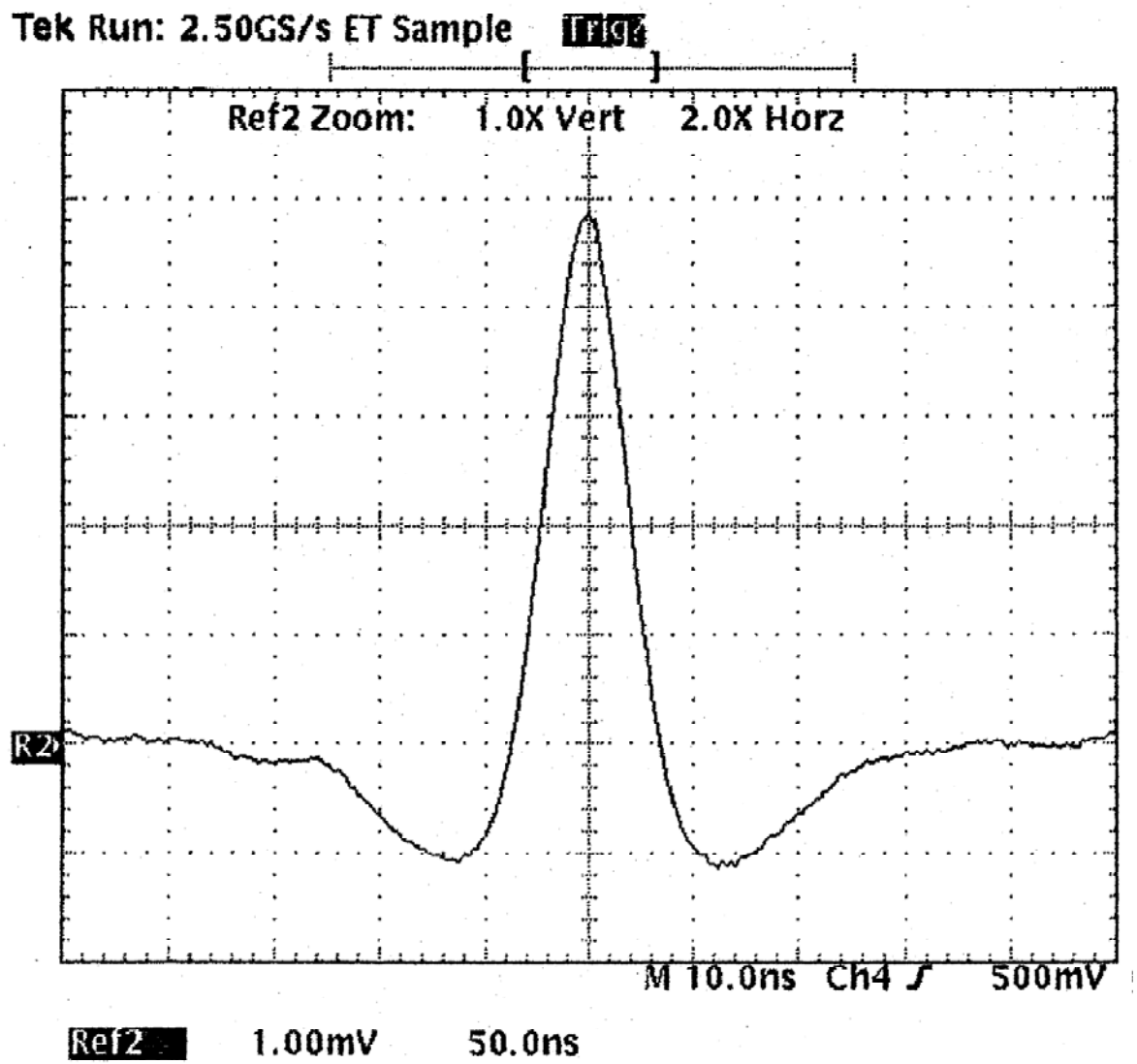
A.6 Autocorrelation Function as a Diagnostic Tool



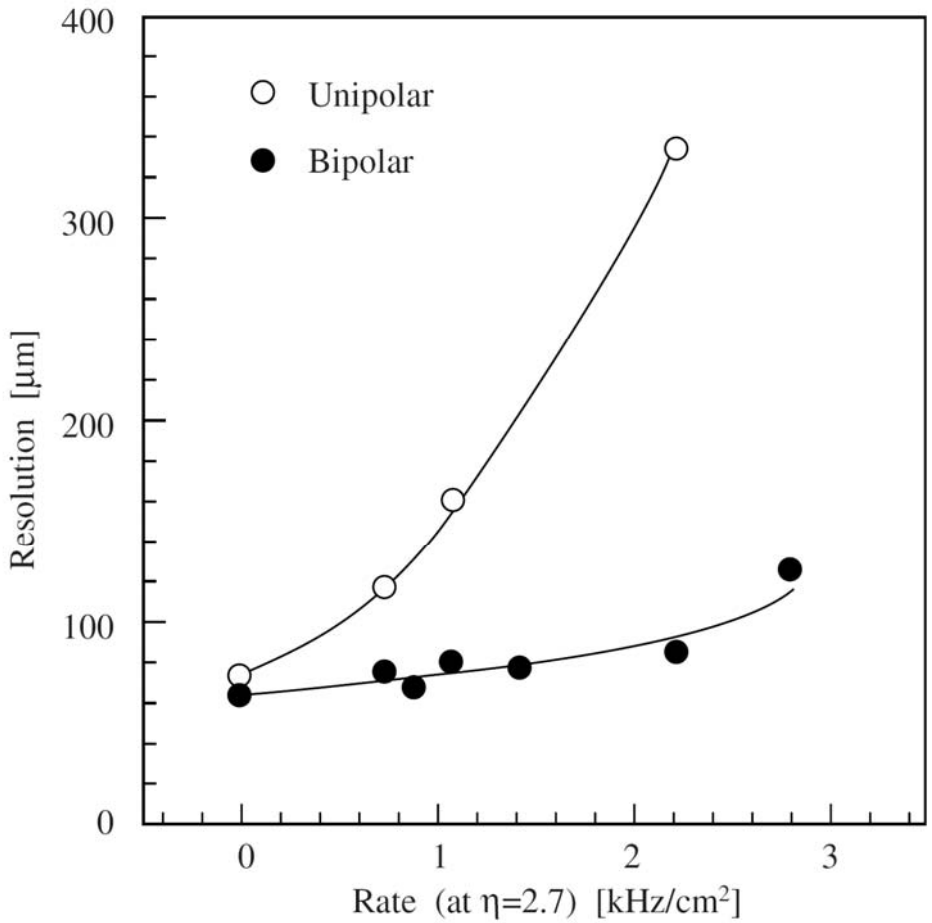
$$\frac{\overline{X(\tau)}}{X_0} = \frac{K(\tau)}{K(0)} = k(\tau)$$

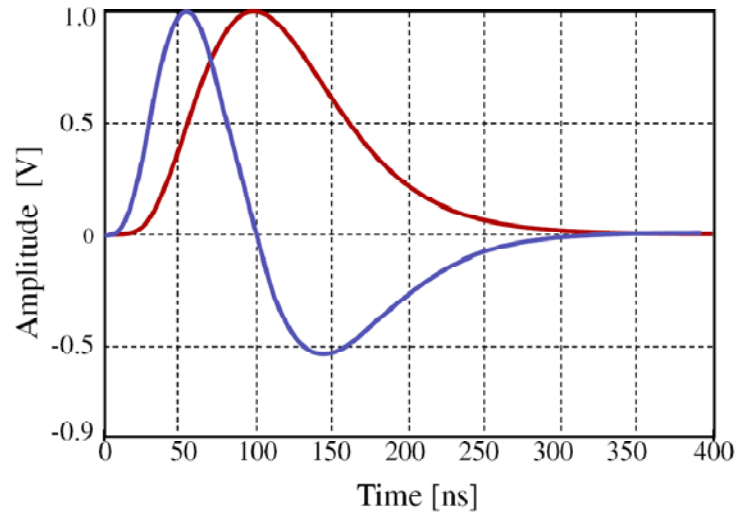
$$\sigma_k^2 = K(0) - \frac{K^2(\tau)}{K(0)} = \sigma^2\left[1 - k^2(\tau)\right]$$

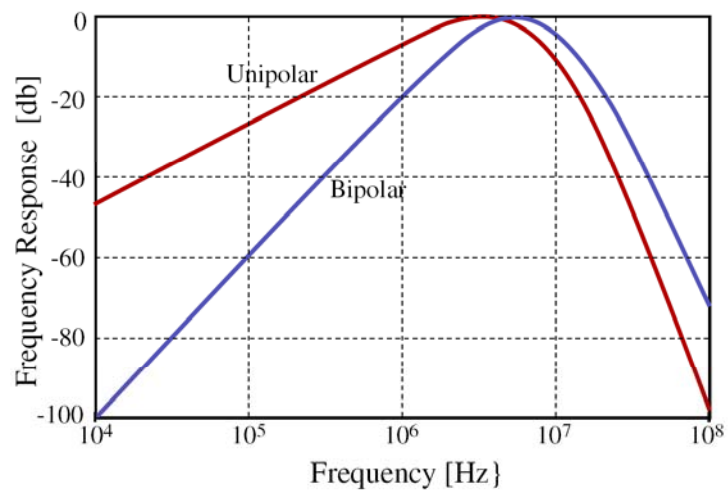
An Example of Noise Autocorrelation Measurement by Digital Oscilloscope



A.7 Pileup Effect on Centroid Position Resolution for Unipolar and Bipolar Shaping (Weighting Function)







Detector: 1.5 m long MWPC with interpolating cathode strip readout; Peaking time ~ 250 ns

2010 Nuclear Science Symposium,
Medical Imaging Conference and
17th Room Temperature Semiconductor Detector Workshop

October 30, 2010 – November 6, 2010 – Knoxville, Tennessee

Semiconductor Technology for Integrated Circuit Front Ends

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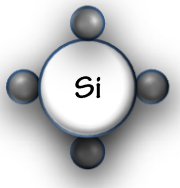
Outline

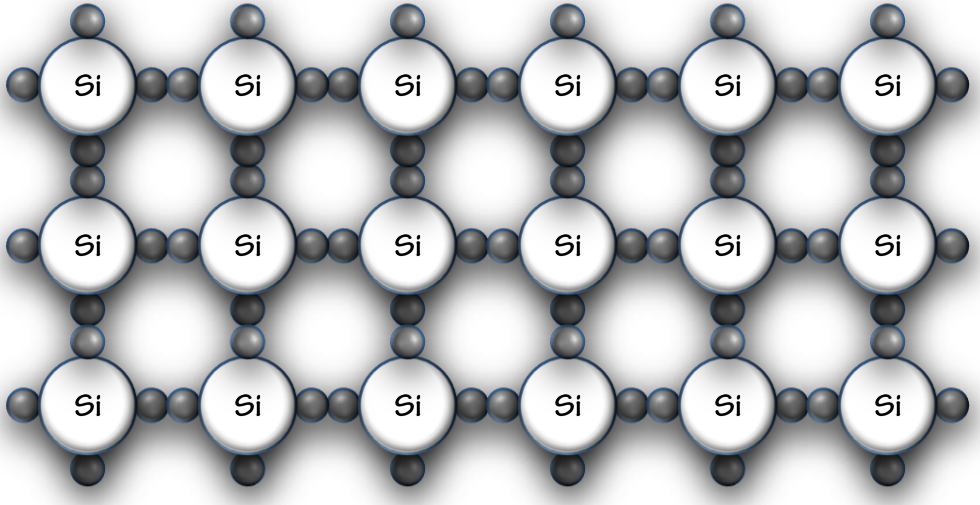
- Basic semiconductor operation
- Devices & models
  - Diodes
  - Bipolar transistors
  - MOS transistors
    - Strong inversion model
    - Moderate and weak inversion
- Device fabrication processes

Basic (e.g. silicon) semiconductor operation

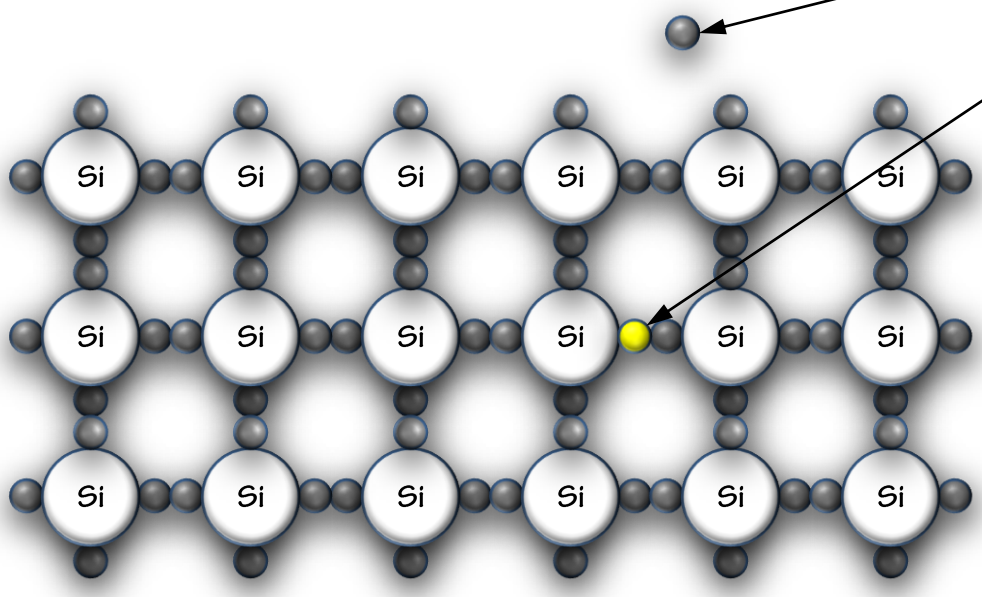
- Silicon (atomic number 14) has 4 valence electrons in outer shell (as does Ge)



- Most stable (lowest energy) state has "filled outer shell" of 8 electrons
- Collections of Si atoms arrange themselves so as to form lowest energy configuration
- Each Si atoms shares its 4 electrons with 4 neighbors (covalent bonds)

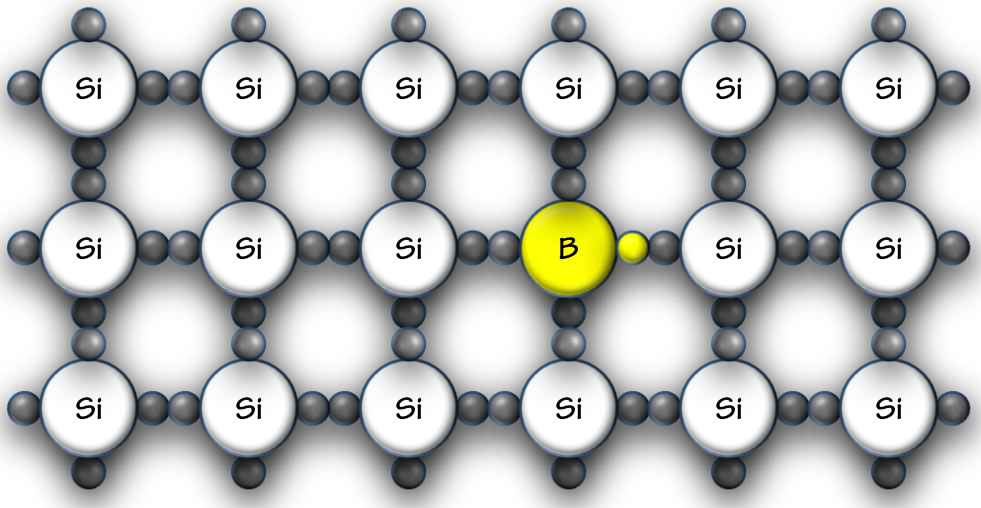


- Covalent bonds can be broken resulting in liberated <u>electron</u> and <u>hole</u>



- Average energy to liberate electron-hole pair : 1.2eV in silicon (bandgap energy)
- Energy can be supplied by particle, photon, or phonon (thermal energy)
- Electrons and holes can move independently in the lattice by
  - Diffusion
  - Electric field
- Electron mobility (velocity/field strength) ~ 3x hole mobility

- Average thermal energy per electron in lattice ~ 25 meV << 1.2 eV
- Very few electrons/hole pairs actually do get liberated thermally (~ 1 in 10^{12})
- Electron or hole concentrations can be dramatically increased by "dopants"
- N type dopants (donors) have extra valance electron than silicon (column V in periodic table: e.g. Arsenic)
- P type dopants (acceptors) have one fewer valance electron than silicon (column III in periodic table – e.g. Boron)



- Donor/acceptor atoms contribute electron/holes on one-to-one basis
- Generally applied by ion implantation (or gaseous diffusion in older processes)
- Ion implantation provides better precise control of concentration and depth profile

Acceptors

Elemental semiconductors

Donors

													III	IV	V			
hydrogen 1 H 1.0079																		helium 2 He 4.0026
lithium 3 Li 6.941	beryllium 4 Be 9.0122												boron 5 B 10.811	carbon 6 C 12.011	nitrogen 7 N 14.007	oxygen 8 O 15.999	fluorine 9 F 18.998	neon 10 Ne 20.180
sodium 11 Na 22.990	magnesium 12 Mg 24.305												aluminium 13 Al 26.982	silicon 14 Si 28.086	phosphorus 15 P 30.974	sulfur 16 S 32.065	chlorine 17 Cl 35.453	argon 18 Ar 39.948
potassium 19 K 39.098	calcium 20 Ca 40.078		scandium 21 Sc 44.956	titanium 22 Ti 47.867	vanadium 23 V 50.942	chromium 24 Cr 51.996	manganese 25 Mn 54.938	iron 26 Fe 55.845	cobalt 27 Co 58.933	nickel 28 Ni 58.693	copper 29 Cu 63.546	zinc 30 Zn 65.39	gallium 31 Ga 69.723	germanium 32 Ge 72.61	arsenic 33 As 74.922	selenium 34 Se 78.96	bromine 35 Br 79.904	krypton 36 Kr 83.80
rubidium 37 Rb 85.468	strontium 38 Sr 87.62		yttrium 39 Y 88.906	zirconium 40 Zr 91.224	niobium 41 Nb 92.906	molybdenum 42 Mo 95.94	technetium 43 Tc [98]	ruthenium 44 Ru 101.07	rhodium 45 Rh 102.91	palladium 46 Pd 106.42	silver 47 Ag 107.87	cadmium 48 Cd 112.41	indium 49 In 114.82	tin 50 Sn 118.71	antimony 51 Sb 121.76	tellurium 52 Te 127.60	iodine 53 I 126.90	xenon 54 Xe 131.29
caesium 55 Cs 132.91	barium 56 Ba 137.33	57-70 *	lutetium 71 Lu 174.97	hafnium 72 Hf 178.49	tantalum 73 Ta 180.95	tungsten 74 W 183.84	rhenium 75 Re 186.21	osmium 76 Os 190.23	iridium 77 Ir 192.22	platinum 78 Pt 195.08	gold 79 Au 196.97	mercury 80 Hg 200.59	thallium 81 Tl 204.38	lead 82 Pb 207.2	bismuth 83 Bi 208.98	polonium 84 Po [209]	astatine 85 At [210]	radon 86 Rn [222]
francium 87 Fr [223]	radium 88 Ra [226]	89-102 * *	lawrencium 103 Lr [262]	rutherfordium 104 Rf [261]	dubnium 105 Db [262]	seaborgium 106 Sg [266]	bohrium 107 Bh [264]	hassium 108 Hs [269]	meitnerium 109 Mt [268]	ununnilium 110 Uun [271]	unununium 111 Uuu [272]	ununbium 112 Uub [277]		ununquadium 114 Uuq [289]				

<u>Doping levels & nomenclature</u>

- Intrinsic silicon (non-doped) ~ 5×10^{22} Si atoms/cm^3
- N- ~ 10^{14} donor atoms/cm^3
- N ~10^{16} donor atoms/cm^3
- N+ ~10^{18} donor atoms/cm^3
- N++ ~10^{20} donor atoms/cm^3 (~ 1% concentration in silicon)
- Similar (but somewhat higher) number s for P-, P, P+, P++

<u>Mobilities of electrons & holes (independent of concentration)</u>

$$\mu_n \approx 1500 \ \frac{cm^2}{V \cdot s} \qquad \mu_p \approx 500 \ \frac{cm^2}{V \cdot s}$$

<u>Resistivity of doped silicon</u>

$$\rho = \frac{1}{q_e} \cdot \frac{1}{\mu_n \cdot n + \mu_p \cdot p}$$

→ Wide range of resistivity possible via doping (controlled by majority carriers)

Motion of charge carriers through lattice

- Drift
  - Carriers are pushed by electric fields
  - Velocity proportional to electric field strength [V/m]
  - Constant of proportionality is *mobility*, μ (different for electrons and holes)

$$v = \mu \cdot E$$

- Diffusion
  - Carriers move by thermal motion from regions of high concentration to regions of lower concentration.
  - Flux is proportional to gradient of carrier concentration
  - Constant of proportionality is the diffusion coefficient, D, also different for electrons and holes.

$$J = q_e \cdot D \cdot \frac{\partial \rho}{\partial x}$$

Motion of charge carriers through lattice

$$D = \mu \cdot \frac{k \cdot T}{q_e}$$ for either holes or electrons [1]

- Note D has units [Lenght^2/time] or "area velocity"

- Recombination
  - Moving electrons can find holes and "drop in". Characterized by *carrier lifetime,* τ, the average time required for probability of annihilation to be 1/e.
  - Diffusion length defined as

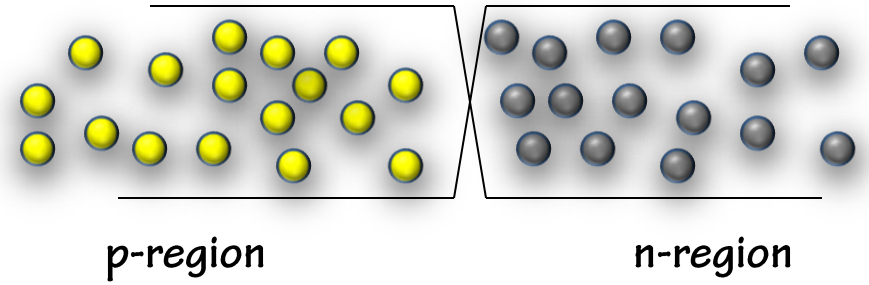
$$L_D \equiv \sqrt{D \cdot \tau}$$

  - Diffusion length is the same as mean-free-path of minority carriers

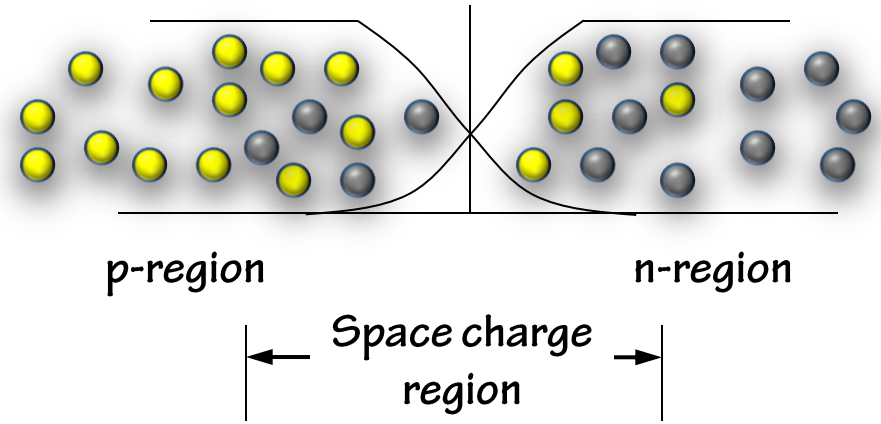
[1] A. Einstein (1905) , in connection with work on statistical physics and Brownian motion

p-n junction diodes

- Any direct contact between p-type and n-type material will form p-n junction diode
- Initial concentrations of majority carriers



- With no applied voltage, there is no field to drive drift of carriers
- Majority carriers in each region move by *diffusion* across junction

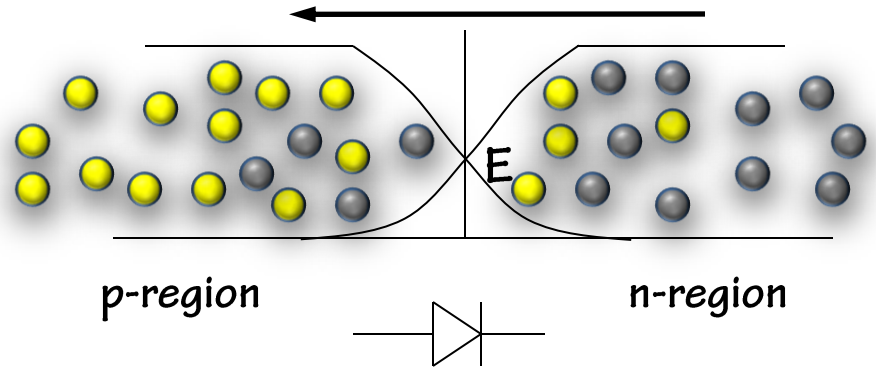


- Note: Frequently one side is more heavily doped than the other

→lopsided distribution of essentially one type of carrier.

p-n junction diodes

- Space charge builds up internal electric field – "*built-in field*"



- Built-in field stops the flow of carriers across the junction
- Externally applied field in *opposite* to built-in field produces current flow. → Forward bias

- p-n junction consists of high electron concentrations separated from high hole concentrations by space charge region, hence form a capacitor → Diffusion capacitance
- Large reverse bias increases the size of the space charge region. → Cd decreases with increasing reverse bias.

p-n junction diodes

Diode current-voltage relationship

$$I = I_s \cdot (e^{\frac{q \cdot V}{n \cdot k \cdot T}} - 1) \approx I_s \cdot e^{\frac{V}{n \cdot V_T}}$$

- *Is = reverse saturation leakage current, generally pico-amps to nano-amps, and is very temperature dependent.*
- Approximation valid for forward bias >a few Vt
- *k= Boltzmann's constant (1.38 x 10^{-23} Volt-Coul/degK)*
- *kT/q = Vt →Thermal voltage (~ 25 mV @ room temp)*
- *n = Ideality factor, generally ~ 2 for pn diode*
- *Small signal conductance in forward bias*

$$G \equiv \frac{\partial I}{\partial V} = \frac{I}{n \cdot V_T} \approx 20 \cdot \frac{ma}{Volt}$$

p-n junction diodes

Junction (diffusion) capacitance

- Diffusion capacitance is defined in terms of "small signal" model
- Incremental increase in V injects additional carriers into space charge region

$$C_D \equiv \frac{\partial Q}{\partial V} = \frac{\partial}{\partial V}(I \cdot \tau) = G \cdot \tau = \frac{I \cdot \tau}{V_T}$$

where τ is the carrier lifetime.

- Note that carrier lifetime is the same as junction time constant. E.g. If the current is made to change abruptly, the voltage will change with single pole response with time constant τ

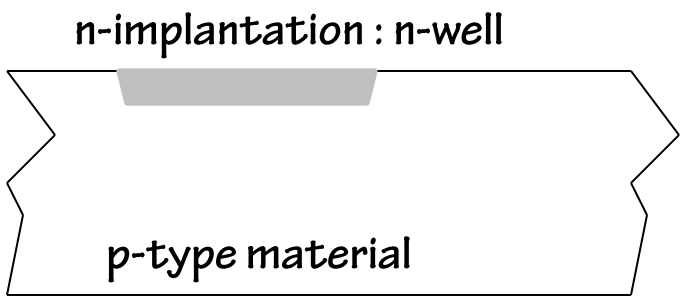
Example

A diode has a carrier lifetime of 100ps. What is diffusion capacitance at 2 ma of bias current?

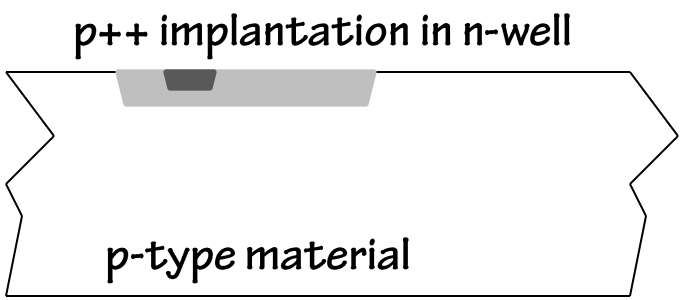
→ At 2 ma, G ~ 10ma/V → C_d ~ $10 \times 10^{-3} \times 100 \times 10^{-12}$ = ~ 1pf

p-n junction diodes Examples

Typical parasitic diodes in CMOS processes

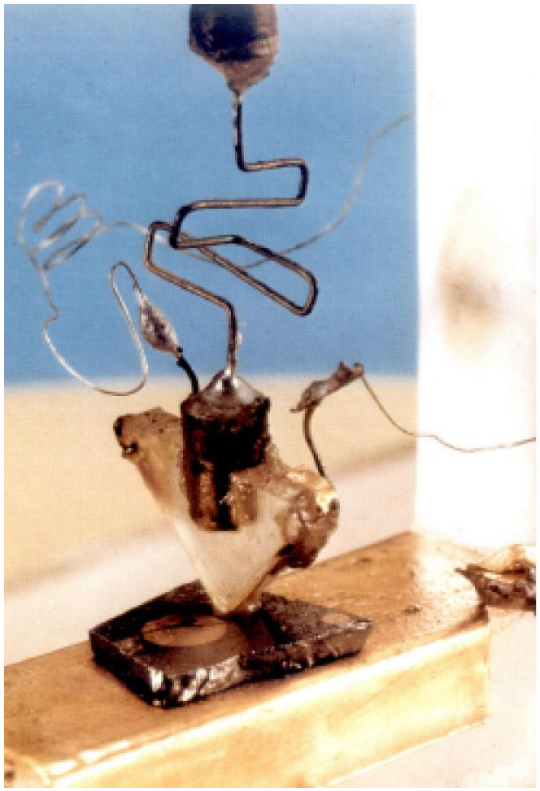


Substrate diode, generally reverse biased



P++ in n-well. Parasitic diode in MOSFETs, generally reverse biased, but can be used as diode in forward direction, or as "input protection" diode.

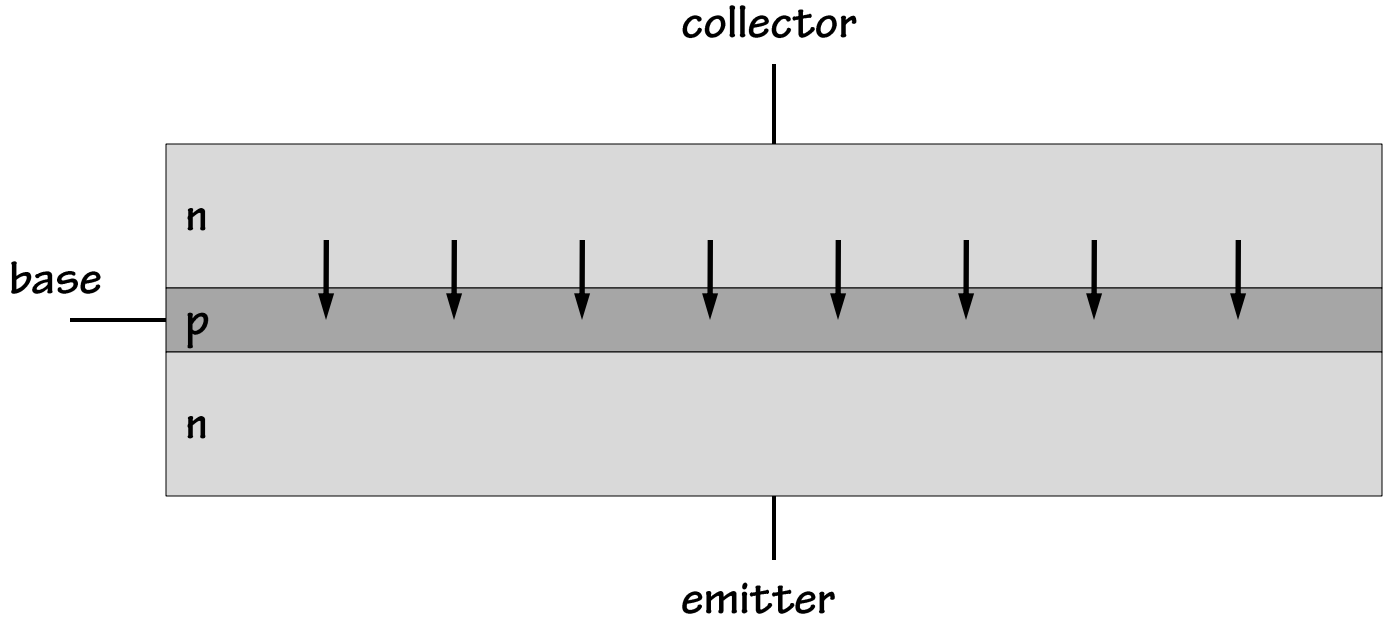
Bipolar transistors

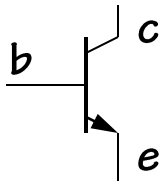


Point Contact Transistor
Bardeen, Brattain 1947

Junction Transistor
Shockley 1948

Bipolar transistors npn



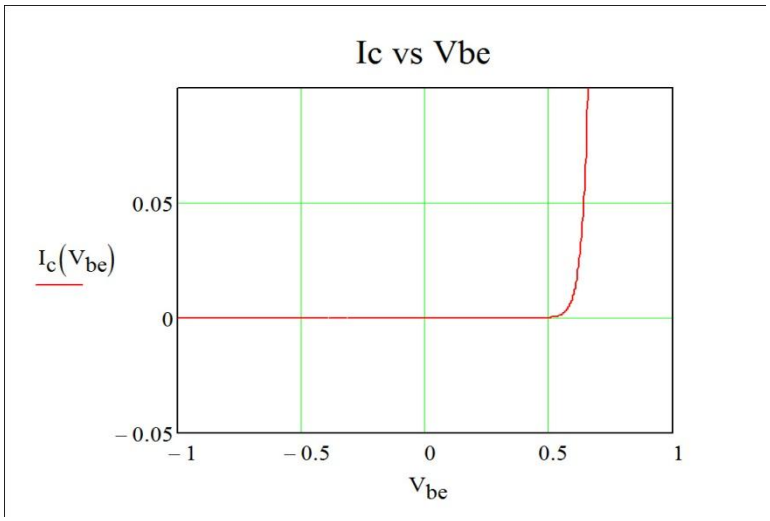


- c-b junction (n-p) is reverse biased with positive voltage.
- Electric field is formed in c-b junction
- b-e junction is forward biased.
- Electrons flow (are injected) from emitter to base, but are swept up by collector by electric field in c-b junction.
- Base typically lightly doped (low hole concentration), long diffusion length, and thin (<< Ld)
- Some recombination occurs in base. → $I_c < I_e$.
- $I_c = I_e - I_b = h_{fe} \times I_b$

Bipolar transistors npn

Collector current vs base-emitter voltage

$$I_c = I_s \cdot (e^{\frac{q \cdot V}{k \cdot T}} - 1) \approx I_s \cdot e^{\frac{V}{V_T}} \quad \rightarrow$$



n = ideality factor ~ 1

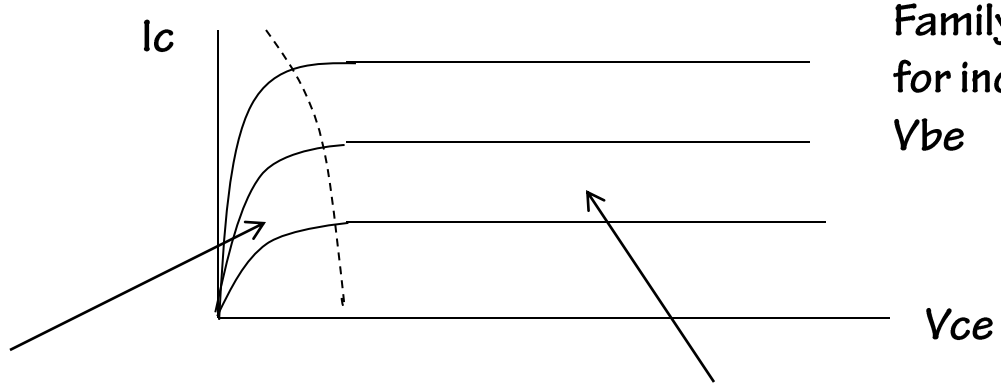
Transconductance (units "mhos" or "Siemens")

$$G_m \equiv \frac{\partial I_c}{\partial V} = \frac{I_c}{V_T} \quad \rightarrow \quad \frac{G_m}{I_c} = 40 \ [V^{-1}]$$

Note: Gm/I for bipolar transistor is gold standard for any particular semiconductor.
→ Highest Gm per unit current

Bipolar transistors npn

Ideal collector current characteristics



Family of curves for increasing Vbe

<u>Saturation region</u>

- Insufficient collector voltage to sweep up all injected electrons

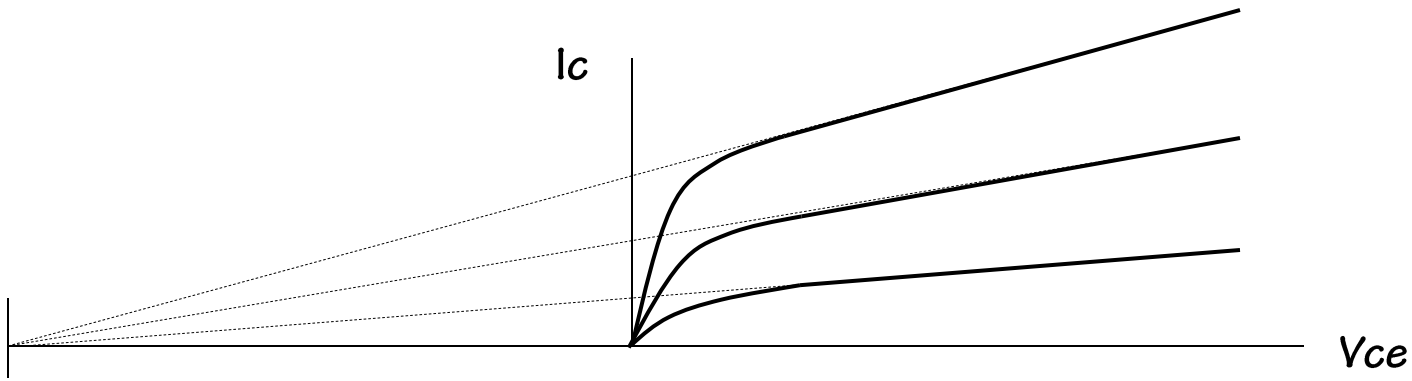
<u>Active or linear region</u>

- Collector sweeps up all injected charge
- I_c independent of V_{ce}
- Output conductance is infinite.

Bipolar transistors npn

Non-ideal collector current characteristics

- Increasing V_{ce} increases the size of the space charge region
- This decreases the effective width (thickness) of the base
- Increases the collector current.
- "Early effect" (shown exaggerated below)



V_A : "Early voltage"

- Finite output (collector) small signal conductance

$$g_o \equiv \frac{\partial(I_c)}{\partial V_{ce}} \approx \frac{I_c}{V_{ce} + V_A}$$

Bipolar transistors npn

Additional effects and small signal modeling

- Base spreading resistance : $R_{bb'}$: Physical ohmic resistance in the base region. Typically 10s to 100s of Ωs
- Effective collector impedance $R_c \sim 1/g_o$
- Base-emitter resistance R_{be}.

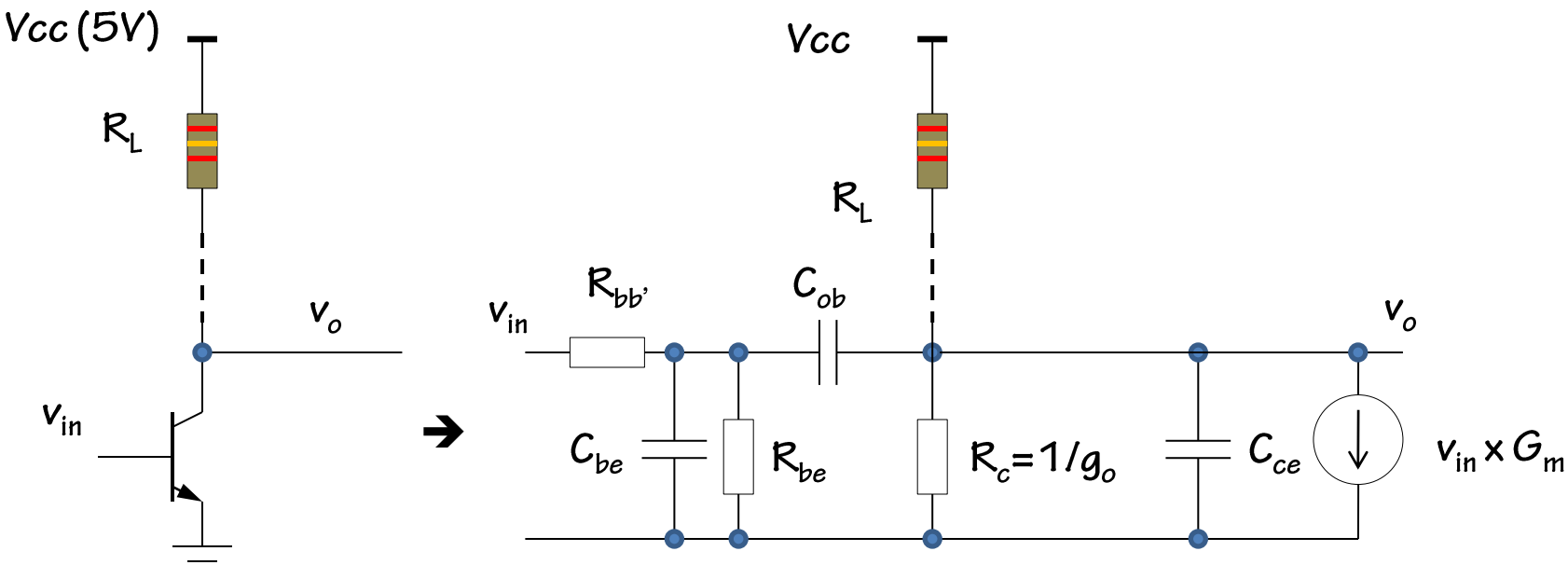
$$R_{be} \equiv \frac{\partial(V_{be})}{\partial I_b} = \frac{\partial(V_{be})}{\partial(I_c / h_{fe})} = \frac{h_{fe}}{G_m}$$

Example

- Ic = 2ma → Gm = 2ma/25mV=80 mS
  →1/Gm = 12.5Ω

- hfe = 120 → Rbe = 120 x 12.5 = 1.5kΩ

Common emitter amplifier & "Hybrid π model (somewhat simplified)"

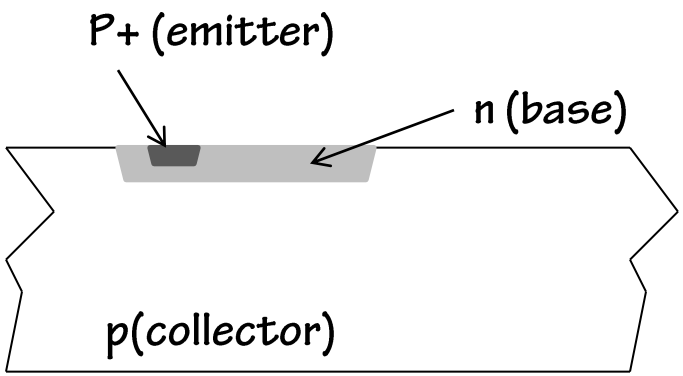


- Can be viewed as
  - Current amplifier
    - → low frequency gain h_{fe}
    - → Dominant pole $1/(C_{be} R_{be})$
    - → Unity (current) gain bandwidth @ $\omega_t = G_m/C_{be}$
    - → Both bipolar transistors and MOSFETs are characterized by ω_t
  - VCCS – Transconductance amplifier – Much higher frequency configuration

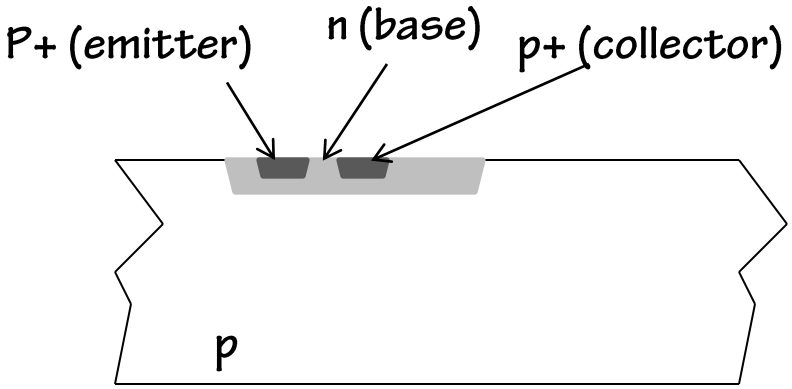
Bipolar transistors

Simple (sometimes parasitic) transistor structures

Vertical pnp (common collector)

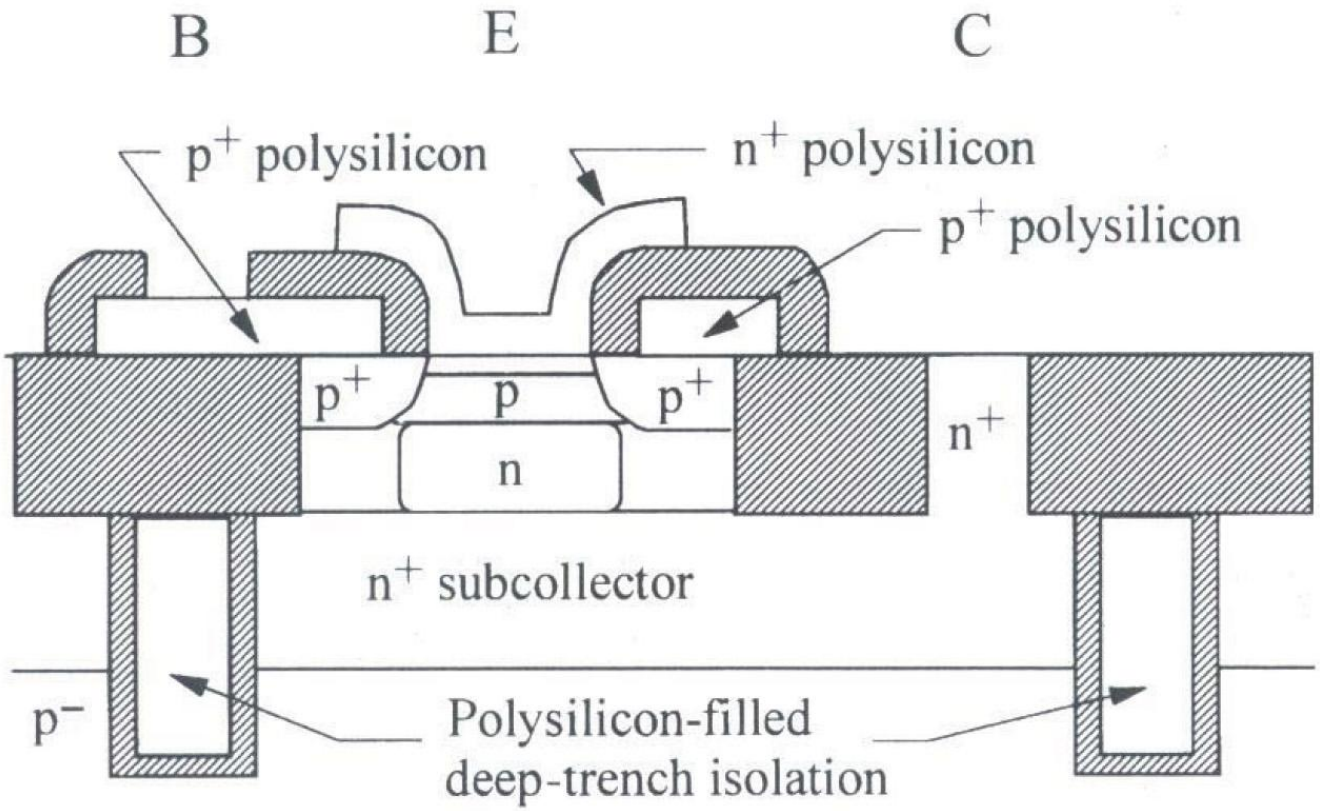


Lateral pnp



Bipolar transistors
npn c

Deep-trench-isolated, double-polysilicon, self-aligned bipolar technology



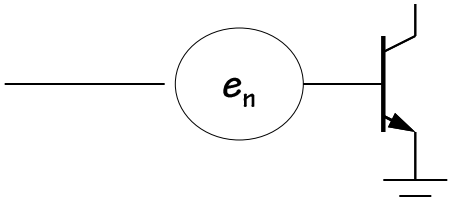
Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.

From slides by G. Anelli – pg 37

Bipolar transistors
Noise model

<u>Base spreading resistance,</u> $R_{bb'}$

Thermal voltage noise source in series with base



$$e_n = \sqrt{4kT \cdot R_{bb'}}$$

Example

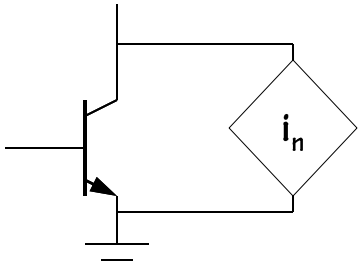
$R_{bb'} = 62\Omega \rightarrow e_n = 1$ nV/Root(Hz)

Bipolar transistors Noise model

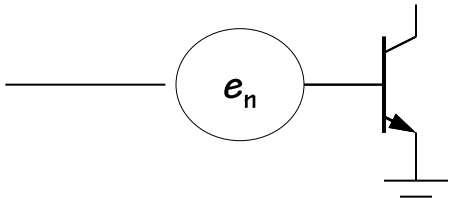
- Collector-base junction is reverse biased. → Collector current suffers <u>shot (Poisson) noise</u>

$$i_n = \sqrt{2 \cdot q_e \cdot I_c}$$

where i_n is current noise density in amps/Root(Hz)



- For purposes of analysis, collector shot noise can be represented as an equivalent voltage current density (e_n) across the base-emitter junction. e_n has units of volts/Root(Hz)



$$e_n = \frac{i_n}{g_m} = \frac{V_T}{I_c} \cdot \sqrt{2 \cdot q_e \cdot I_c} = V_T \cdot \sqrt{\frac{2 \cdot q_e}{I_c}}$$

More current →lower noise in common emitter configuration

Bipolar transistors
Noise model

Collector shot noise can be expressed in terms of an "Equivalent noise resistance"

$$e_n = V_T \cdot \sqrt{\frac{2 \cdot q_e}{I_c}} \equiv \sqrt{4kT \cdot R_{noise}}$$

$$R_{noise} = \frac{1}{2} \cdot \frac{V_T}{I_c}$$

Example

- Transistor at room temperature
- I_c = 1 ma

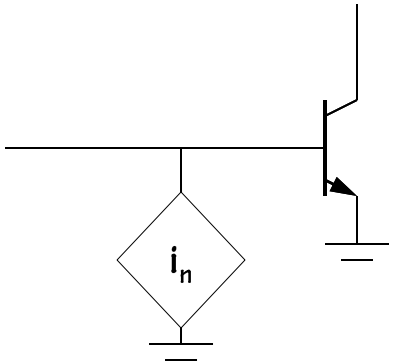
→ R_{noise} = 12.5 Ω

→ For transistor in previous example, input series noise dominated by $R_{bb'}$ (62 Ω)

Bipolar transistors
Noise model

<u>Base current shot noise</u>

$$i_n = \sqrt{2 \cdot q_e \cdot I_b} = \frac{\sqrt{2 \cdot q_e \cdot I_c}}{\sqrt{h_{fe}}}$$



Noise source is in parallel with input
→"parallel" noise source.

MOSFETs

Field Effect Transistor Patent – Lilienfeld, 1927

I Claim:-

272437

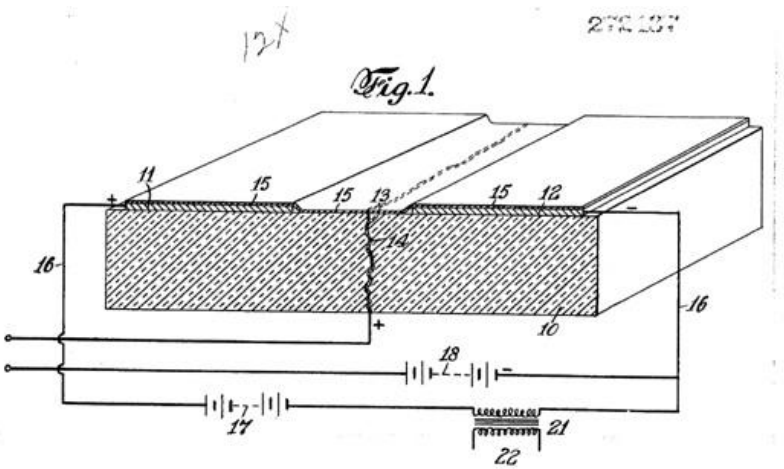
Jul. 19, 1927

-1-

The method of controlling the flow of an electric current in an electrically conducting solid, which comprises establishing an electrostatic influence in proximity to said flow.

-2-

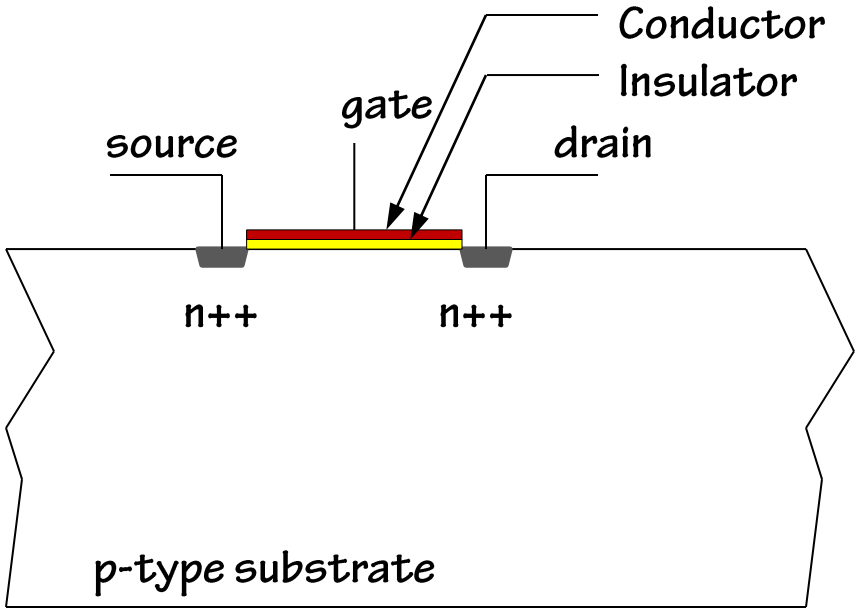
The method of controlling the flow of an electric current in an electrically conducting medium of minute thickness, which comprises subjecting the same to an electrostatic influence.



¾ century later

Quad Core Intel® Xeon™ 7110M (server) – 1,328,000,000 (90nm) transistors

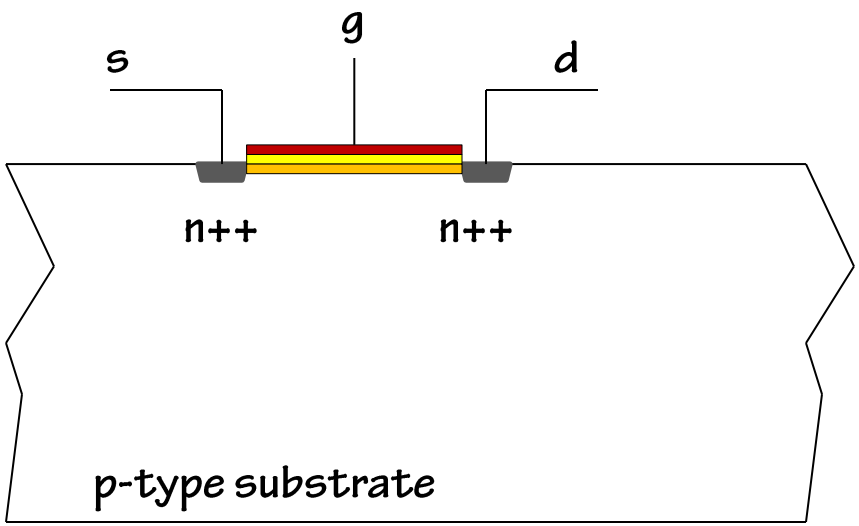
MOSFET
n-channel



Initial conditions

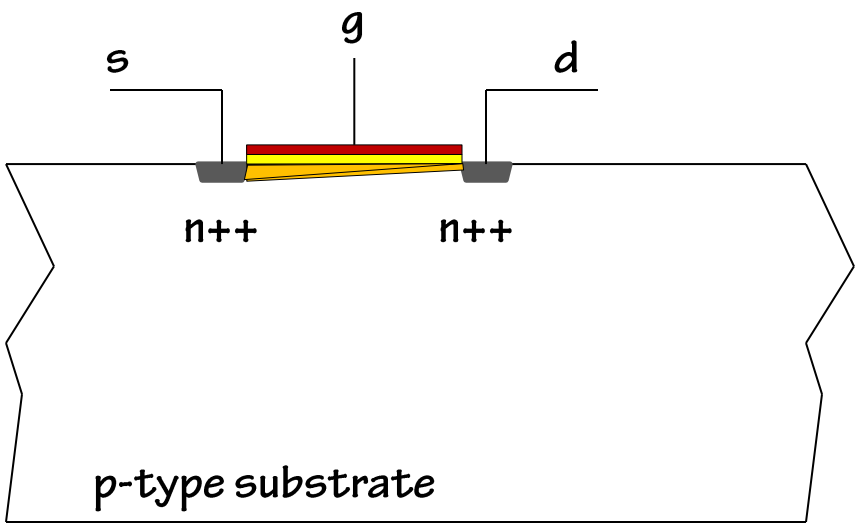
- Set Vsub=0V
- Vs = 0V
- For Vg=0V, no current flows regardless of Vd (back-to-back diodes)

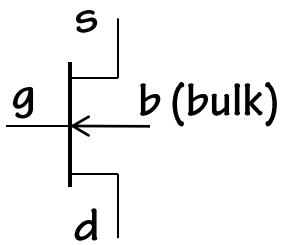
MOSFET
n-channel



- Increasing Vgs establishes electric field from gate to source
- Field attracts repulses holes ~attracts electrons (minority carriers)
- Majority carrier concentrations decrease, minority carrier concentrations increase
- For Vgs > Vth, an "inversion layer" (orange) is formed under gate →conductive layer with n>p
- Typical Vth ~ 0.7V (long channel)
- Electrons become the new majority carriers in inversion channel

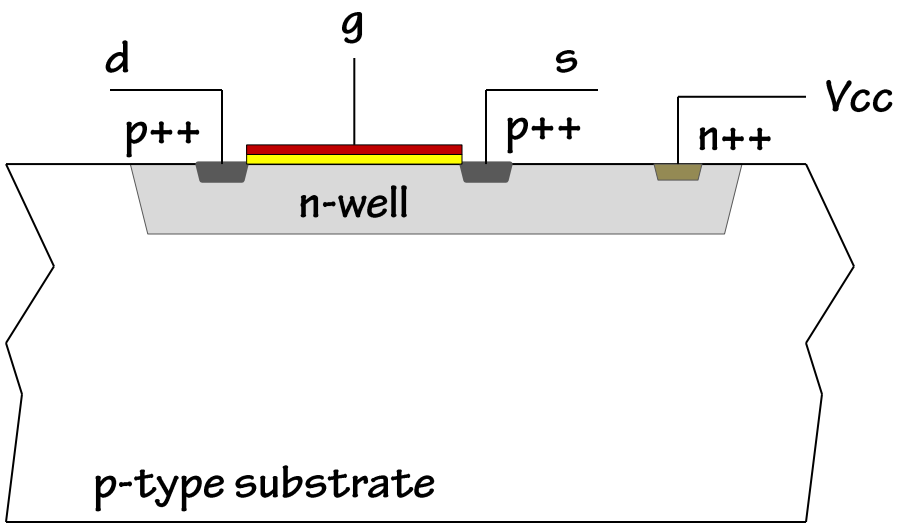
MOSFET
n-channel

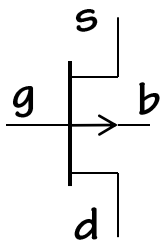




- For any fixed $V_{gs} > V_{th}$, channel is conductive. For small V_{ds}, it is resistive ($I_d \sim V_{ds}$)
- As V_{ds} increases, channel becomes lopsided $\rightarrow E_d < E_s$
- Channel depth shrinks near drain.
- Increasing V_{ds} further does not appreciably increase I_d ("pinch-off)

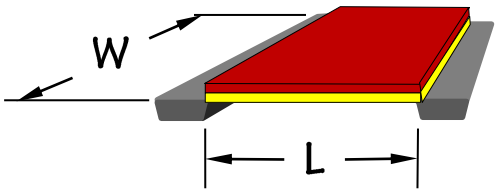
MOSFET
p-channel in p-substrate





Simplified mosfet model Nfet-Strong Inversion

<u>Strong inversion</u> → Vgs-Vth > few hundred mV



<u>Resistive region</u>

- $V_{ds} << V_{gs}-V_{th}$
- No electrons under gate until Vgs>Vth
- For $V_{gs}>V_{th}$, → Total charge under gate

$$Q_g = W \cdot L \cdot C_{ox} \cdot (V_{gs} - V_{th})$$

where C_{ox} is oxide capacitance per unit area

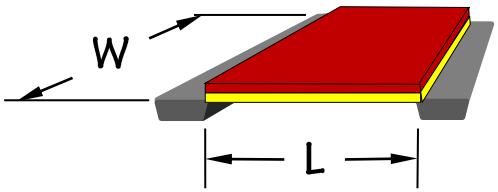
- Time required for charge to be swept from source to drain

$$\tau = \frac{L}{v} = \frac{L}{\mu \cdot E_{ds}} = \frac{L}{\mu \cdot (V_{ds}/L)} = \frac{L^2}{\mu \cdot V_{ds}}$$

Simplified mosfet model nfet

<u>Resistive region</u>

Drain current



$$I_d = \frac{W}{L} \cdot \mu \cdot C_{ox} \cdot (V_{gs} - V_{th}) \cdot V_{ds}$$

- Drain-source "on resistance"

$$R_{ds}(on) = \frac{L}{W} \cdot \frac{1}{\mu \cdot C_{ox} \cdot (V_{gs} - V_{th})}$$

- Definitions used for simplicity

$$K_n \equiv \mu \cdot C_{ox} [\frac{A}{V^2}]$$

Typical values (~ 50 to several 100) μA/V2

$$V_e \equiv V_{gs} - V_{th}$$

Simplified mosfet model nfet

<u>Transition region</u>

V_{ds} comparable to V_{gs}-V_{th}

Charge density under gate

$$\rho(0) = C_{ox} \cdot (V_{gs} - V_{th})$$

$$\rho(L) = C_{ox} \cdot [(V_{gs} - V_{th}) - V_{ds}]$$

Total charge

$$Q = W \cdot L \cdot C_{ox} \cdot [(V_{gs} - V_{th}) - \frac{V_{ds}}{2}]$$

Drain current

$$I_d = \frac{W}{L} \cdot K_n \cdot (V_{gs} - V_{th} - \frac{V_{ds}}{2}) \cdot V_{ds}$$

Quadratic in Vds

Peaks (saturates) at V_{ds}=(V_{gs}-V_{th})

Simplified mosfet model nfet

Saturation region

$$I_d = \frac{W}{2 \cdot L} \cdot K_n \cdot (V_{gs} - V_{th})^2$$

Drain conductance (output conductance)

$$g_o \equiv \frac{\partial I_d}{\partial V_{ds}} = 0$$

→ Infinite output impedance

Transconductance

$$g_m \equiv \frac{\partial I_d}{\partial V_{gs}} = \sqrt{2 \cdot K_n \cdot \frac{W}{L} \cdot I_d}$$

Transconductance per unit drain current

$$\frac{g_m}{I_d} = \sqrt{2 \cdot K_n \cdot \frac{W}{L \cdot I_d}}$$

Simplified mosfet model Weak Inversion

Can MOSFET's transconductance per unit drain current rival that of bjt??

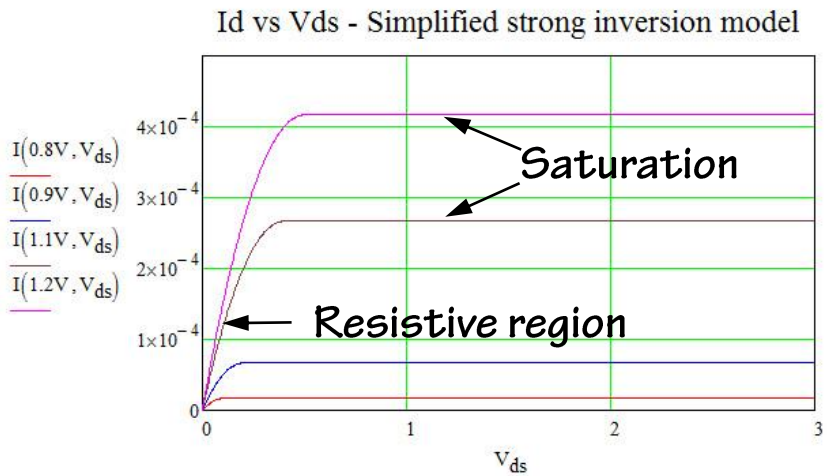
$$\sqrt{2 \cdot K_n \cdot \frac{W}{L \cdot I_d}} \approx \frac{1}{V_T} \approx \frac{1}{25 \cdot mV}$$

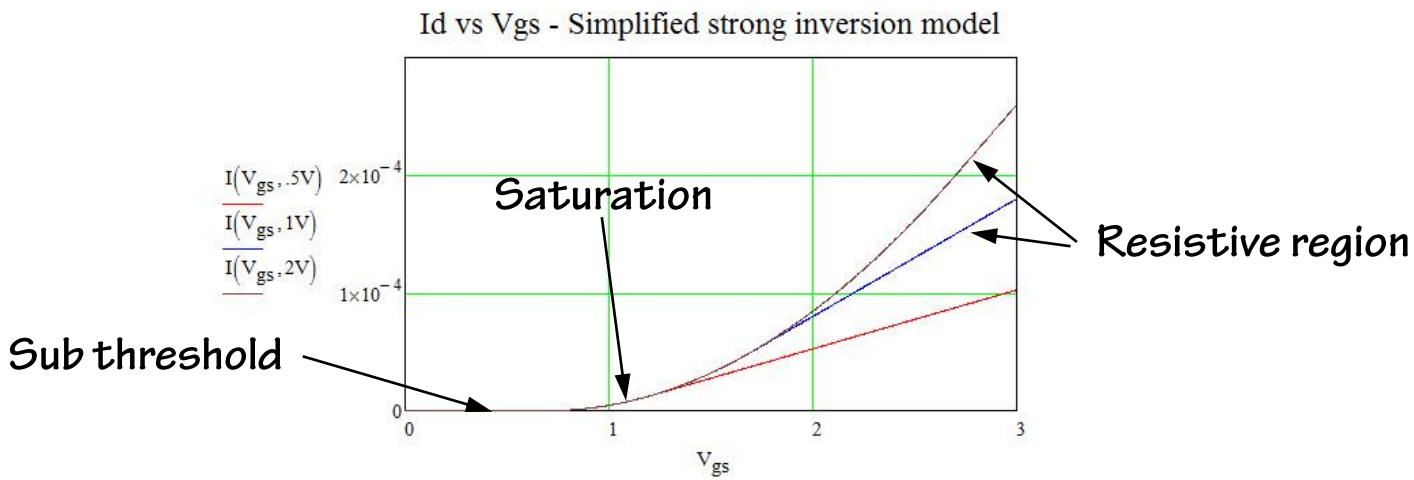
Expressing this in terms of gate voltage, this should occur when

$$V_{gs} - V_{th} \leq 2 \cdot V_T \approx 50 \cdot mV$$

But this doesn't happen because "strong inversion" assumption becomes invalid.
→At very small values of "effective" gate voltage, operation enters "weak inversion" where strong inversion equations do not apply.
→ Can also be viewed as region in which drain current "density" (Id per unit W) becomes very small.
→ Drain current expressions become exponential, similar to those of bjt.

Simplified mosfet model nfet





Note: In this example, Kn=100 x10^{-6} A/V^2 and W/L = 1

Simplified mosfet model
Channel length modulation

Model can be tweaked "by hand" to make drain conductance finite

→ In linear & saturation regions, make following replacements

Linear

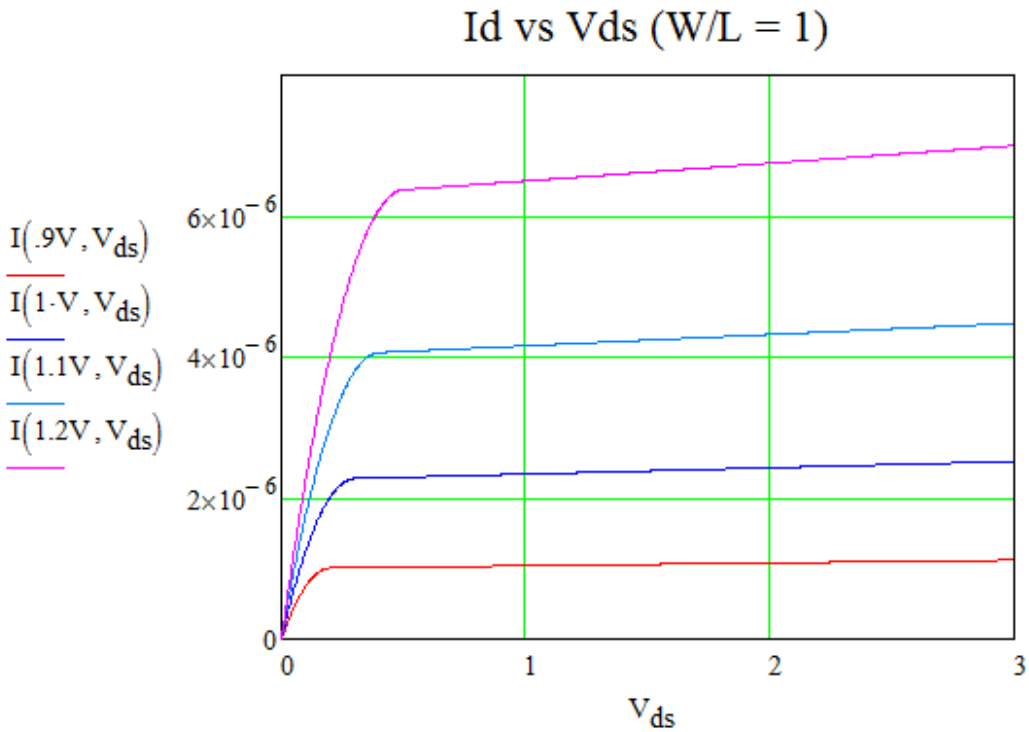
$$I_d = \frac{W}{L} \cdot K_n \cdot (V_{gs} - V_{th} - \frac{V_{ds}}{2}) \cdot V_{ds} \Rightarrow \boxed{\frac{W}{L} \cdot K_n \cdot (V_{gs} - V_{th} - \frac{V_{ds}}{2}) \cdot V_{ds} \cdot (1 + \lambda \cdot V_{ds})}$$

Saturation

$$I_d = \frac{W}{2 \cdot L} \cdot K_n \cdot (V_{gs} - V_{th})^2 \Rightarrow \boxed{\frac{W}{2 \cdot L} \cdot K_n \cdot (V_{gs} - V_{th})^2 \cdot (1 + \lambda \cdot V_{ds})}$$

where λ is an empirical Early coefficient (units of V^{-1})

Simplified mosfet model
Basewidth modulation



Output conductance

$$g_o \equiv \frac{\partial I_d}{\partial V_{ds}} = \frac{\lambda \cdot I_d}{1+\lambda \cdot V_{ds}} \approx \lambda \cdot I_d$$

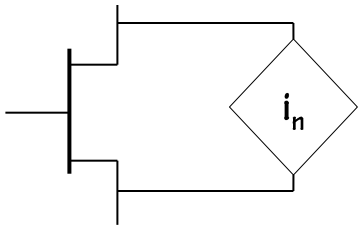
Example

Id=4uA, λ=1/25V
→go ~ 1/60kΩ

MOSFET
Noise models

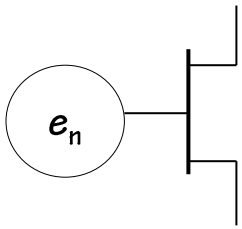
- In saturation, dominant noise source is <u>thermal noise</u> in drain resistance
- Physical drain resistance can be approximated by [1]

$$R_{eq} \approx \frac{3}{2} \cdot \frac{1}{g_m}$$



$$i_n = \sqrt{\frac{4 \cdot kT}{R_e}} = \sqrt{\frac{8}{3} \cdot kT \cdot g_m}$$

- Can be expressed as an equivalent noise voltage source in series with gate



$$e_n = \sqrt{\frac{8}{3} \cdot \frac{kT}{g_m}}$$

[1] "Analog MOS Integrated Circuits for Signal Processing" R. Gregorian, G. Temes - Wiley

MOSFET Noise models

1/f noise

- Thermal and shot noise are examples of "white" noise → density is frequency independent
- MOSFETs have additional "pink" noise → Power per unit frequency is proportional to 1/frequency
- Thus, power per decade of frequency is independent of frequency.
- 1/f noise density scales as gate area (gate capacitance) → W x L

$$e_T^2 = \frac{8}{3} \cdot \frac{kT}{g_m} + \frac{K_f \cdot I_d}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f}$$

where Kf is "flicker noise coefficient"

- Can be characterized by "1/f noise corner frequency" at which the two terms above become equal
- Above f_{corner}, white noise dominates. Below f_{corner} 1/f noise dominates
- 1/f noise tends to dominate for "long shaping time" circuits
- Can frequently be fixed by increasing transistor size, both W & L
- Tends to be smaller in pfets than in nfets.

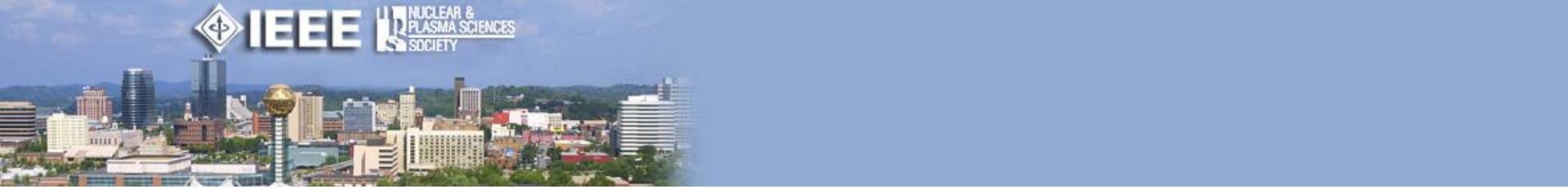
MOSFET Modeling

Summary and conclusions

- Simple MOSFET models, including noise, are intuitive and can guide initial designs
- Models are similar to SPICE Level-3 models
- Not nearly as accurate as BSIM models, available through vendors MOSIS, or Euro-practice. The shorter the gate length, the more this is true.
- ASIC designs CAN be made with BSIM/SPICE models alone, but one has to rely on simulator "sensitivity" modeling.

- Unvarnished opinion
  - Start with simple model hand calculations
  - Estimate transconductances, choose initial Ws and Ls, include major noise sources, 1/f contribution, etc
  - Tune up the models with more accurate SPICE simulations →iterative procedure

- For those who are interested in pursuing more extensive physics based models, there is EKV (See bibliography)



Bibliography

1. "Electronic Principles – Physics, Models, and Circuits" P. Gray, C. Searl – Wiley
2. "Analog MOS Integrated Circuits for Signal Processing". R. Gregorian, G. Temes – Wiley
3. "Silicon VLSI Technology" J. Plummer, M. Deal, P. Griffin – Prentiss Hall
4. "Analog VLSI Design" M. Haskard, I. May – Prentiss Hall
5. "A Physics Based MOSFET Noise Model for Circuit Simulators" K. Hung, P. Ko, C. Hu, Y. Cheng – IEEE Transactions on Electron Devices Vol 37, No 5 (1990)
6. "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications" Enz, Krummenacher, Vittoz

IEEE Nuclear Science Symposium & Medical Imaging Conference
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29th October 2006

Semiconductor Technology for Integrated Circuit Front Ends

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Outline

- Operation and characteristics of MOS and Bipolar transistors
- Sub-micron CMOS and BiCMOS technologies
- Feature size scaling
- Radiation effects and reliability
- Mixed-signal circuits

Outline

- Operation and characteristics of MOS and Bipolar transistors
  - MOS transistor equations and characteristics
  - MOS transistor small-signal equivalent circuit
  - Bipolar transistor equations and characteristics
  - Bipolar transistor small-signal equivalent circuit
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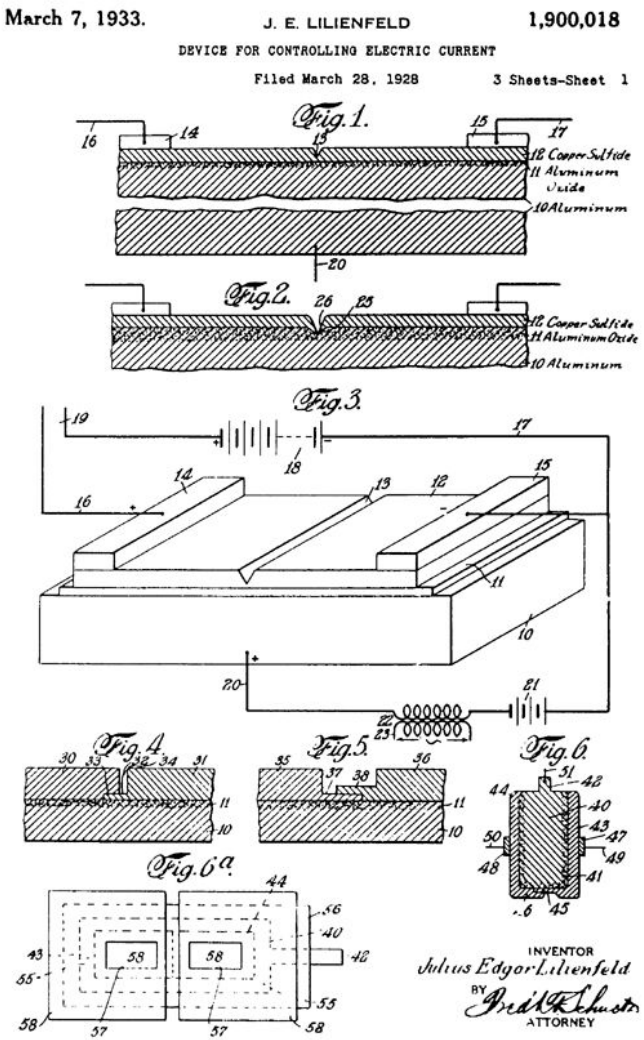
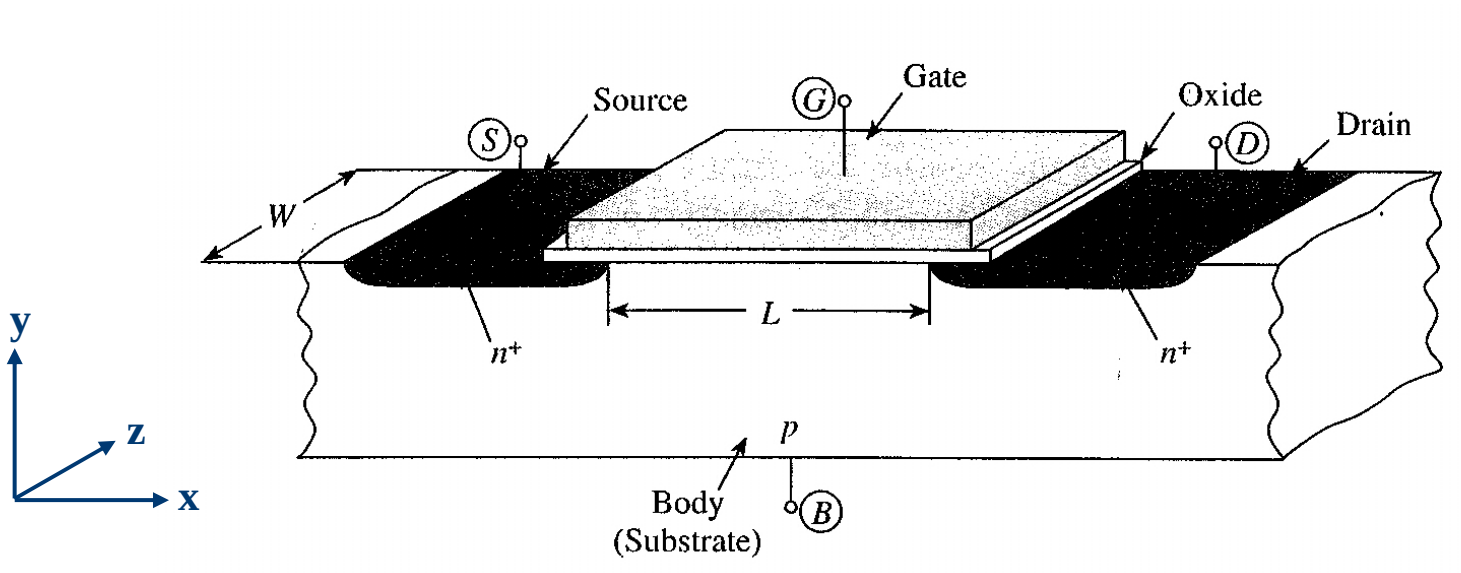
The MOSFET

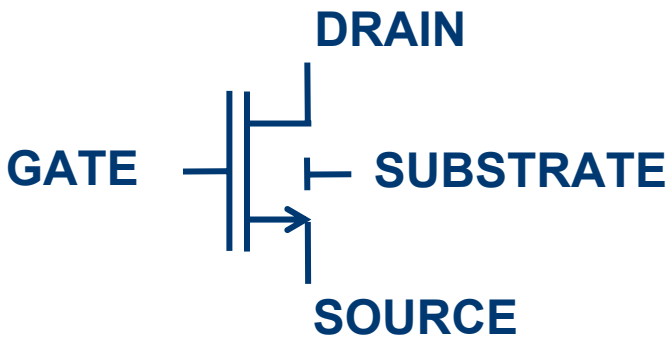


The basic idea behind Field Effect Transistors (FETs) was first patented by J. Lilienfeld in 1930 for the MESFET (MEtal Semiconductor FET) and in 1933 for the MOSFET (Metal Oxide Semiconductor FET). But we had to wait until 1960 to have a technology capable to make a working device.

The first working MOSFET was made in 1960 at the Bell Laboratories by D. Kahng and M. M. Atalla.

The (N)-MOS transistor





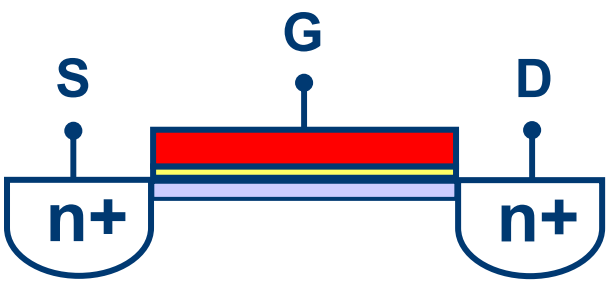
What is a MOS transistor?

Analog circuits: amplifier (V to I)

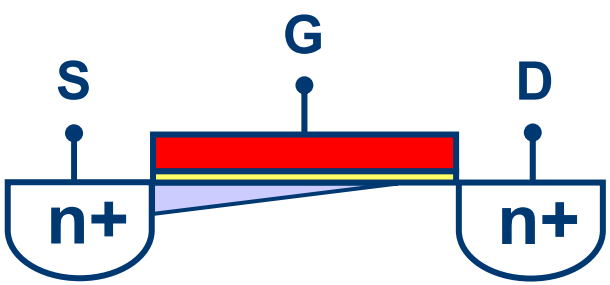
Digital circuits: switch

Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999.

Linear and Saturation regions



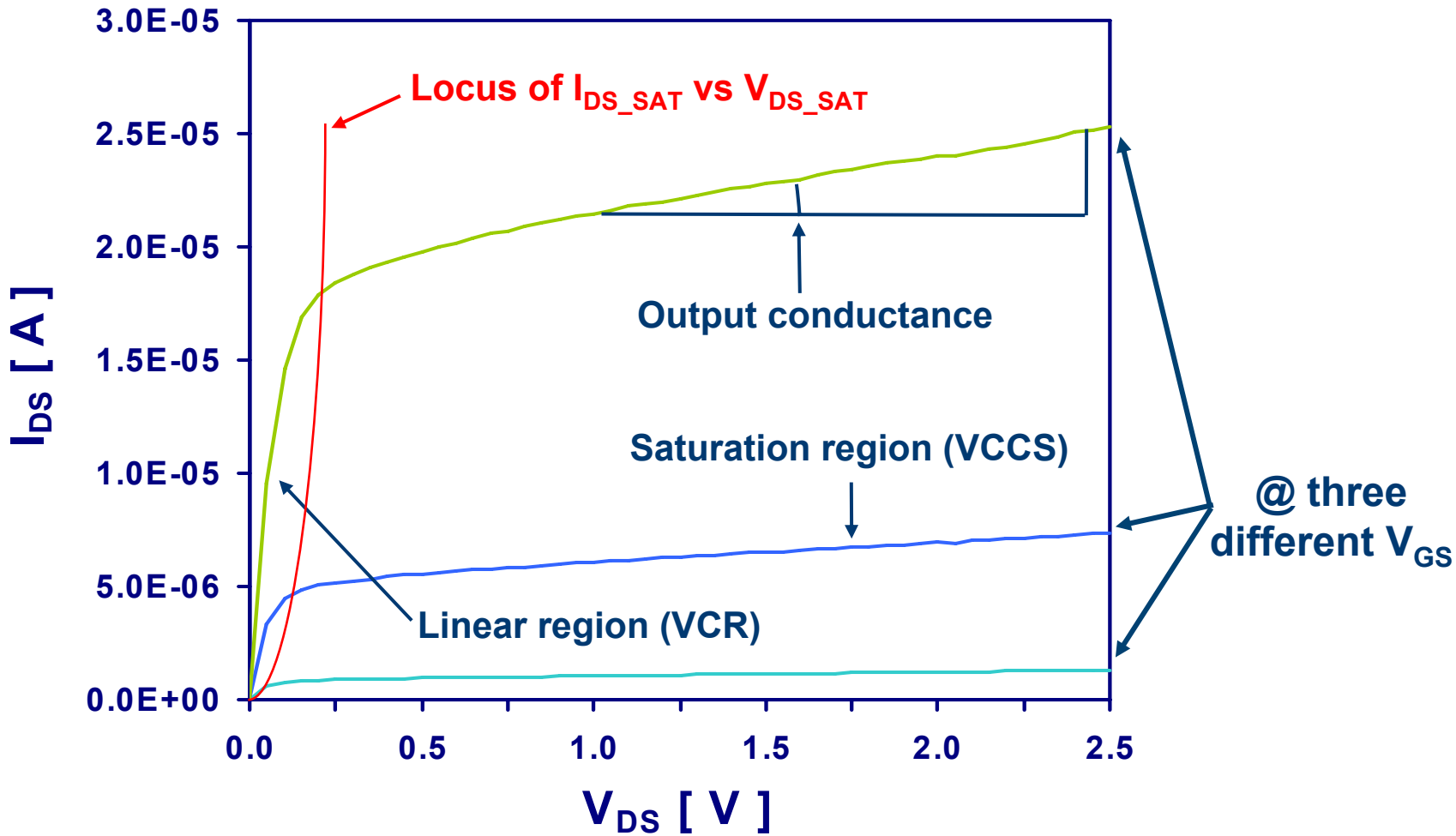
LINEAR REGION (Low V_{DS}):
Electrons are attracted to the SiO_2 – Si interface. A conductive channel is created between source and drain. We have a Voltage Controlled Resistor (VCR).



SATURATION REGION (High V_{DS}):
When the drain voltage is high enough the electrons near the drain are insufficiently attracted by the gate, and the channel is pinched off. We have a Voltage Controlled Current Source (VCCS).

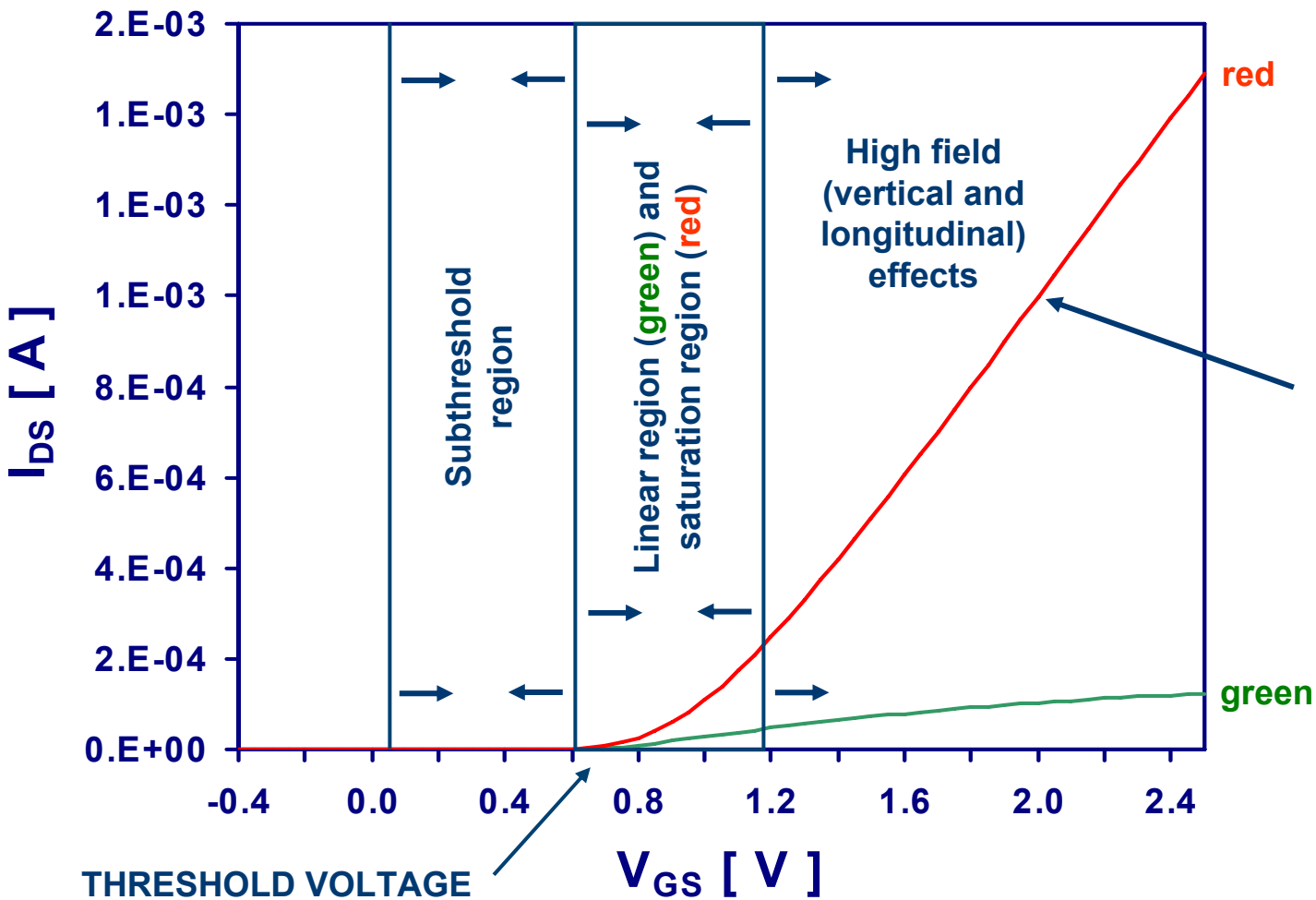
Drain current vs Drain voltage

This is a real device measurement !



Drain current vs Gate voltage

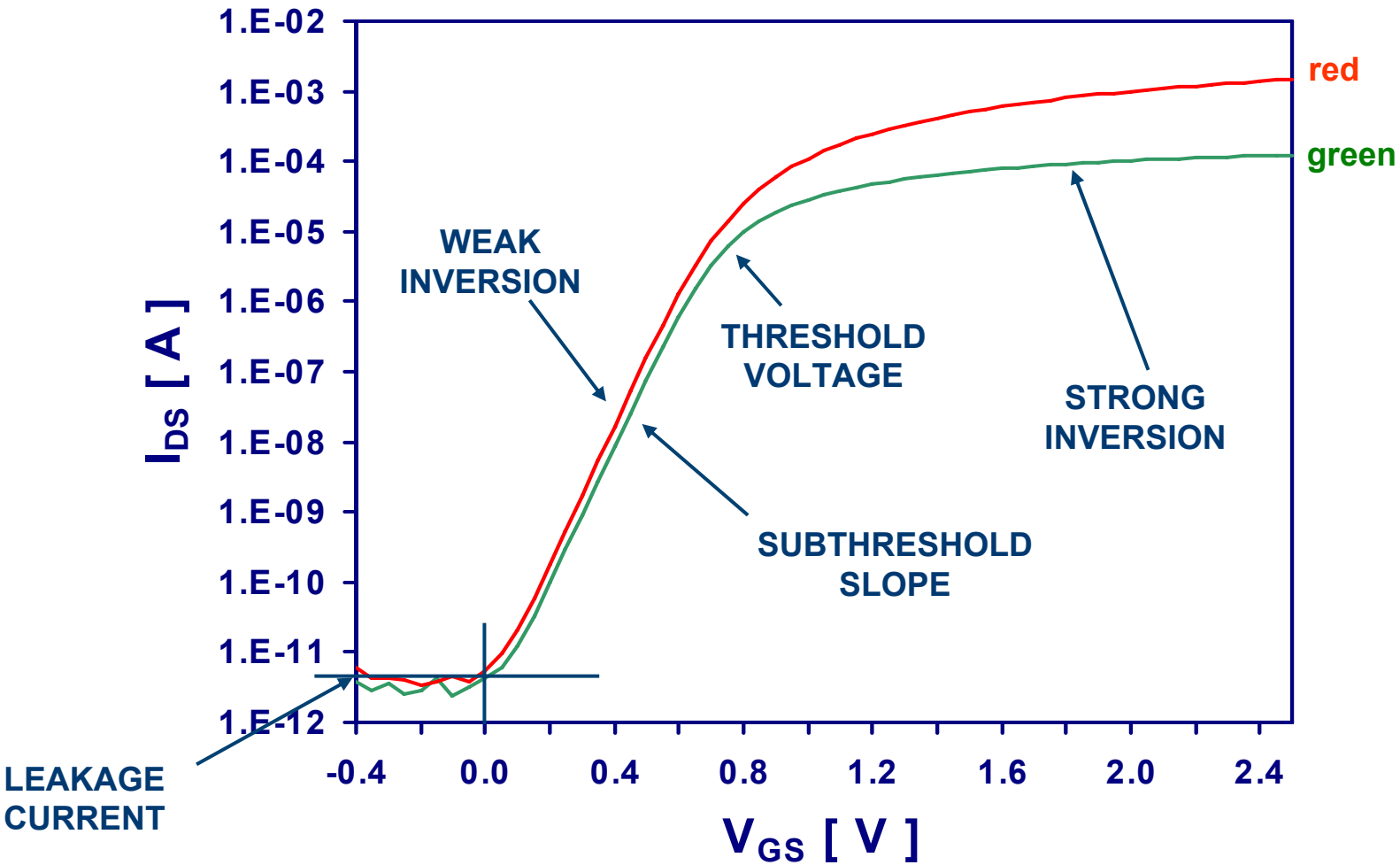
This is also a measurement, same device.



The SLOPE of this plot is called *Transconductance*, and is a very important parameter for analog design (is the "gain" of the V-to-I amplifier).

Log(I_{DS}) vs V_{GS}

Exactly same measurement as before, but semi log scale



Equations: strong inversion

LINEAR REGION:

$$V_{DS} < \frac{V_{GS} - V_T}{n} = V_{DS_SAT}$$

$$I_{DS} = \beta \left(V_{GS} - V_T - \frac{nV_{DS}}{2}\right) V_{DS}$$

Transconductance: $$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta V_{DS}$$

SATURATION REGION:

$$V_{DS} > \frac{V_{GS} - V_T}{n} = V_{DS_SAT}$$

$$I_{DS} = \frac{\beta}{2n} (V_{GS} - V_T)^2$$

Transconductance: $$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\beta}{n}(V_{GS} - V_T) = \sqrt{2\frac{\beta}{n} I_{DS}}$$

$$n = \frac{g_m + g_{mb}}{g_m} \approx 1.x \qquad g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} \qquad \beta = \mu C_{ox} \frac{W}{L} \qquad C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

Equations: weak inversion

$$I_{DS} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{n\phi_t}} \left(1 - e^{-\frac{V_{DS}}{n\phi_t}}\right)$$

If $V_{DS} > 4n\phi_t$ then the drain current does not depend on V_{DS} any longer (saturation)

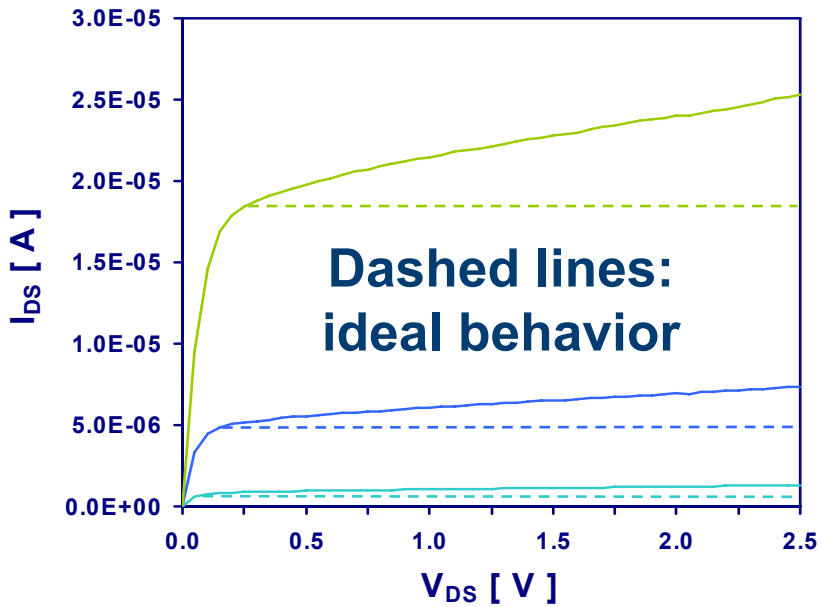
$$I_{DS} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{n\phi_t}}$$

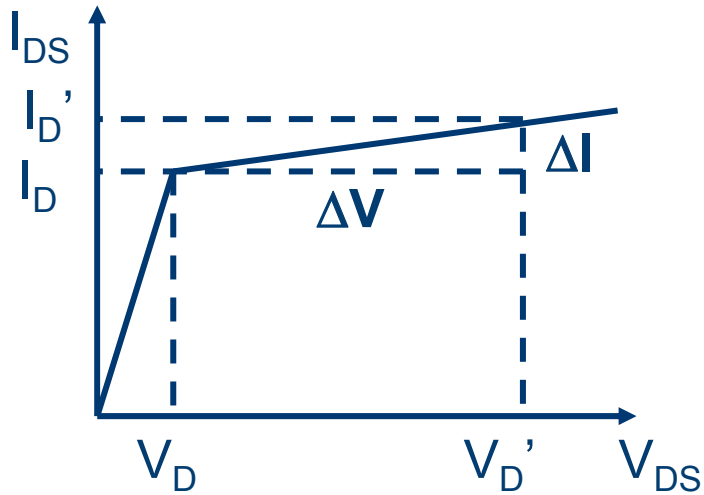
$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{DS}}{n\phi_t}$$

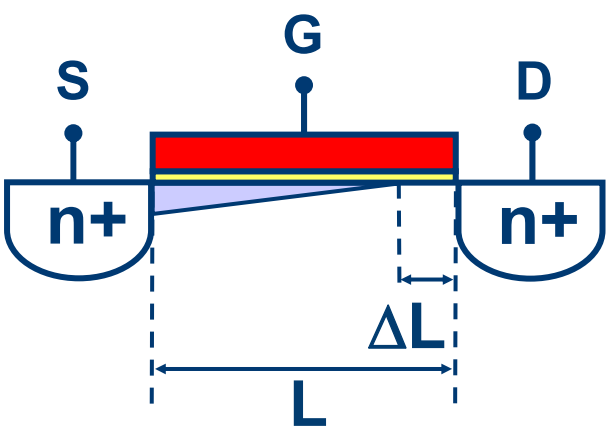
Almost like a bipolar transistor (see later)!

$$\phi_t = \frac{kT}{q} \approx 25 \text{ mV @ } 300 \text{ K}$$

Output conductance







$$G_{out} = \frac{\Delta I}{\Delta V} = \frac{I_D}{\Delta V} \cdot \frac{\Delta L}{L - \Delta L}$$

The non-zero output conductance is related to a phenomenon called *channel length modulation*

Output conductance / resistance

Drain-to-source current in saturation

$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) = I_{DS_SAT} \cdot (1 + \lambda V_{DS})$$

Output conductance

$$g_{out} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda \cdot I_{DS_SAT}$$

Output resistance

$$r_0 = \frac{1}{g_{ds}} = \frac{1}{\lambda \cdot I_{DS_SAT}} = \frac{V_E \cdot L}{I_{DS_SAT}}$$

$$\lambda = \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L - \Delta L} \quad \text{where } \Delta L = f(V_{DS}, N_{Doping})$$

Remember: λ is proportional to 1/L

Equations: addendum

Bulk effect

$$\Delta V_T = \gamma \cdot \left(\sqrt{V_{sb} + \phi_{Si}} - \sqrt{\phi_{Si}} \right) \qquad \gamma = \frac{\sqrt{2 q \varepsilon_{Si} N_a}}{C_{ox}}$$

Source parasitic resistance

$$g_m' = \frac{g_m}{1 + g_m R_S}$$

Vertical electric field effect

$$\mu = \frac{\mu_0}{1 + \theta (V_{GS} - V_T)}$$

Maximum frequency

$$f_{max} = \frac{1}{2\pi} \frac{g_m}{C_{gs}} = \frac{1}{2\pi} \frac{\mu}{nL^2} (V_{GS} - V_T) \quad \text{in s.i.}$$

K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994, Chapter 1.

Equations: velocity saturation

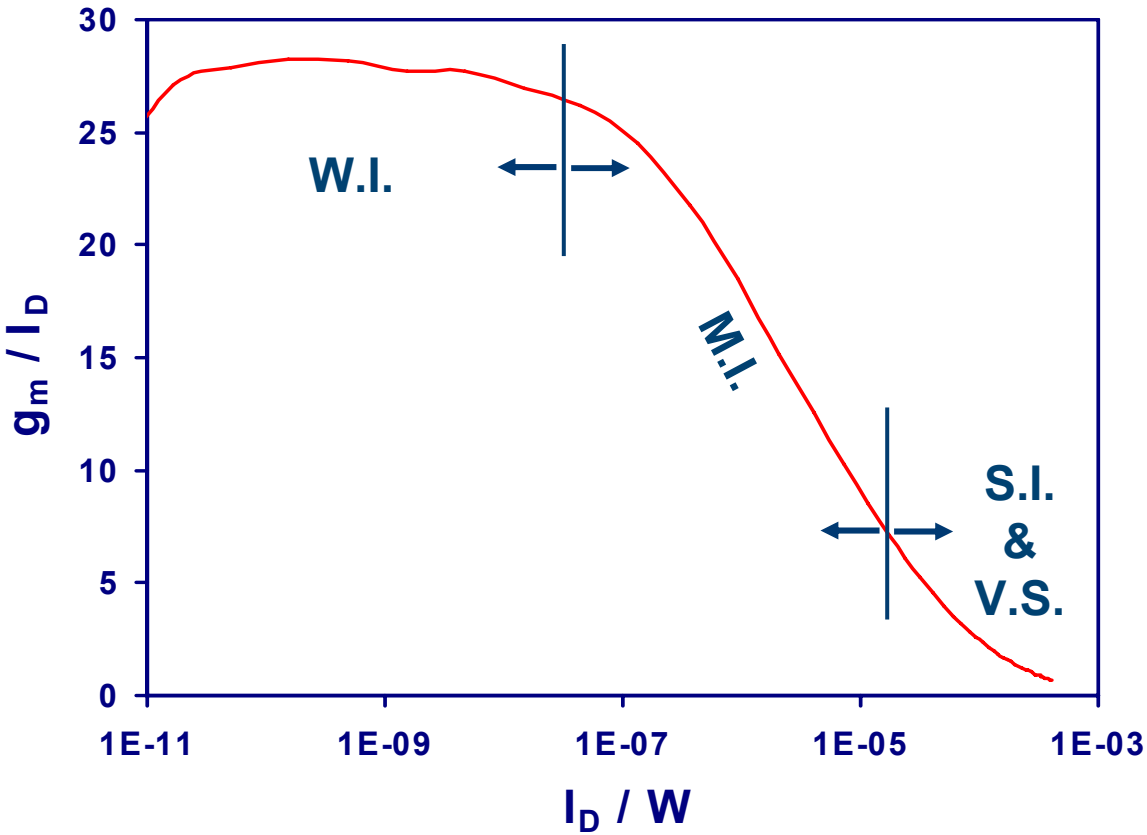
For low values of the longitudinal electric field, the velocity of the carriers increases proportionally to the electric field (and the proportionality constant is the mobility). For high values of the longitudinal electric field (3 V/μm for electrons and 10 V/μm for holes) the velocity of the carriers saturates.

$$I_{DS_v.s.} = WC_{ox}v_{sat}(V_{GS} - V_T) \quad \text{with} \quad v_{sat} = 10^7 \frac{cm}{s}$$

$$g_{m_v.s.} = WC_{ox}v_{sat}$$

$$f_{max_v.s.} = \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{1}{2\pi}\frac{v_{sat}}{L}$$

g_m / I_D vs $\log(I_D / W)$



Weak Inversion (W.I.)

$$g_m = \frac{I_{DS}}{n\phi_t} \longrightarrow \frac{g_m}{I_D} = \frac{1}{n\phi_t}$$

Strong Inversion (S.I.)

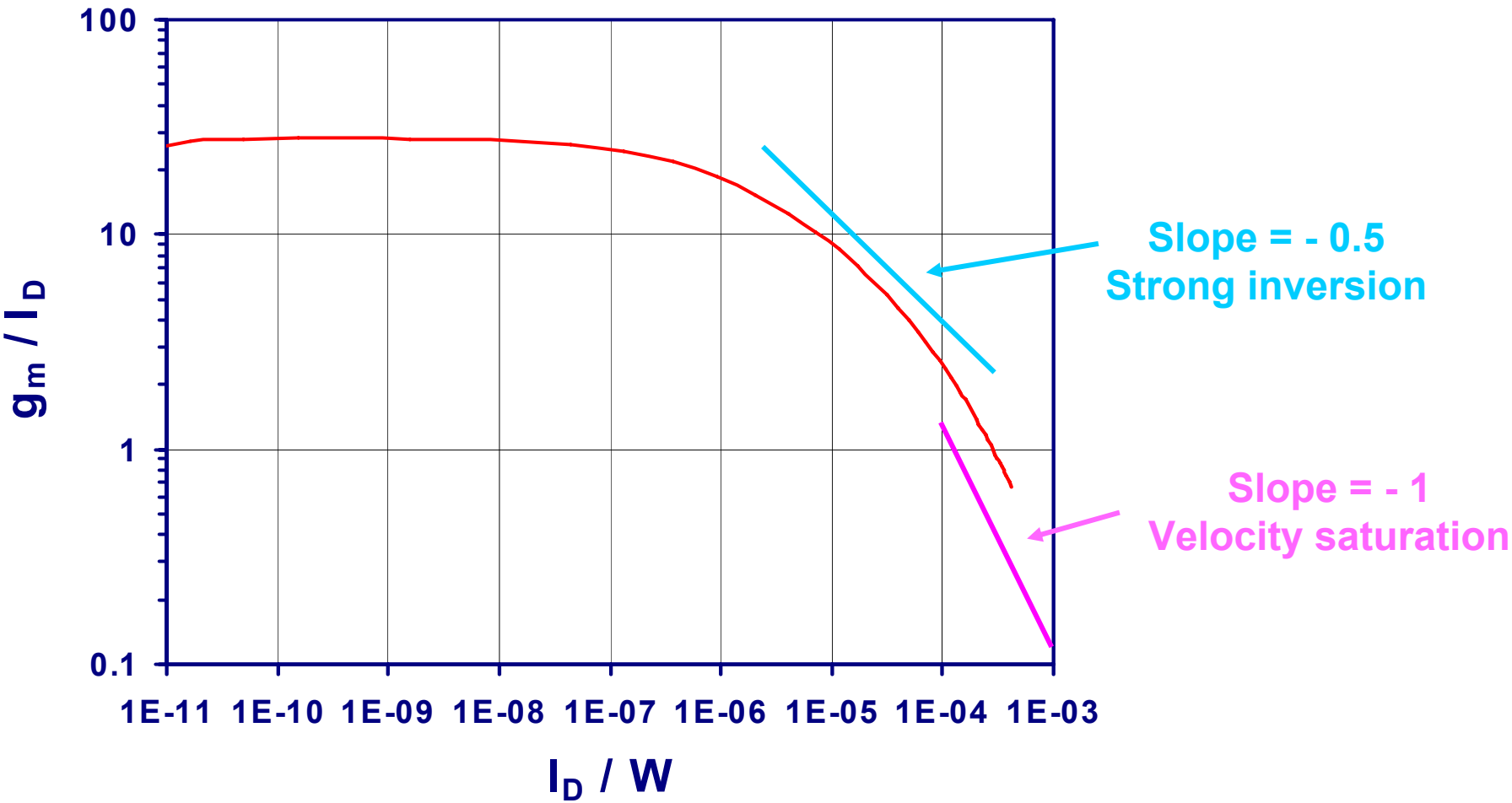
$$g_m = \sqrt{2\frac{\beta}{n}I_{DS}} \longrightarrow \frac{g_m}{I_D} = \sqrt{2\frac{\beta}{n}\frac{1}{I_{DS}}}$$

Velocity Saturation (V.S.)

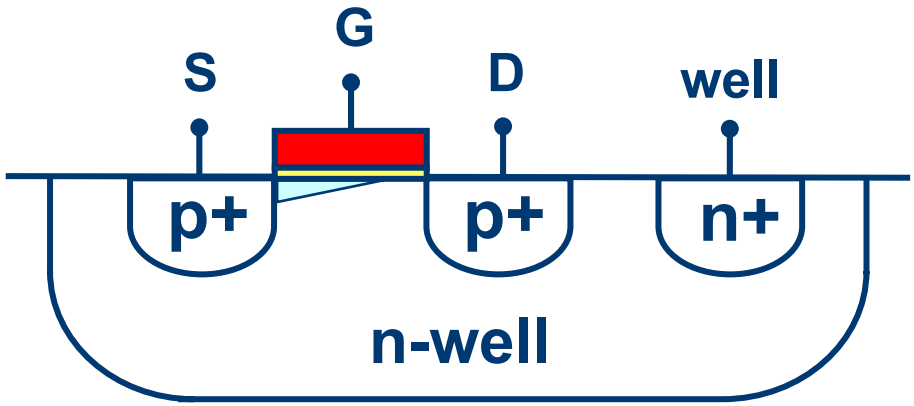
$$g_m = WC_{ox}v_{sat} \longrightarrow \frac{g_m}{I_{DS}} = \frac{WC_{ox}v_{sat}}{I_{DS}}$$

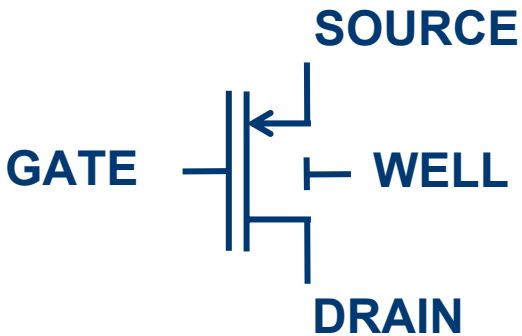
Moderate Inversion (M.I.): No Simple Equations

$Log(g_m / I_D)$ vs $log(I_D / W)$



The poor PMOS transistor

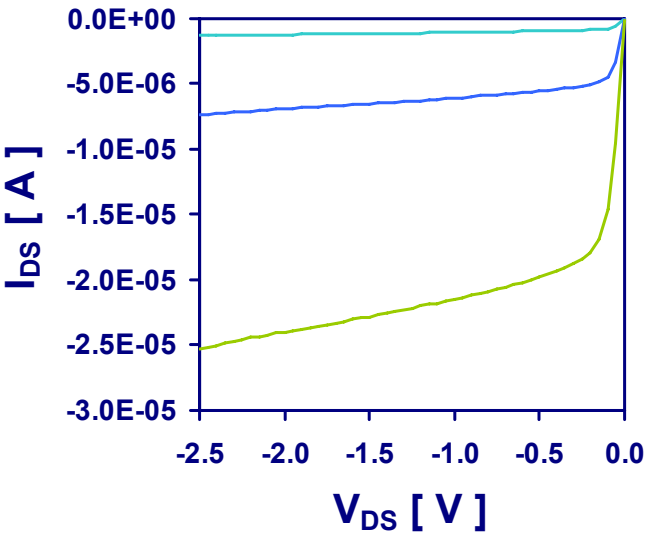




$V_T < 0$ V

$V_{GS} < 0$ V

$I_{DS} < 0$ V

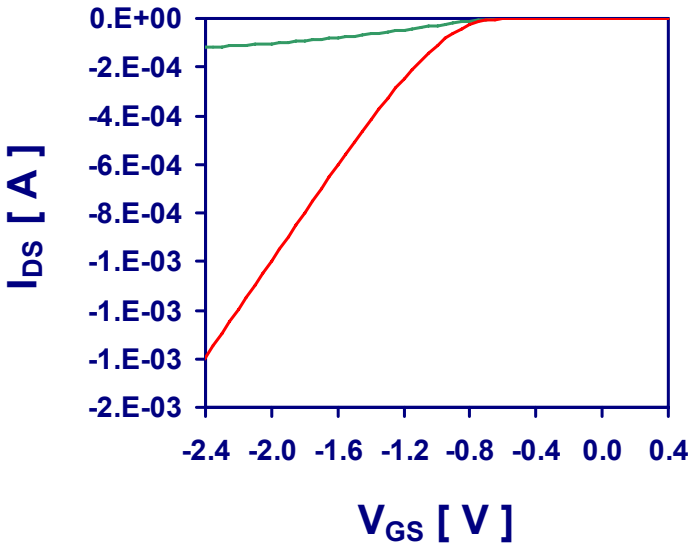


$$I_{DS} = -\frac{\beta}{2n}(V_{GS} - V_T)^2$$

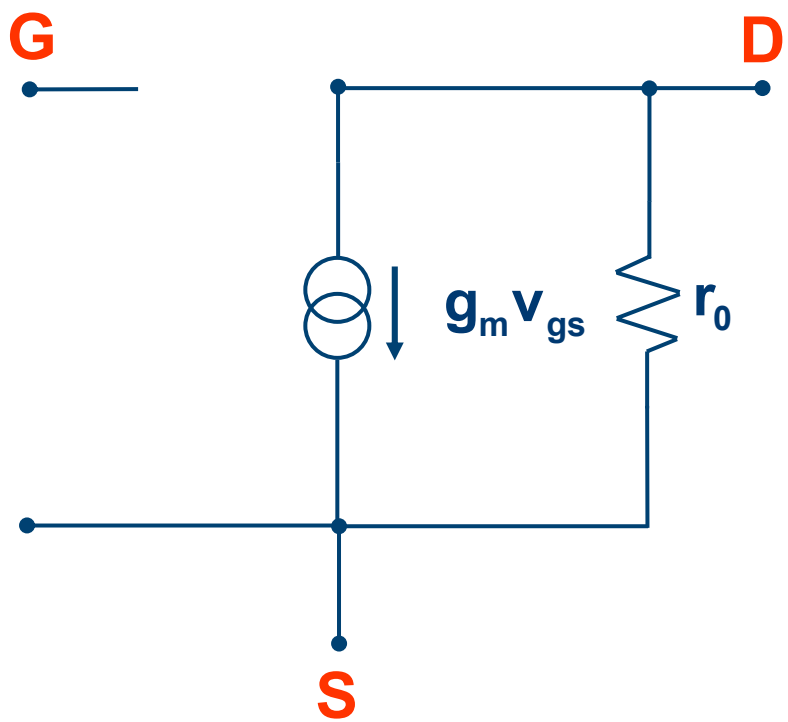
$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} =$$

$$= -\frac{\beta}{n}(V_{GS} - V_T) =$$

$$= \sqrt{-2\frac{\beta}{n} I_{DS}}$$



Small-signal equivalent circuit



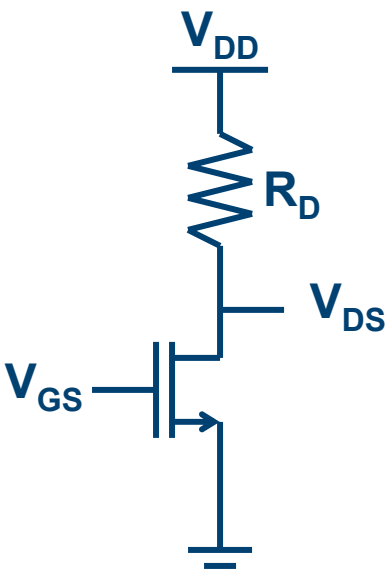
Valid only in saturation and at very low frequencies

No bulk effect

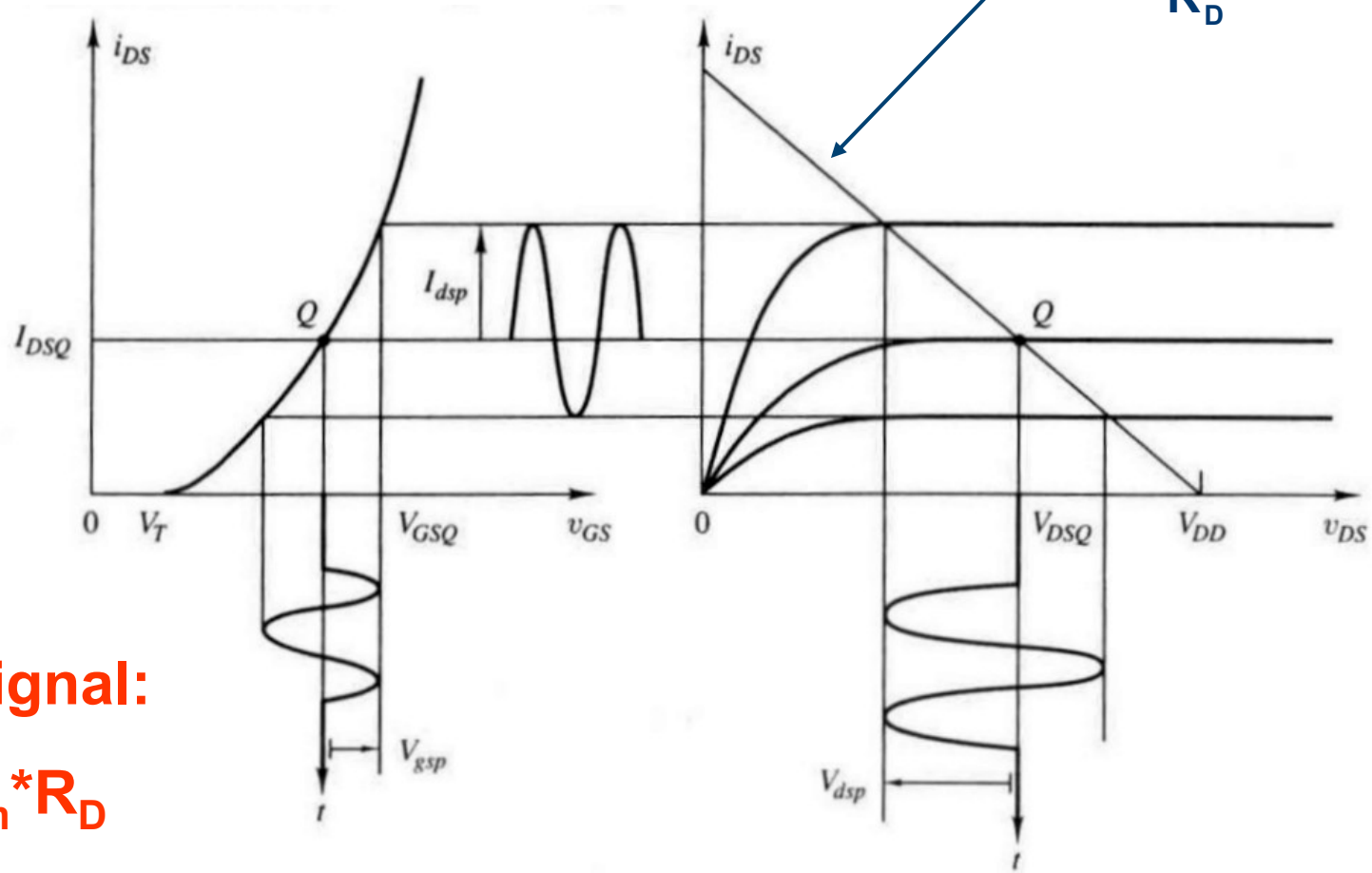
$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$ → **This equation fixes the bias point**

$$i_{ds} = g_m \cdot v_{gs}$$ → **This equation defines the small signal behavior**

A very simple amplifier



$$i_{DS} = \frac{V_{DD} - V_{DS}}{R_D}$$

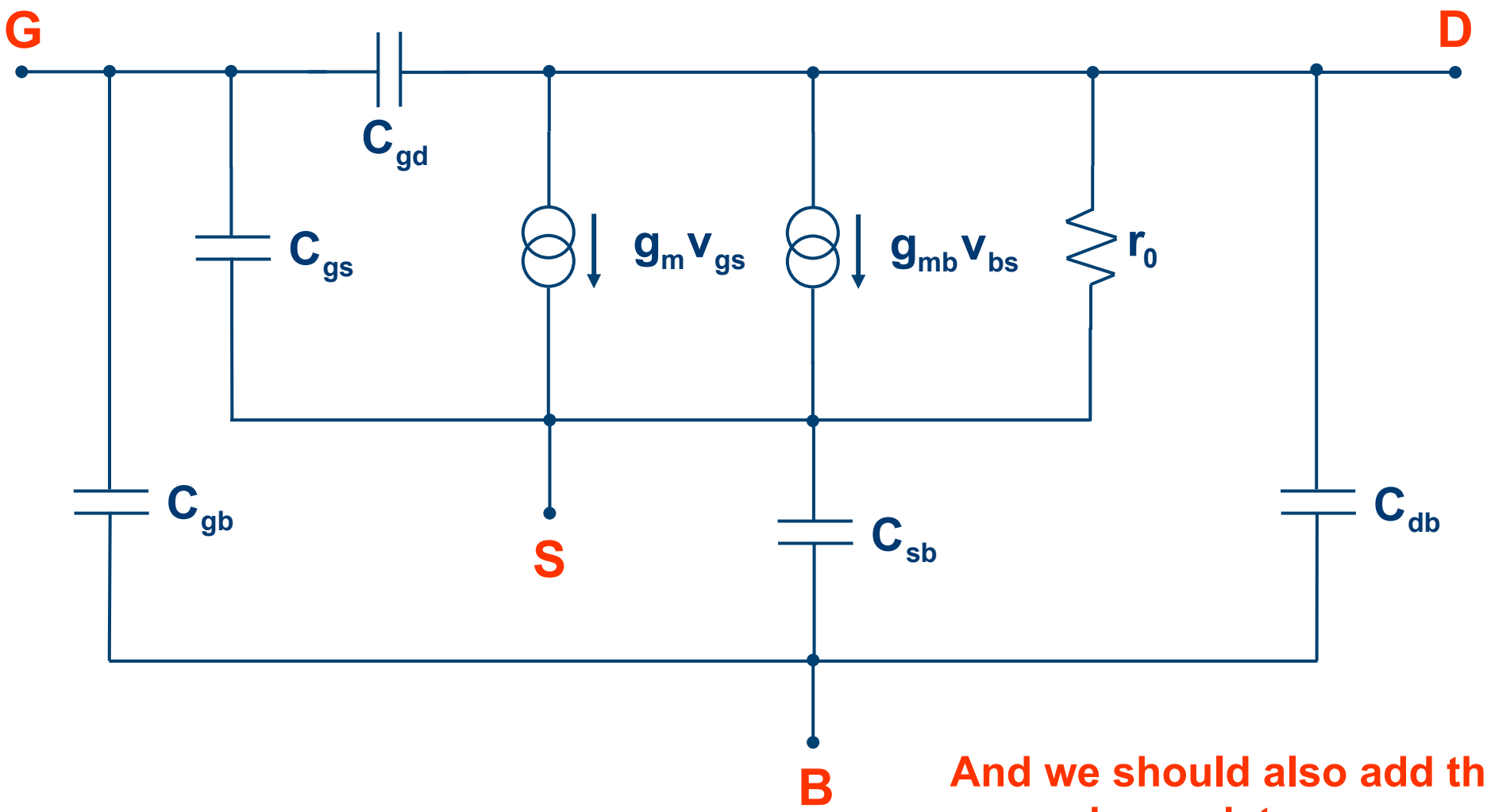


For a small signal:

$$v_{ds} = -v_{gs} * g_m * R_D$$

K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994.

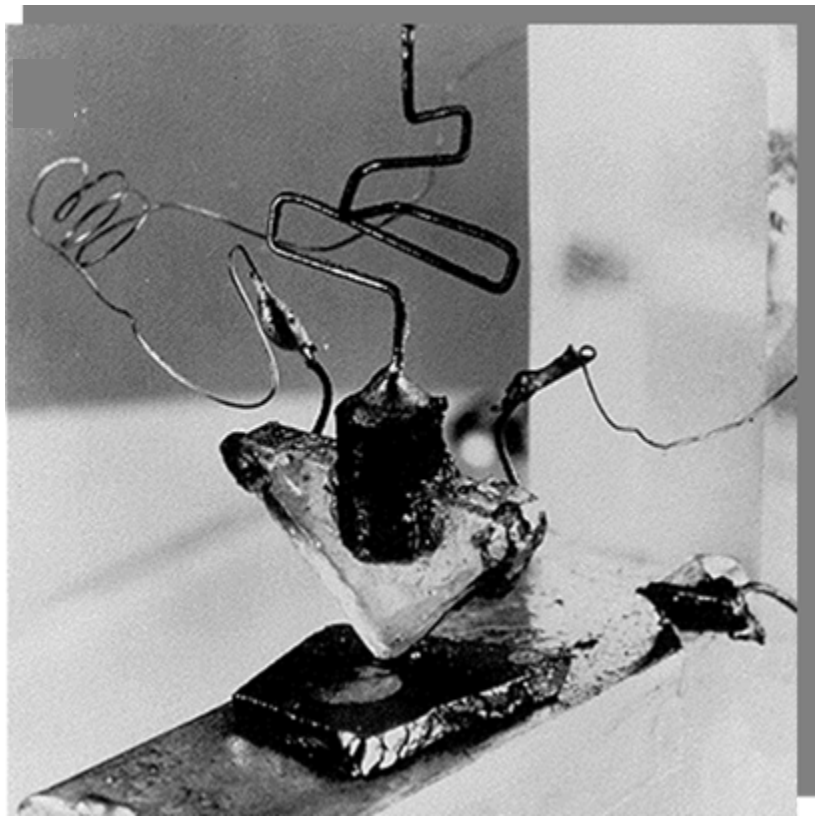
A better equivalent circuit



And we should also add the series resistances…

The First Transistor

First Point Contact Transistor



Bardeen and Brattain, 1947
Bell Laboratories

The Nobel Prize in Physics 1956

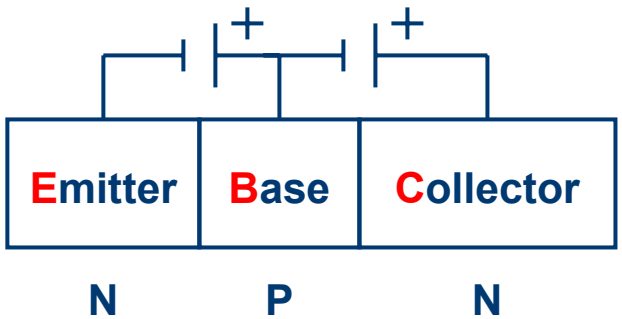
"for their researches on semiconductors and their discovery of the transistor effect"

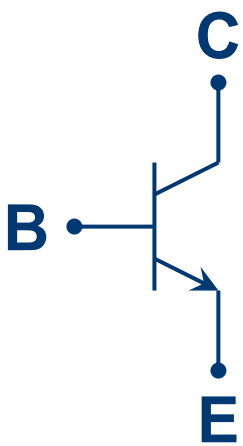
William Bradford Shockley
1/3 of the prize
USA
Semiconductor Laboratory of Beckman Instruments, Inc. Mountain View, CA, USA
b. 1910 (in London, United Kingdom) d. 1989

John Bardeen
1/3 of the prize
USA
University of Illinois Urbana, IL, USA
b. 1908 d. 1991

Walter Houser Brattain
1/3 of the prize
USA
Bell Telephone Laboratories Murray Hill, NJ, USA
b. 1902 d. 1987

The Bipolar Junction Transistor (BJT)



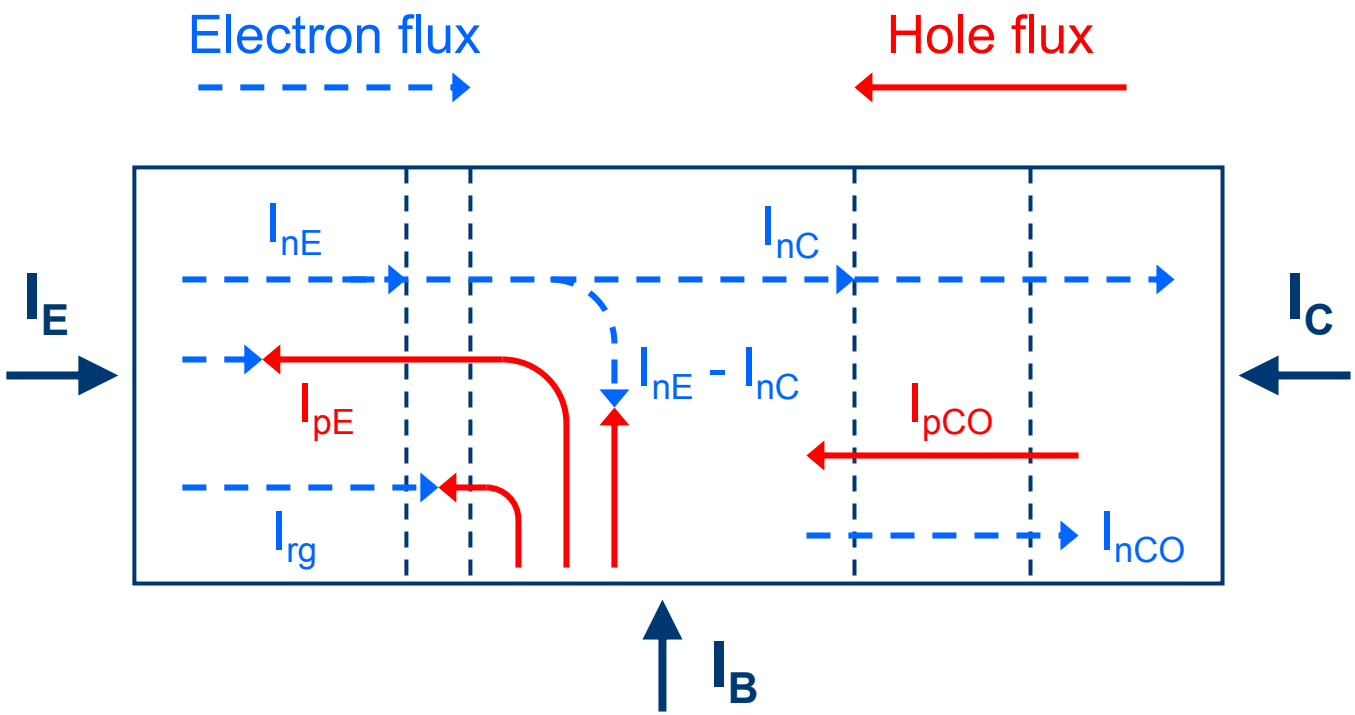


In normal operation condition (also called active region) the Emitter – Base diode is forward biased and the Base – Collector diode is reverse biased. Electrons are injected from the Emitter into the Base. They diffuse then towards the Collector, where they are collected.

At the same time holes are injected from the base into the emitter, but in a much smaller number since the base is normally much less doped than the emitter.

A fraction of the electrons injected into the base will not reach the collector because it will recombine with holes in the base. To make this a negligible effect the electrons lifetime must be long so that their diffusion length is much larger than the base width.

Currents in a bipolar transistor



$-I_E = I_{pE} + I_{nE} + I_{rg}$

$I_B = I_{pE} + I_{rg} + (I_{nE} - I_{nC}) - I_{CO}$

$I_C = I_{nC} + I_{CO}$

$I_E + I_B + I_C = 0$

I_{nE}: electron current injected into the base

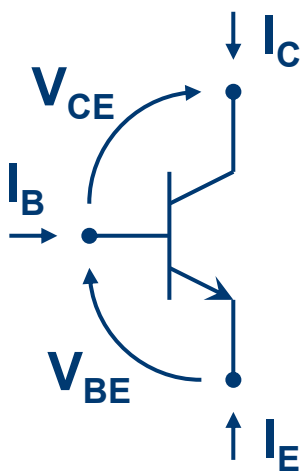
I_{nC}: electron current collected by the collector

I_{rg}: emitter space-charge-layer recombination current

I_{nCO} and I_{pCO}: collector reverse saturation currents ($I_{nCO} + I_{pCO} = I_{CO}$)

E. S. Yang, *Microelectronic Devices*, McGraw-Hill, 1988.

Currents in a bipolar transistor



Common base current gain $\alpha = \frac{I_C - I_{CO}}{-I_E} = \frac{I_{nC}}{I_{nE} + I_{pE} + I_{rg}} = \gamma \cdot \beta_T$

Emitter injection efficiency $\gamma = \frac{I_{nE}}{I_{nE} + I_{pE} + I_{rg}}$

Base transport factor $\beta_T = \frac{I_{nC}}{I_{nE}}$

γ, β_T and therefore α are normally very close to 1 (but not 1)

$$I_C = \frac{\alpha}{1-\alpha} \cdot I_B + \frac{I_{CO}}{1-\alpha} = h_{FE} \cdot I_B + I_{CEO}$$

h_{FE} is the common emitter current gain (sometimes also called β). If α is 0.99 h_{FE} is 99!

Current vs voltage equations

$$I_{nE} = qA_{EB}D_n \frac{n_i^2}{N_{aB}W_B} e^{\frac{V_{BE}}{\phi_t}}$$

$$I_{pE} = qA_{EB}D_p \frac{n_i^2}{N_{dE}W_E} e^{\frac{V_{BE}}{\phi_t}}$$

$$\longrightarrow \quad \gamma = \frac{1}{1 + \frac{D_p N_{aB} W_B}{D_n N_{dE} W_E}}$$

A_{EB}: E-B junction area

D: diffusion constant ($=\mu\phi_t$)

n_i: intrinsic carrier conc.

N: dopant concentration

W: E or B width

ϕ_t: thermal voltage

$$I_{nB} = I_{nE} - I_{nC} = \frac{qA_{EB}W_B n_{po}}{2\tau_n} e^{\frac{V_{BE}}{\phi_t}} \longrightarrow \beta_T = 1 - \frac{W_B^2}{2L_n^2} \qquad L_n = \sqrt{D_n \tau_n}$$

$$I_{rg} \propto e^{\frac{V_{BE}}{2\phi_t}} \longrightarrow I_B \propto e^{\frac{V_{BE}}{n\phi_t}}$$

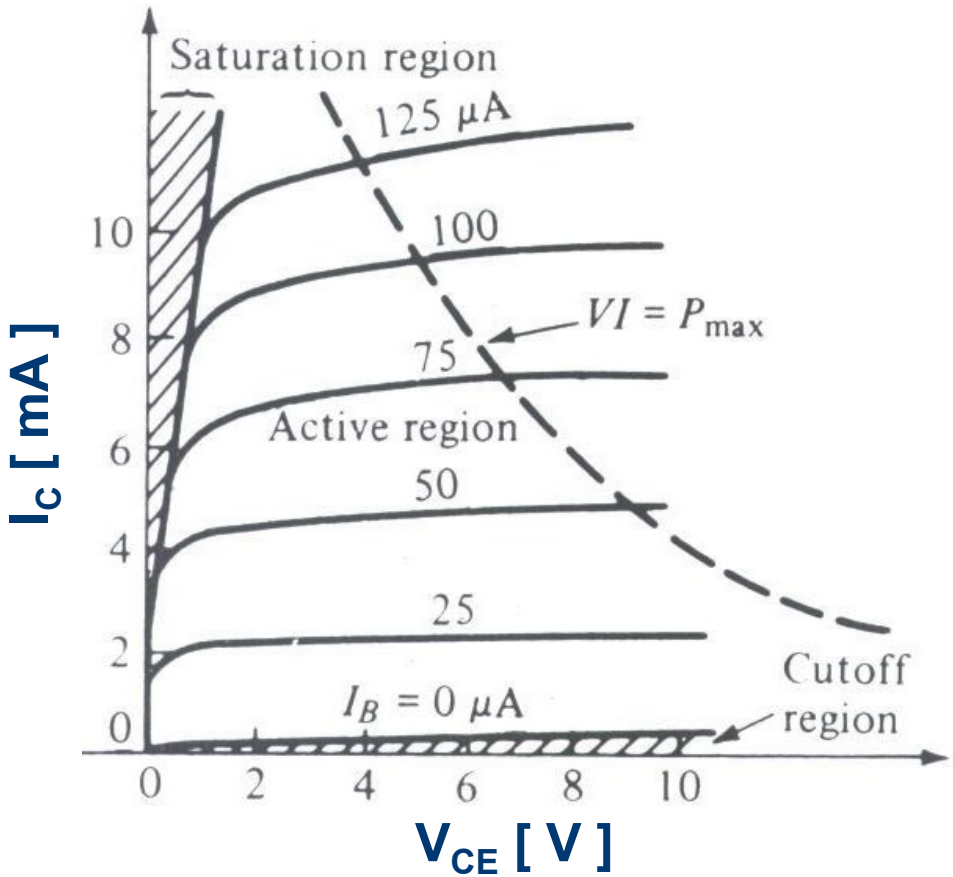
n_{po}: equilibrium electron density in the base ($=n_i^2/N_{aB}$)

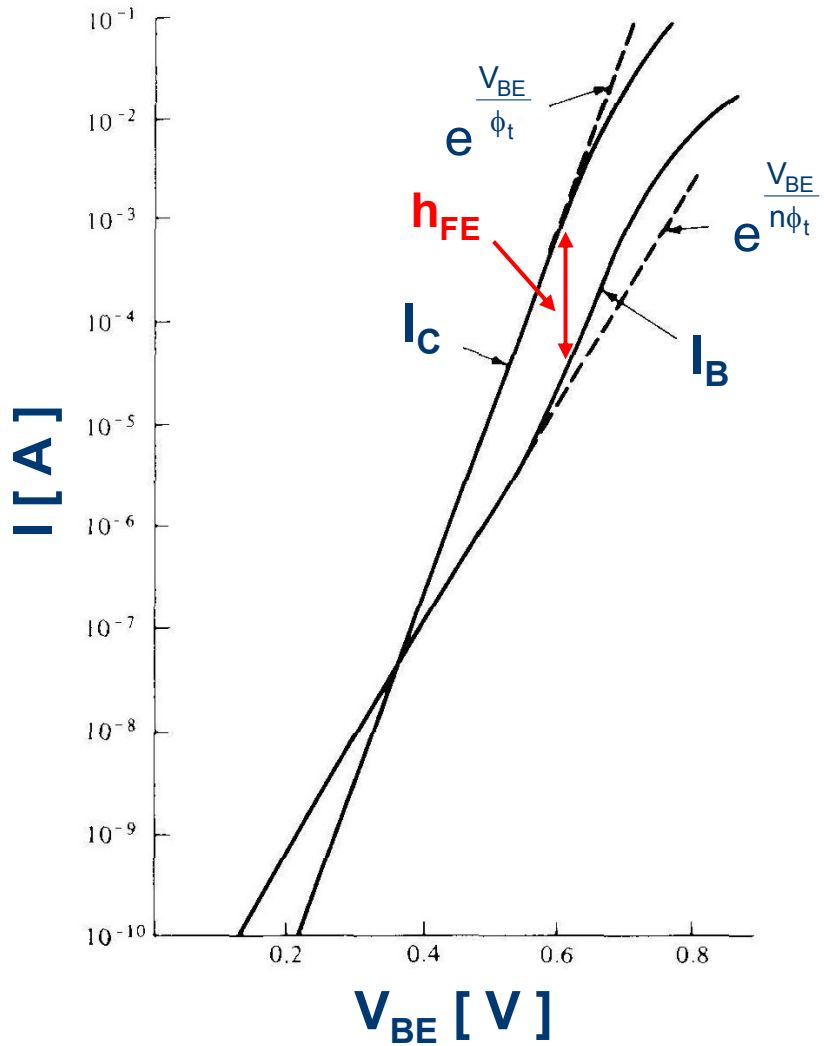
τ_n: electron lifetime in the base

L_n: diffusion length

n: number between 1 and 2

Bipolar transistor characteristics





E. S. Yang, *Microelectronic Devices*, McGraw-Hill, 1988.

A “few” important equations

Collector current

$$I_C \approx I_{nE} = I_S e^{\frac{V_{BE}}{\phi_t}} \qquad I_S = qA_{EB}D_n \frac{n_i^2}{N_{aB}W_B}$$

Transconductance

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{\phi_t} \qquad \frac{g_m}{I_C} = \frac{1}{\phi_t} = 40 \text{ @ } 300\,\text{K}$$

Input resistance

$$r_\pi = \frac{h_{FE}}{g_m}$$

Output resistance

$$r_0 = \frac{V_E}{I_C} \qquad V_E = \frac{qA_{BC}N_{aB}W_B}{C_{jC}}$$

Max frequency

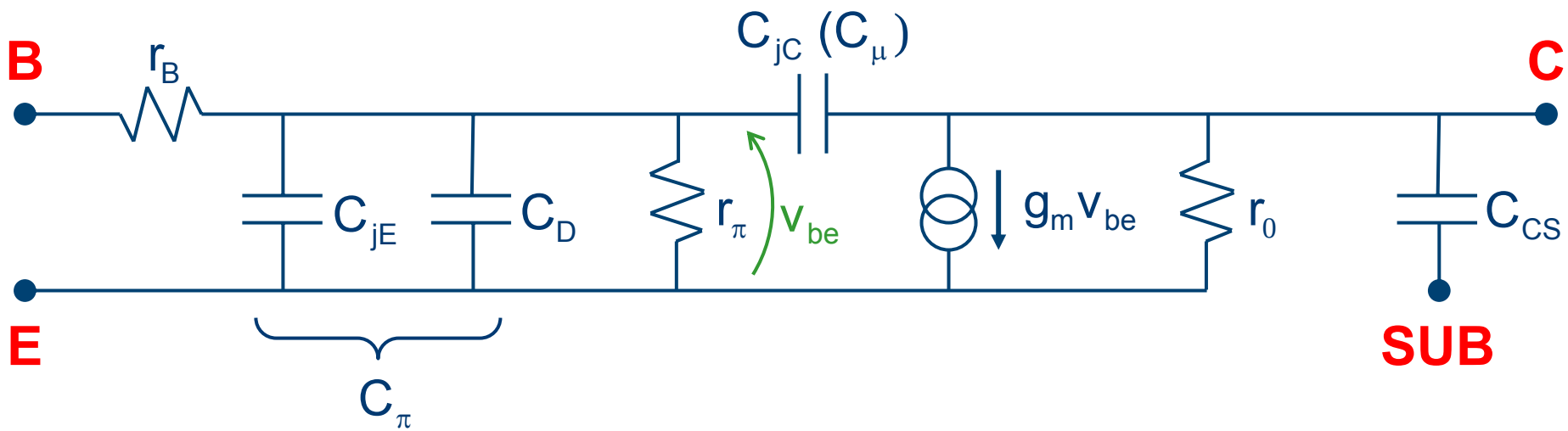
$$\omega_T = \frac{2D_n}{W_B^2}$$

Diffusion capacitance

$$C_D = \frac{\partial Q_B}{\partial V_{BE}} = g_m \frac{W_B^2}{2D_n} = \frac{g_m}{\omega_T}$$

Small-signal equivalent circuit

The hybrid-π model



r_B is the base resistance, which is layout dependent

K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994.

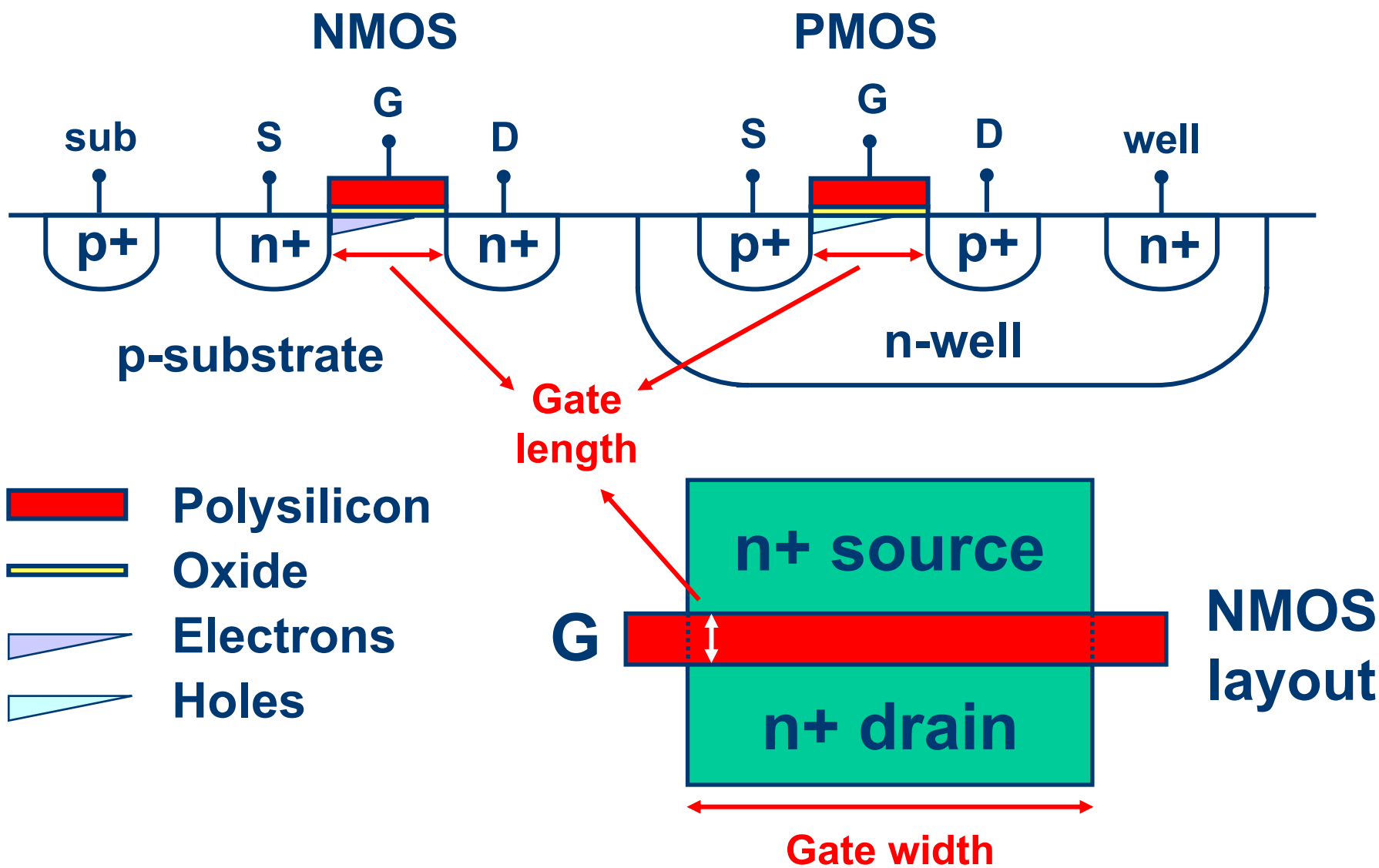
Comparison MOS - Bipolar

	MOS Transistor	Bipolar Transistor
I_{IN}	0	I_C / h_{FE}
R_{IN}	∞	$r_\pi + r_B$
$V_{DSsat} / V_{CEactive}$	$(V_{GS}-V_T) / n$	few ϕ_t
g_m / I	**w.i.** - $1 / n\phi_t$	$1 / \phi_t$
	s.i. - $2 / (V_{GS}-V_T) = \sqrt{2\beta/(nI_{DS})}$	
	v.s. - $WC_{OX}v_{sat} / I_{DS} = 1 / (V_{GS}-V_T)$	
Design variables	W / L, $V_{GS}-V_T$	ϕ_t
I range	~ 2 decades	> 5 decades
Max f_T @ low I	g_m / C_{gs}	g_m / C_D
Max f_T @ high I	v_{sat} / L_{eff}	v_{sat} / W_B
Thermal Noise	$4kT\ (0.7/g_m + R_G)$	$4kT\ (0.5/g_m + r_B)$
1/f noise	Higher for MOS than for bipolar transistors	

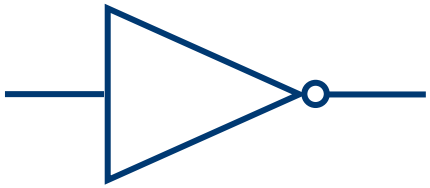
Outline

- Operation and characteristics of MOS and Bipolar transistors
- Sub-micron CMOS and BiCMOS technologies
  - CMOS technology
  - Integrated Bipolar Transistors
  - Technology price comparison
- Feature size scaling
- Radiation effects and reliability
- Mixed-signal circuits

Complementary MOS technology



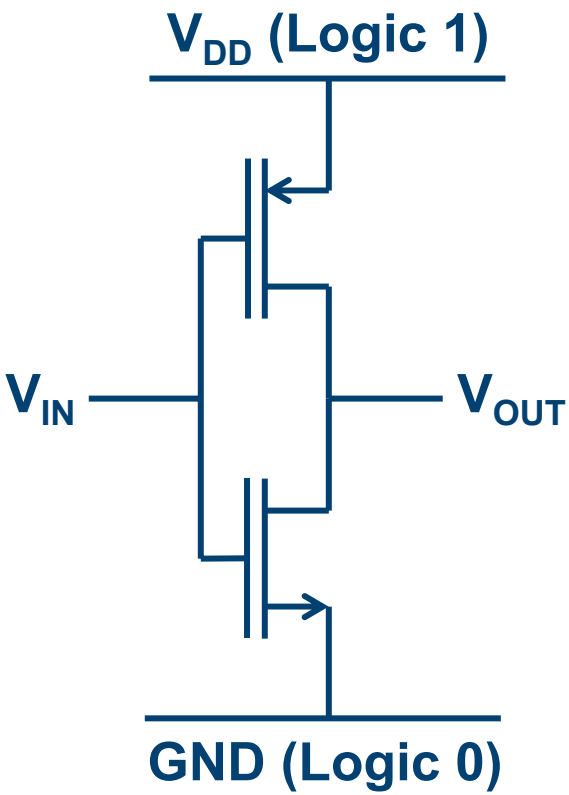
Why is CMOS logic so attractive?

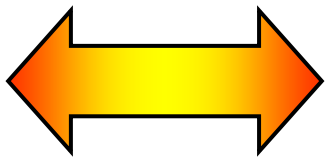


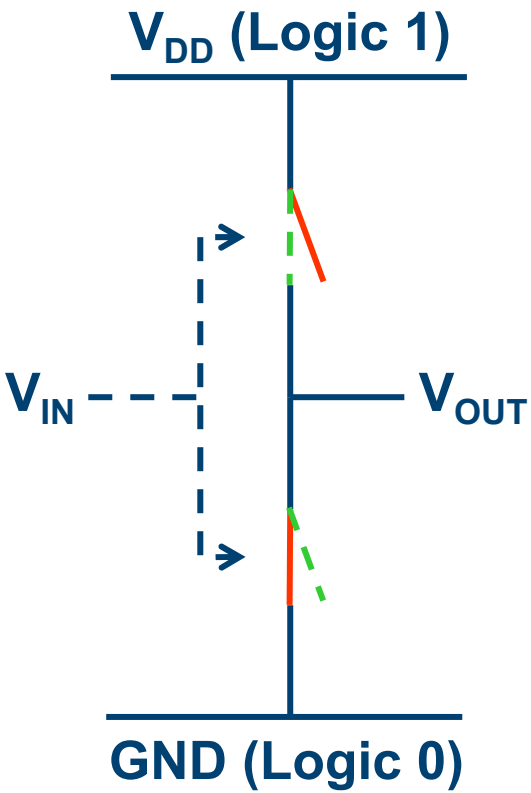
THE INVERTER

Truth table

IN	OUT
0	1
1	0

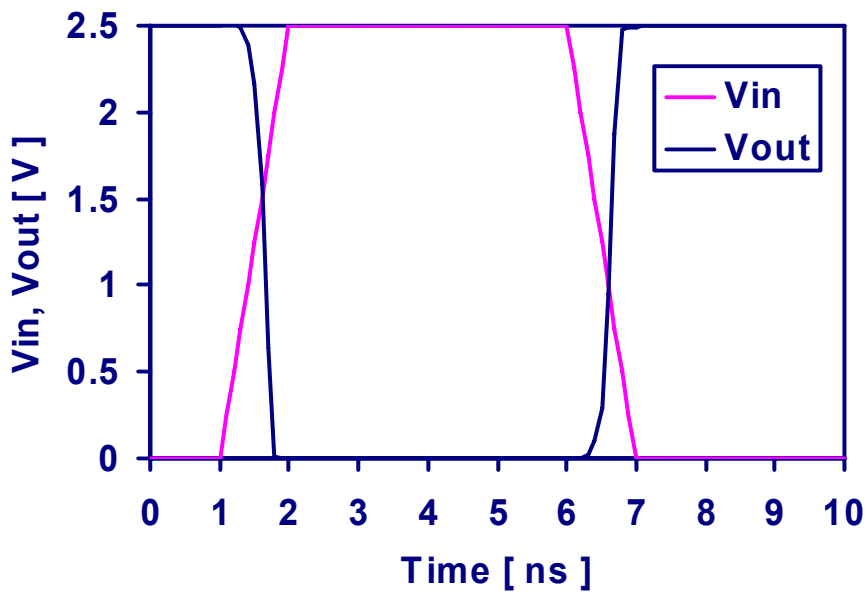


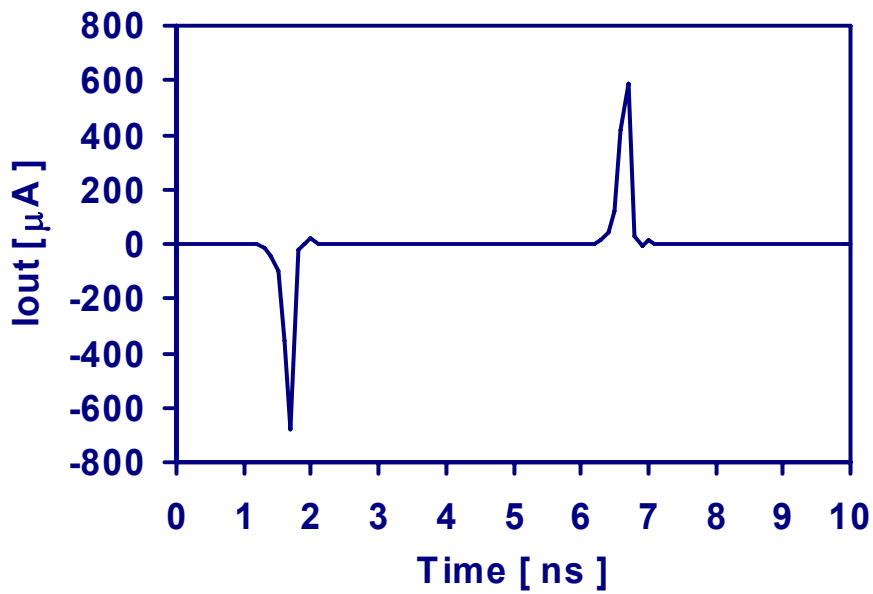




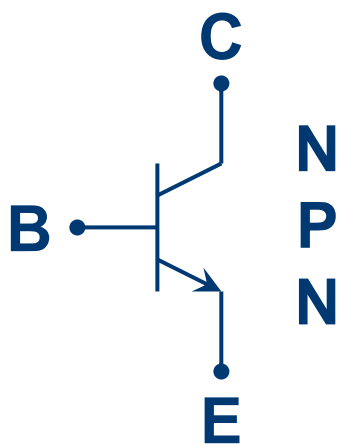
Dynamic current in an inverter

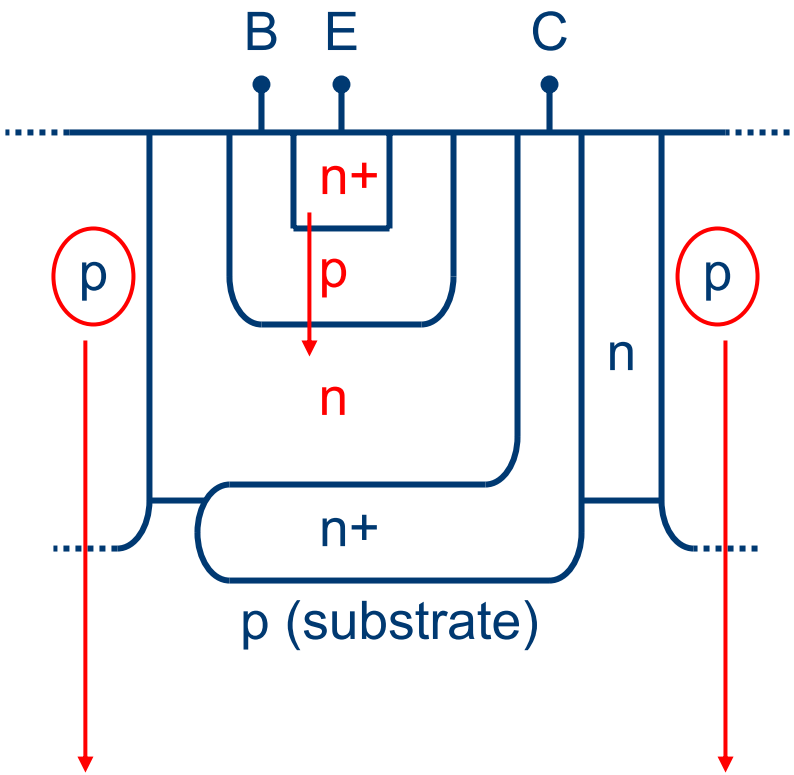
Simulation of a chain of two inverters in a 0.25 μm CMOS technology





Integrated Bipolar Transistors

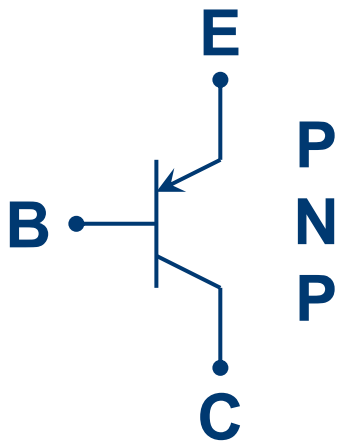


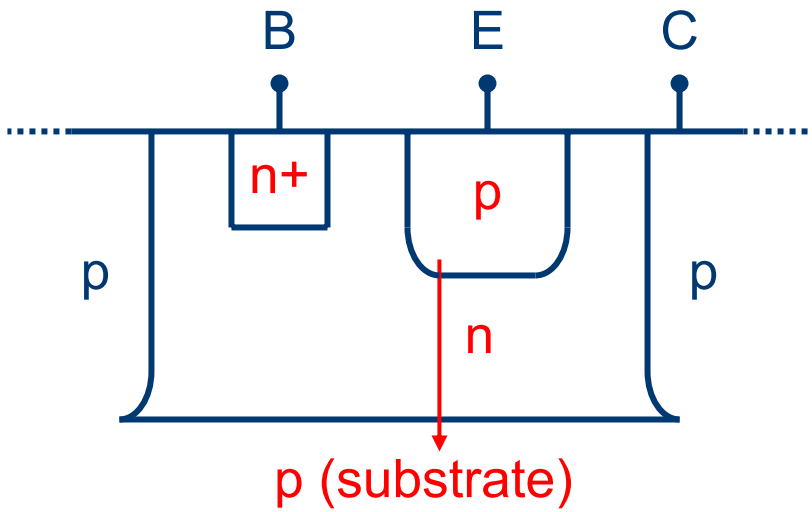


Vertical NPN

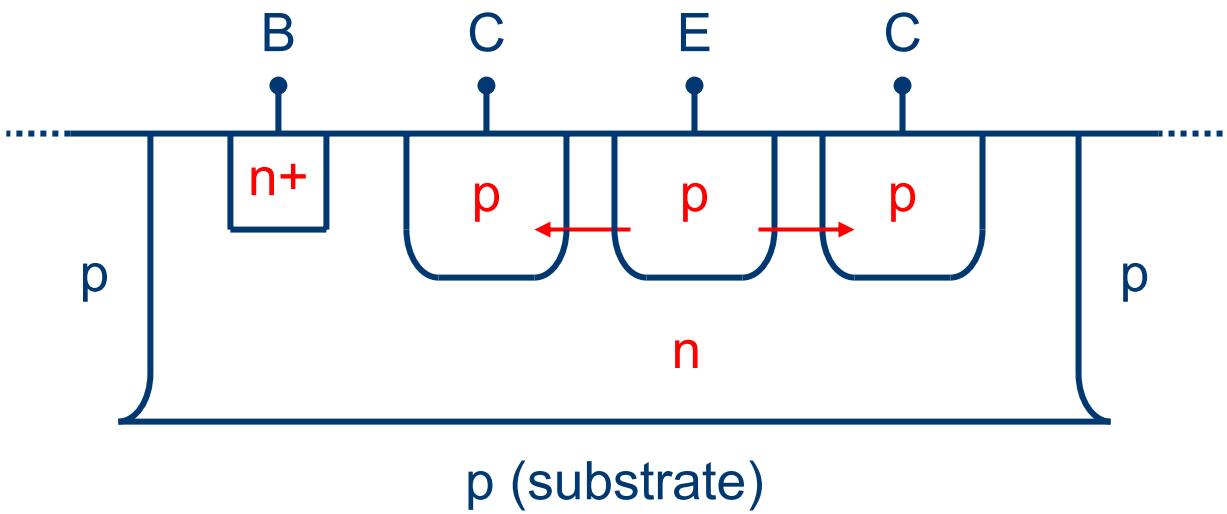
p-type pockets to isolate devices one from another

Integrated Bipolar Transistors





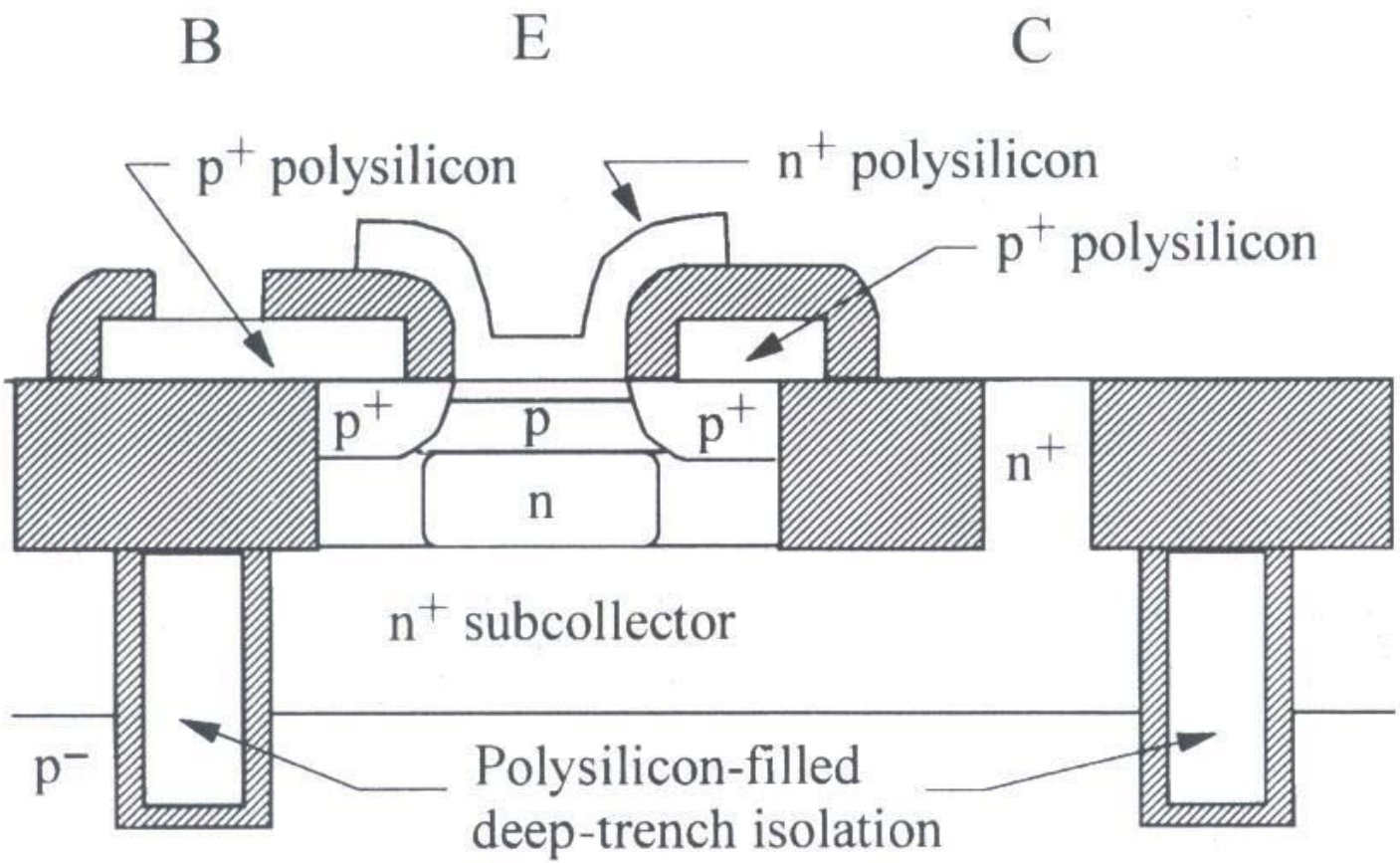
Vertical PNP (Common collector!)



Lateral PNP

A modern npn BJT

Deep-trench-isolated, double-polysilicon, self-aligned bipolar technology



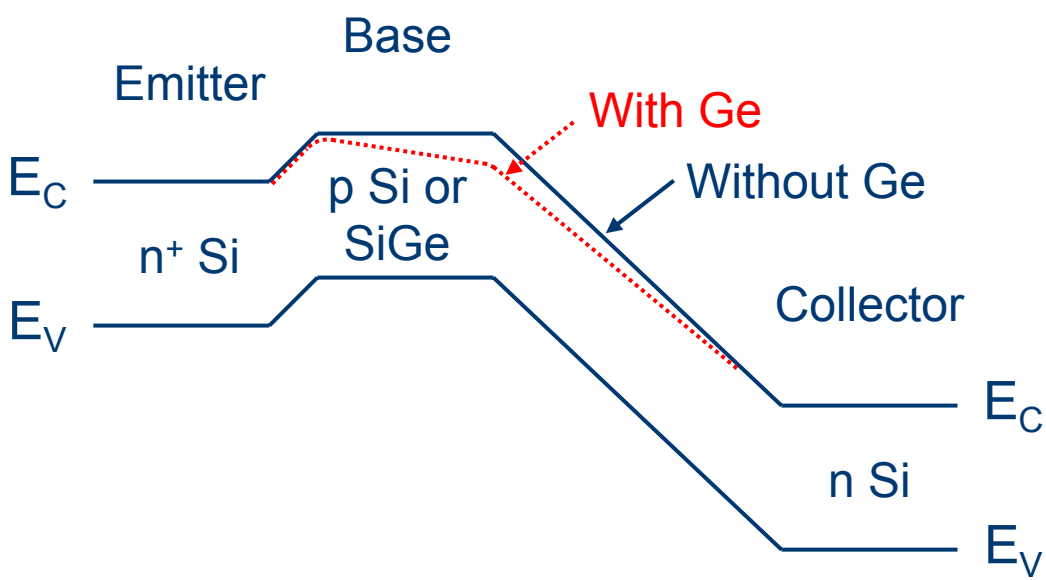
Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.

Main innovations in modern BJTs

- **Deep trench isolations: reduce significantly the device horizontal dimensions. p-type diffusions were normally used in the past, but they are as wide as they are deep**
- **Polysilicon emitter: compared to a diffused emitter, it gives smaller emitter junction depth and has a lower thermal cycle**
- **Self-aligned polysilicon base contact: reduces dimensions and allows thin-base transistors to be made more easily**
- **SiGe graded-base-bandgap transistors (also referred to as Heterojunction Bipolar Transistors – HBTs): Germanium is incorporated into the base region of a standard Si bipolar transistor. This is normally done with the ultrahigh-vacuum chemical vapor deposition epitaxial growth technique. The many advantages are discussed in the next slides**

SiGe bipolar transistors

The bandgap of Germanium (0.66 eV) is smaller than that of Silicon (1.22 eV). Incorporating Ge into the base region of a Si bipolar transistor modifies the bandgap in the base region. Ge concentration is normally higher closer to the collector, so that an electric field is created in the base which helps the electrons drifting from Emitter to Collector. This has an important impact on the collector current and does not change the base current.



A 100 meV change of the bandgap across a base width of 100 nm gives a 10 kV/cm field

SiGe bipolar transistors

The effects of base-bandgap grading obtained by the inclusion of Ge in the base are all beneficial:

- **The collector current increases while the base current does not change → the current gain increases (x4)**
- **The Early voltage increases (x12)**
- **The base transit time decreases (x2.5), and therefore the speed increases**

(The factors in parenthesis refer to a total base bandgap narrowing of 100 meV)

Why is CMOS so widespread?

- The IC market is driven by digital circuits (memories, microprocessors, …)
- Bipolar logic and NMOS - only logic had a too high power consumption per gate
- Progress in the manufacturing technology made CMOS technologies a reality
- Modern CMOS technologies offer excellent performance (especially for digital): high speed, low power consumption, VLSI, relatively low cost, high yield

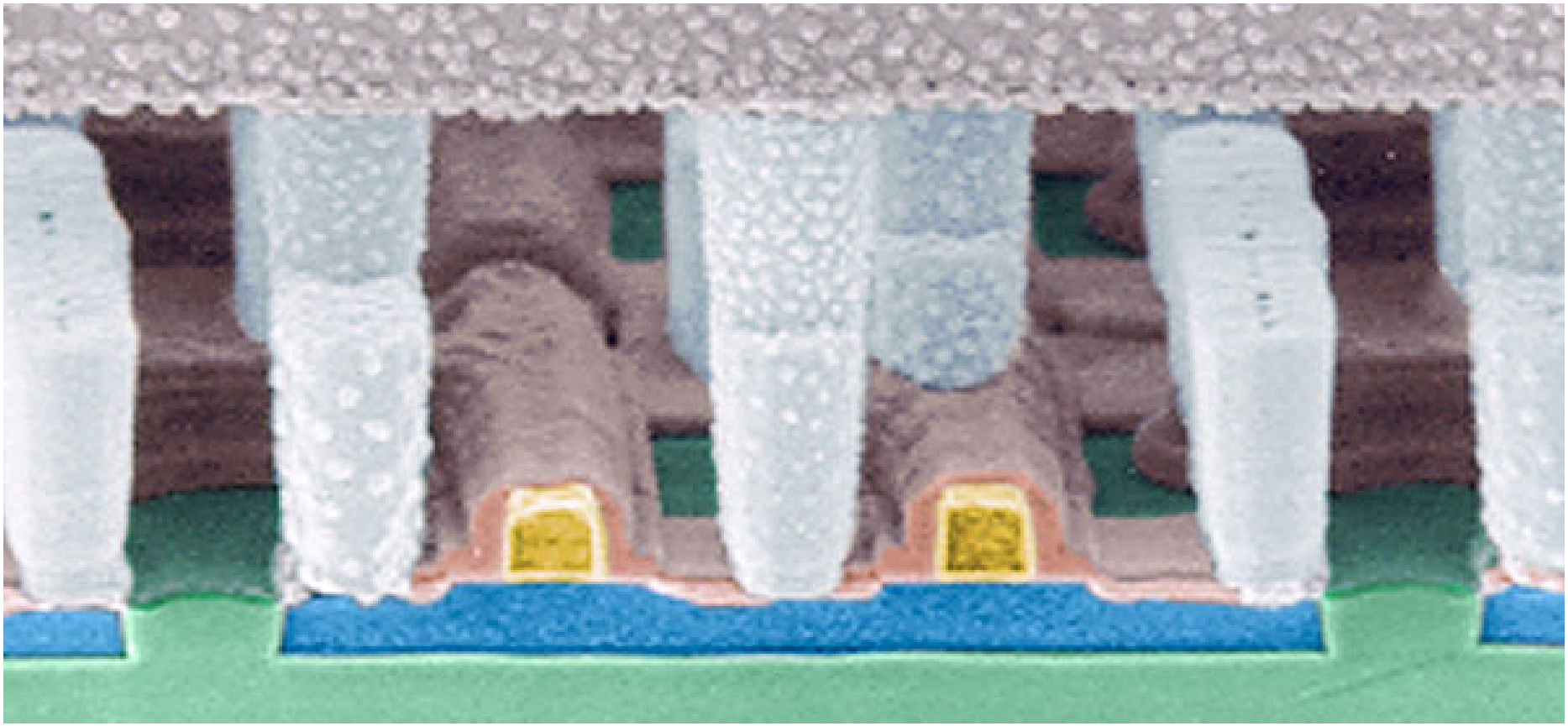
CMOS technologies occupies the biggest portion of the IC market

BiCMOS technologies offer, in addition, high performance npn bipolar transistors, but are more expensive

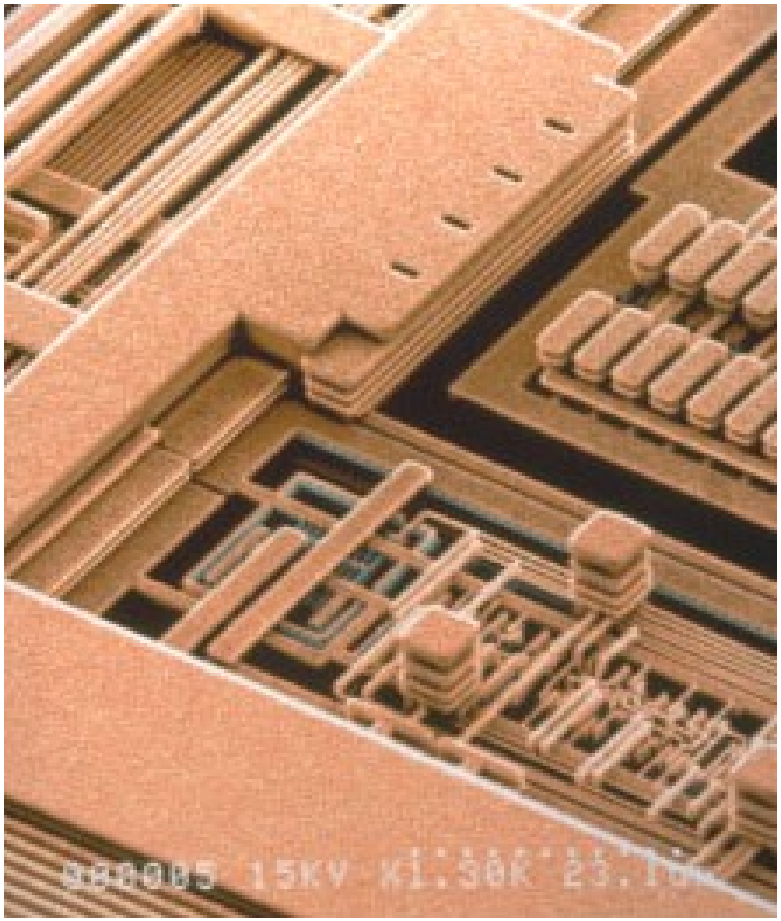
How much does all this cost?

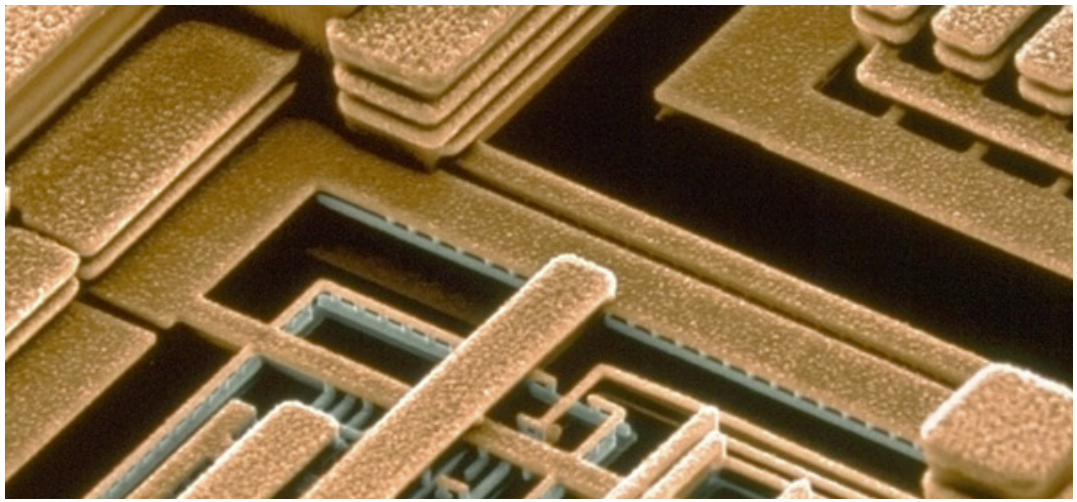
Vendor	Technology	Number of Metal Levels	Price for 10 mm² [k$]	Price for 25 mm² [k$]	Price for 50 mm² [k$]
MOSIS					
IBM	0.13 μm CMOS MixMode	8	57.5	135.1	250.1
IBM	0.13 μm SiGe BiCMOS	7	165	412.5	825
IBM	0.18 μm CMOS MixMode	6	36	70	126.8
IBM	0.18 μm SiGe BiCMOS	7	56	89	144
IBM	0.25 μm CMOS	5	21	47.2	77.2
EUROPRACTICE					
UMC	0.13 μm CMOS	8	Min price given for 25 mm²	55.4	110.8
UMC	0.18 μm CMOS	6		30.4	60.8
UMC	0.25 μm CMOS	5		16.2	32.4
IHP	0.25 μm SiGe BiCMOS	4	30 - 91	75 – 227.5	150 - 455

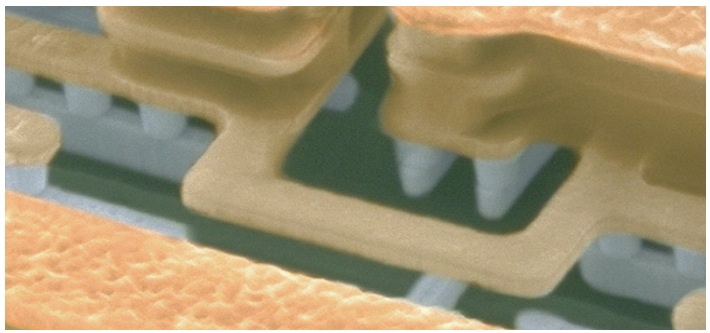
SOI CMOS from IBM



Metallization examples (IBM)





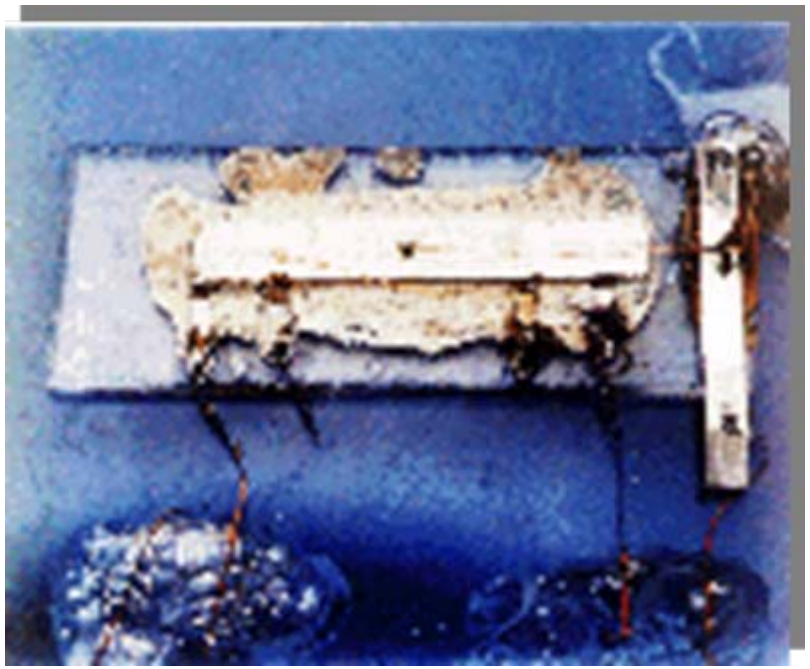


Outline

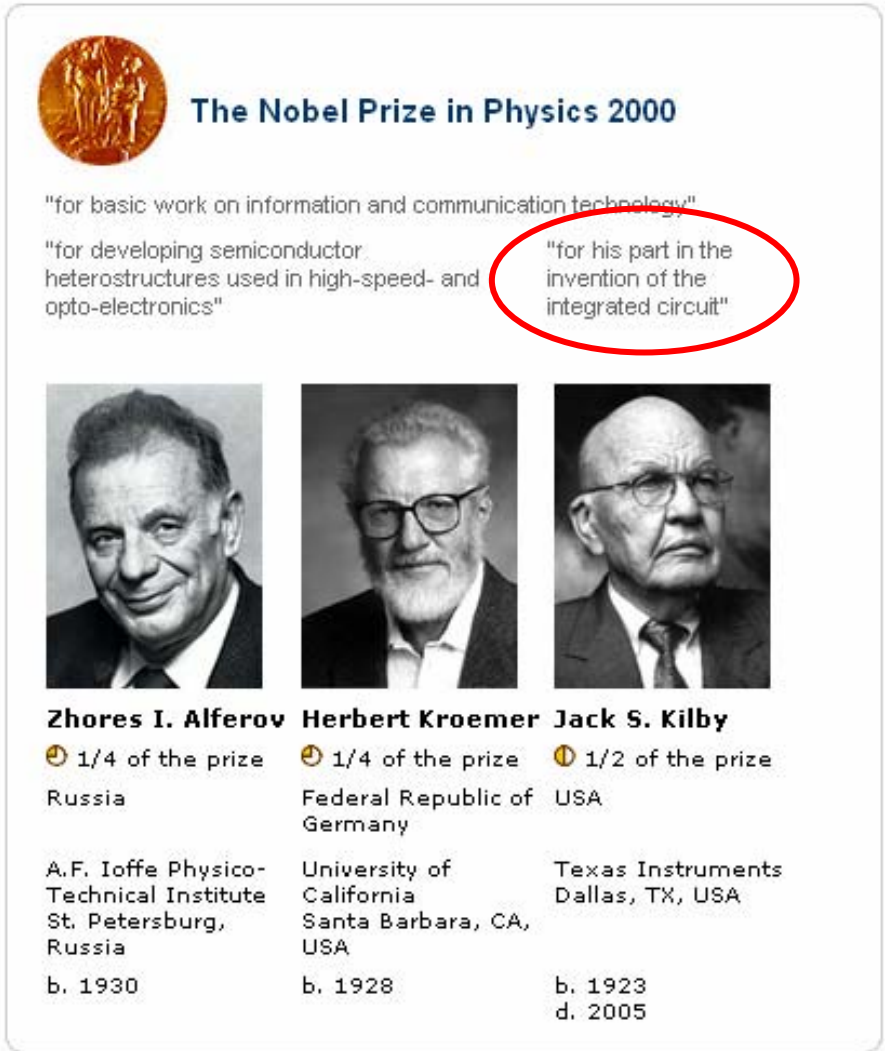
- Operation and characteristics of MOS and Bipolar transistors
- Sub-micron CMOS and BiCMOS technologies
- Feature size scaling
  - A bit of history
  - A look into the future
  - CMOS scaling: how does it work?
  - Scaling of Bipolar Transistors
  - Scaling impact on CMOS analog circuits
- Radiation effects and reliability
- Mixed-signal circuits

The first IC

First integrated circuit



Jack S. Kilby, 1958
Texas Instruments



The Nobel Prize in Physics 2000

"for basic work on information and communication technology"

"for developing semiconductor heterostructures used in high-speed- and opto-electronics"

"for his part in the invention of the integrated circuit"

Zhores I. Alferov	Herbert Kroemer	Jack S. Kilby
1/4 of the prize	1/4 of the prize	1/2 of the prize
Russia	Federal Republic of Germany	USA
A.F. Ioffe Physico-Technical Institute St. Petersburg, Russia	University of California Santa Barbara, CA, USA	Texas Instruments Dallas, TX, USA
b. 1930	b. 1928	b. 1923 d. 2005

Moore's law

1965: Number of Integrated Circuit components will double every year

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

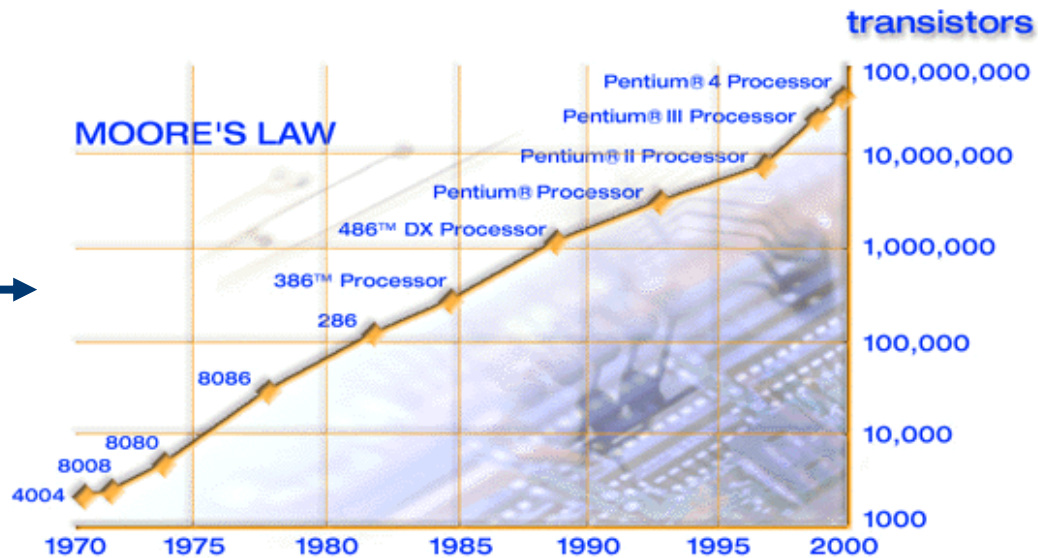
1975: Number of Integrated Circuit components will double every 18 months

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

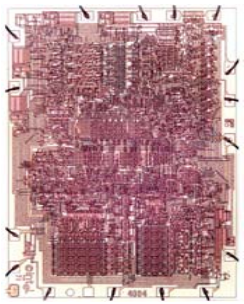
An example:
Intel's Microprocessors



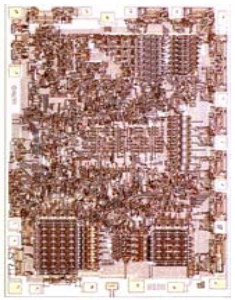
http://www.intel.com/

The intel Microprocessors

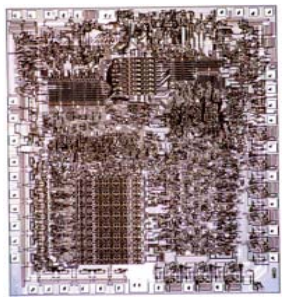
4004
11 / 1971
2300
10 μm
108 KHz



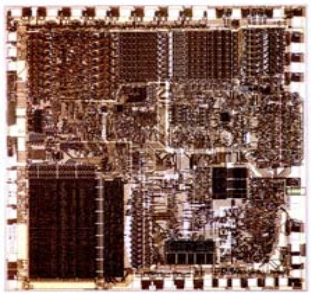
8008
04 / 1972
3500
10 μm
200 KHz



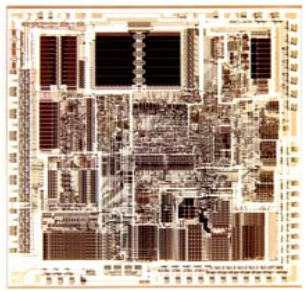
8080
04 / 1974
4500
6 μm
2 MHz



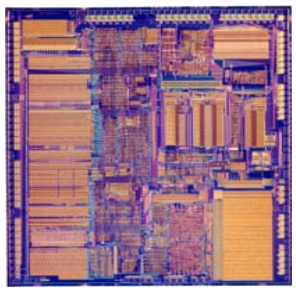
8088
06 / 1979
29000
3 μm
8 MHz



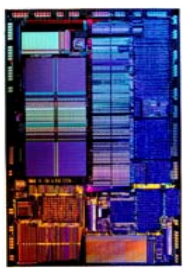
80286
02 / 1982
134000
1.5 μm
12 MHz



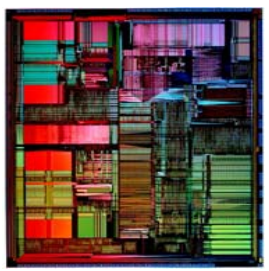
Intel386™
10 / 1985
275000
1 μm
16 MHz



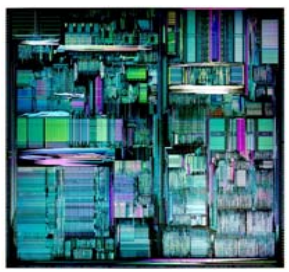
Intel486™ DX
04 / 1989
1.2 M
1 μm
25 MHz



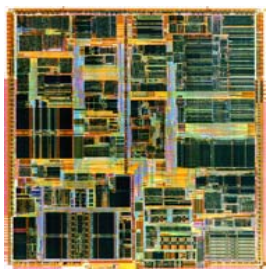
Pentium®
03 / 1993
3.1 M
0.8 μm
66 MHz



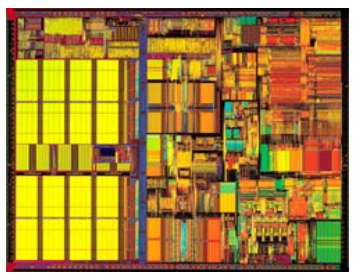
Pentium® Pro
11 / 1995
5.5 M
0.6 μm
150 MHz



Pentium® II
05 / 1997
7.5 M
0.35 μm
233 MHz



Pentium® III
02 / 1999
9.5 M
0.25 μm
500 MHz



Pentium® 4
11 / 2000
42 M
0.18 μm
1.5 GHz

http://www.intel.com/

The Roadmap History

- **The National Technology Roadmap for Semiconductors (NTRS):**

  Sponsored by the Semiconductor Industry Association (SIA)

  Edited in 1992, 1994 and 1997

- **The International Technology Roadmap for Semiconductors (ITRS):**

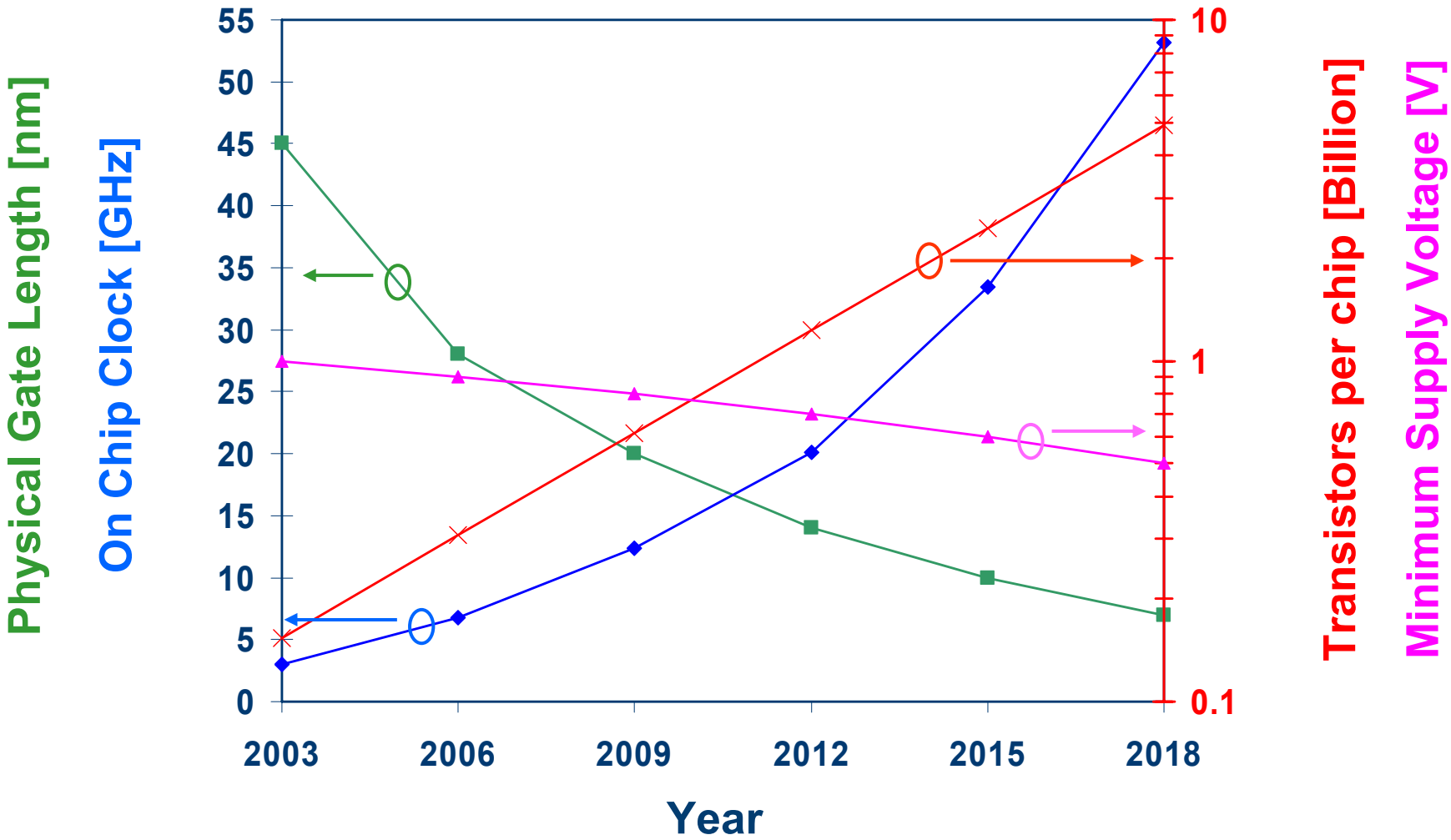
  Sponsored by:

  - **Semiconductor Industry Association**
  - **European Semiconductor Industry Association**
  - **Korea Semiconductor Industry Association**
  - **Japan Electronics and Information Technology Industries Association**
  - **Taiwan Semiconductor Industry Association**

  Edited in 1998 (Update), 1999, 2000 (Update), 2001, 2002 (Update), 2003, 2004 (Update), 2005

These documents always contained a 15-year outlook of the semiconductor industry major trends

Future perspectives

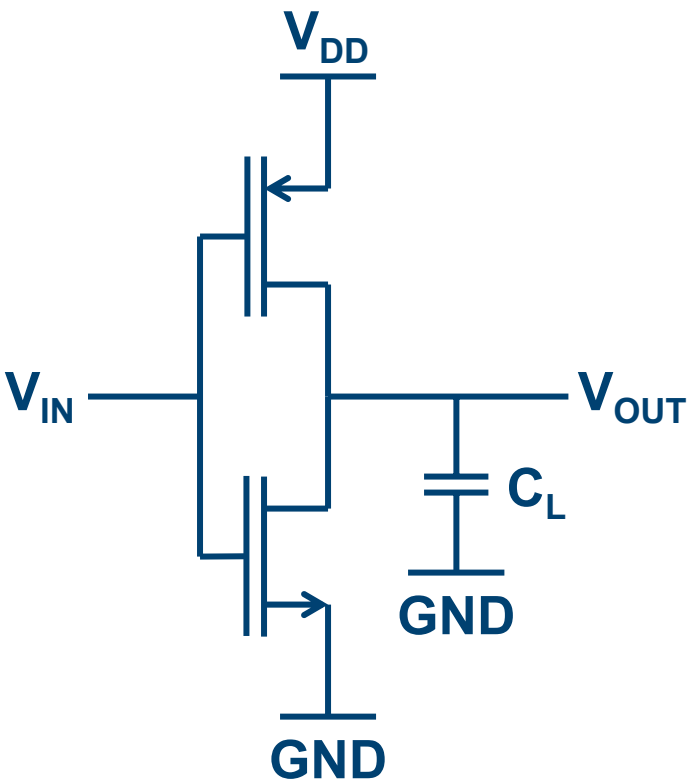


Data taken from the International Technology Roadmap for Semiconductors (2004 Update)

Why CMOS scaling?

Scaling improves density, speed and power consumption of CMOS digital circuits

Example: CMOS inverter



$$P_{static} = I_{leakage} \cdot V_{DD}$$

$$P_{dynamic} = C_L \cdot V_{DD}^2 \cdot f$$

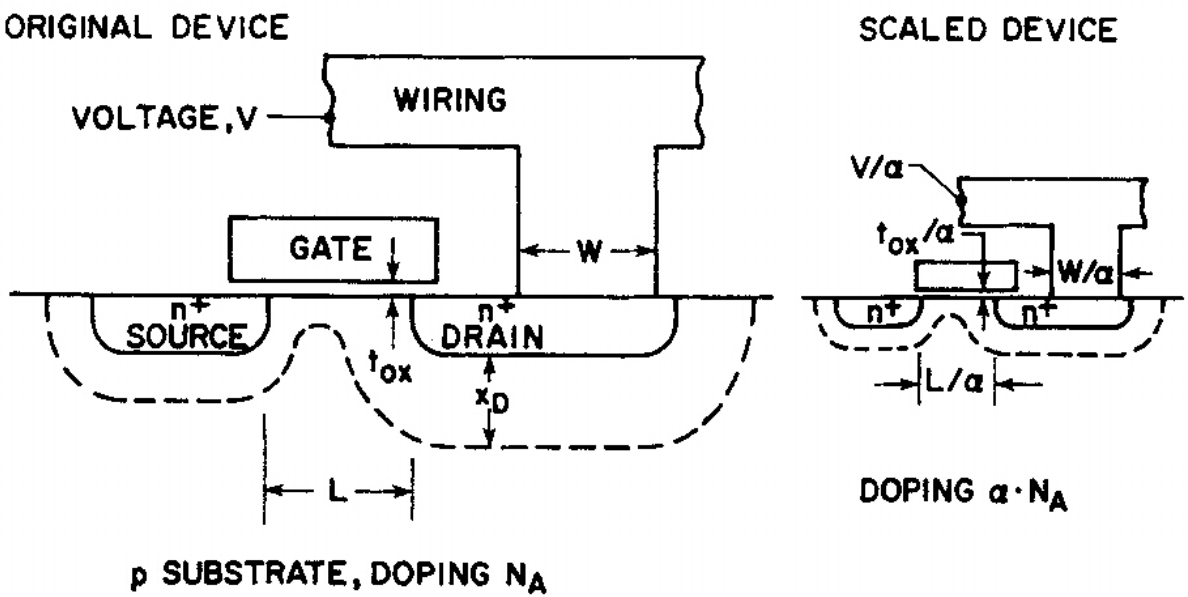
$$PDP = C_L \cdot V_{DD}^2$$

Power-delay product

$t_{ox} \downarrow$ $V_{DD} \downarrow$ $C_L \downarrow$

Constant field scaling

The aim of scaling is to reduce the device dimensions (to improve the circuit performance) without introducing effects which could disturb the good operation of the device.



$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}}\sqrt{\phi_{bi} + V}$$

$$\alpha > 1$$

B. Davari et al., "CMOS Scaling for High Performance and Low Power - The Next Ten Years", *Proc. of the IEEE*, vol. 87, no. 4, Apr. 1999, pp. 659-667.

Constant field scaling

Summary of the scaling factors for several quantities

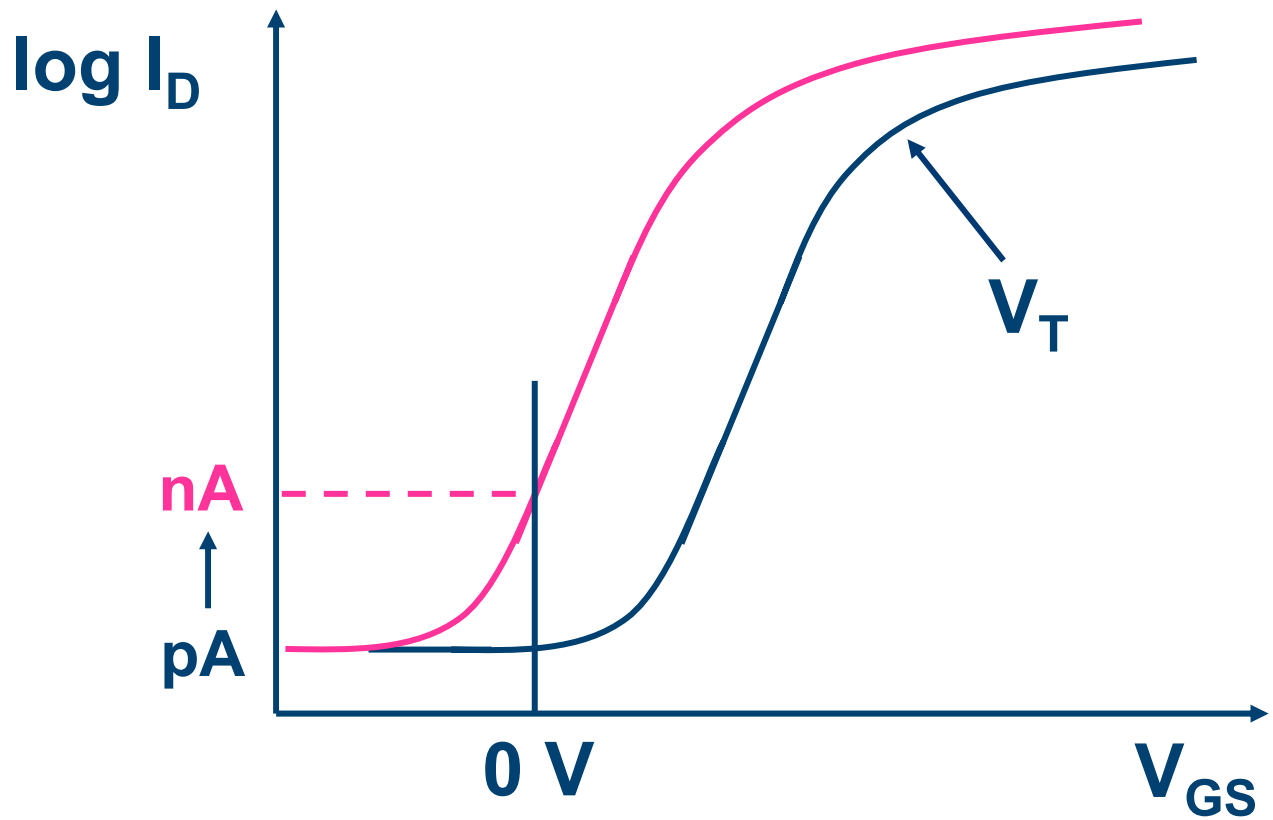
Quantity	Scaling Factor	Quantity	Scaling factor
Device dimensions (L, W, t_{ox}, x_D)	$1/\alpha$	Capacitances	$1/\alpha$
Area	$1/\alpha^2$	Capacitances per unit area	α
Devices per unit of chip area (density)	α^2	Charges	$1/\alpha^2$
Doping concentration (N_A)	α	Charges per unit area	1
Bias voltages and V_T	$1/\alpha$	Electric field intensity	1
Bias currents	$1/\alpha$	Body effect coefficient (γ)	$1/\sqrt{\alpha}$
Power dissipation for a given circuit	$1/\alpha^2$	Transistor transit time (τ)	$1/\alpha$
Power dissipation per unit of chip area	1	Transistor power-delay product	$1/\alpha^3$

$$\alpha > 1$$

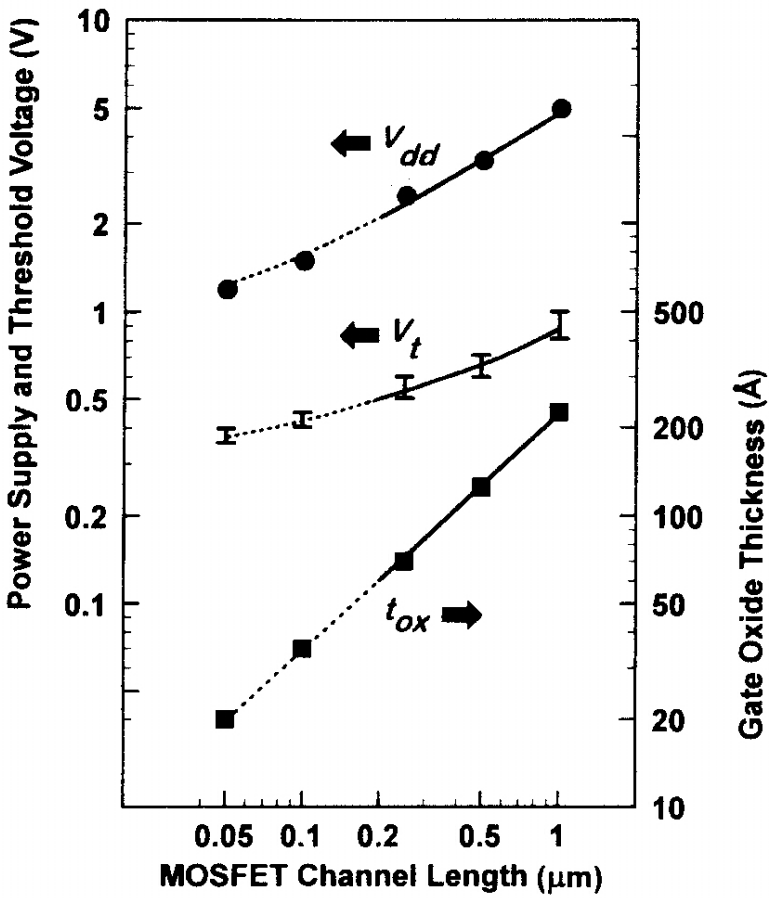
$$C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

Constant field scaling problem

Subthreshold slope and width of the moderate inversion region do not scale. This can have a devastating impact on the static power consumption of a digital circuit.



Generalized scaling

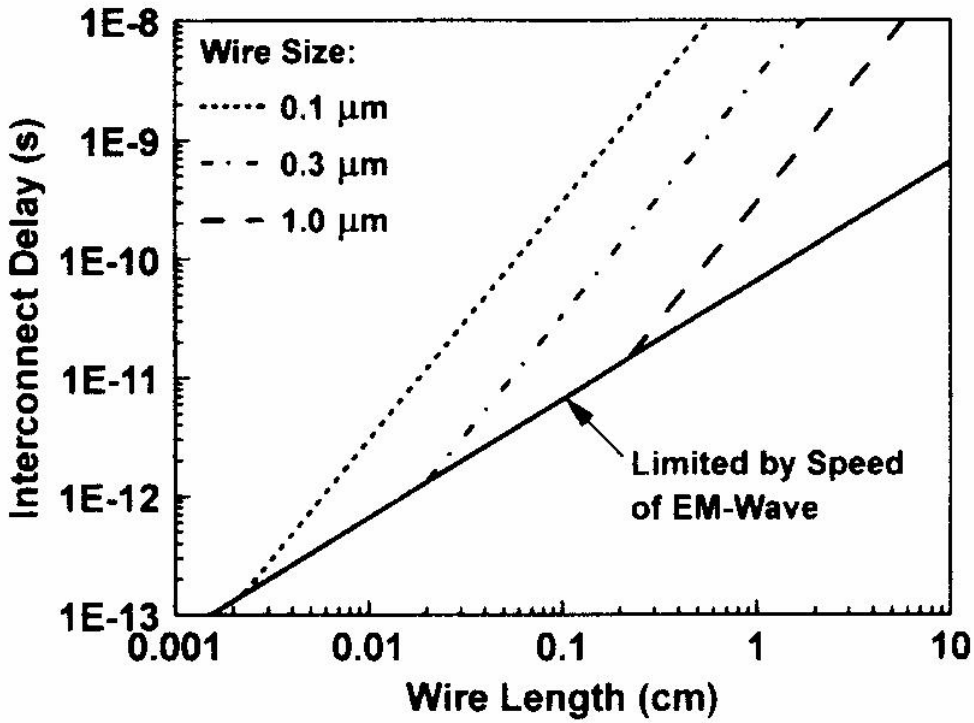


- The dimensions in the device scale as in the *constant field* scaling
- V_{dd} scales to have reasonable electric fields in the device, but slower than t_{ox}, to have an useful voltage swing for the signals
- The doping levels are adjusted to have the correct depletion region widths
- To limit the subthreshold currents, V_T scales more slowly than V_{dd}

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proc. of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.
Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 186.

Scaling of interconnections

An accurate scaling of the interconnections is needed as well, so that we can profit at the circuit level of the improvements made at the device level. Interconnections are becoming more and more important in modern technologies because the delay they introduce is becoming comparable with the switching time of the digital circuits.

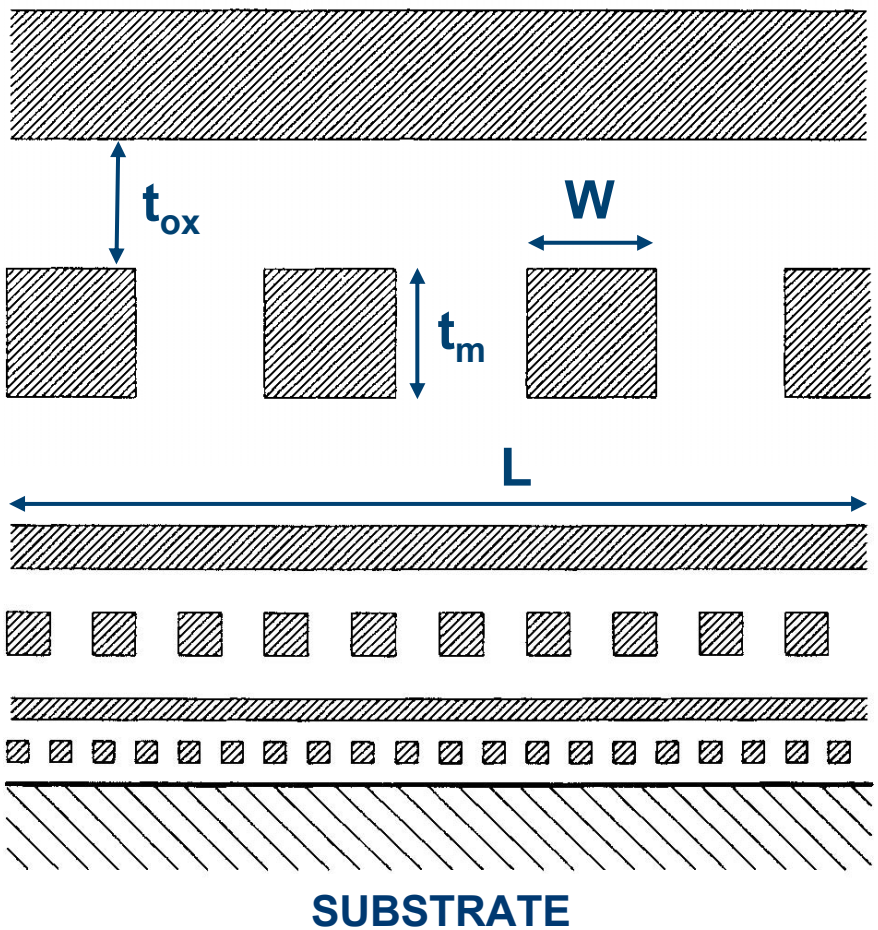


Wires with square section

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proceedings of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.
T. N. Theis, "The future of interconnection technology", *IBM Journal of Research and Development*, vol. 44, no. 3, May 2000, pp. 379-390.

"Reverse" scaling

The scaling method is different from the one applied to devices



If W, L, t_m and t_{ox} are decreased by α

- **Current density increases by α**
- **R increases by α, C decreases by α**
- **RC (delay) does not scale!!!**

In practice, wires dimensions are reduced only for local interconnections (but not t_m). At the chip scale, t_m and t_{ox} are increased (reverse scaling).

G. A. Sai-Halasz, "Performance trends in high-end processors", *Proceedings of the IEEE*, vol. 83, no. 1, January 1995, pp. 20-36.

Bipolar transistors scaling

Scaling has been much less emphasized for bipolar than for MOS transistors, but reducing the lateral and vertical dimensions of a BJT has a beneficial impact on its performance.

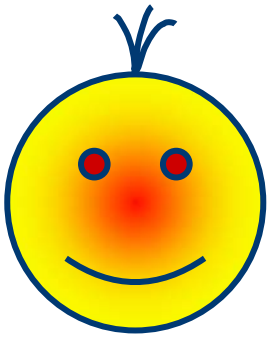
Reducing the lateral dimensions increases the density and reduces the parasitic resistances and capacitances (→ speed increases).

Reducing the vertical dimensions (in particular the base width / depth W_B) increases the collector current density, the current gain and the speed.

Scaling must be performed adjusting doping levels and bias voltages accordingly (breakdown voltages!).

Scaling impact on CMOS analog ICs

t_{ox} scales ⟶ for the same device dimensions



- Threshold voltage matching improves $\sigma_{\Delta V_{th}} = \dfrac{Const \cdot t_{ox}}{\sqrt{W\,L}}$
- 1/f noise decreases $\dfrac{\overline{v_{in_1/f}^2}}{\Delta f} = \dfrac{K_a}{C_{ox}^2\,WL}\dfrac{1}{f^{\alpha}}$
- Transconductance increases (same current) $g_m = \sqrt{\dfrac{2}{n}\mu C_{ox}\dfrac{W}{L}I_{DS}}$
- White noise decreases

Scaling impact on CMOS analog ICs

- **New noise mechanisms**
- **Modeling difficulties**
- **Lack of devices for analog design**
- **Reduced signal swing (new architectures needed)**
- **Substrate noise in mixed-signal circuits**
- **Velocity saturation. Critical field: 3 V/μm for electrons,**

  10 V/μm for holes

$$g_{m_vel.sat.} = WC_{ox}v_{sat}$$

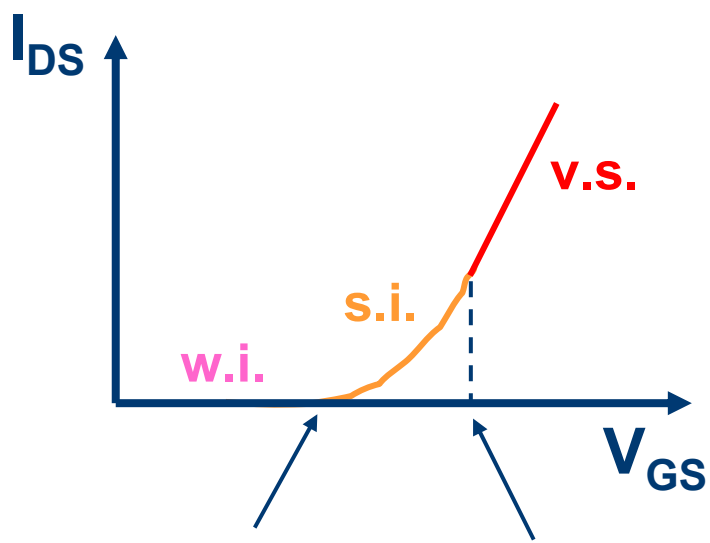
From weak inversion to velocity saturation

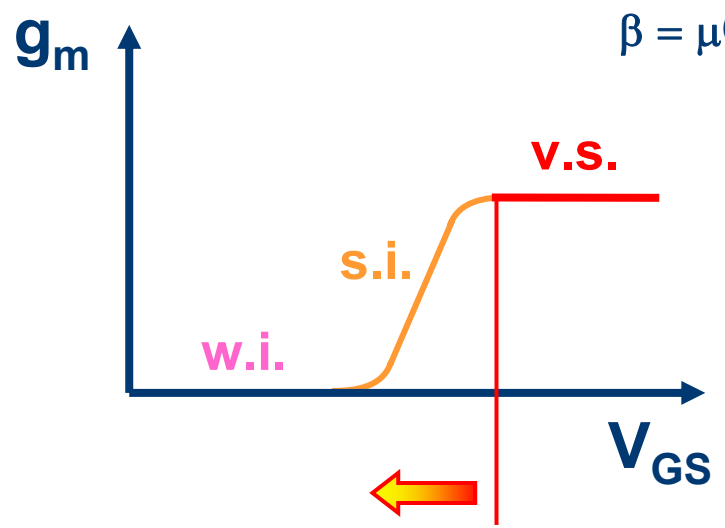
Weak inversion (w.i.) $I_{DS_w.i.} = I_{D0}\frac{W}{L}e^{\frac{V_{GS}}{n\phi_t}}$ $g_{m_w.i.} = \frac{I_{DS}}{n\phi_t}$

Strong inversion (s.i.) $I_{DS_s.i.} = \frac{\beta}{2n}(V_{GS} - V_T)^2$ $g_{m_s.i.} = \sqrt{2\frac{\beta}{n}I_{DS}}$

Velocity saturation (v.s.) $I_{DS_v.s.} = WC_{ox}v_{sat}(V_{GS} - V_T)$ $g_{m_v.s.} = WC_{ox}v_{sat}$

$$\beta = \mu C_{ox}\frac{W}{L}$$





$$V_{w.i._to_s.i.} = 2n\phi_t \qquad V_{s.i._to_v.s.} = 2nL\frac{v_{sat}}{\mu}$$

$V_{s.i._to_v.s.}$ **decreases with scaling!!!**

Scaling impact on power, speed, SNR

$$PWR = I_{DS} \cdot V_{DD}$$

$$\overline{v^2_{n_white}} = 4kTn\gamma \frac{1}{g_m}$$

$$SNR_w = \frac{V_{DD}}{\sqrt{\overline{v^2_{n_white}}}}$$

Assuming constant field scaling and strong inversion:

W	L	β	I_{DS}	PWR	C_{ox}*W*L	Q	$\Delta t = Q/I$	$\sqrt{\overline{v^2_{n_white}}}$	SNR_w
$1/\alpha$	$1/\alpha$	α	$1/\alpha$	$1/\alpha^2$	$1/\alpha$	$1/\alpha^2$	$1/\alpha$	1	$1/\alpha$
1	$1/\alpha$	α^2	1	$1/\alpha$	1	$1/\alpha$	$1/\alpha$	$1/\alpha^{1/2}$	$1/\alpha^{1/2}$
$1/\alpha$	1	1	$1/\alpha^2$	$1/\alpha^3$	1	$1/\alpha$	α	$\alpha^{1/2}$	$1/\alpha^{3/2}$
1	1	α	$1/\alpha$	$1/\alpha^2$	α	1	α	1	$1/\alpha$
α	$1/\alpha$	α^3	α	1	α	1	$1/\alpha$	$1/\alpha$	1

To maintain the same SNR we do not gain in Power !!!

Outline

- Operation and characteristics of MOS and Bipolar transistors
- Sub-micron CMOS and BiCMOS technologies
- Feature size scaling
- Radiation effects and reliability
  - Introduction
  - Total Ionizing Dose (TID) effects
  - Displacement Damage
  - Single Event Effects (SEE)
  - Solutions to the problems induced by radiation in CMOS technologies
  - Reliability issues
- Mixed-signal circuits

Interaction radiation-matter

The two most important phenomena to be considered are ionization and nuclear displacement.

Neutrons give origin mainly to nuclear displacement.

Photons give ionization.

Charged hadrons and heavy ions give both at the same time.

For ionization we talk about Total Ionizing Dose (TID), for nuclear displacement about Fluence

Interaction radiation - ICs

Cumulative Effects

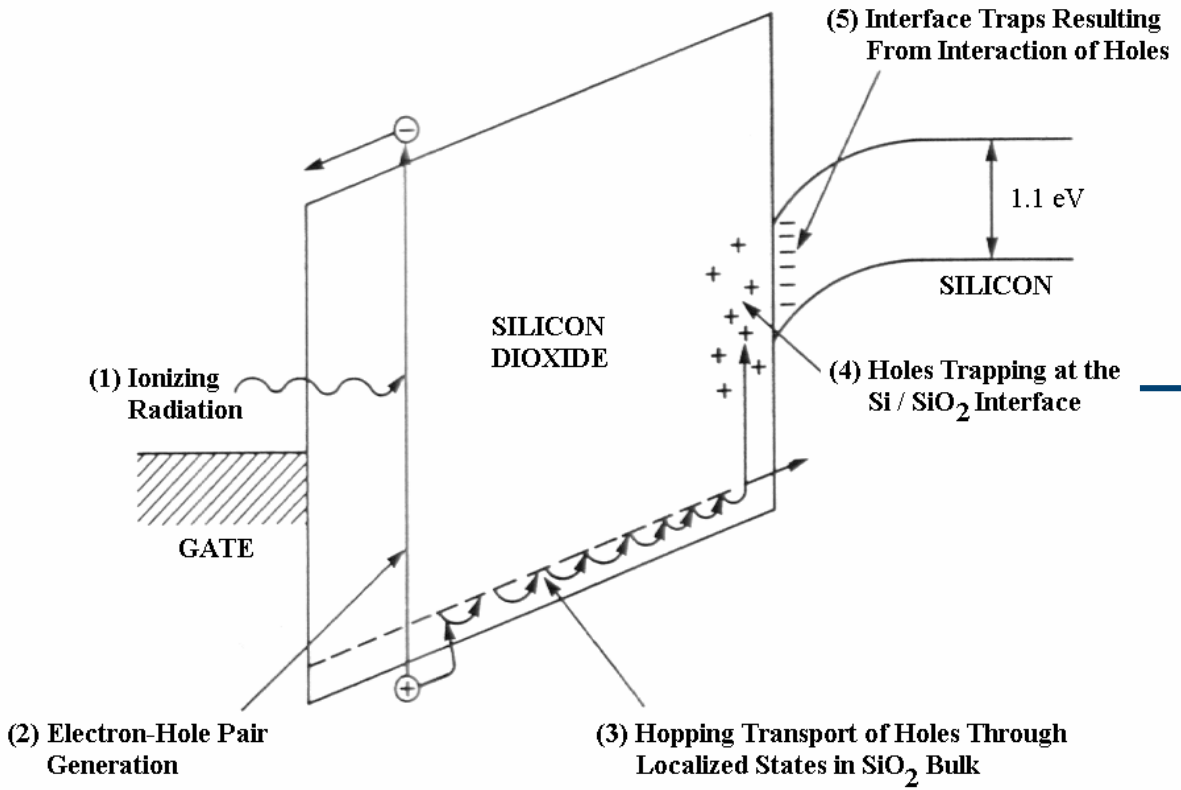
- **TID**
  - **MOS**
  - **Bipolars**
- **Displacement**
  - **Bipolars**
  - **Optoelectronics**

Single Event Effects (SEE)

- **Non Catastrophic (SEU)** → **MOS**
- **Catastrophic (SEGR, SEL)** → **MOS**

Ionizing particles through a MOST

Problems due to ionization in the thin gate oxide



- Threshold voltage shift
- Mobility degradation
- Swing degradation

(4) → Threshold voltage shift

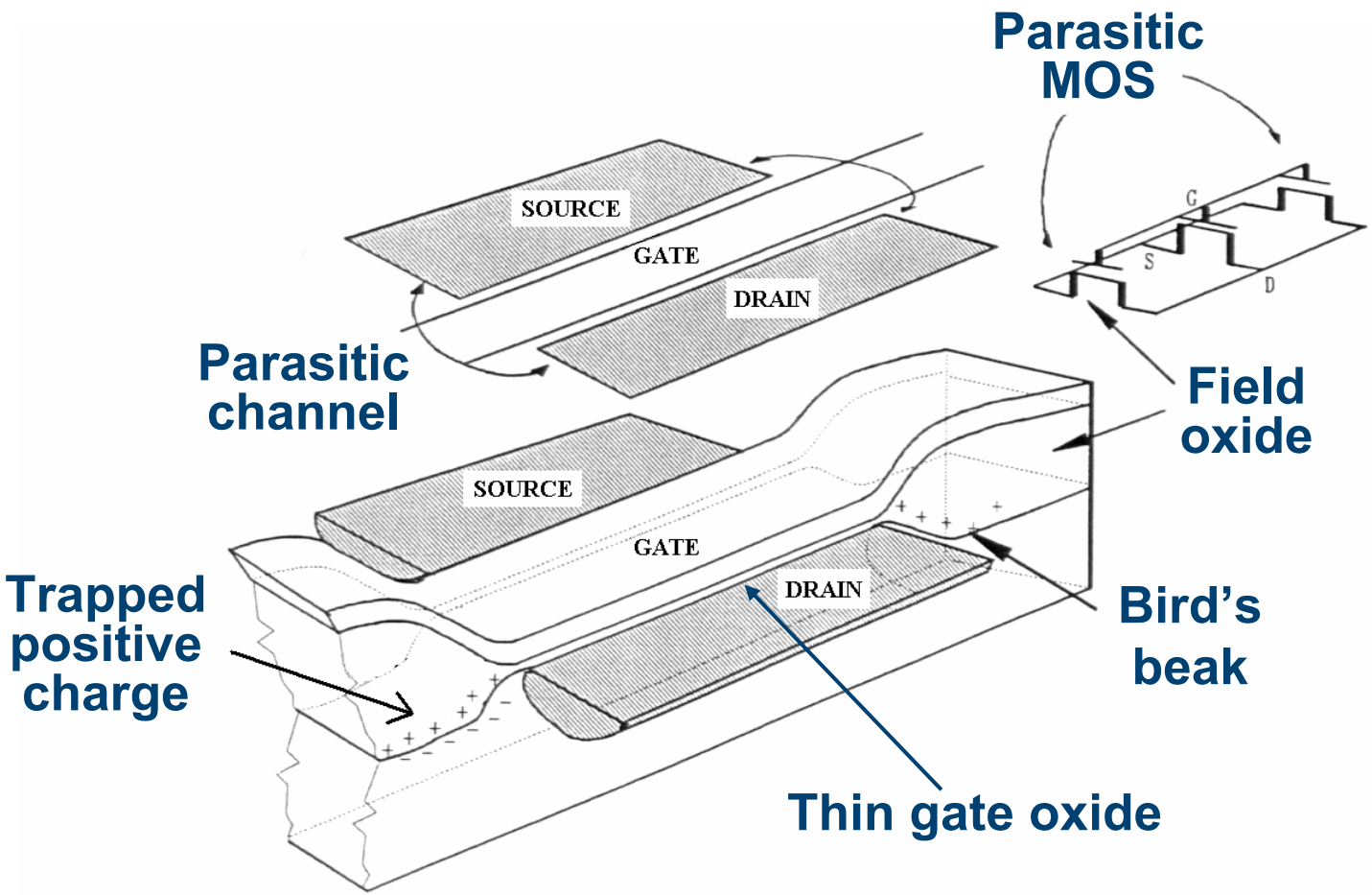
Other degradations:

- Transconductance
- Noise
- Matching

F. B. McLean and T. R. Oldham, Harry Diamond Laboratories Technical Report, No. HDL-TR-2129, September 1987.

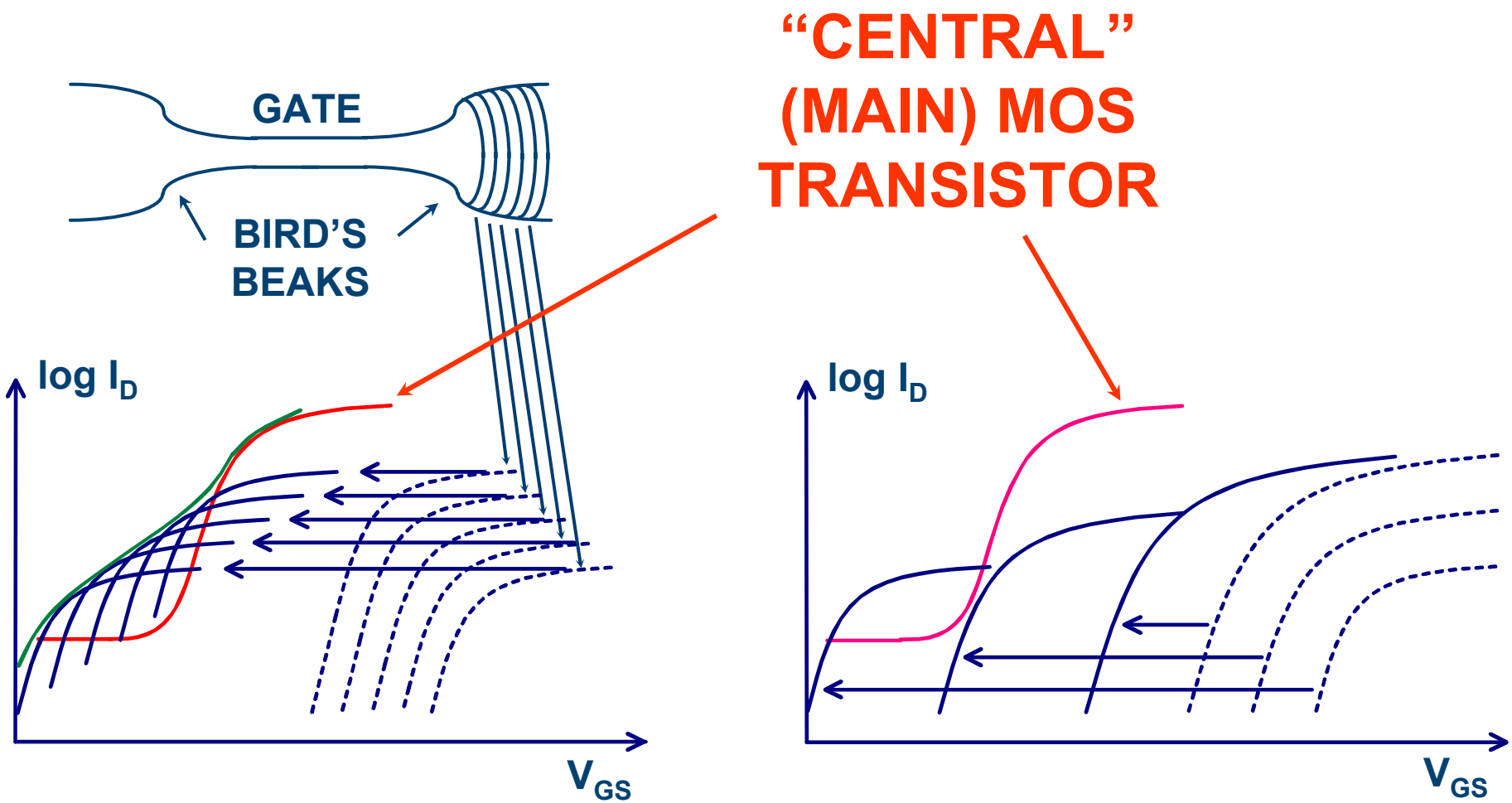
Transistor level leakage (NMOS)

Problem due to ionization in the thick field (lateral) oxide



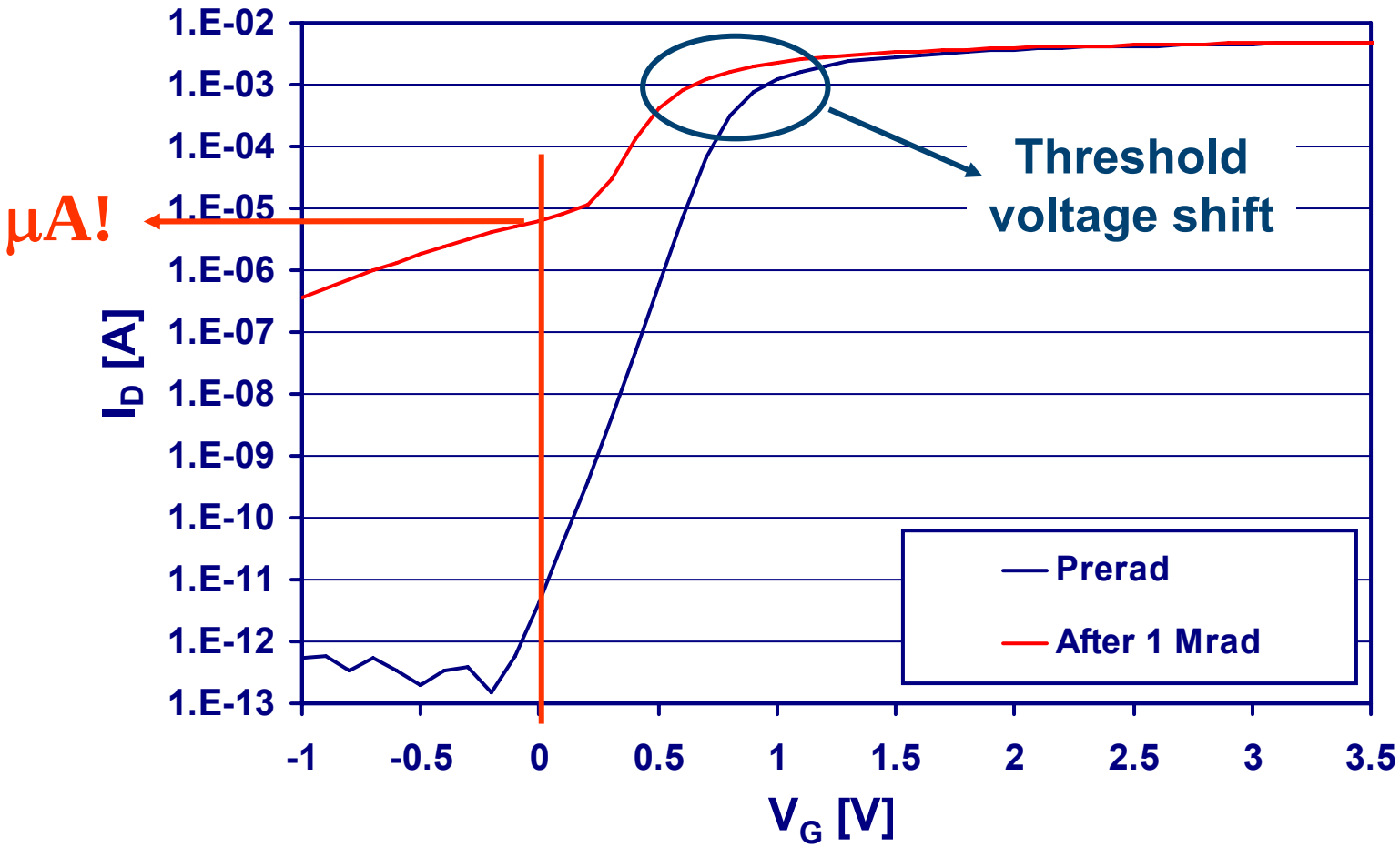
R. Gaillard, J.-L. Leray, O. Musseau et al., "Techniques de durcissement des composant, circuits, et systemes electroniques", Notes of the Short Course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), Sept. 1995.

Transistor level leakage (NMOS)



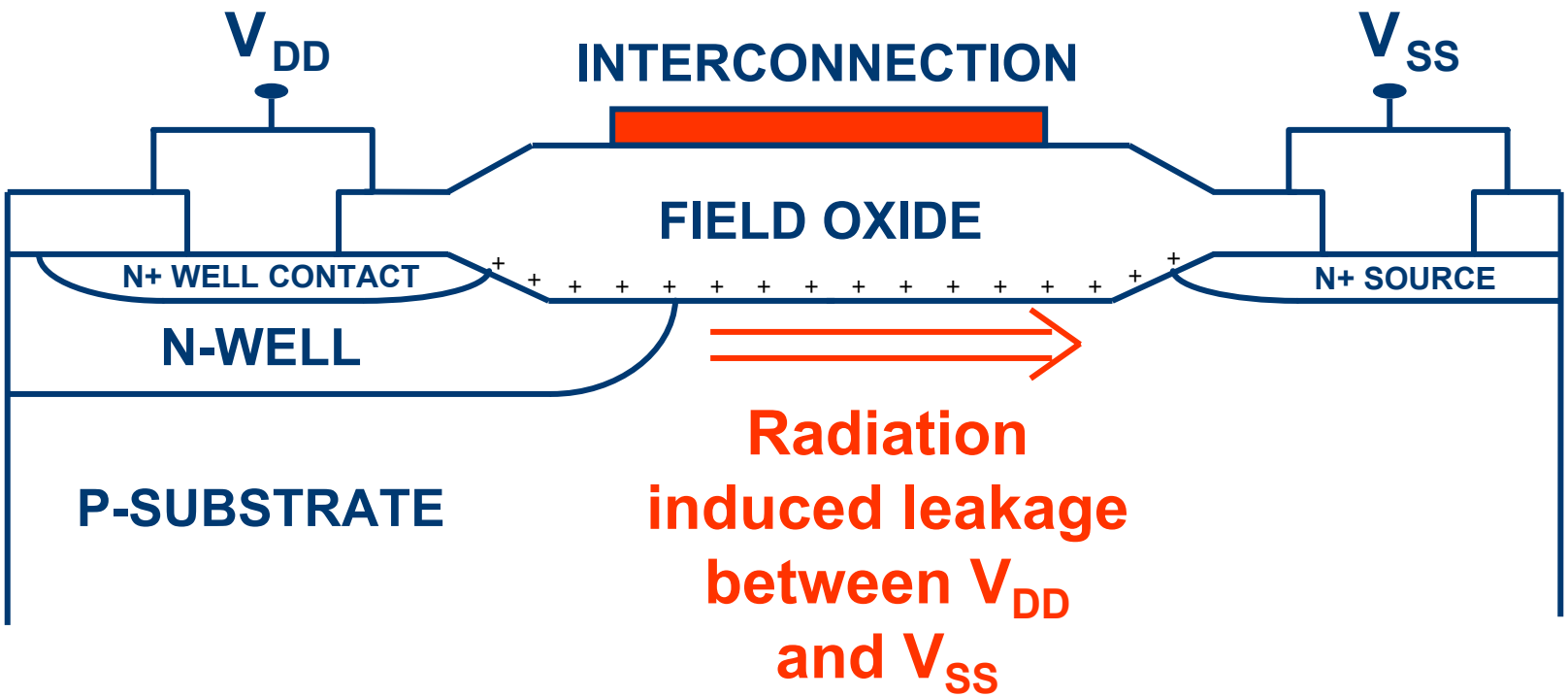
Transistor level leakage: example

NMOS - 0.7 μm technology - t_{ox} = 17 nm

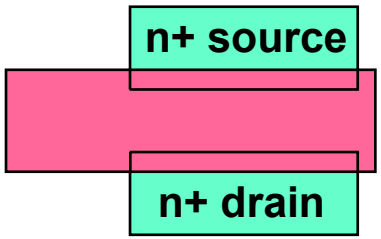


Field oxide leakage

Again problem due to ionization in the thick field (also called lateral or isolation) oxide

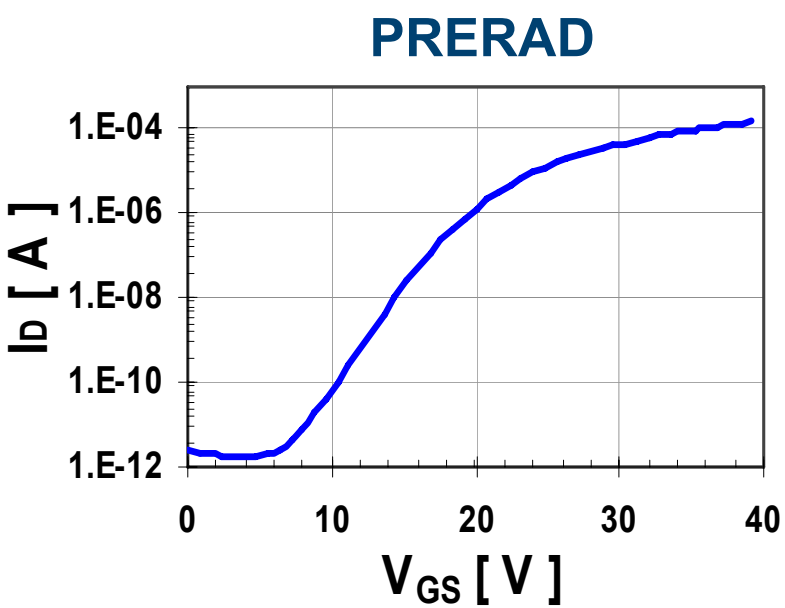


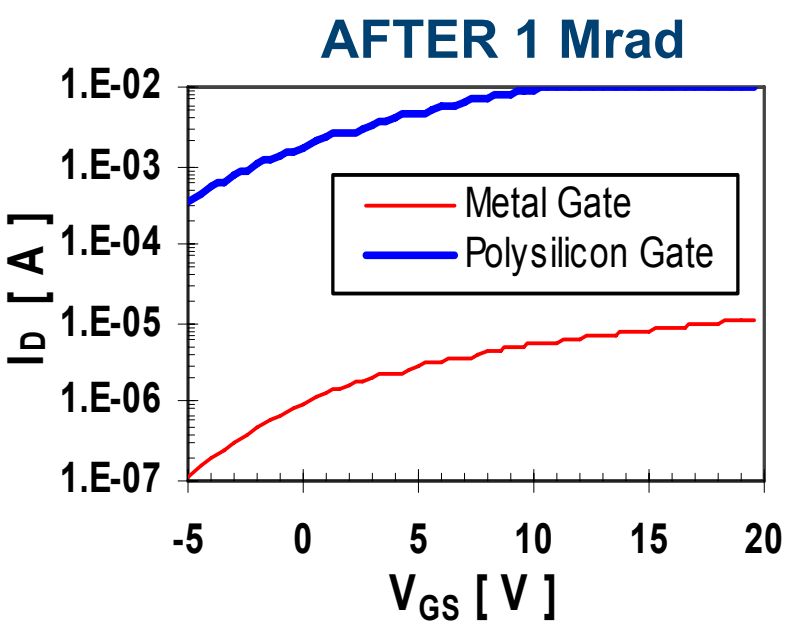
The Field Oxide Transistor



Post-irradiation leakage currents depend on

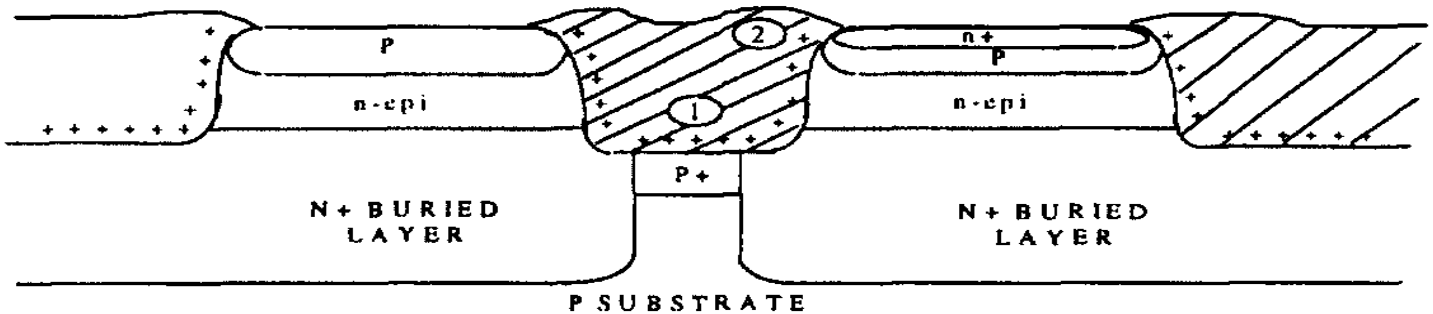
- **Total Dose**
- **Bias conditions**
- **Gate Material**
- **Field oxide quality**

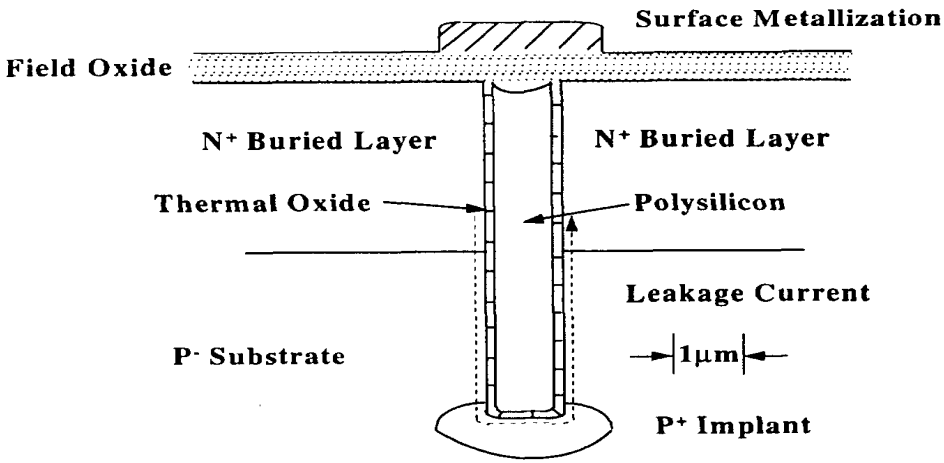




TID damage in bipolar devices

Substrate, sidewall and surface inversion (in oxide-isolated processes)

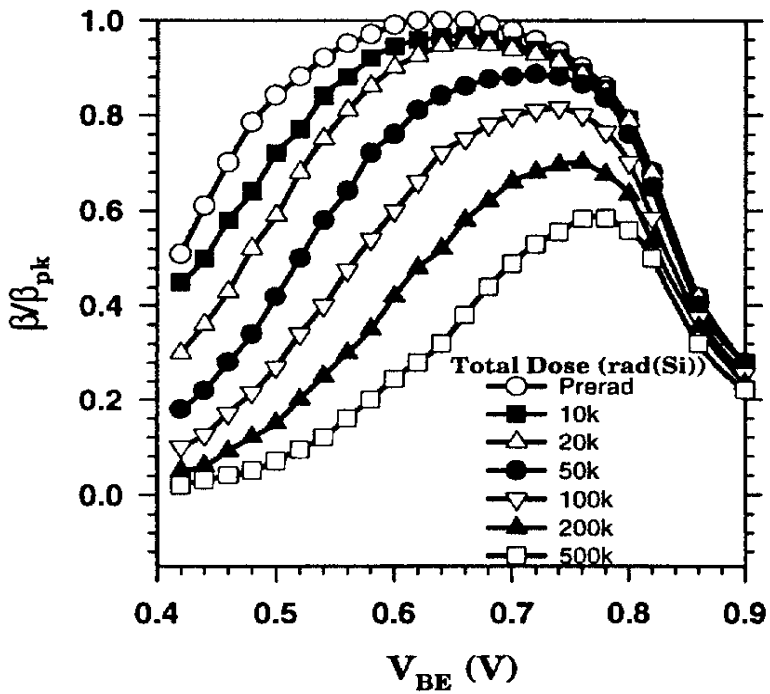


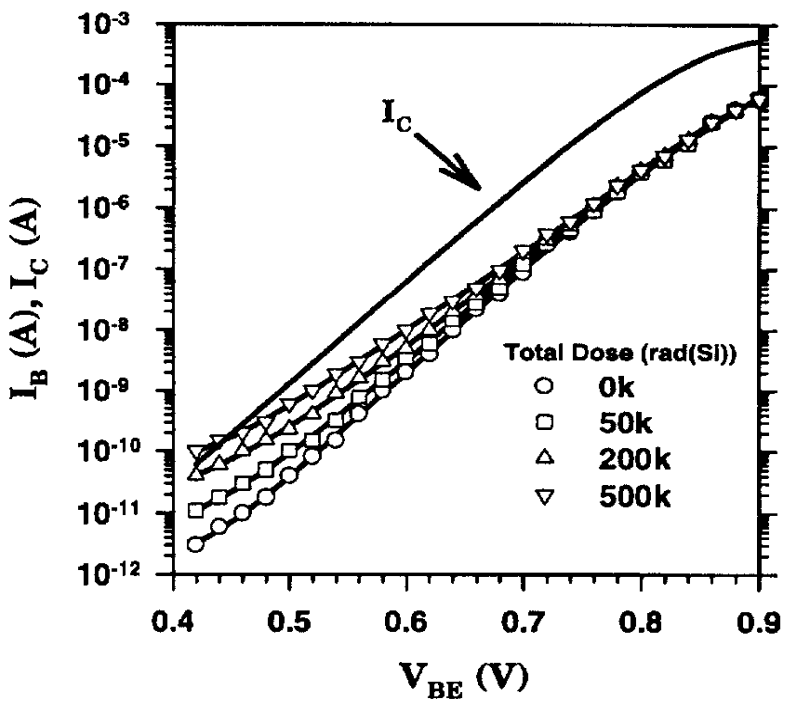


R.L. Pease et al., IEEE Trans. Nucl. Science. Vol.32, N.6, 1985
E.W. Enlow et al., IEEE Trans. Nucl. Science. Vol.36, N.6, 1989

TID damage in bipolar devices

Gain degradation:
Increase of the surface component of the base current





R. N. Nowlin et al., IEEE Trans. Nucl. Science. Vol. 39, N. 6, 1992

TID damage in bipolar devices

Factors affecting TID response of bipolar transistors

- Transistor polarity
- Oxide thickness over base-emitter region
- Oxide trap efficiency
- Vertical and fringing electric field
- Base and Emitter surface concentration
- Emitter perimeter-to-area ratio
- Transistor geometry (ratio of lateral to vertical current flow)
- Injection level
- Dose rate
- Temperature

Displacement damage

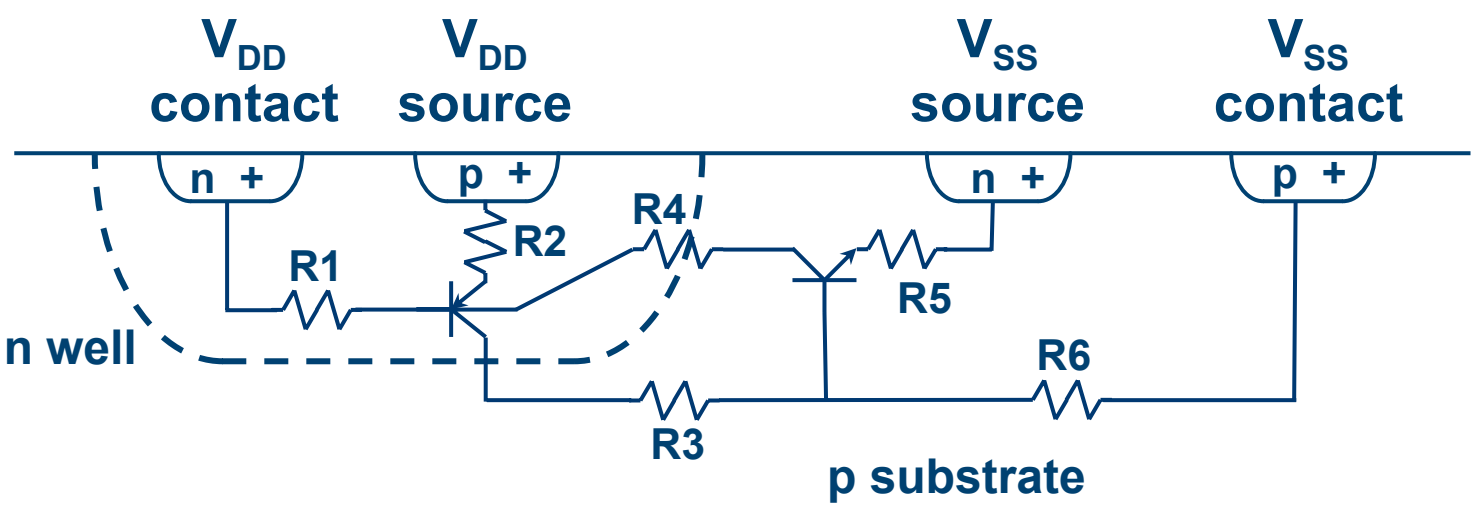
Displacement increases the recombination of minority carriers in the silicon bulk.

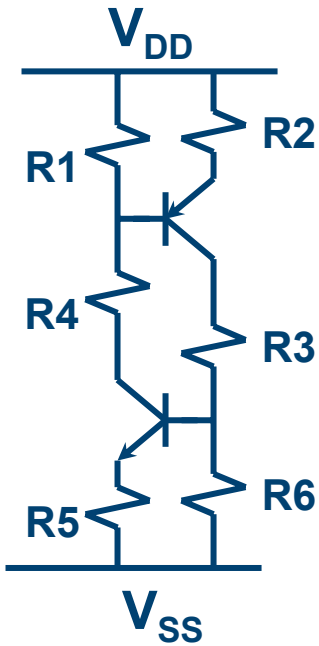
MOS transistors are not sensitive to displacement damage, since they are majority carrier devices and the transistor action takes place close to the SiO_2-Si interface (not in the silicon bulk).

Bipolar transistors, on the other hand, are sensitive to displacement damage, since they are minority carrier devices and the transistor action takes place in the silicon bulk. The increased recombination in the base increases the base current and reduces the gain.
Scaling of bipolar transistors helps reducing the sensitivity to displacement damage, since it reduces the transistor active volume.

Single Event Latch-up (SEL)

Electrical latch-up in CMOS processes might be initiated by electrical transients on input / output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.



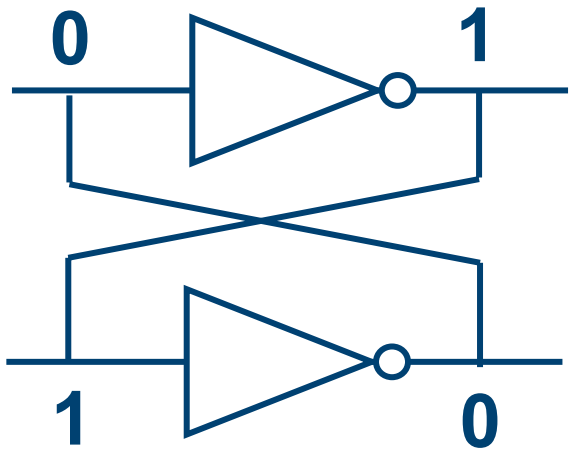


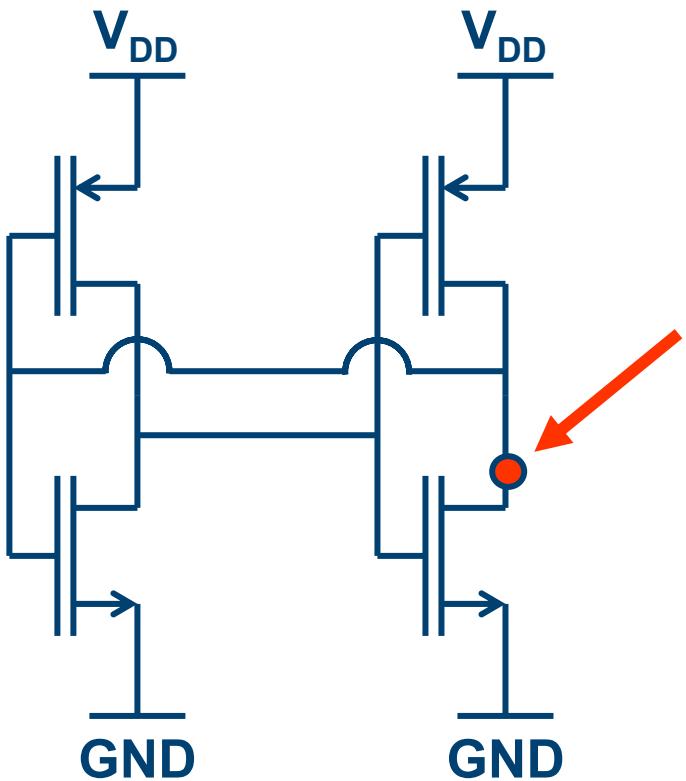
Latch-up can be initiated by ionizing particles (SEL).

If the supply is not cut quickly enough, it can be destructive!

Single Event Upset (SEU)

Static RAM cell





Highly energetic particle

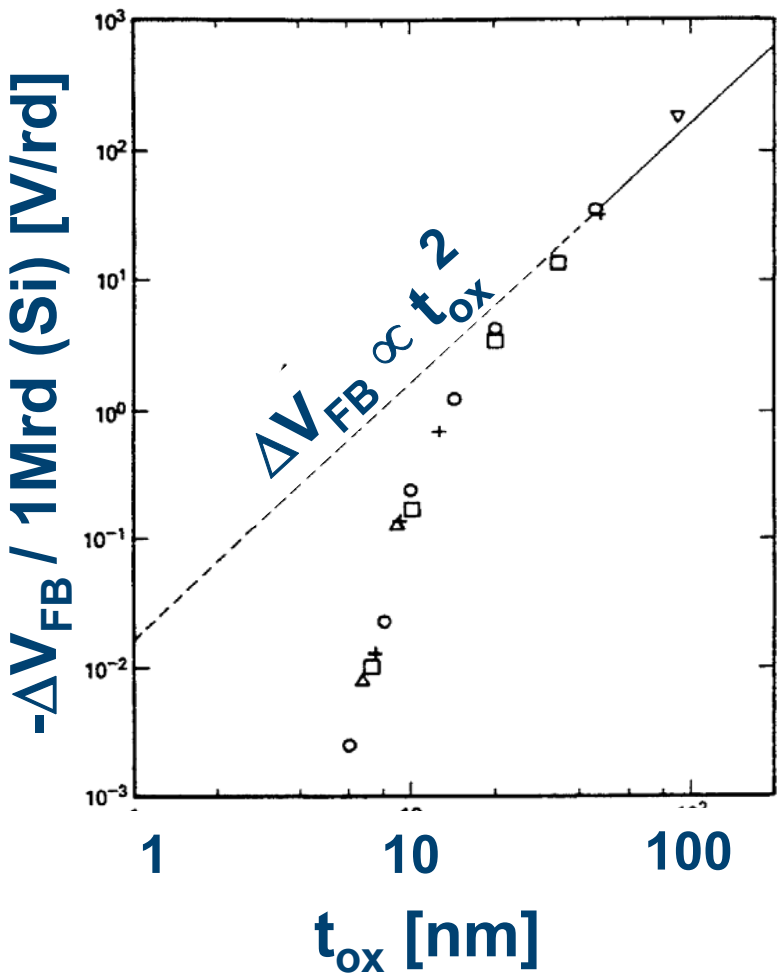
1 ⟶ 0

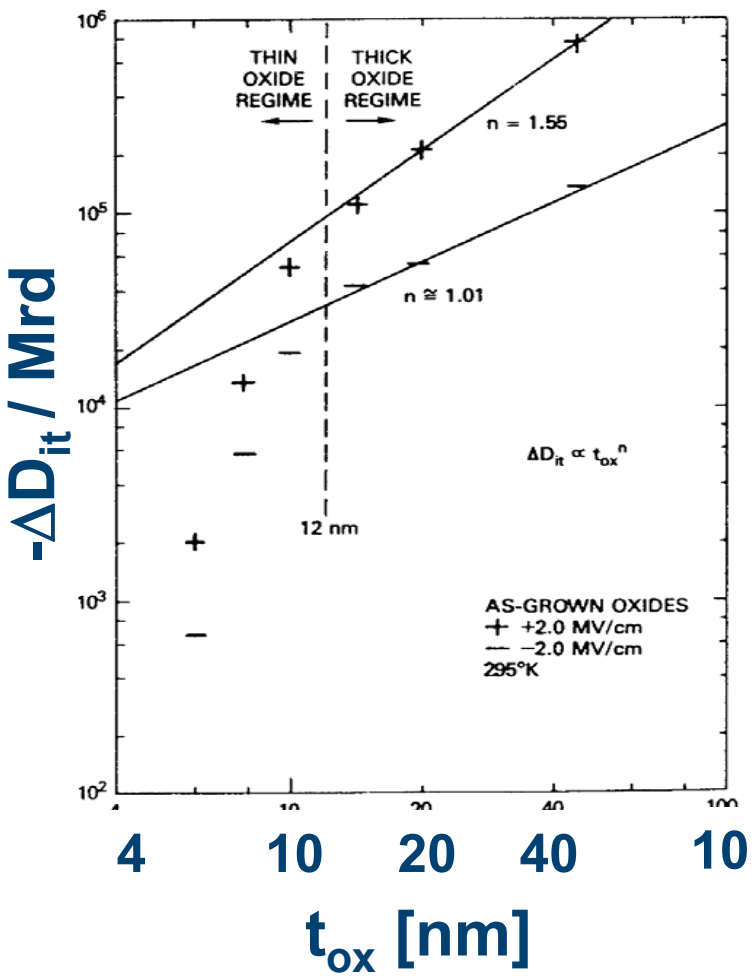
Never destructive, always (very) annoying.

Fighting SEU in a chip is a matter of risk management!

TID damage and CMOS scaling

MOS transistor gate oxide (thickness t_{ox})





N. S. Saks et al., *IEEE TNS*, vol. 31, no. 6, Dec. 1984, and vol. 33, no. 6, Dec. 1986.

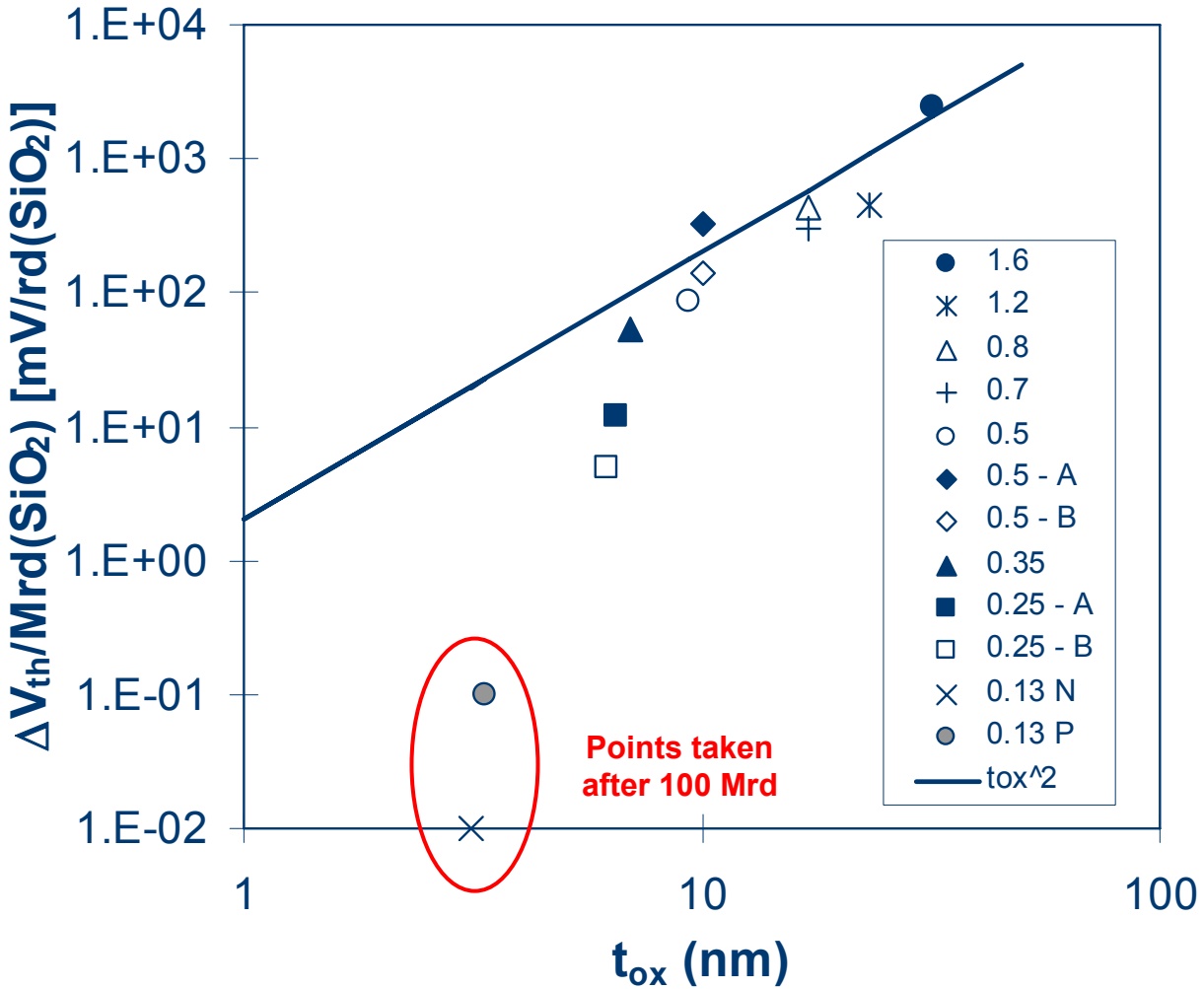
TID damage and CMOS scaling

Decreasing t_{ox} we decrease the degradation of:

- $\Delta V_T, \frac{\Delta V_T}{V_T}, \frac{\Delta V_T}{V_{DD}}$
- $\mu = \frac{\mu_0}{1 + \alpha \cdot (\Delta N_{it})}$
- **Transconductance**
- **Subthreshold slope**
- **Noise**

ΔV_T and CMOS scaling

Measurements done in our group @ CERN: it is really true!!!

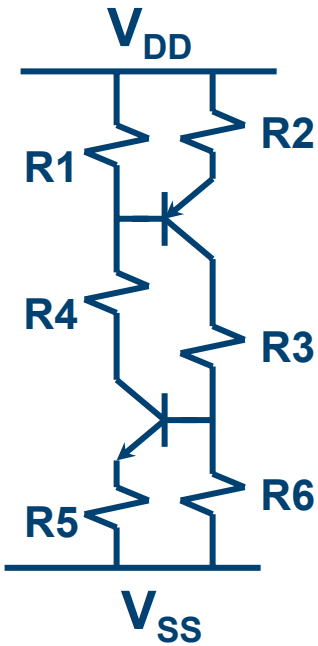


SEL and scaling

Modern CMOS technologies have:

- Retrograde wells
- Thinner epitaxial layers
- Trench isolation
- V_{DD} reduced

} R1 and R6 reduced



All these issues help in preventing SEL, but they might not be always effective

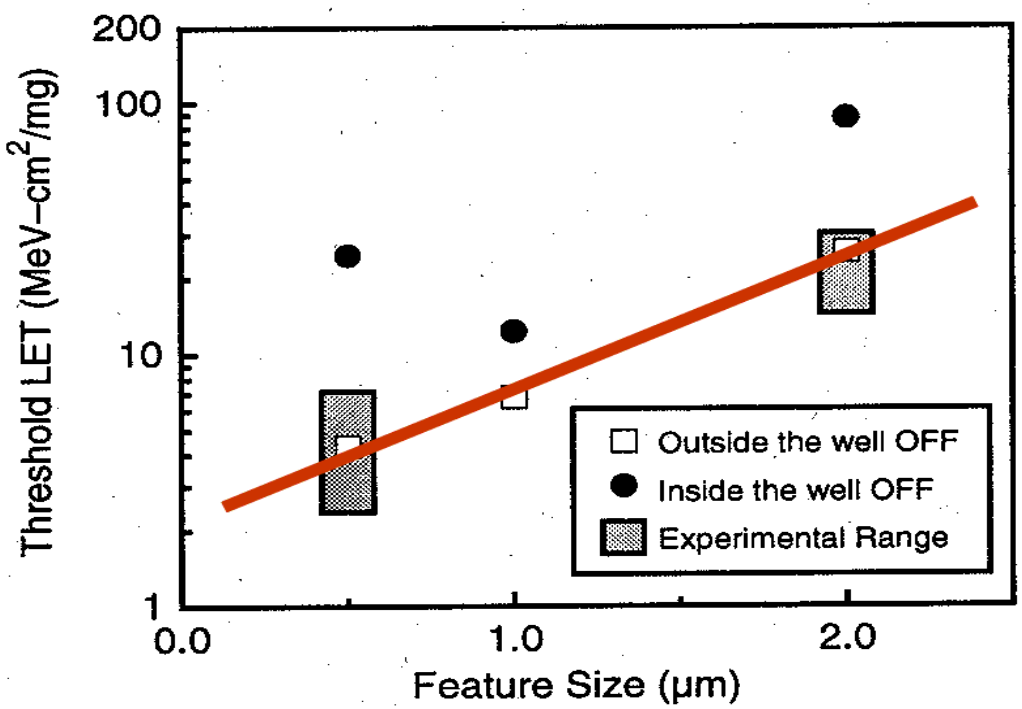
A. H. Johnston, *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, Apr. 1996, pp. 505-521.

SEU and scaling

- V_{DD} reduced
- Node C reduced

  BUT

- Charge collected reduced



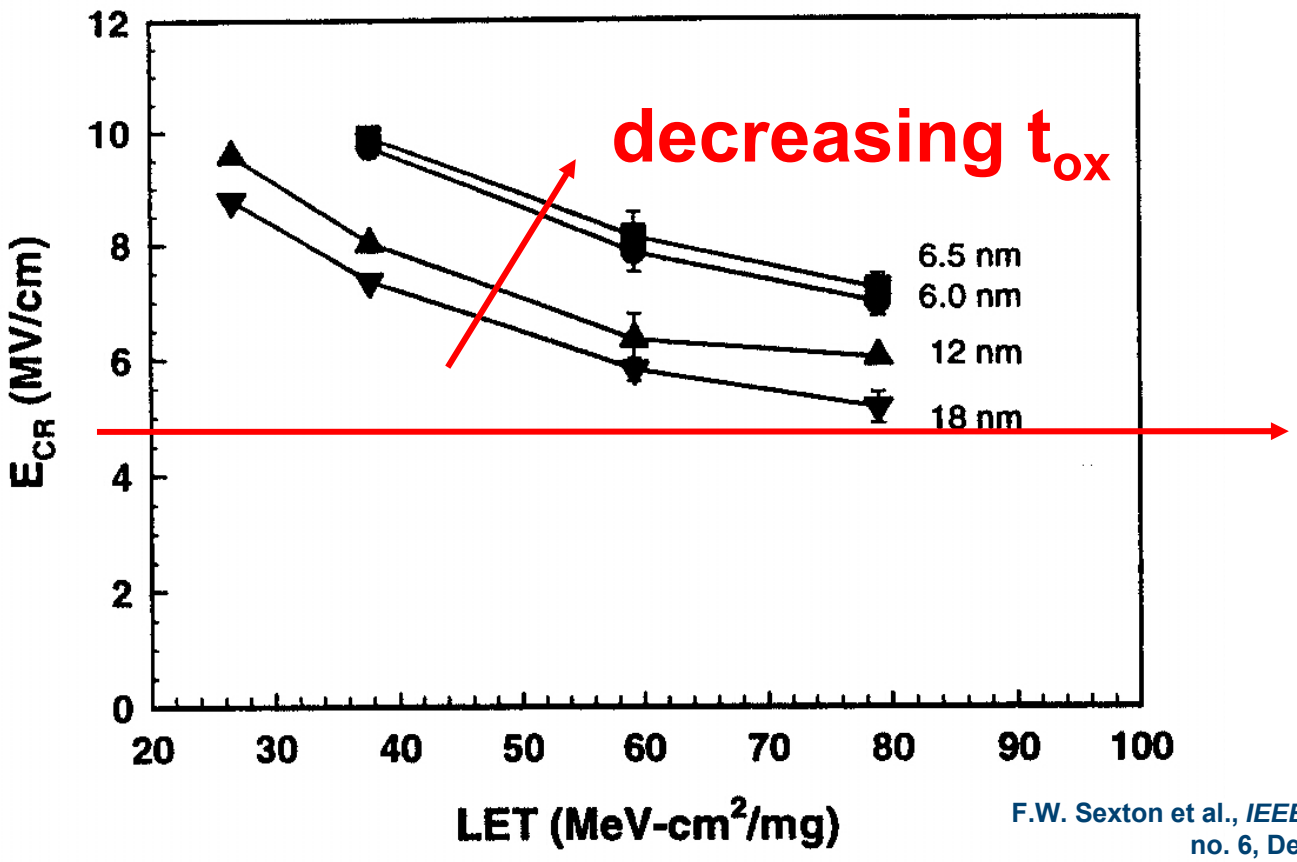
The SEU problem (may) worsen with scaling

P.E. Dodd et al., *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, Dec. 1996, pp. 2797-2804.

SEGR and scaling

SEGR: Single Event Gate Rupture

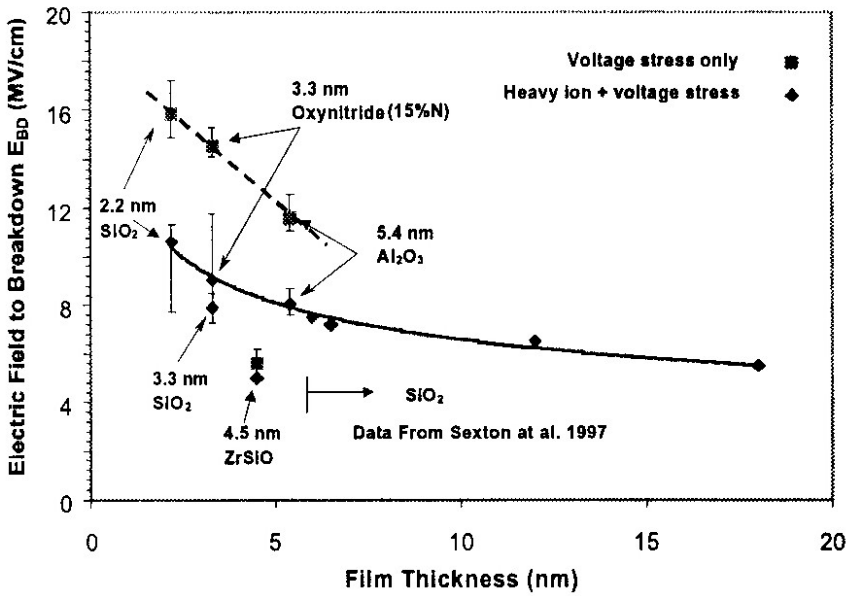
It is caused by a highly ionizing particle going through the gate of a MOS. It is a destructive effect (gate rupture).

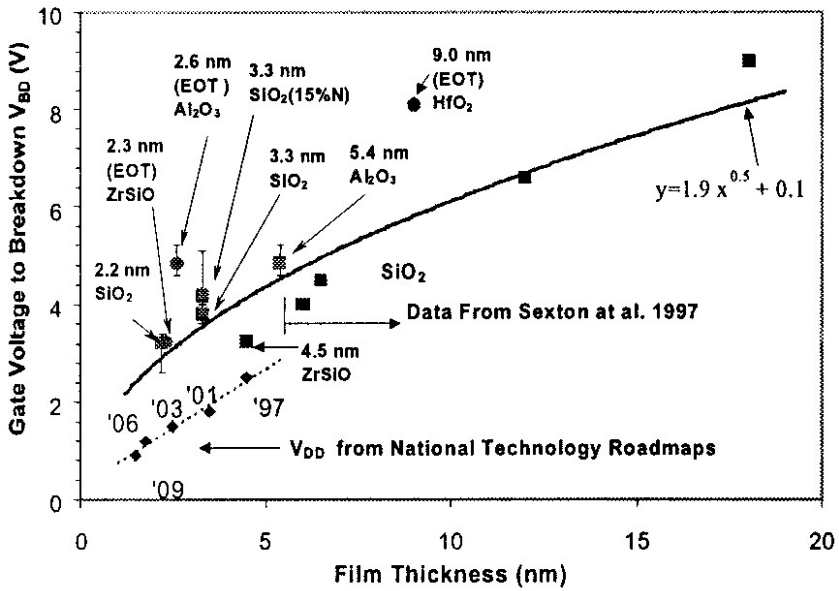


Maximum electric field for a quarter micron technology

F.W. Sexton et al., *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, December 1997, pp. 2345-2352.

SEGR in ULSI CMOS





SEGR is not a problem even in the most advanced CMOS processes.

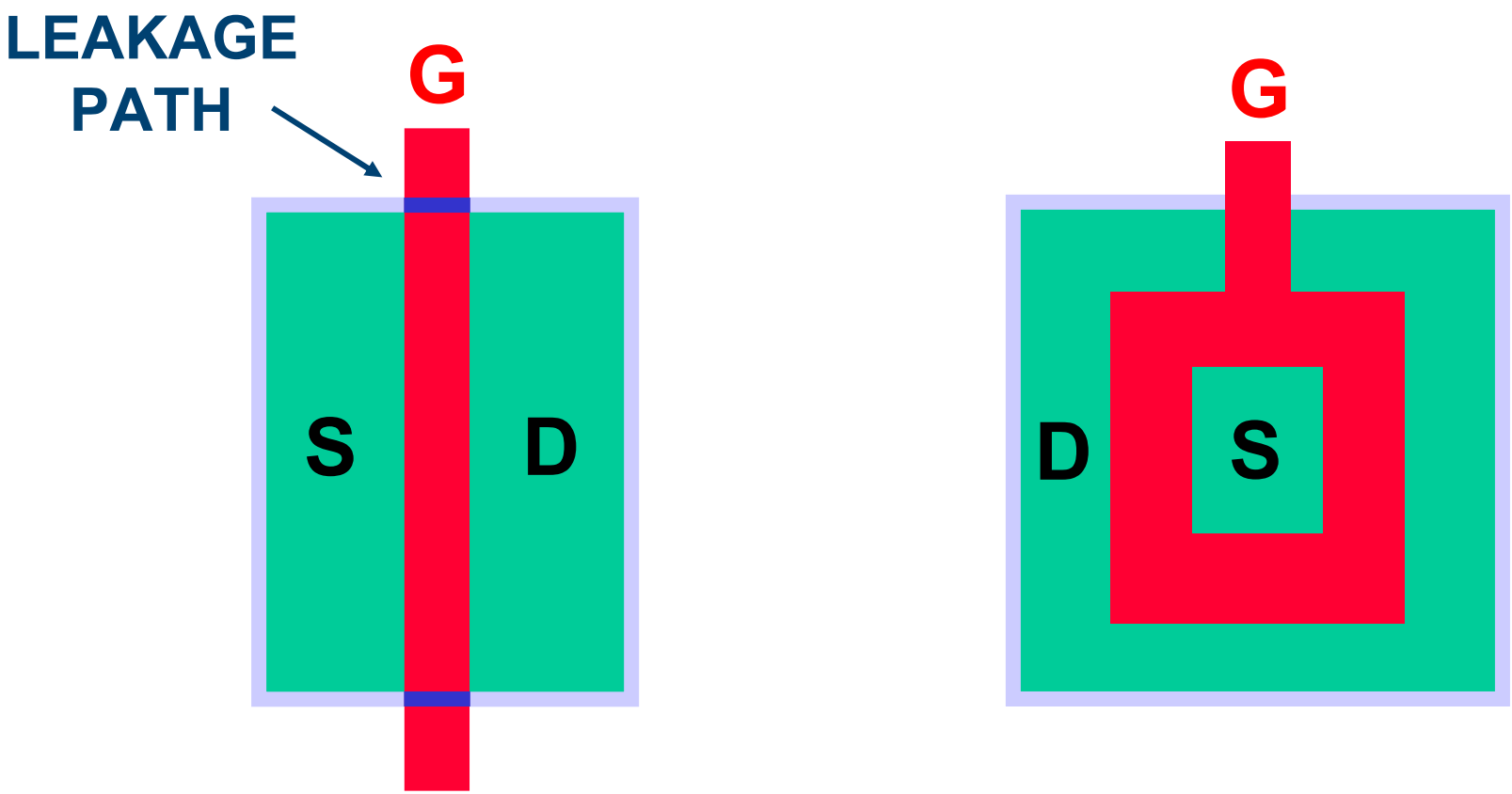
F.W. Massengill et al., *IEEE Transactions on Nuclear Science,* vol. 48, no. 6, December 2001, pp. 1904-1912.

Summary of problems in CMOS

- TID in thin oxide → Mainly V_T shift → Smaller in deep sub-μ CMOS processes.
- TID in Field Oxide → Leakage (in NMOS transistors and between transistors) → Might be better in more advanced technologies, but still a very big issue to be solved.

- SEU → Is it a Problem? This has to be evaluated and, in case it is, solved. Might become worse in deep sub-μ CMOS.
- SEL → Does not seem to be a problem, but care should be taken anyway.
- SEGR → Not a problem in deep sub-μ CMOS.

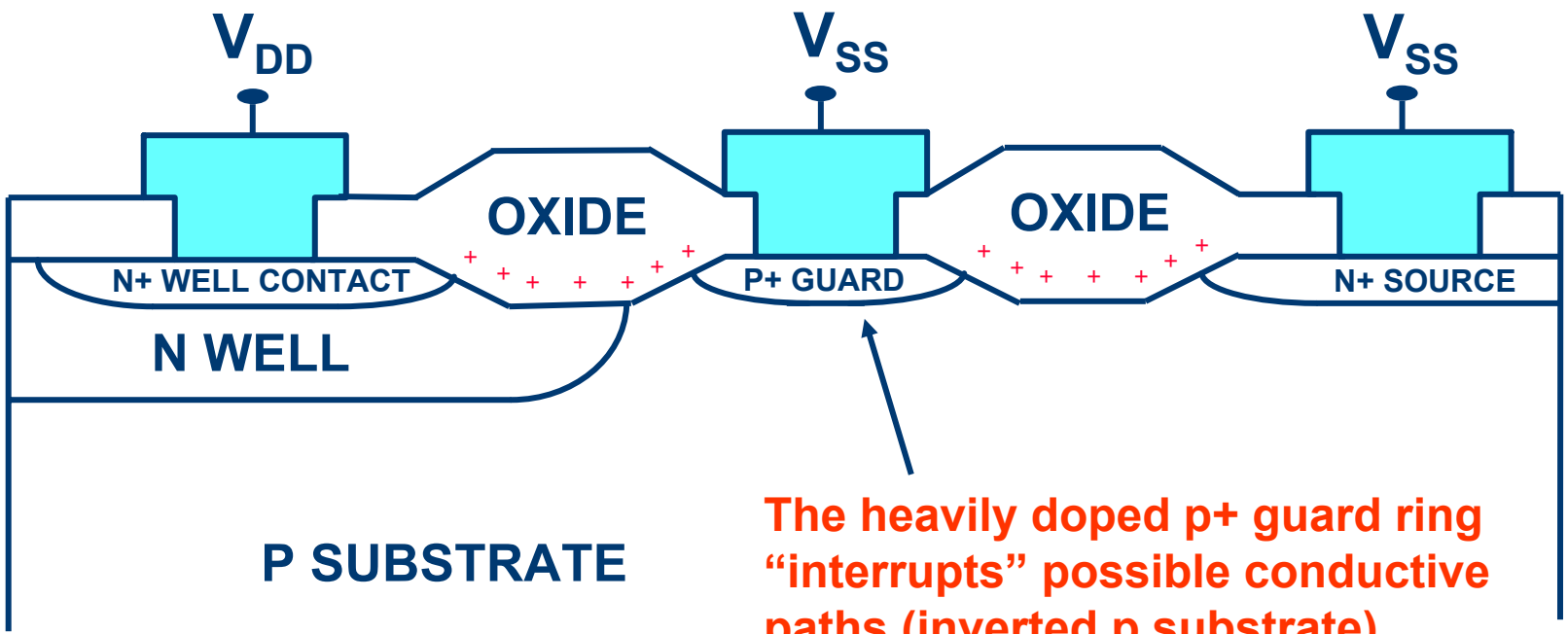
Enclosed Layout Transistor (ELT)



ELTs solve the leakage problem in the NMOS transistors

At the circuit level, guard rings are necessary

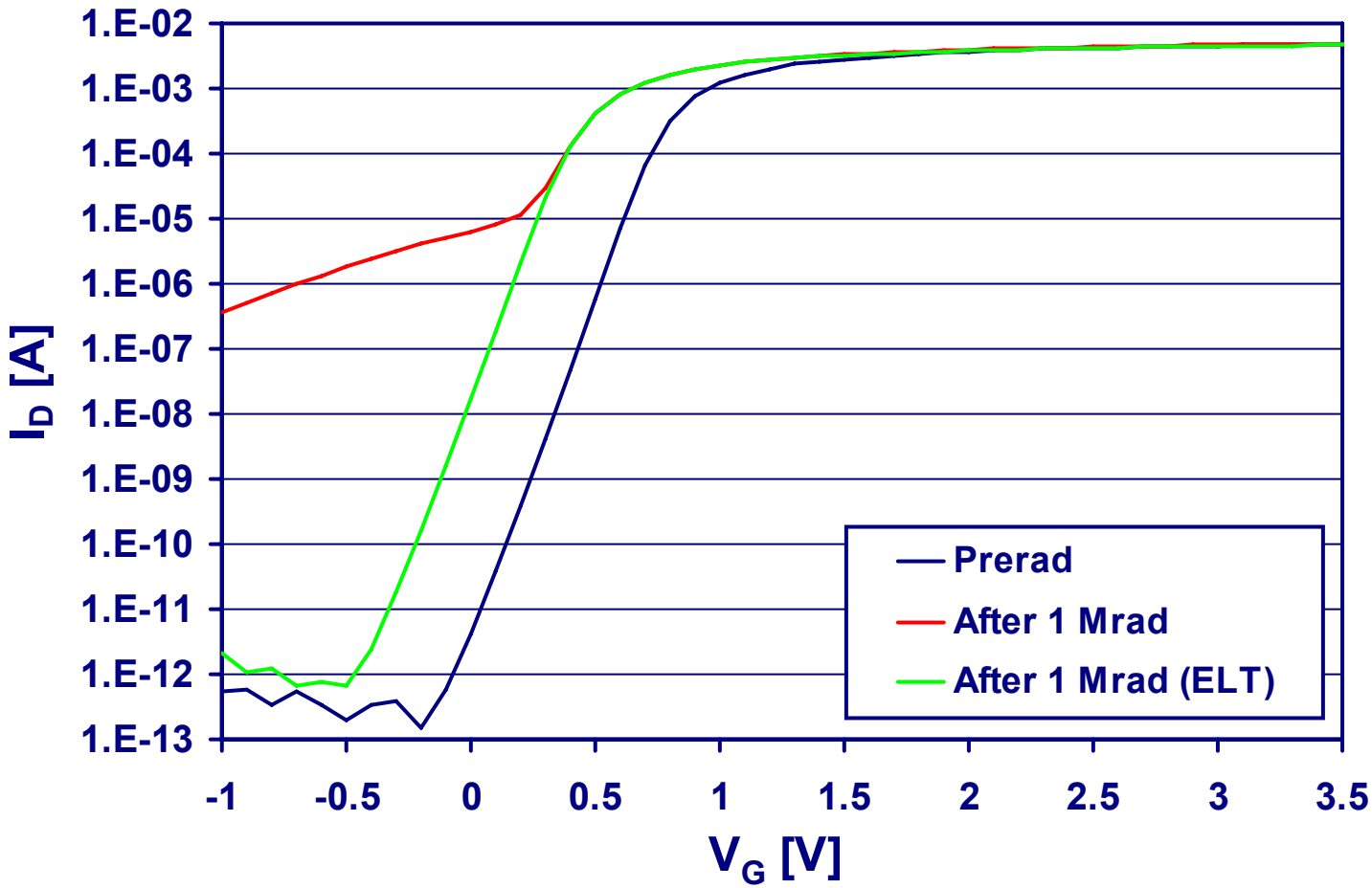
Guard rings



The heavily doped p+ guard ring "interrupts" possible conductive paths (inverted p substrate), preventing inter-device leakage currents

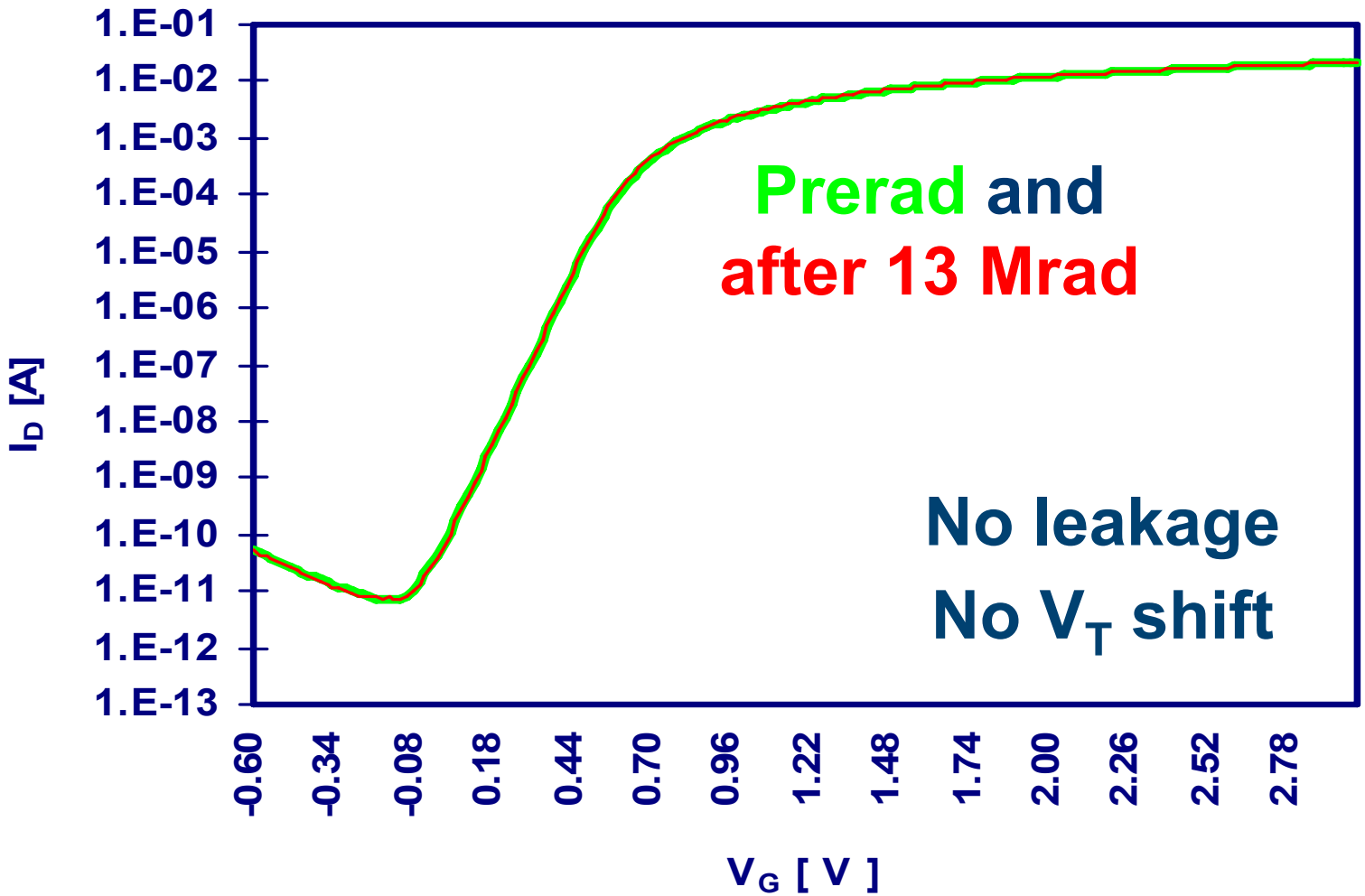
Effectiveness of ELTs

NMOS - 0.7 μm technology - t_{ox} = 17 nm

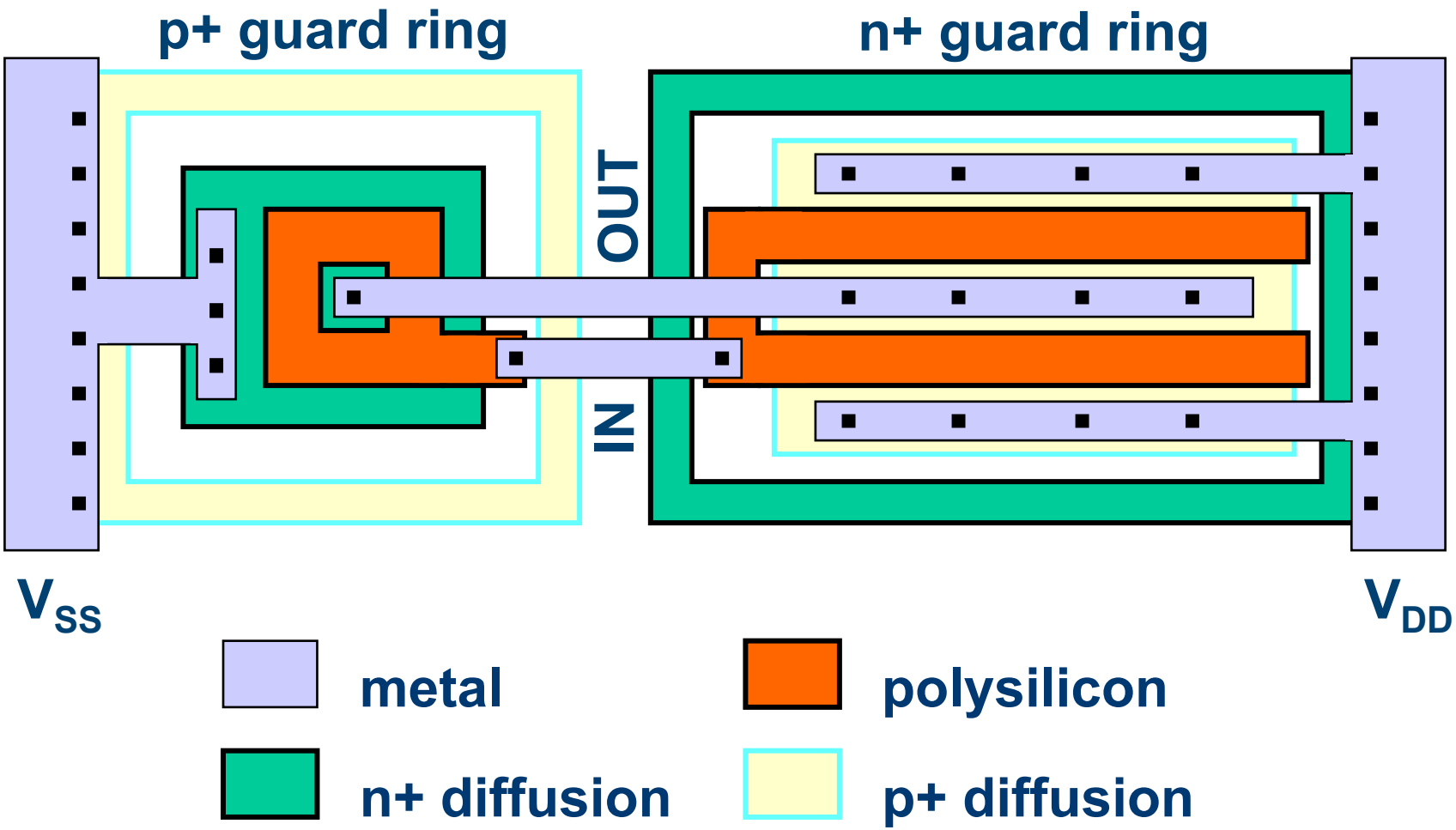


ELT & deep submicron

NMOS - 0.25 μm technology - t_{ox} = 5 nm



A radiation-hard inverter



Total Ionizing Dose tolerance

$\Delta V_{th} \propto t_{ox}^{n}$ + ELT's and guard rings = TID Radiation Tolerance

Deep sub-μm means also:

- speed
- low power
- VLSI
- low cost
- high yield

Single Event Effects

SEL

The systematic use of guard rings is <u>ALSO</u> an effective tool against SEL

SEGR

Never observed in our circuits

SEU

The higher gate capacitance of ELTs decreases the sensitivity, but other techniques might be necessary (at the circuit level)!

Reliability

Reliability: probability that a circuit will perform a required function under stated conditions for a stated period of time.

Reliability has become very important due to the aggressive scaling of device dimensions (without a corresponding scaling of the voltages).

This implied:

- **Higher electric fields**
- **Higher current densities**
- **Higher power dissipation**
- **Higher chip temperature**
- **Higher technology complexity (e.g. number of metal levels)**

http://www.imec.be/mtc/

G. Groeseneken et al., "Reliability, Yield and Failure Analysis", IMEC Microelectronics Training Center Course, Leuven, Belgium, 24-26/11/03

Failure mechanisms at the chip level

- **Devices:**
  - **Oxide breakdown → due to high electric field in the oxide**
  - **Hot Carriers → create interface traps and charge trapping @ the drain**
  - **Electro Static Discharge (ESD) → discharge of static charge coming from human body**
  - **Latch-up**
- **Interconnects:**
  - **Electromigration (wires and contacts) → mass transport of metal ions by momentum exchange with conduction electrons**
- **Packages:**
  - **Thermomechanical fatigue**
  - **Die cracking**
  - **Bond aging**

Outline

- Operation and characteristics of MOS and Bipolar transistors
- Sub-micron CMOS and BiCMOS technologies
- Feature size scaling
- Radiation effects and reliability
- Mixed-signal circuits
  - Analog design in digital CMOS processes
  - Digital noise in mixed-signal circuits

Analog design in digital processes

The integrated circuit market is driven by digital circuits, such as memories and microprocessors. This led to an increasing interest in integrating analog circuits together with digital functions in processes optimized for digital circuits, making what it is called a System on a Chip (SoC). This approach has several advantages and disadvantages.

ADVANTAGES:

- Lower wafer cost
- Higher yield
- Higher speed
- Lower power consumption (not always)
- Complex digital functions on chip (DSP)

DISADVANTAGES:

- Low power supplies
- Lack of "analog" components
- Inadequate modeling
  - Output conductance
  - Different inversion regions
- "Digital" noise

- E. A. Vittoz, "The Design of High-Performance Analog Circuits on Digital CMOS Chips", *IEEE JSSC*, vol. 20, no. 3, June 1985, pp. 657-665.
- W. Sansen, "Challenges in Analog IC Design in Submicron CMOS Technologies", *Proceedings of the 1996 IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design*, Pavia, Italy, 13-14 September 1996, pp. 72-78.
- C. Azaredo Leme and J. E. Franca, "Analog-Digital Design in Submicrometric Digital CMOS Technologies", *Proceedings of the 1997 IEEE International Symposium on Circuits and Systems*, Hong Kong, 9-12 June 1997, vol. 1, pp. 453-456.

Analog components availability

Analog design needs high-quality passive components. These are not always present in processes optimized for digital design, or at least not in the first stages of the process development. These analog "options" are:

- **High-resistivity polysilicon for resistors**
- **Diffusion resistors**
- **Trimming options**
- **Linear <u>and</u> dense capacitors**
  - **Metal to metal (at least one special metal layer required)**
  - **Metal to poly**
  - **Poly to poly**

Integrated capacitors

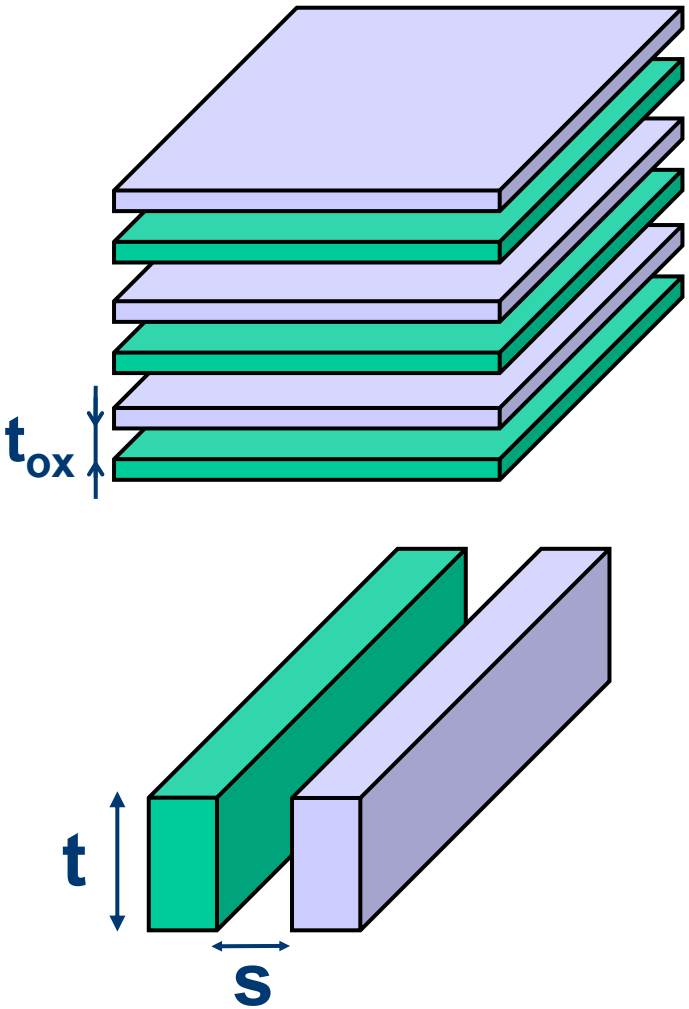
- High-linearity capacitors can be obtained with metal-to-metal structures. This requires adding a special metal layer to the technology, in order to reduce the dielectric thickness between the metal plates. The density reached is generally around a few fF/μm^2.

- Dense capacitors can be obtained exploiting the high capacitance density of the thin gate oxide. This allows having dense and precise capacitors, good matching but very poor linearity. This solution can be adopted in any process.

- A third possible solution is suggested by the availability of many interconnection layers. Exploiting the parasitic capacitance between metal wires in a clever way, one can obtain linear capacitors with good matching and linearity and densities up to 1.5 fF/μm^2. These capacitors can be integrated in any process!!

- A. T. Behr et al., "Harmonic Distortion Caused by Capacitors Implemented with MOSFET Gates", *IEEE JSSC*, vol. 27, no. 10, Oct. 1992, pp. 1470-1475.
- D. B. Slater, Jr. and J. J. Paulos, "Low-Voltage Coefficient Capacitors for VLSI Processes", *IEEE JSSC*, vol. 24, no. 1, February 1989, pp. 165-173.
- J. L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors", *IEEE JSSC*, vol. 16, no. 6, Dec. 1981, pp. 608.
- S. Pavan, Y. Tsividis and K. Nagaraj, "Modeling of accumulation MOS capacitors for analog design in digital VLSI processes", *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, Orlando, Florida, USA, 30 May – 2 June 1999, vol. 6, pp. 202-205.

Multi-metal-layer capacitors



This solution is a possibility, but it does not exploit the fact that in deep submicron processes the highest parasitic capacitance can be obtained "horizontally" rather than vertically, i.e. $t_{ox} > s$

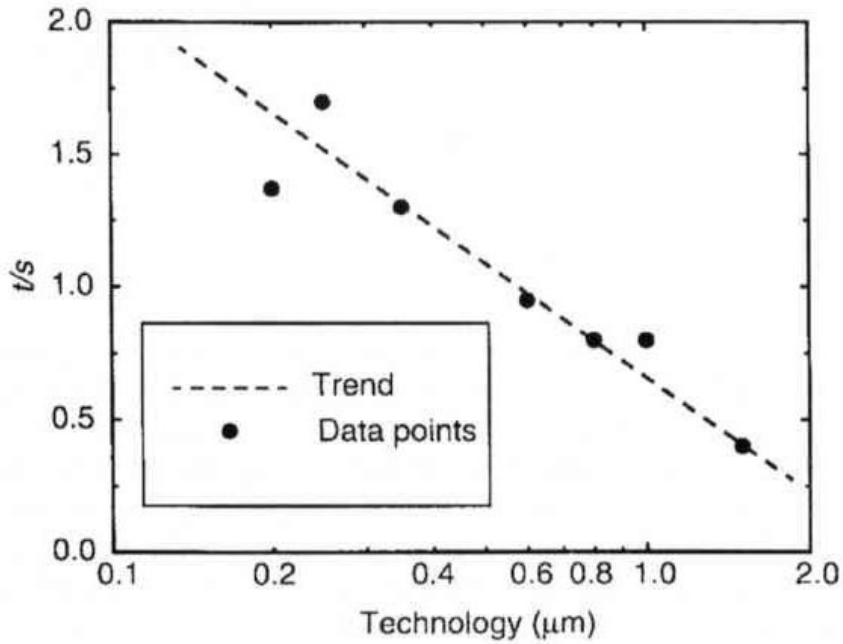
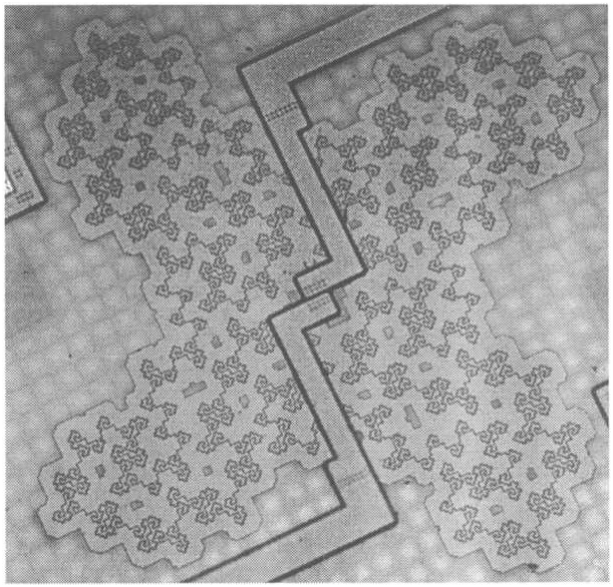
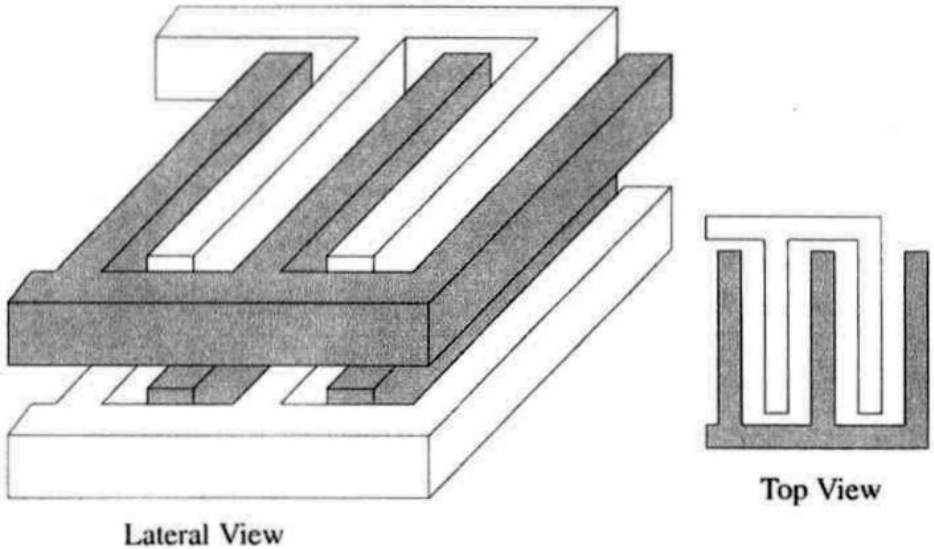


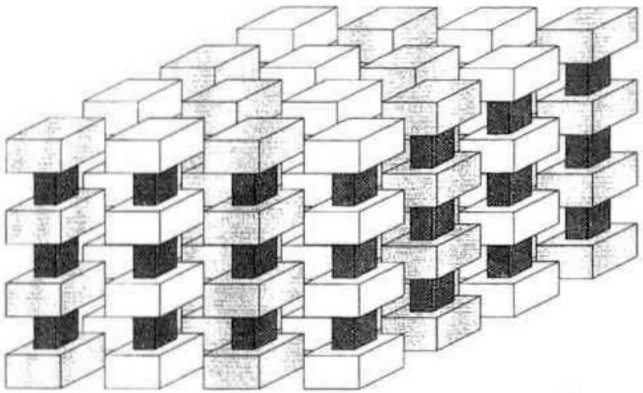
Fig. 3. Ratio of metal thickness to horizontal metal spacing versus technology (channel length).

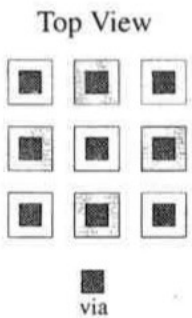
- **Hirad Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 1998, pp. 2035-2041.**

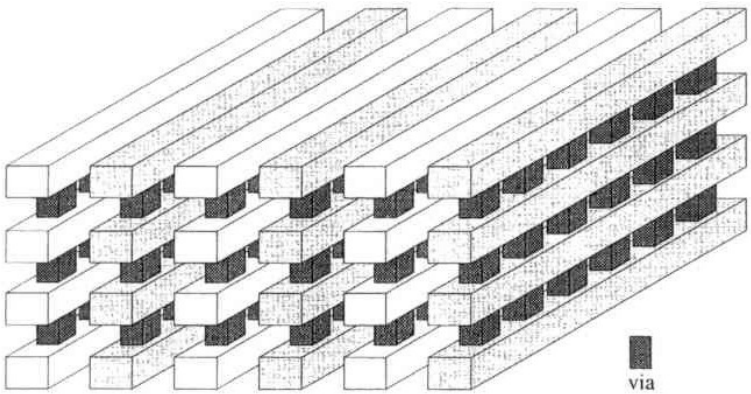
Multi-metal-layer capacitors









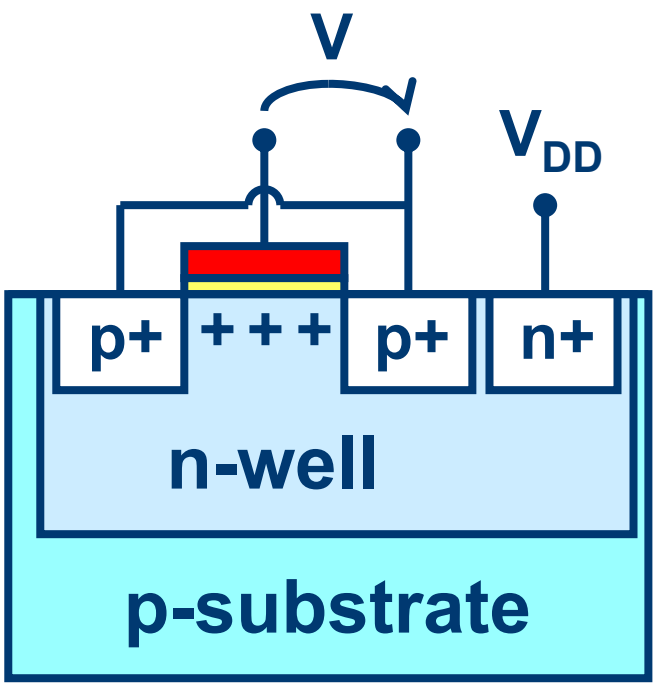


- **Hirad Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 1998, pp. 2035-2041.**
- **R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors", *IEEE JSSC*, vol. 37, no. 3, March 2002, pp. 384-393.**

MOS capacitors

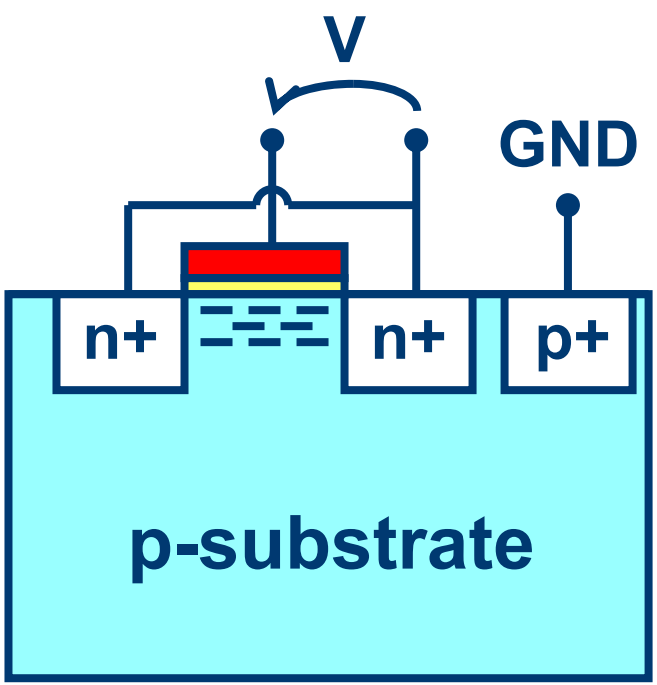
PMOS

Inversion Region



NMOS

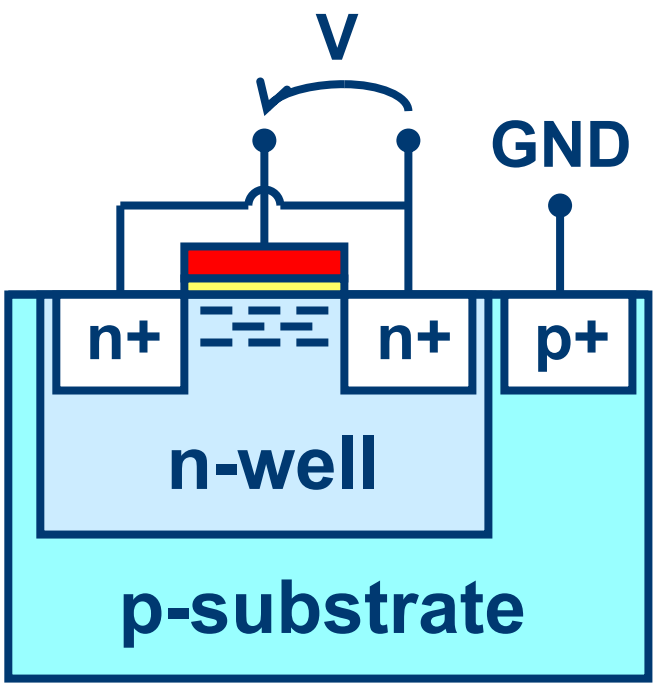
Inversion Region



MOS capacitors

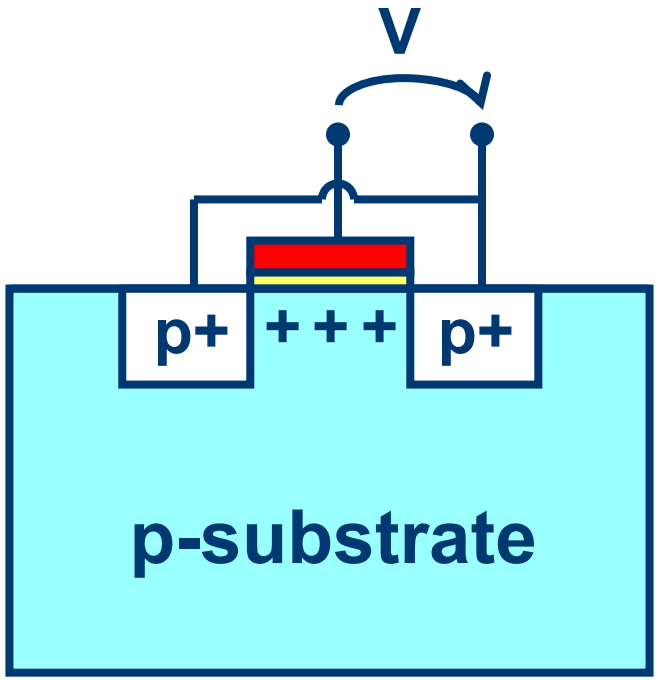
NMOS in an N well

Accumulation Region

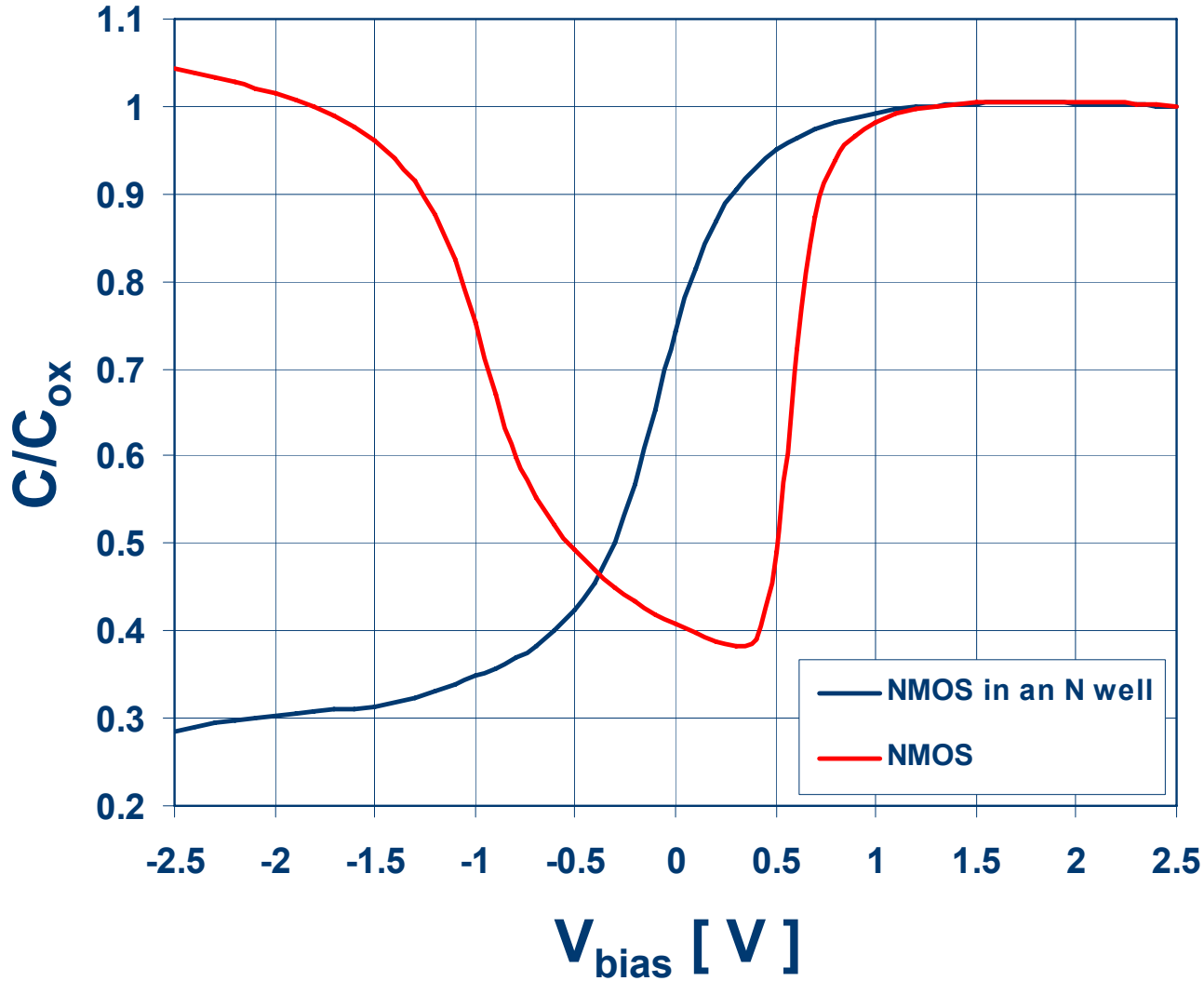


MOS structure

Accumulation Region



C-V characteristics



The NMOS in an N well capacitor is in accumulation for V > 0 V.

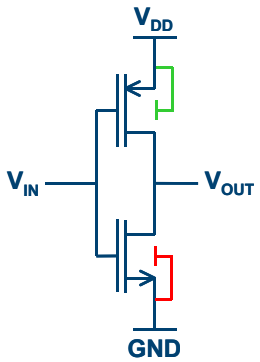
The NMOS capacitor is in inversion for V > 0.

Digital noise in mixed-signal ICs

Integrating analog blocks on the same chip with digital circuits can have some serious implications on the overall performance of the circuit, due to the influence of the "noisy" digital part on the "sensitive" analog part of the chip.

The switching noise originated from the digital circuits can be coupled in the analog part through:

- **The power and ground lines**
- **The parasitic capacitances between interconnection lines**
- **The common substrate**



The substrate noise problem is the most difficult to solve.

- A. Samavedam et al., "A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's", *IEEE JSSC*, vol. 35, no. 6, June 2000, pp. 895-904.
- N. K. Verghese and D. J. Allstot, "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits", *IEEE JSSC*, vol. 33, no. 3, March 1998, pp. 314-323.
- M. Ingels and M. S. J. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC's", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, July 1997, pp. 1136-1141.

Noise reduction techniques

- Quiet the Talker. Examples (if at all possible !!!):
  - Avoid switching large transient supply current
  - Reduce chip I/O driver generated noise
  - Maximize number of chip power pads and use on-chip decoupling
- Isolate the Listener. Examples:
  - Use on-chip shielding
  - Separate chip power connections for noisy and sensitive circuits
  - Other techniques depend on the type of substrate. See next slide
- Close the Listener's ears. Examples:
  - Design for high CMRR and PSRR
  - Use minimum required bandwidth
  - Use differential circuit architectures
  - Pay a lot of attention to the layout

•N. K. Verghese, T. J. Schmerbeck and D. J. Allstot, "Simulations Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits", Kluwer Academic Publishers, Boston, 1994.

Different types of substrates

There are mainly two types of wafers:

1. **Lightly doped wafers: “high” resistivity, in the order of 10 Ω-cm.**

2. **Heavily doped wafers: usually made up by a “low” resitivity bulk (~ 10 mΩ/cm) with a “high” resistivity epitaxial layer on top.**

TSMC, UMC, IBM and STM (below 180 nm) offer type 1

R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits", *IEEE JSSC*, vol. 31, no. 3, 1996, pp. 344-353.

Substrate noise: how to reduce it

To minimize the impact of disturbances coming from the substrate on the sensitive analog blocks, we have mainly three ways:

- **Separate the "noisy" blocks from the "quiet" blocks. This is effective especially in uniform lightly doped substrates. For heavily doped substrates, it is useless to use a separation greater that about 4 times the epitaxial layer thickness.**
- **In n-well processes, p+ guard rings can be used around the different blocks. Unfortunately, this is again effective mainly for lightly doped substrates. Guard rings (both analog and digital) should be biased with separate pins.**
- **The most effective way to reduce substrate noise is to ground the substrate itself in the most "solid" possible way (no inductance between the substrate and ground). This can be done using many ground pins to reduce the inductance, or, even better, having a good contact on the back of the chip (metallization) and gluing the chip with a conductive glue on a solid ground plane.**
- **Separate the ground contact from the substrate contact in the digital logic cells, to avoid to inject the digital switching current directly into the substrate.**

D. K. Su, M. J. Loinaz, S. Masui and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, April 1993, pp. 420-429.

Analog Design

- Electronic Design Automation Tools and Foundry Access
- Analog CMOS Circuit Design
- Packaging, Interconnect and Systems Issues

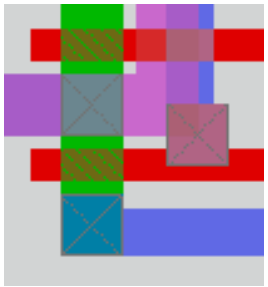
Paul O'Connor, Brookhaven National Laboratory

IEEE Nuclear Sciences Symposium/Medical Imaging Conference

October 30, 2010

Electronic Design Automation (EDA)

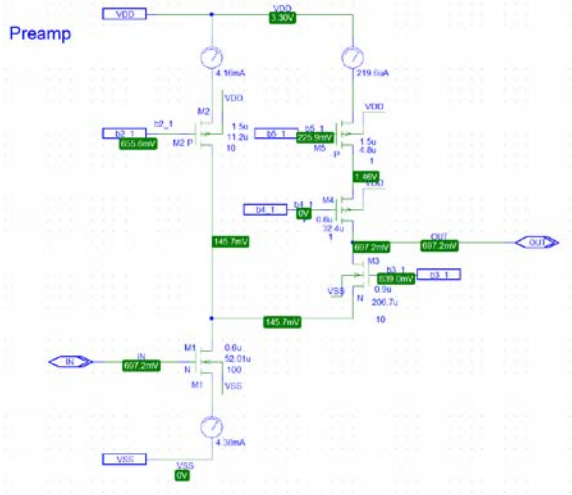
- Commercial: Cadence, Mentor, Synopsys, Tanner
- Public domain: http://www-cad.eecs.berkeley.edu/software.html is a good starting point. See also http://opencircuitdesign.com/magic/ for Magic, a VLSI Layout Editor.



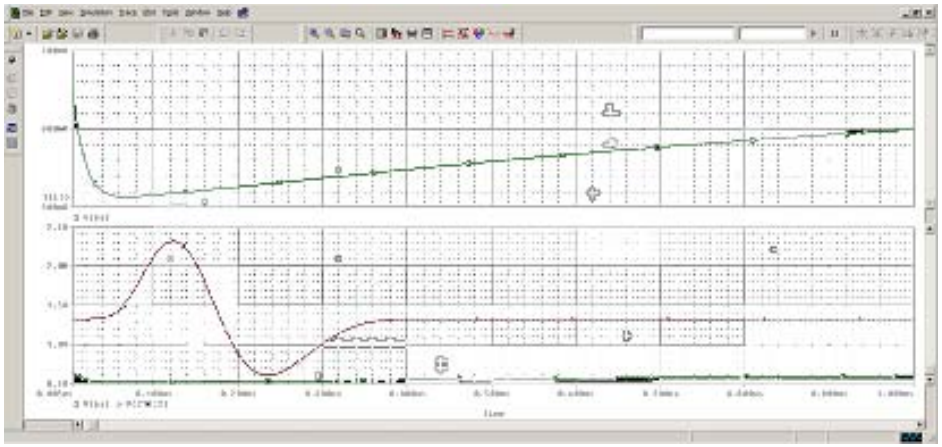
Essential tools for circuit-level design

- Transistor-level circuit simulator
  - *Matrix solution of network equations of your circuit*
  - *PSPICE, HSPICE, SPECTRE are the standards*
  - *inputs: circuit topology, device models, source driving functions*
  - *Outputs:*
  - *DC bias point, source sweep, temperature sweep*
  - *Frequency sweep using linearized model of active devices*
  - *Noise analysis in freq. domain*
  - *Time sweep*
  - *Monte-Carlo facility, samples from user-defined parameter distributions*
- Transistor models
  - *Strike a balance between*
    - Accurate in all transistor operating regions
    - Physics-based
      - Surface-potential based
      - Inversion charge based
    - Computational efficiency
    - Simple parameter extraction methodology
  - *Recent interest in CMOS for high-frequency RF applications and imagers has led to improved analog models*
  - *BSIM, EKV, MOS9 for advanced CMOS*
  - *Usually supplied by foundry*

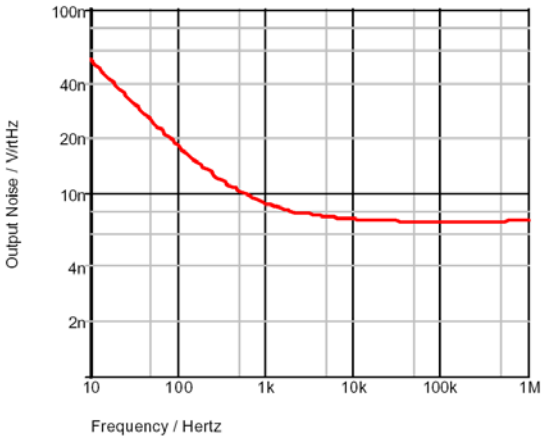
SPICE input & outputs



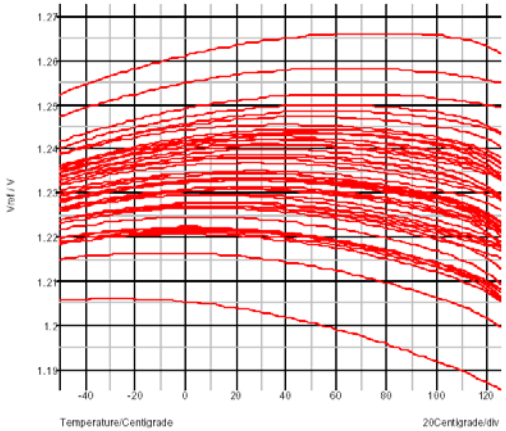
Schematic entry with backannotated node voltages and currents



Transient analysis result: voltages vs. time



Noise analysis: equivalent input noise density vs. frequency



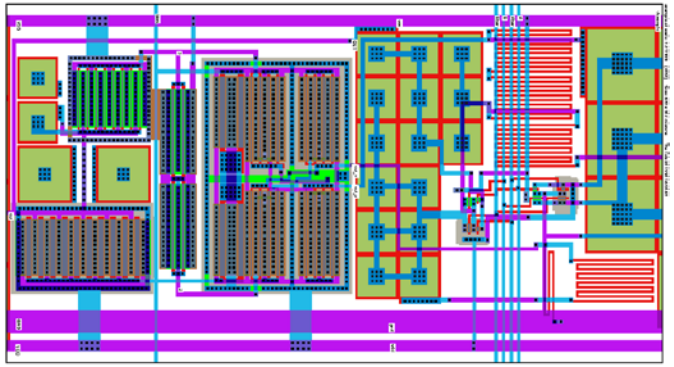
Monte Carlo analysis: node voltage vs. temperature, 50 runs from parameter distribution

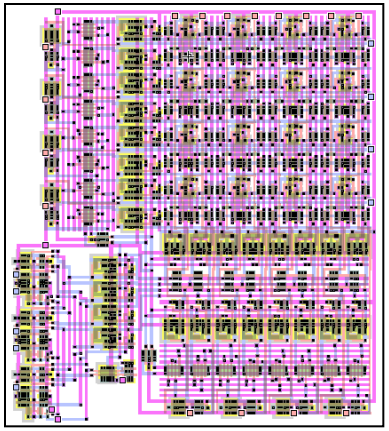
EDA tools for physical design

- Chip layout (full custom, no pre-designed blocks)
  - *Polygon-level mask editor with built-in process knowledge*
- Design rule checker
  - *Checks mask geometry, flags violations of foundry design rules*
- Connectivity verification
  - *Layout-to-schematic network comparison*
- Parasitic extraction
  - *Find capacitance, resistance associated with interconnect lines on chip*

Layout with MAGIC

500μm



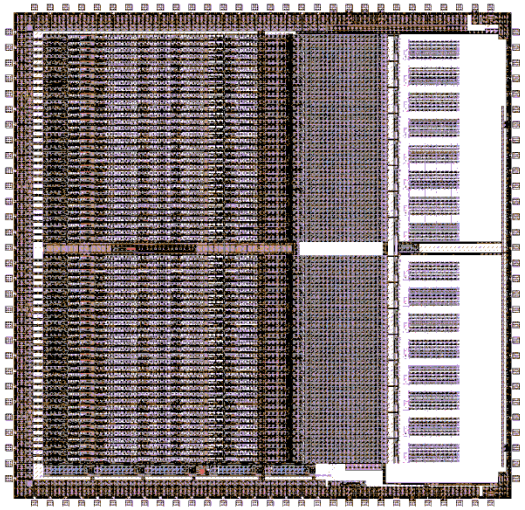


Analog and digital layout, 1.2μm CMOS

```
****** top level cell is ./preampflat.ext
C1 IN 2 5.00932e-13
Cxxnull 2 vss 1.323e-13
M1 BGND IN 1 GND! nch M=48 W=87.6U L=1.2U GEO=3
M2 1 VB1 Vdd Vdd pch M=2 W=42.0U L=3.0U GEO=3
M3 3 VB1 Vdd Vdd pch W=30.0U L=3.0U GEO=3
M4 VSS 2 3 Vdd pch W=12.0U L=1.8U GEO=3
M5 2 BGND 1 Vdd pch M=6 W=83.4U L=1.2U GEO=3
M6 2 VB2 VSS GND! nch W=199.8U L=40.2U GEO=3
M7 VSS VB2 OUT GND! nch M=3 W=199.8U L=40.2U GEO=3
M8 OUT 3 Vdd GND! nch M=24 W=87.6U L=1.2U GEO=3
R1 IN 3 57166.5
C3 9_2072_18# OUT 1.0F
C4 9_226_18# BGND 1.0F
C5 1 VSS 2.3F
C6 BGND IN 8.6F
C7 Vdd 3 3.0F
C8 9_720_18# BGND 1.0F
C9 1 IN 5.3F
C10 BGND Vdd 1.8F
C11 OUT 3 4.2F
C12 Vdd VSS 1.1F
C13 OUT VB2 3.8F
C14 VSS VB2 6.2F
C15 9_1806_18# OUT 1.0F
C16 OUT VSS 2.6F
C17 BGND VSS 4.3F
C18 Vdd VB1 1.1F
C19 1 GND 404.4F
C20 2 GND 79.6F
C21 3 GND 98.5F
C22 9_2072_18# GND 1.0F
C23 VSS GND 439.1F
C24 Vdd GND 447.6F
C25 BGND GND 449.7F
C26 9_226_18# GND 1.0F
C27 9_720_18# GND 1.0F
C28 OUT GND 275.9F
C29 IN GND 149.9F
C30 9_1806_18# GND 1.0F
C31 VB1 GND 23.2F
C32 VB2 GND 96.3F
.END
```

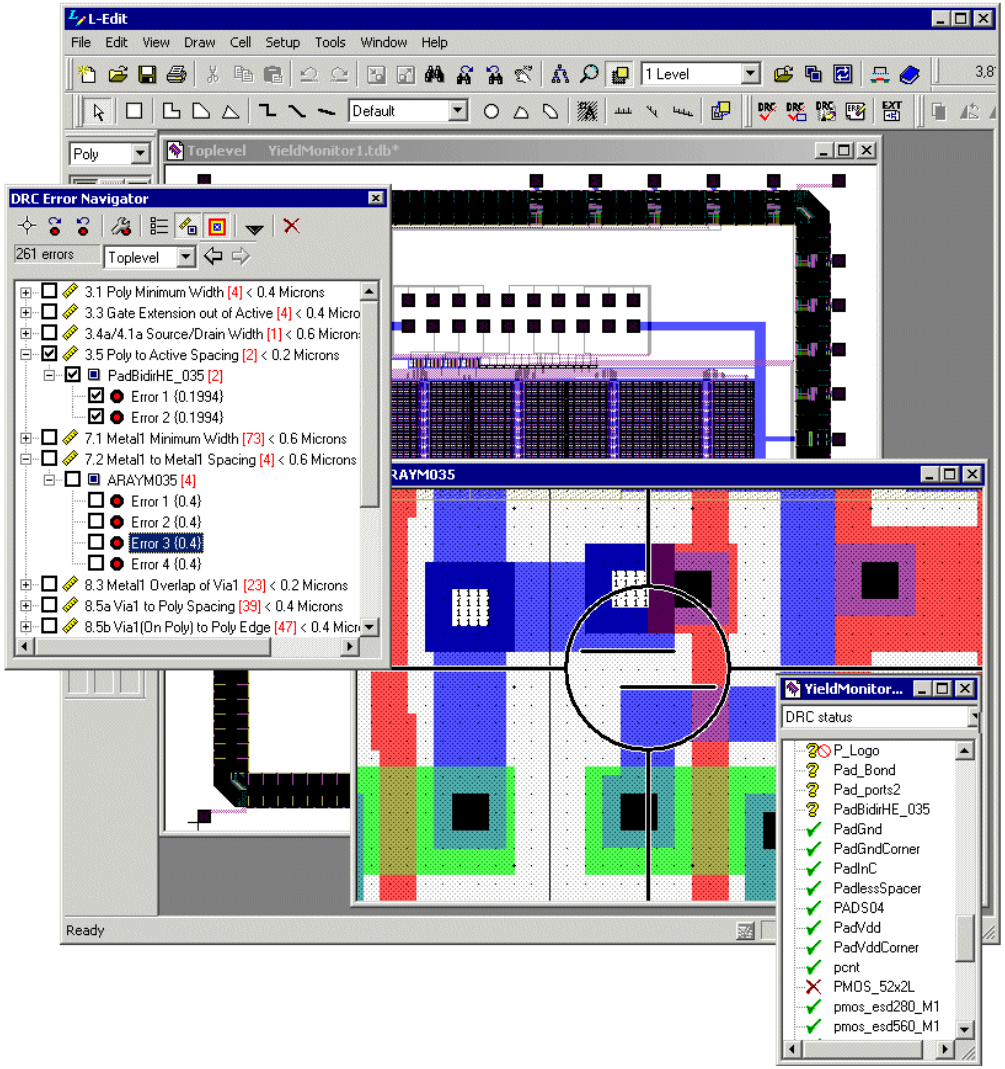
Circuit netlist extracted from layout w/ parasitic capacitances

6 mm



Mixed-signal circuit, 6×10^5 transistors, 0.25μm CMOS

Graphical Design Rule Check



Multiproject services for low-cost prototyping

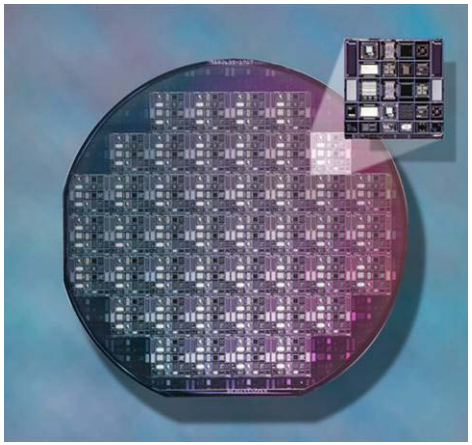
- Organize regularly-scheduled multiproject runs (MPW)
- Collect and merge designs and provide production-compatible masks to foundry
  - *share costs among users*
    - mask-area weighted
- Access to latest production processes from major foundries
  - *CMOS, BiCMOS, SiGe, CIS, (GaAs, InP, MEMS)*
- User support:
  - *design kit*
  - *models*
  - *parametric process data*
    - process control monitor and reference design probed after each MPW run
    - statistical process database
    - quality/yield monitor
  - *access to wafer thinning, dicing, wirebonding, and packaging services*
  - *low-volume production*

Multiproject services

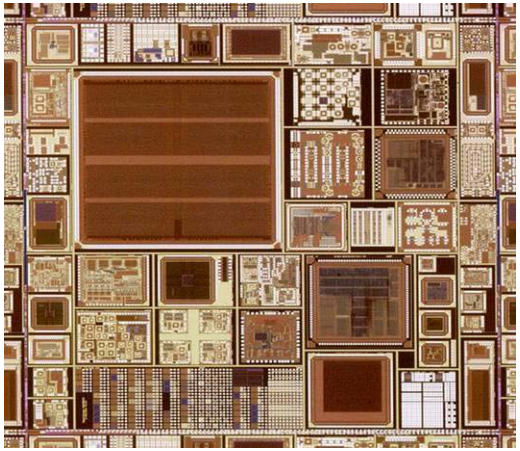
- Multi-foundry:
  - *MOSIS* *www.mosis.org*
  - *Europractice* *www.imec.be/europractice*
  - *Canadian Microelectronics* *www.cmc.ca*
- Foundry-based:
  - *TSMC* *www.tsmc.com*
  - *XFAB* *www.xfab.com*
  - *Austria Microsystems* *www.austriamicrosystems.com*
  - *TowerJazz Semicond.* *www.jazzsemi.com*

MPW examples

wafer



reticle (0.18μm CMOS)



Cost comparison

Process	chip size	lot size	cost
	mm²	no. parts	$K
1.5μm CMOS	5	5	1.1
0.5μm CMOS	5	40	6.5
0.35μm CMOS	15	40	20.7
0.25μm CMOS mixed	25	40	47.3
0.18μm CMOS	50	40	126.8
0.35μm SiGe BiCMOS	50	40	90.0

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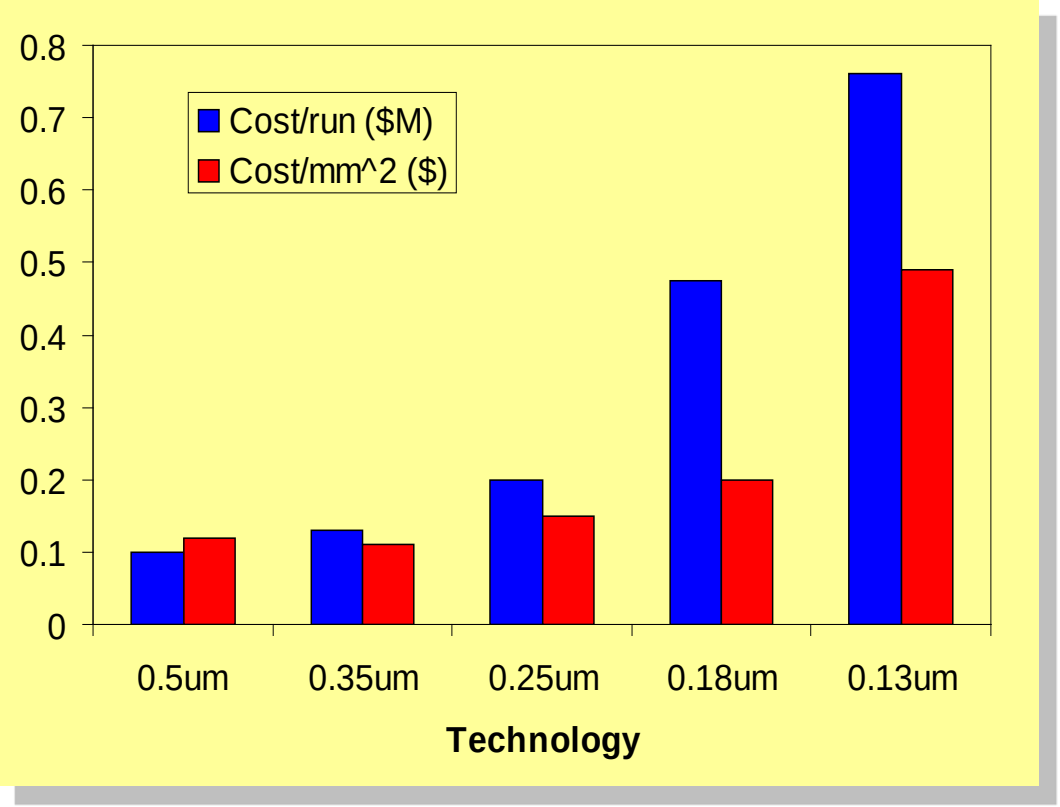
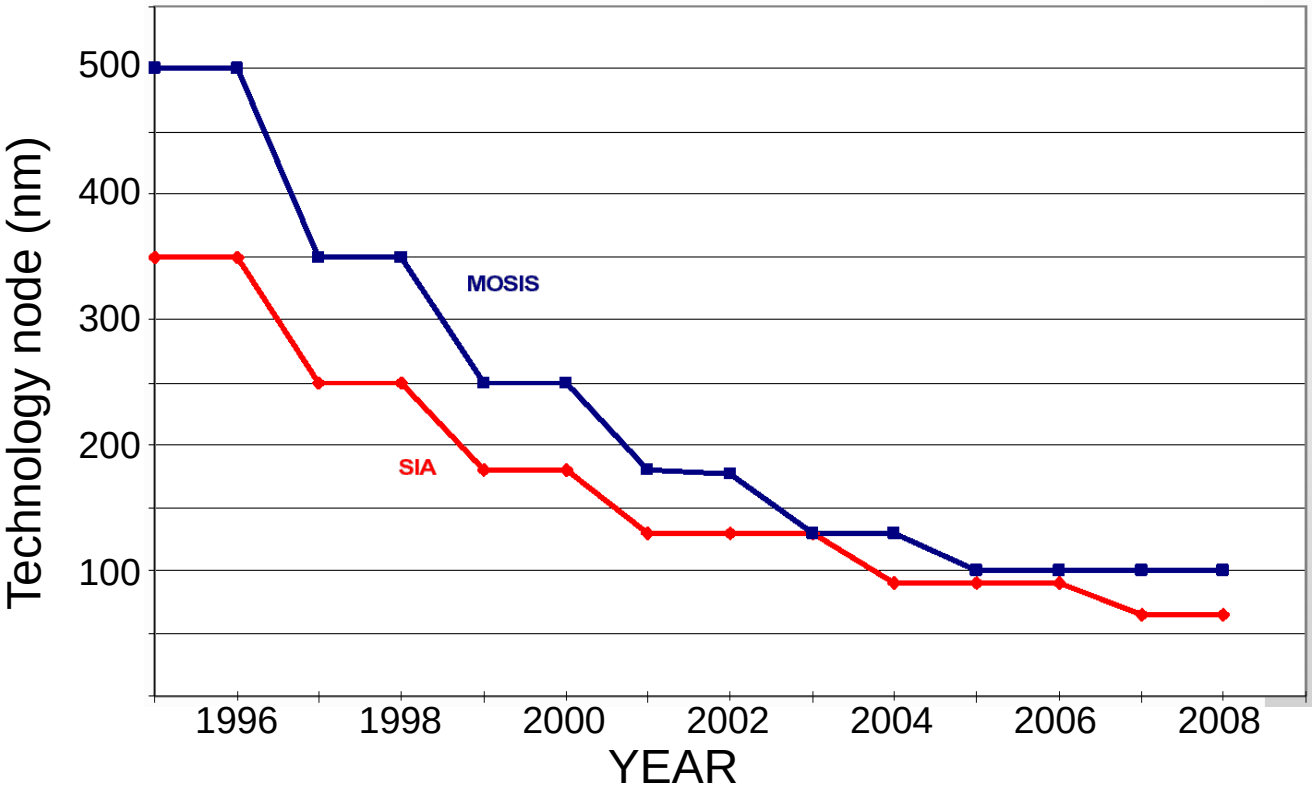
Engineering run costs

Typical engineering run = 20 wafers



Technology introduction roadmap
MOSIS and Semiconductor Industry Association



www.mosis.org
public.itrs.net

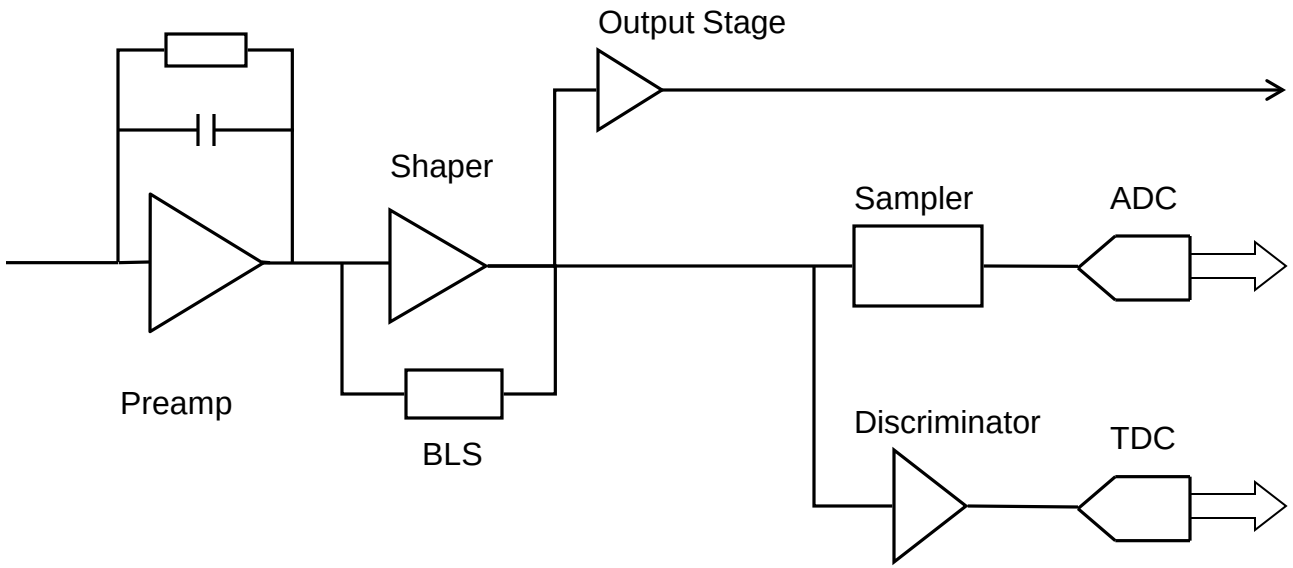
Analog CMOS Circuit Design

Paul O'Connor, Brookhaven National Laboratory

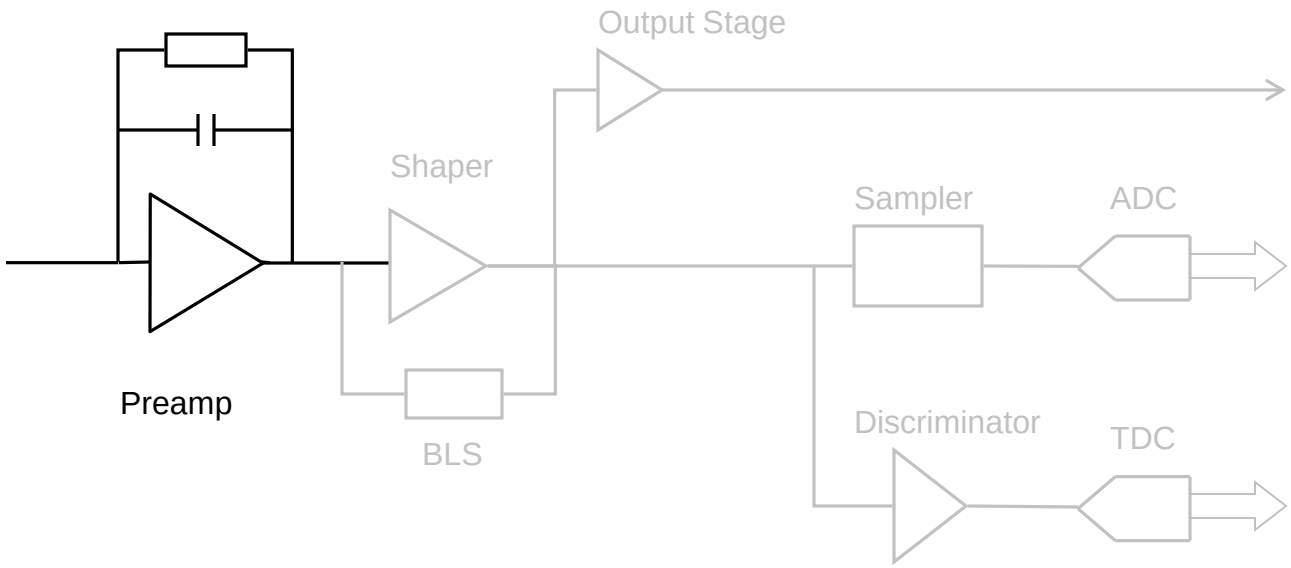
IEEE Nuclear Sciences Symposium/Medical Imaging Conference

October 30, 2010

Signal Chain Block Diagram

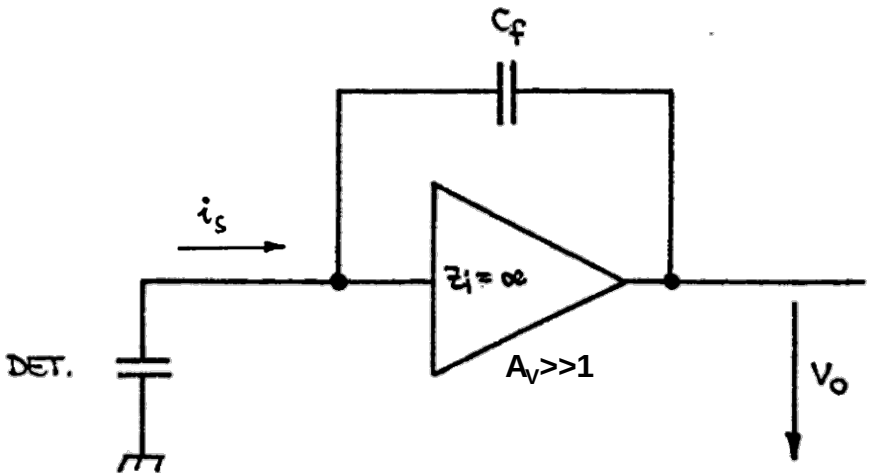


Charge Sensitive Preamplifier



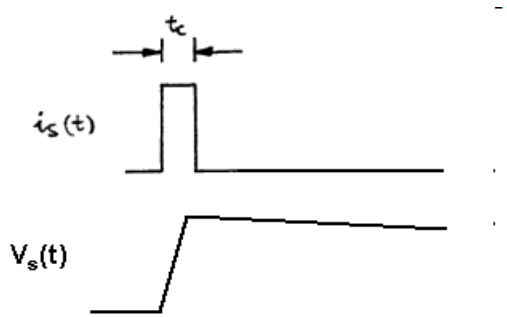
Low noise charge amplification

- Charge sensitive configuration (active integrator)



for $Z_{in}, |A_V| \to \infty$

$$V_s = \frac{\int i_s(t)dt}{C_f} = \frac{Q_s}{C_f}$$

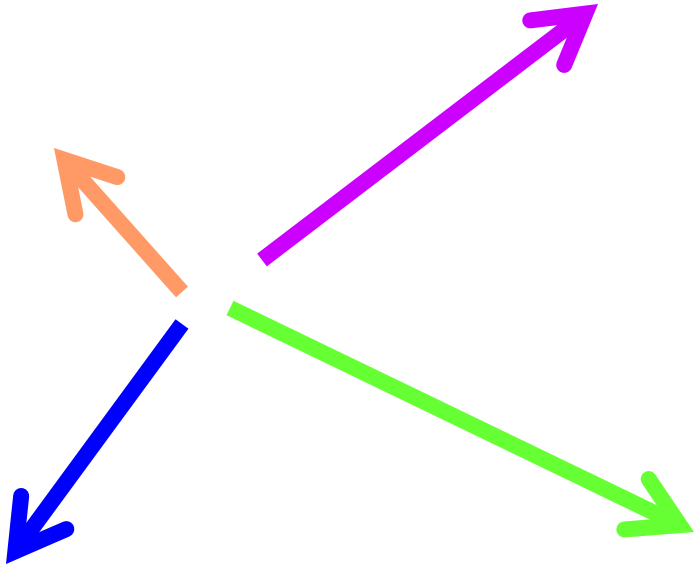


Gain <u>insensitive</u> to C_{det} and A_V

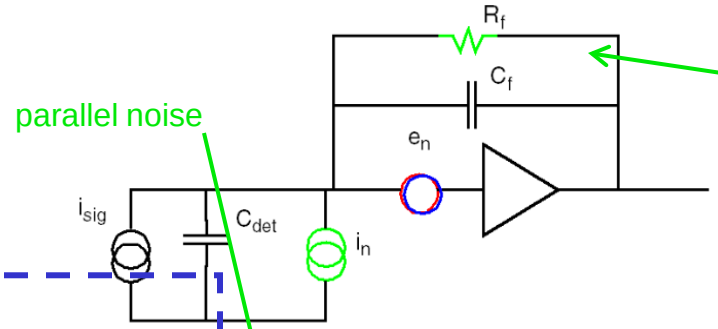
MOS charge amplifier design

- Key parameters:
  - C_{det} , I_{det} , Q_{max} *(detector)*
  - *Rate,* P_{diss} *(system)*
  - f_T , K_F , I_{in} *(technology)*

- Key design decisions
  - *NMOS/PMOS*
  - L_g
  - C_{gs}/C_{det}
  - *Reset system*
  - *Weighting function*



Charge amplifier noise sources



parallel noise

parallel noise

detector

$$C_{tot} = C_{\det} + C_{in}$$

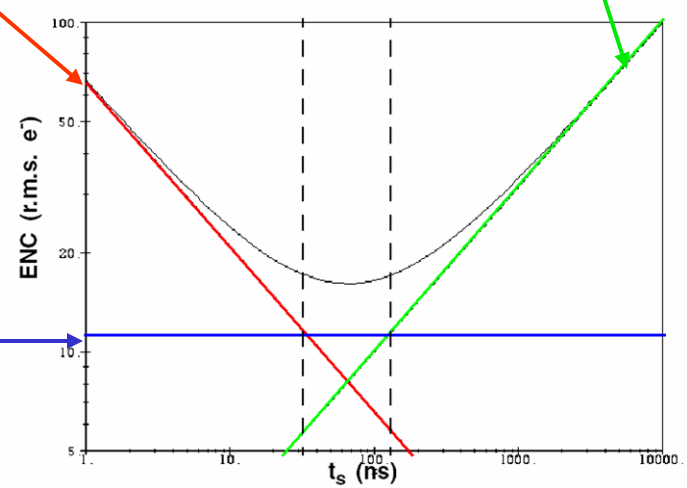
$$ENC^2 = \frac{a_1 e_{nw}^2 C_{tot}^2}{\tau} + a_2 K_F C_{tot}^2 + a_3 i_n^2 \tau$$

series white noise

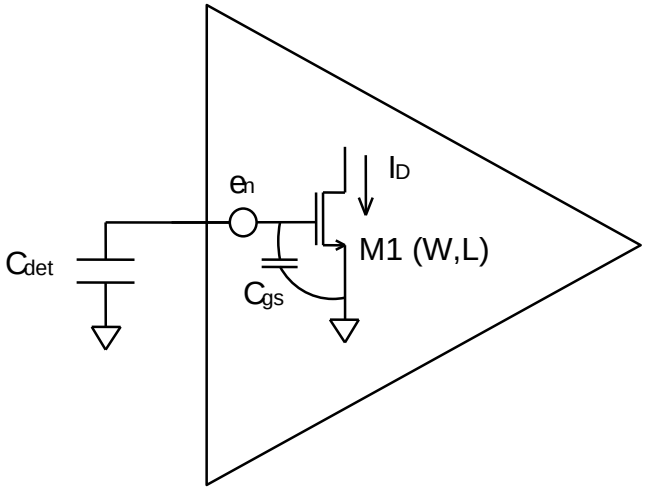
$$e_{nw}^2 = 4kTR_s \qquad i_n^2 = \frac{4kT}{R_f} + 2qI_{leak}$$

series 1/f noise

Shaping time dependence



Dimensioning the input MOSFET for minimum noise



$$ENC^2 = \left(C_{det} + C_{gs}\right)^2 \cdot \left(\frac{4kT\gamma}{g_m \cdot t_m} + \frac{K_F}{C_{gs}}\right)$$

white 1/f

Choose minimum L for best g_m/C_{gs} ratio

Increasing M1 width makes e_n smaller while C_{gs} gets larger

$\Rightarrow$ ***optimum width for M1 must exist***

1/f noise:

$$C_{gs,opt} = C_{det}$$

White -- two cases :

I. Fixed V_{gs} (fixed current density, fixed f_T)

$$g_m \propto C_{gs}$$

$$C_{gs,opt} = C_{det}$$

II. Fixed I_D (practical case)

$$g_m \propto C_{gs}^{1/2} \text{ [strong inversion]}$$

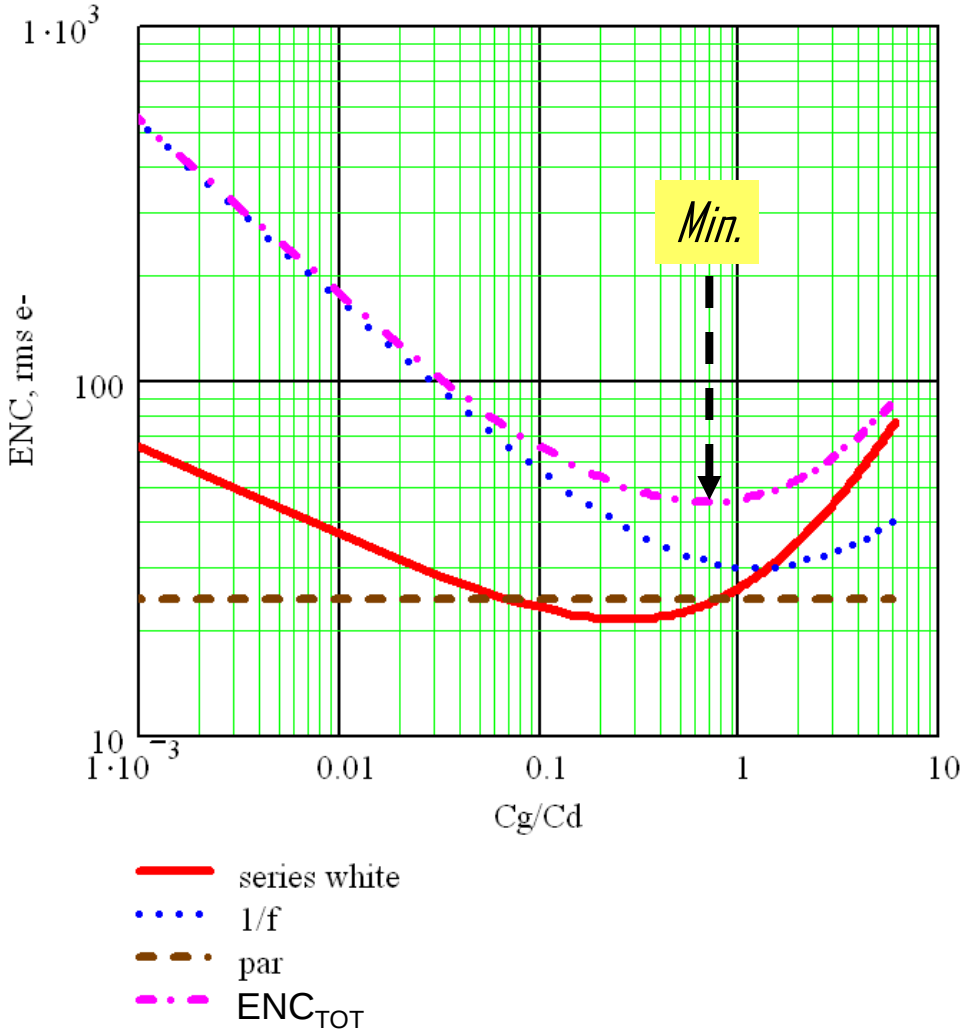
$$C_{gs,opt} = C_{det}/3$$

P. O'Connor, G. De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", NIM A480 (2002), 713 - 725

Composite noise

- C_{det} = 3 pF
- t_p = 0.5 μs
- P_{diss} = 1 mW
- I_{leak} = 100 pA
- Technology: 0.35 μm NMOS

- *Optimum width for series noise is a compromise between white and 1/f components*



Optimizing the input MOSFET using advanced models

Series noise "capacitive match" problem:

$$ENC^2 = ENC_{sw}^2 + ENC_f^2$$

$$ENC_{sw}^2 = \frac{a_1}{2\tau_p} e_{n,sw}^2 (C_d + C_{in})^2$$

$$e_{n,sw}^2 = \frac{4kTn\gamma}{g_m}$$

$$ENC_f^2 = a_2 \pi \frac{K_F}{C_{ox} WL} (C_d + C_{in})^2$$

γ and g_m depend on region of operation:

	γ	g_m
weak	1/2	qI_D / nkT
strong	2/3	$\sqrt{2\mu C_{ox} \frac{W}{L} I_D}$

How to handle moderate inversion?

G.De Geronimo, P.O'Connor , V. Radeka and B. Yu, "Front-end electronics for imaging detectors", *Nuclear Instrum. Methods* A471 (2001) 192-199

P. O'Connor and G.De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", *Nuclear Instrum. Methods* A484 (2002) 713-725

L. Fabris, P. Manfredi, "Optimization of front-end design in imaging and spectrometry applications with room temperature semiconductor detectors", *IEEE Trans Nucl. Sci*., 49 (4) ,1978 –1985, Aug. 2002

M. Manghisoni, L. Ratti, V. Re, and V. Speziali, "Submicron CMOS Technologies for Low-Noise Analog Front-End Circuits", *IEEE Trans. Nucl. Sci.* 49,1783-1790, Aug. 2002

Simplified EKV model for hand calculations

- substrate-referenced compact MOS model
- small, physics-based parameter set
- continuous modeling of weak to strong inversion
- simple set of equations valid for saturation:

Inversion coefficient $i = I_D / I_0$

$$I_0 = 2n\beta \cdot U_T^2 \qquad \beta = \mu \cdot C_{ox} \frac{W}{L} \qquad U_T = \frac{kT}{q}$$

Interpolation function :

$$f(i) = \frac{1}{2}\left(\sqrt{1+4i}+1\right)$$

$$\frac{g_m}{I_D} = \frac{1}{n \cdot U_T} \frac{1}{f(i)}$$

$$\frac{C_{GS}}{WLC_{ox}} = \frac{1}{\frac{3}{2} + \frac{f(i)}{i}}$$

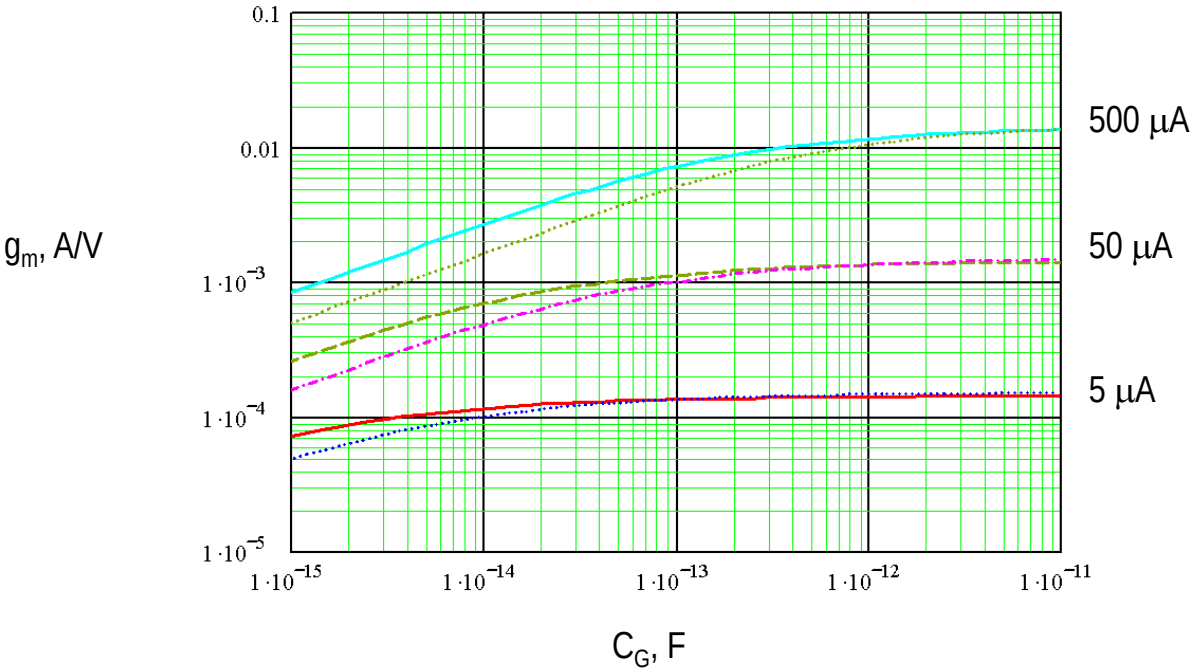
$$\frac{S_{th}}{4kTng_m} = \frac{\frac{1}{2} + \frac{2}{3}i}{1+i} \equiv \gamma$$

short-channel effects not modeled

C. Enz, F. Krummenacher, E. Vittoz, “An Analytical MOS Transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications”, *Analog Integrated Circuits and Signal Processing* 8, 83-114 (June 1995)

g_m vs. C_G vs. scaling

L := .18μ



NMOS (upper) PMOS (lower)

Strong inversion:

$g_m \sim \sqrt{C_G}$

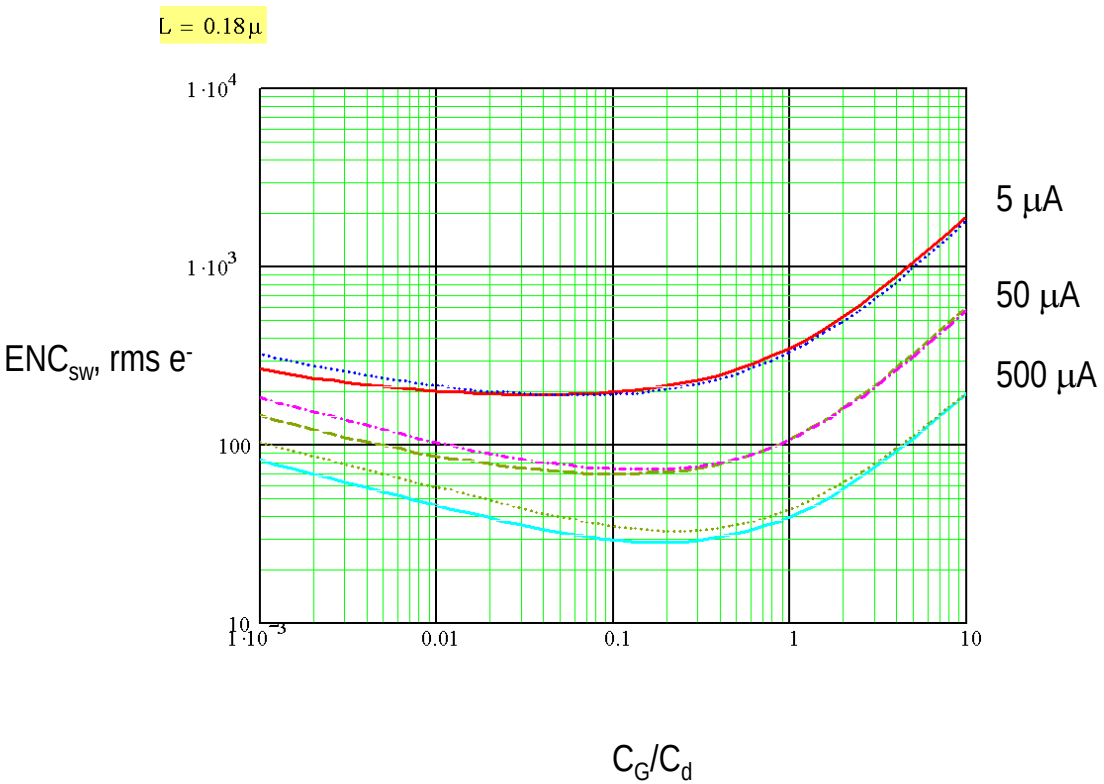
$g_{m,n} \sim 3g_{m,p}$

Weak inversion:

$g_m \sim const.$

$g_{m,n} = g_{m,p}$

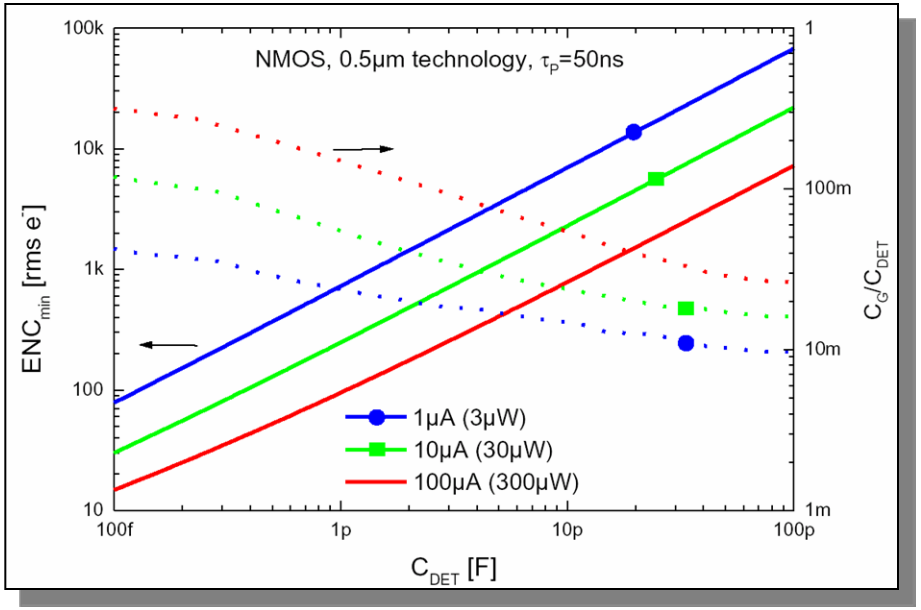
White series noise vs. C_G/C_d vs. scaling



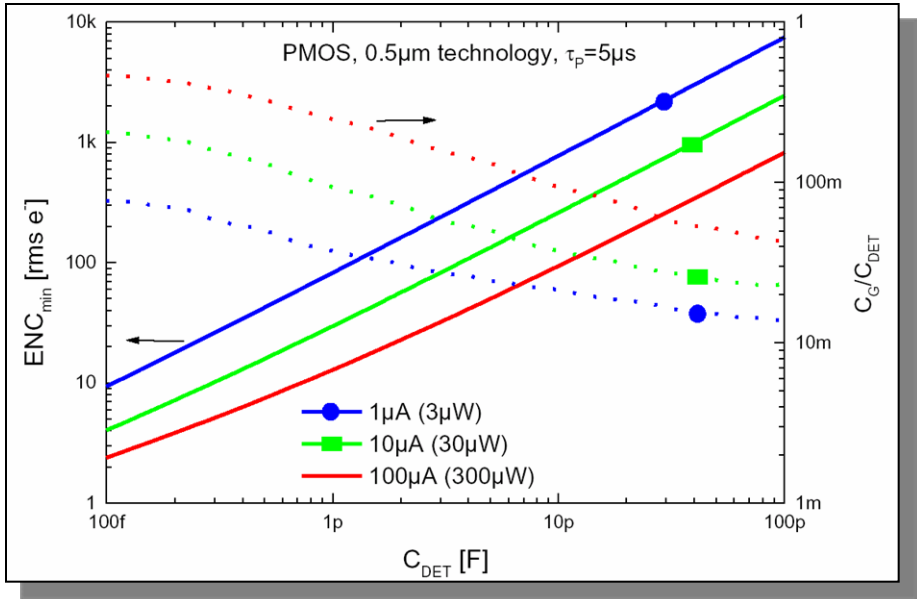
NMOS (upper) PMOS (lower)

White series ENC, $C_{G,opt}/C_{DET}$ vs. C_{DET}

NMOS



PMOS



For fixed power budget,

$$ENC \propto \begin{cases} C_{DET}, \text{ weak inversion} \\ C_{DET}^{3/4}, \text{ strong inversion} \end{cases}$$

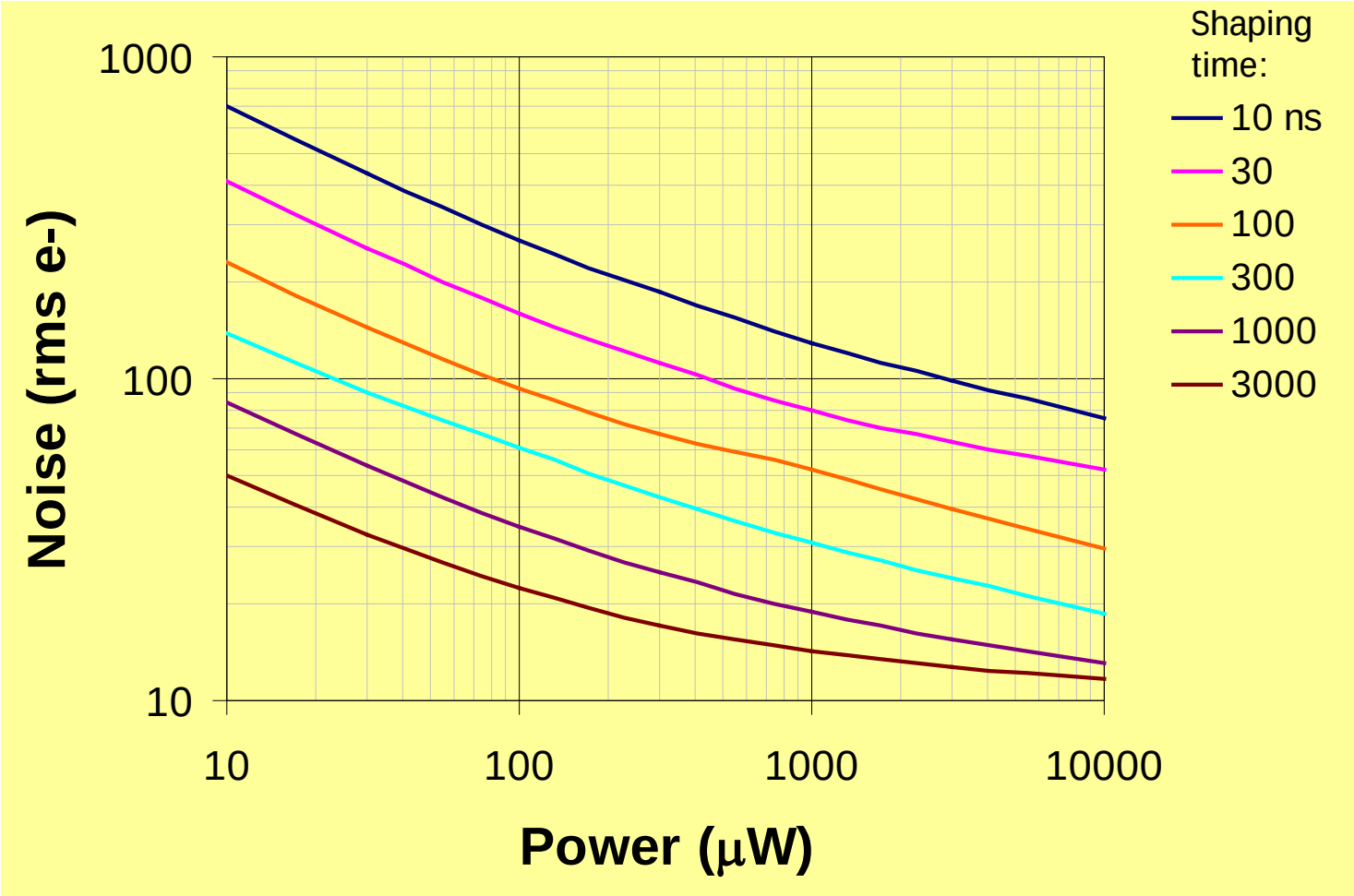
Power allowed to scale with C_{DET}:

$$ENC \propto C_{DET}^{1/2}$$

De Geronimo et al. , NIM A 471 (2001) 192 - 199

Optimized noise vs. power

(MOSFET optimized at each power level and shaping time)

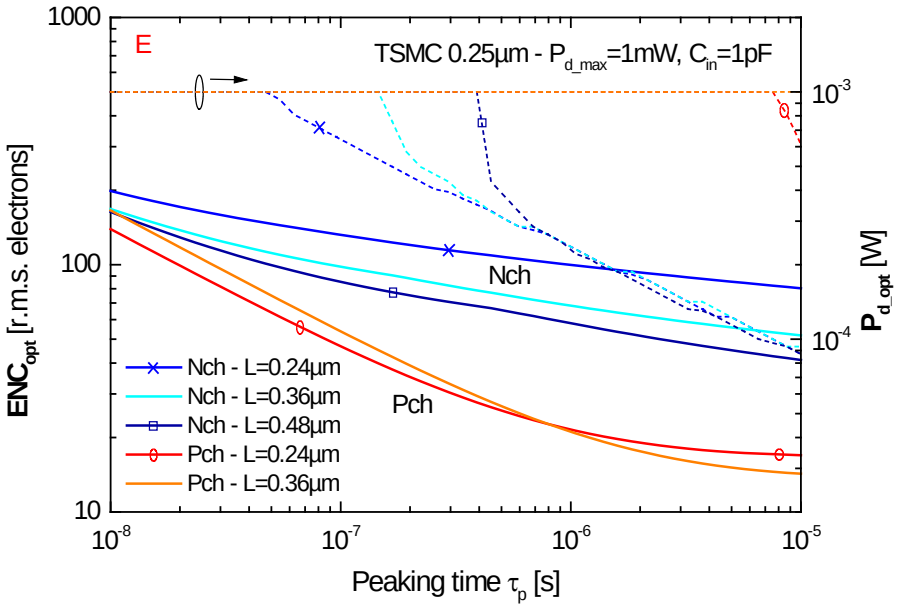


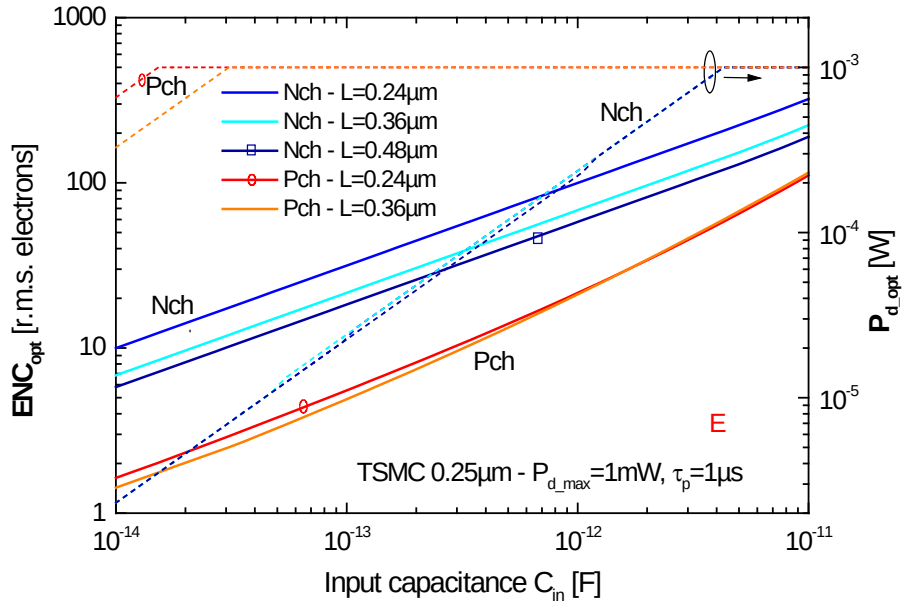
Note:

$$\left|\frac{dN}{dP}\right| \leq 0.4$$

Cd = 1pF
0.25 μm CMOS

0.25μm CMOS optimized noise/power





Enhanced noise model incorporates:

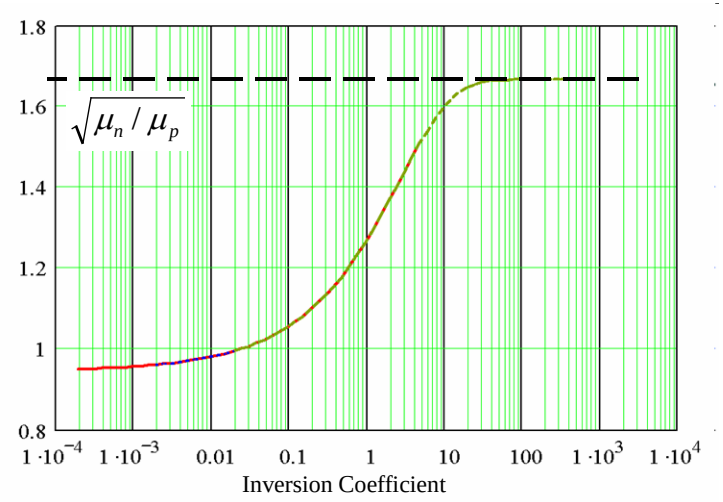
- *Gate capacitance bias dependence*
- *Gate-source and gate-drain overlap capacitance*
- *Length-dependent 1/f noise coefficient*
- *$1/f^{\alpha}$ behavior of low-frequency noise*

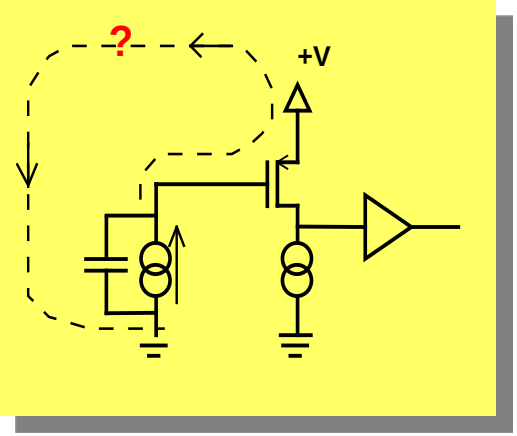
G. De Geronimo, P. O'Connor, to be published in IEEE Trans. Nuc. Sci.

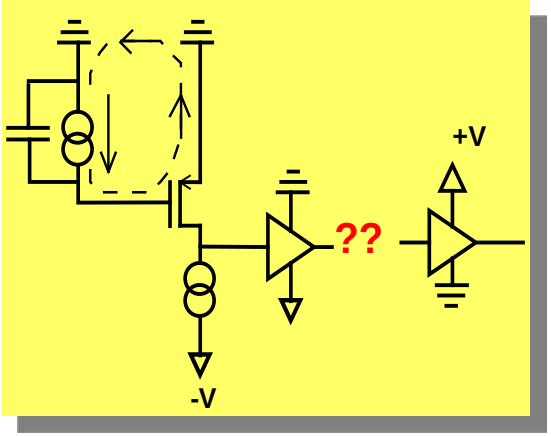
Choice of PMOS vs. NMOS

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse* V_{BS} *to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin* t_{ox}
- *Single-supply operation of PMOS-input preamp awkward:*

g_{mn}/g_{mp} vs IC







Minimum series noise

- Input MOSFET fully optimized:

$$ENC_{sw,opt} \approx \sqrt{kTC_{\det}}\sqrt{\frac{\tau_{el}}{t_m}}$$

$$ENC_{1/f,opt} \approx \sqrt{K_F C_{\det}}$$

τ_{el} = electron transit time under the gate $= C_{gs} / g_m$

- Key ingredients for low series ENC:
  - *low* C_{det}
  - *long* t_m
  - *short* τ_{el}
  - *low* K_F

Gate resistance noise

- Polysilicon gate is resistive:
  - ρ_{poly} **25 Ω/sq.**
  - $\rho_{silicided\ poly}$ **4 Ω/sq.**

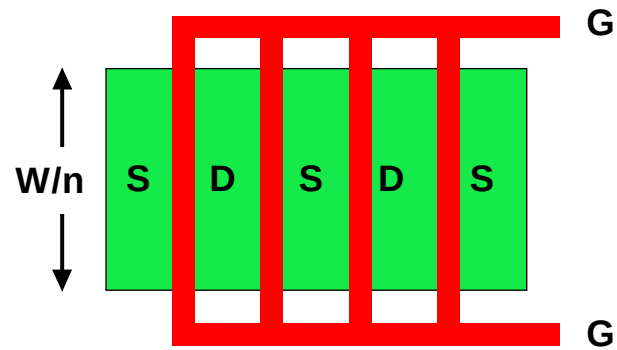
resistance of non-interdigitated gate:

$$R_g = \rho_{poly} \cdot \frac{W}{L}$$

series noise due to gate resistance:

$$e_{ng}^2 = 4kT \cdot R_{eq}$$

FET with interdigitated layout



n gate fingers
n = 4

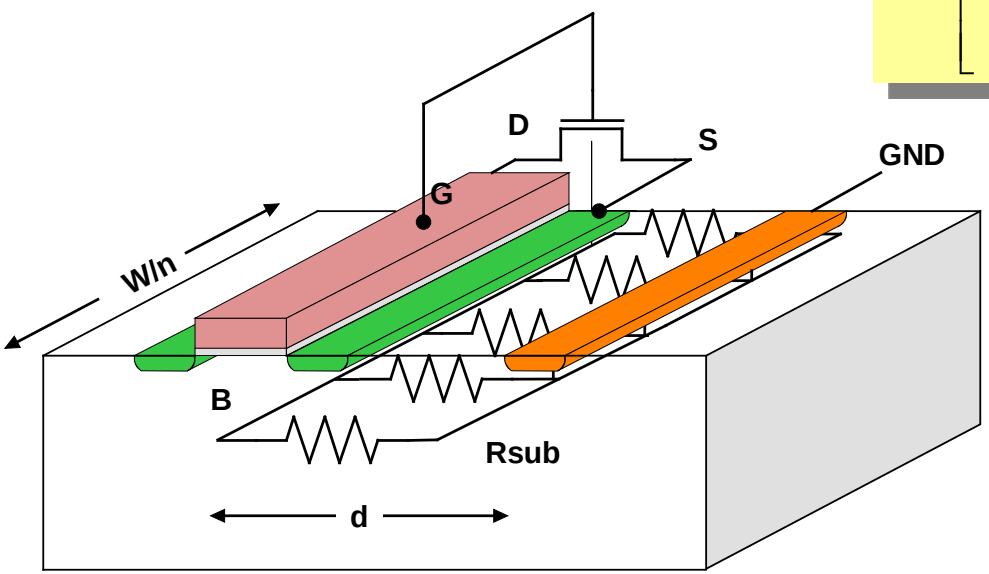
Layout	Req driven one end	Req driven both ends
Single finger	Rg/3	Rg/12
Interdigitated n fingers	$Rg/3n^2$	$Rg/12n^2$

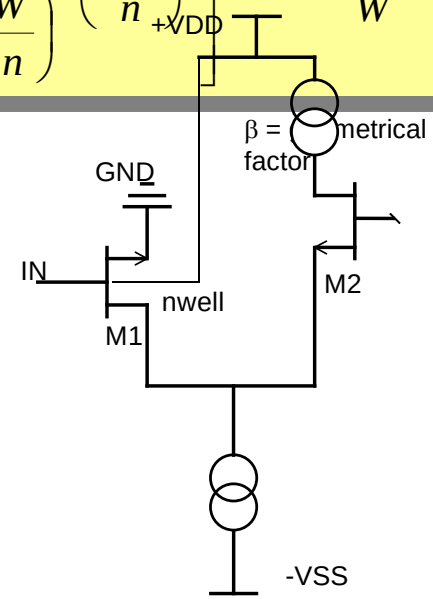
Bulk resistance noise

- Resistive substrate couples to the channel via the back transconductance g_{mb}.
- Substrate resistance is distributed.

leads to noise in the channel:

$$i_{db}^2 = \left[4kT \cdot n \cdot \beta \frac{d}{\left(\frac{W}{n}\right)} \cdot \left(\frac{g_{mb}}{n}\right)^2 \right] = 4kT\beta \frac{d}{W} g_{mb}^2$$



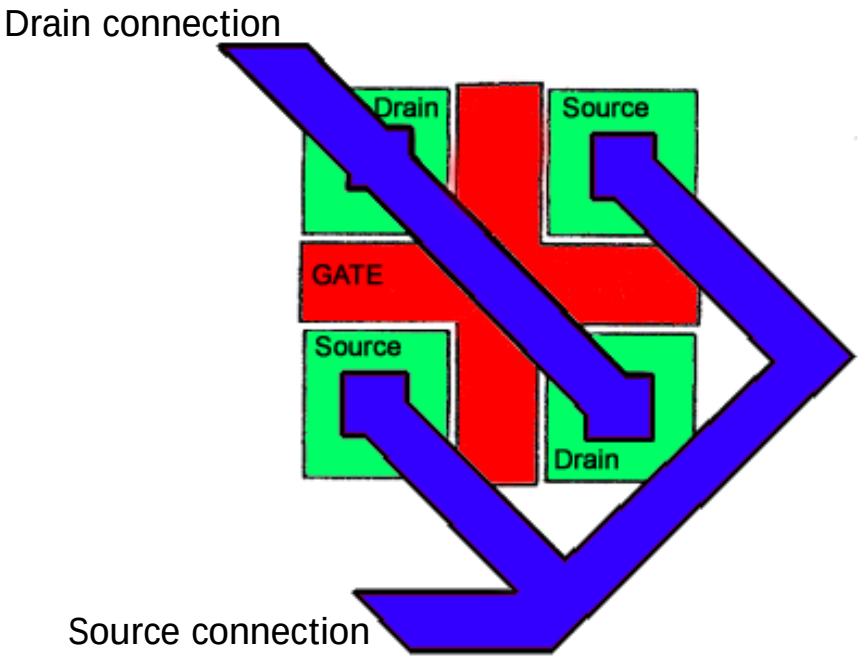


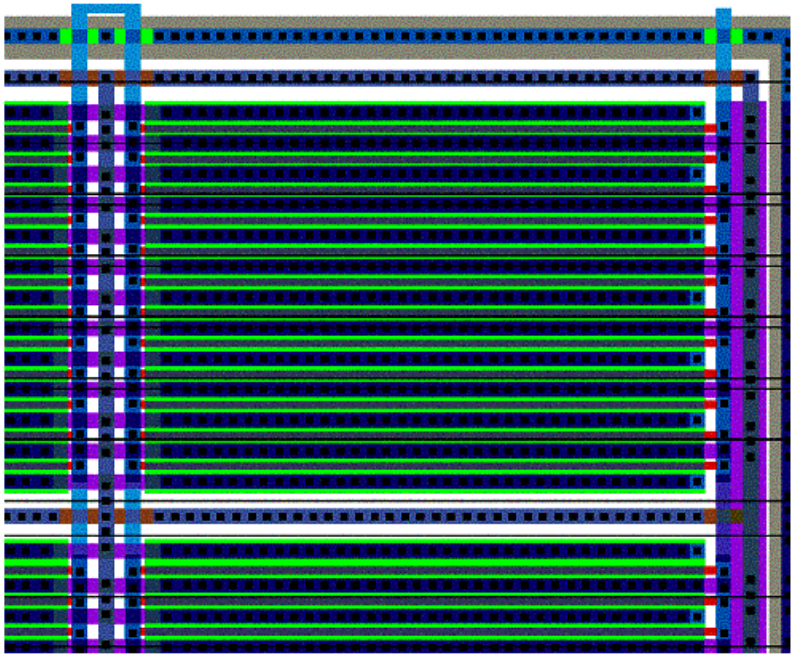
- Minimize by reverse biasing the source-substrate junction.

Layout techniques to reduce gate and bulk resistance noise

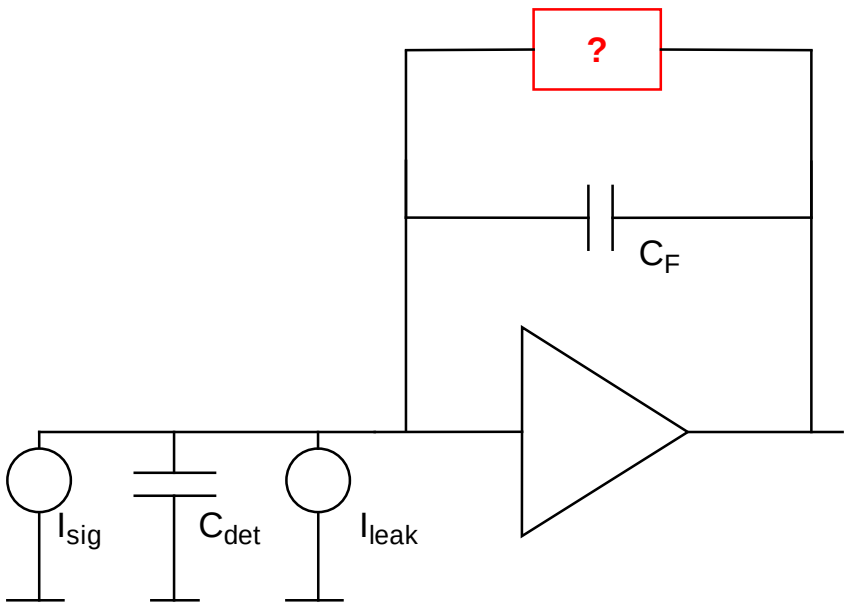
Waffle iron layout

Substrate contacts, guard ring, multiple gate fingers contacted both ends



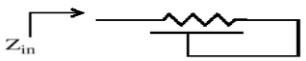


Preamp reset – requirements



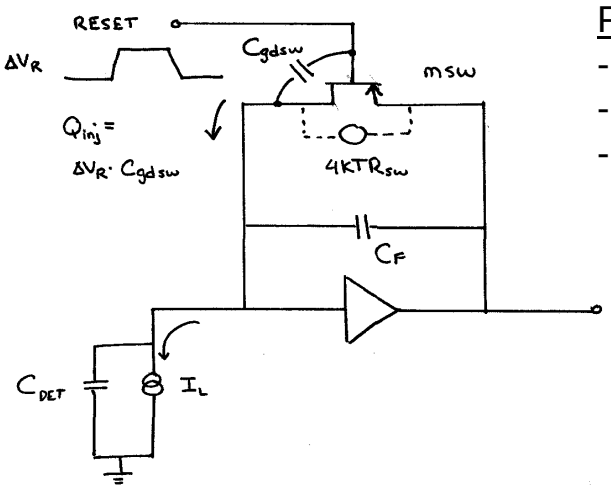
- all charge preamplifiers need DC feedback element to discharge the input node and stabilize the bias point
- usually, a resistor in the MΩ – GΩ range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - *insensitive to process, temperature, and supply variation*
  - *low capacitance*
  - *lowest possible noise*
  - *linear*

Preamplifier reset – monolithic techniques (1)



$$i_n^2 = \frac{4kT}{Re\{Z_{in}\}}$$

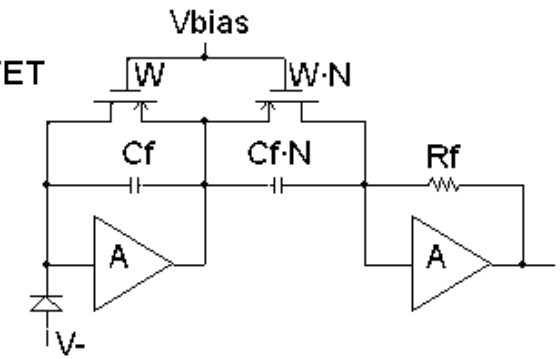
Physical resistor
- always accompanied by parasitic capacitance
- de-stabilizes circuit and increases noise
- noise higher than 4kT/R by factor ~ RC/t_m



Pulsed reset by MOS switch
- sampled noise $\sqrt{kTC_F}$
- Q_{inj} noise from switch control voltage
- leakage current integrates on output node $dV_{out}/dt = I_L/C_F$

Preamplifier reset – monolithic techniques (2)

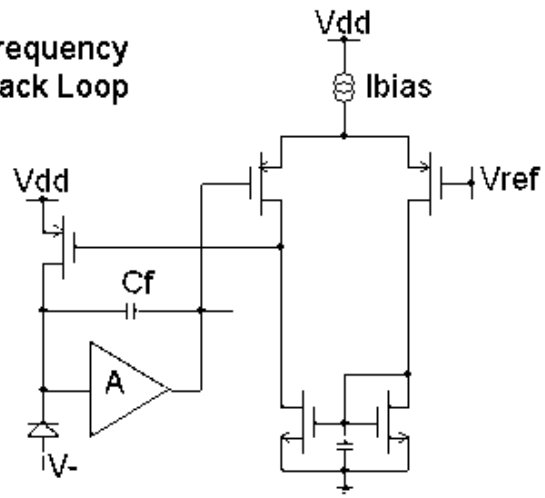
Single MOSFET



O'Connor et al., TNS v44 n3 (1997)
De Geronimo et al., NIM A421 (1999)
De Geronimo et al., TNS v47 n4 (2000)

- provides effective current gain -N
- full compensation (high linearity)
- minimum noise (thermal)
- requires baseline stabilization
- can be realized in multiple stages

Low Frequency Feedback Loop

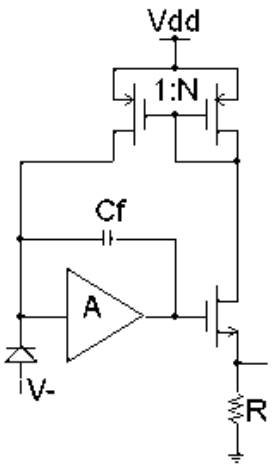


Krummenacher, NIM A350 (1991)
Ludewigt et al., TNS v41 n4, (1994)
Vandenbussche et al., TNS v45, n4 (1998)
Manfredi et al., Nucl.Phys.B 61B, Proc.Suppl. (1998)

- noise can be high
- requires baseline stabilization at high rates
- compensation an issue

Preamplifier reset – monolithic techniques (3)

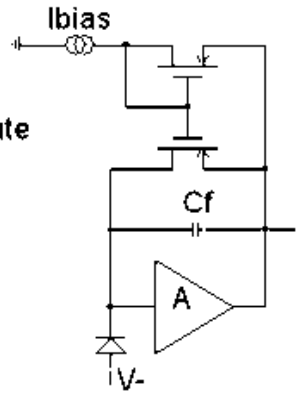
R-Scaling



Santiard et al., CERN-ECP/94-17 (1994)
Chase et al., NIM A409 (1998)
Sampietro et al., Elec.Lett. v34 n19 (1998)

- noise can be high (large values of R and N required)
- linearity an issue
- parasitic capacitor an issue
- compensation available in some configuraitions
- requires baseline stabilization

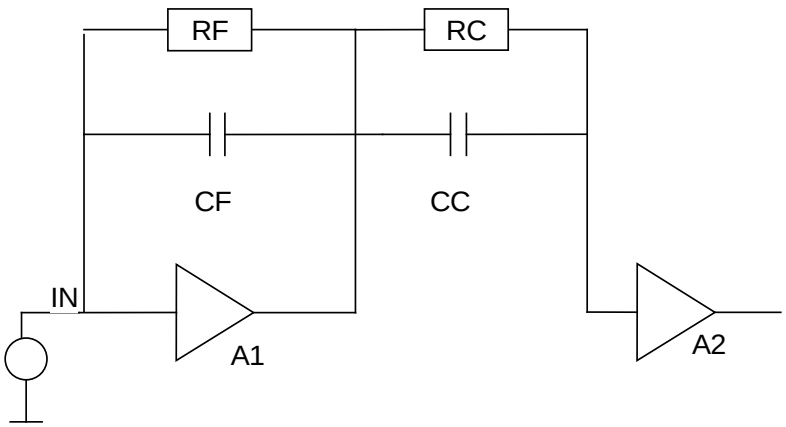
Slew-rate Limited



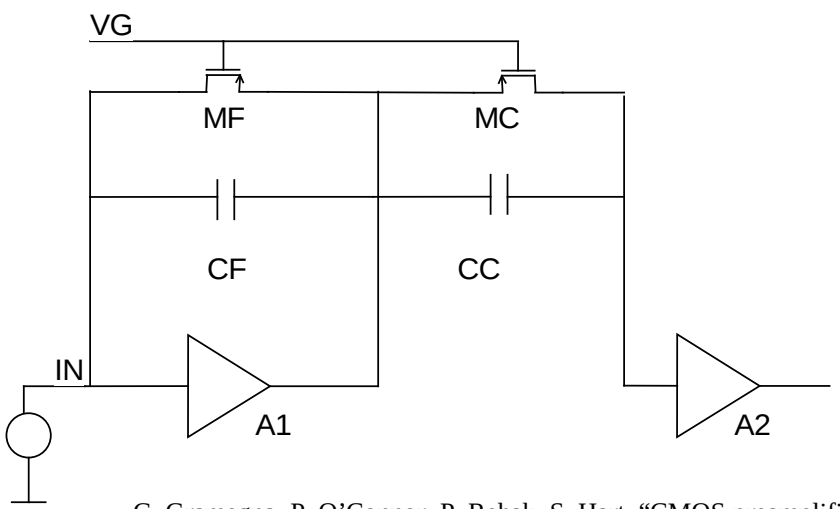
Blanquart et al., NIM A395 (1997)
Blanquart et al., NIM A439 (2000)

- MOSFET operates in saturation only when there is signal activity
- noise can be high (it requires Ibias > Idet)
- parasitic capacitor an issue
- suitable for Time-Over-Threshold processing techniques
- requires baseline stabilization at high rates
- linearity an issue
- compensation an issue

Nonlinear pole-zero compensation



- Classical
  - *RF · CF = RC ·CC*
  - *Zero created by RC,CC cancels pole formed by RF, CF*

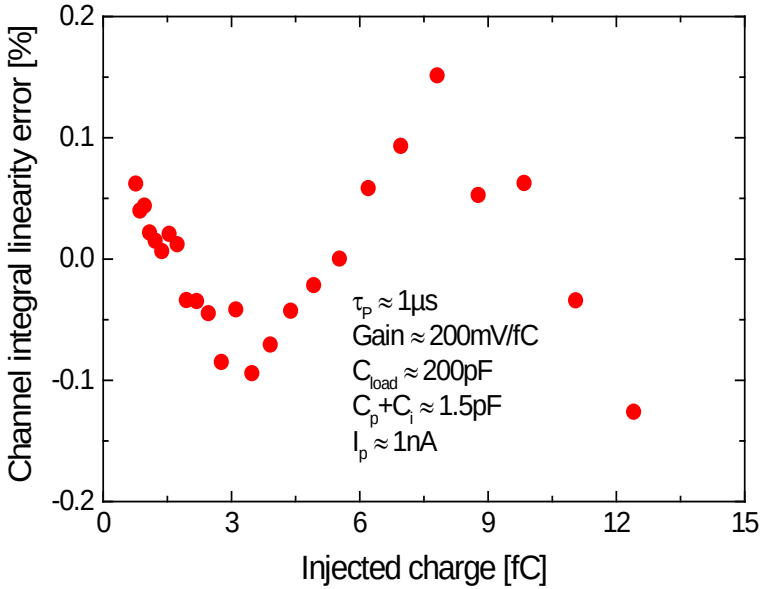


- IC Version
  - *CC = N · CF*
  - *$(W/L)_{MC} = N \cdot (W/L)_{MF}$*
  - *Zero created by MC, CC cancels pole formed by MF, CF*
  - *Rely on good matching characteristics of CMOS FETs and capacitors*

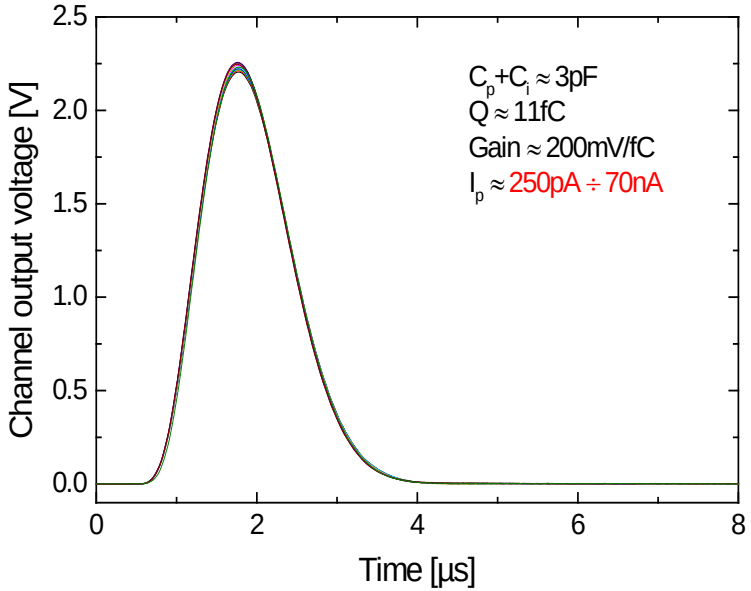
G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

Preamp reset with nonlinear PZ compensation – experimental results

linearity



output vs pixel leakage current

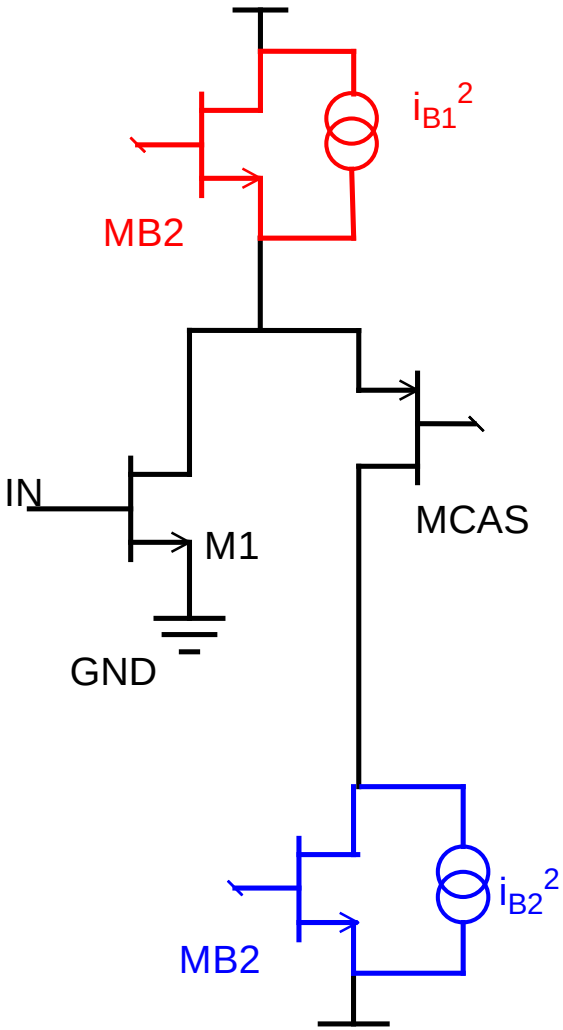


Compensated reset system

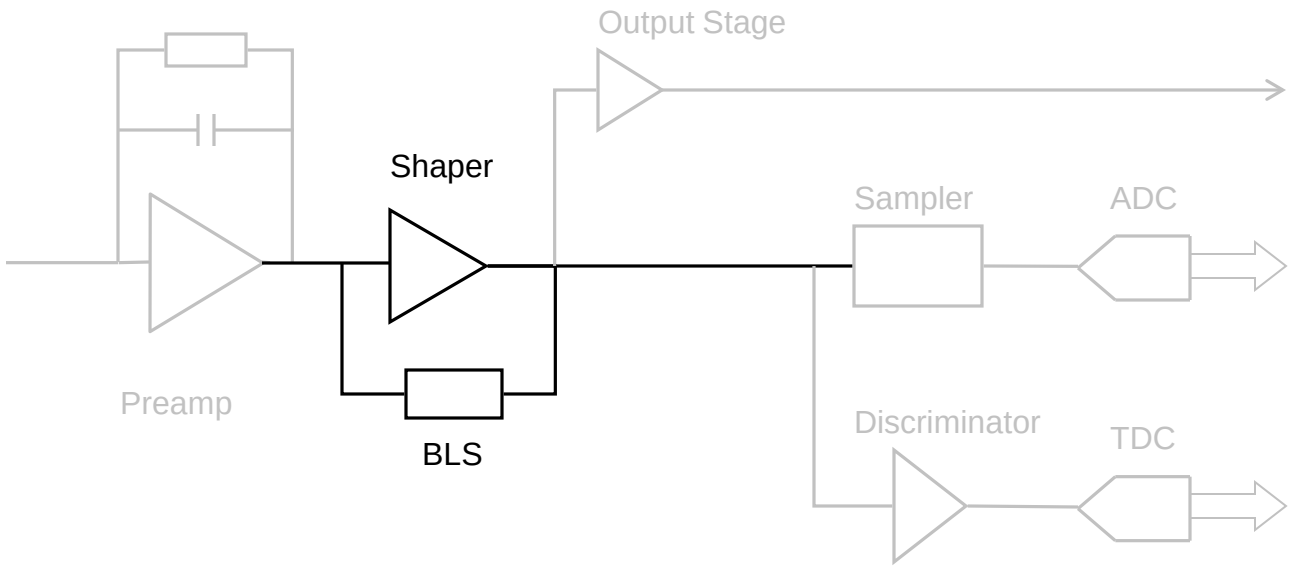
- Advantages:
  - *near theoretical noise contribution*
  - *accepts detector leakage current over wide range*
    - allows DC coupling of detector to preamp
  - *compensate the parasitic preamp feedback pole with a precisely matched zero*
    - allows crude single-element feedback
  - *insensitive to variations in supply voltage, temperature, and process*
  - *internal bias circuit needs no external adjustments*
    - same circuit works for any detector, gain, tp
  - *easy to implement programmable gain*
- Drawbacks:
  - *only works in one polarity*
  - *DC leakage amplified by same factor as signal*
    - requires BLR in 2nd stage
  - *large area consumption*

Secondary noise sources in the preamp

- i_{B1}^2 and i_{B2}^2 are effectively in parallel with the input transistor
- Their contribution to input (white) thermal series noise is $(g_{mB1,2}/g_{m1})^2$.
- We minimize their g_m w.r.t. that of M1
- $g_{mB1,2} = \sqrt{2\mu C_{ox} W I_D / L}$
- use <u>low</u> W/L (i.e. long-gate) devices with large or degenerate with source resistor.
- Keep W/L as small as possible (thus V_{gs}-V_T large) while keeping $V_{DS} > V_{gs}$-V_T.
- Various ways to optimize.



Shaper and baseline stabilizer

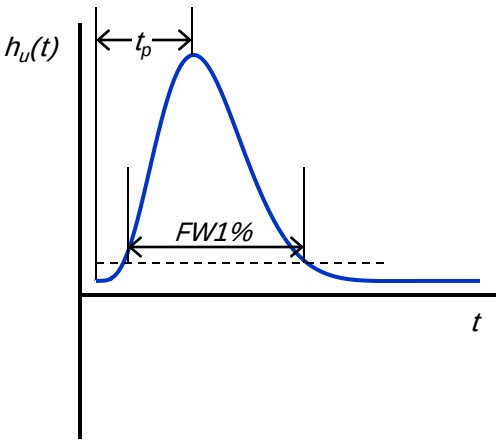


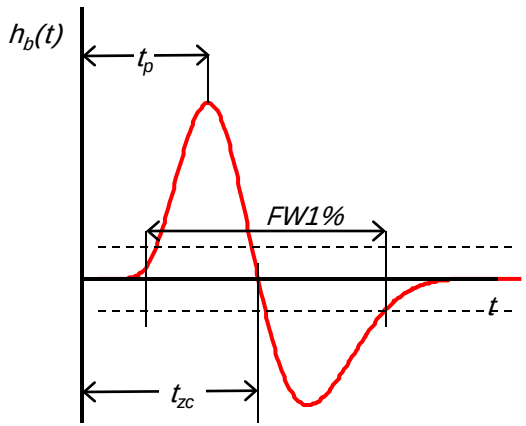
Integrated shaping amplifiers

- Limits the bandwidth for noise
- Gives controlled pulse shape appropriate for rate
- Control baseline fluctuations
- Set slope at threshold crossing for timing
- Bring charge-to-voltage gain to its final value
- By its saturation characteristics, sets upper limit on Q_{in}

- Feedback circuits give the most stable and precise shaping
  - *At the expense of power dissipation*
  - *Poor tolerance of passives limits accuracy of the poles and zeros*
- High-order shapers give the lowest noise for a given pulse width

Shaper Characteristics





first and second moments

$$\int_{-\infty}^{\infty} |h(t)|^2 \, dt$$

$$\int_{-\infty}^{\infty} |h'(t)|^2 \, dt$$

slope at threshold crossing

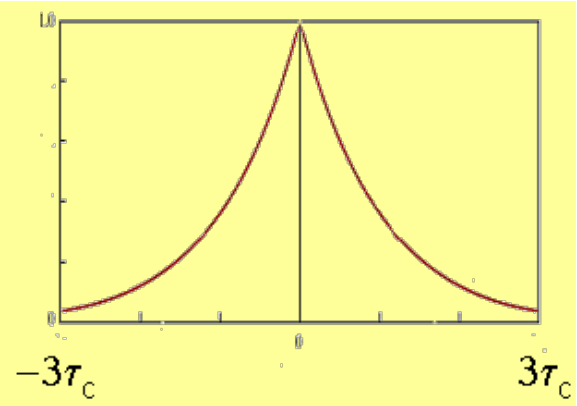
$$h'(t_{TC})$$

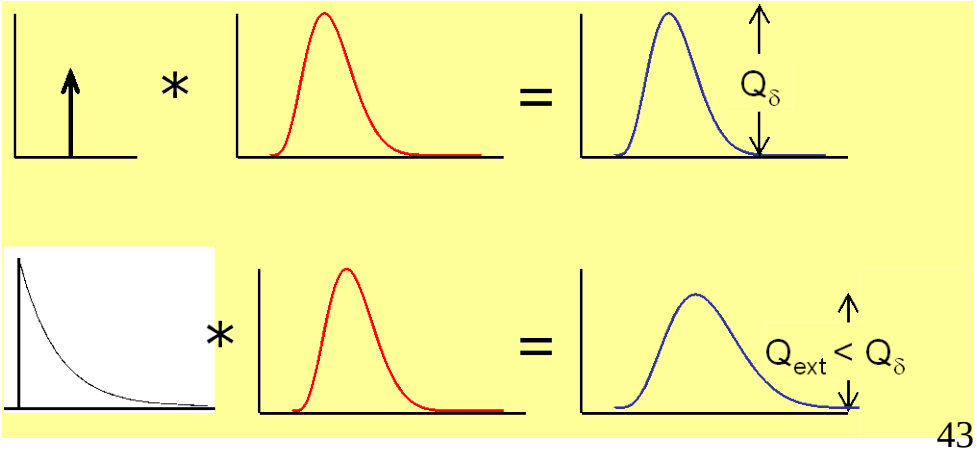
$$\text{where } h(t_{TC}) = V_{th}$$

Pulse shaper – matched filter with compromises

- calculation of matched filter
  - *incomplete knowledge of noise spectrum*
  - *incomplete knowledge of input waveform*
- exact transfer function difficult to realize in practice
- optimum filter requires a long time to respond
  - *pileup ⇔ limited rate capability*
- "ballistic deficit"
  - *input charge is not a δ-function*
  - *width of impulse response must be >> duration of input charge waveform*

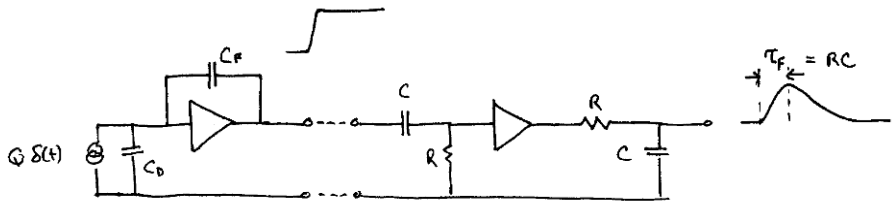
constraints:
- noise corner
- rate^{-1}
- charge collection
- preamp decay





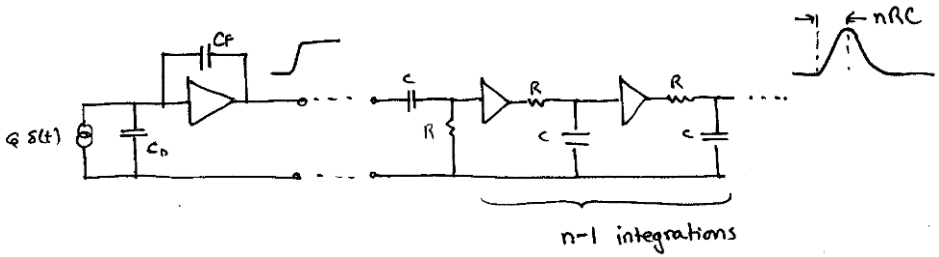
Pulse shaping filters with real poles

Simplest filter: CR-RC

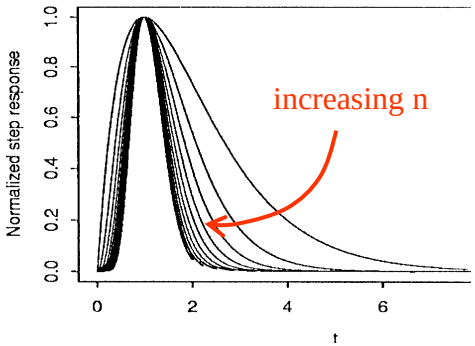


- asymmetric response

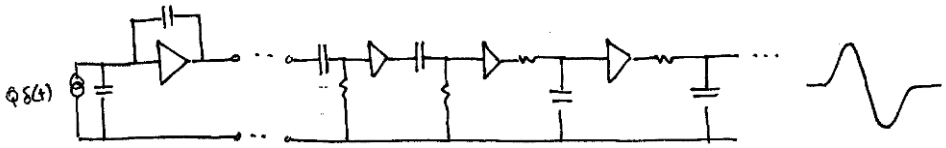
CR-RC^n, unipolar semiGaussian



- Identical real poles
- Symmetry improves with order n:



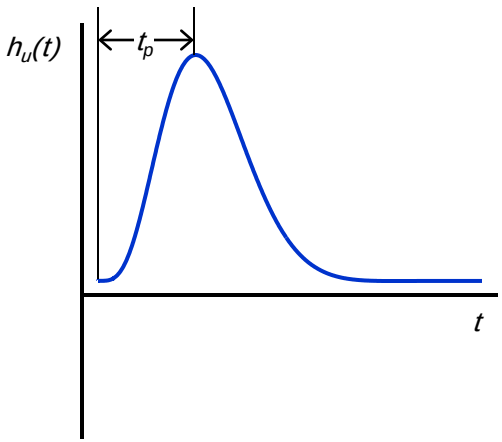
CR^2-RC^n, bipolar semiGaussian



- Area-balanced
- Derivative of CR-RC^n

Properties of real-pole semiGaussian shapers

unipolar CR-RC^n

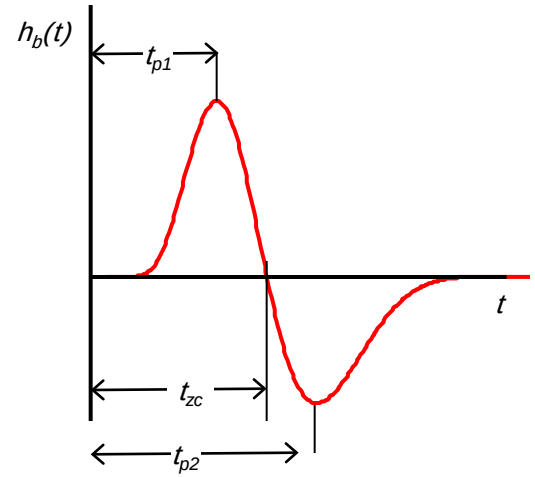


$$H_u(s) = \frac{s\tau}{(1+s\tau)^{n+1}}$$

$$h_u(t) = \frac{1}{n!}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-t/\tau}$$

$$t_p = n\tau$$

bipolar CR^2-RC^n



$$H(s) = \frac{(s\tau)^2}{(1+s\tau)^{n+2}} \qquad \omega_{\max} = \frac{2}{n\tau}$$

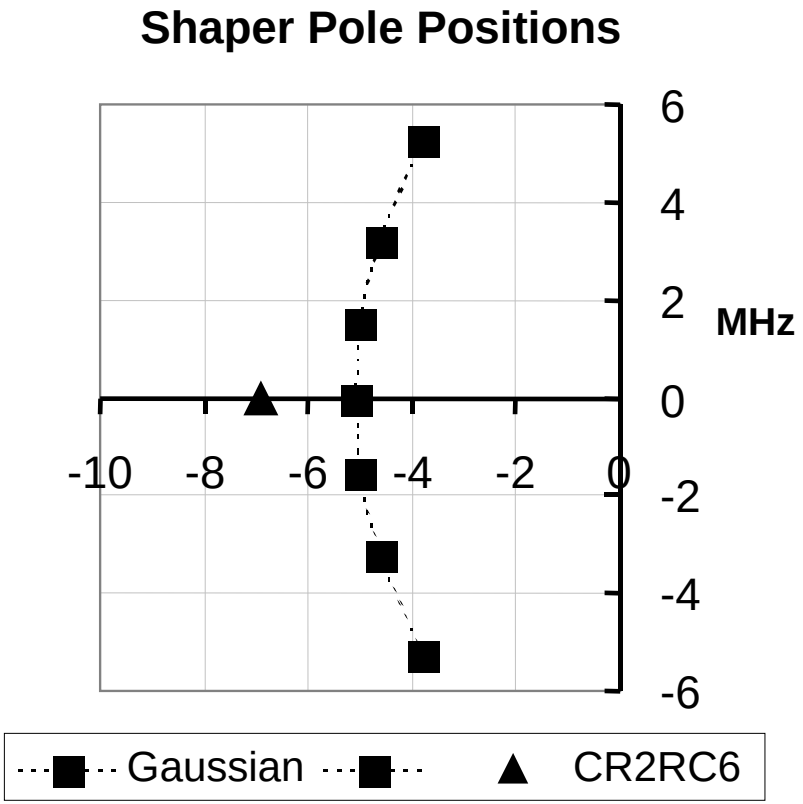
$$h(t) = \frac{1}{(n+1)!\tau}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-t/\tau}\left[t-(n+1)\tau\right]$$

$$t_{p1} = (n+1-\sqrt{n+1})\tau$$

$$t_{zc} = (n+1)\tau$$

$$t_{p2} = (n+1+\sqrt{n+1})\tau$$

Complex pole approximation to Gaussian pulse



Ohkawa synthesis method (Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers")

For given filter order, gives closest approx. to a true Gaussian

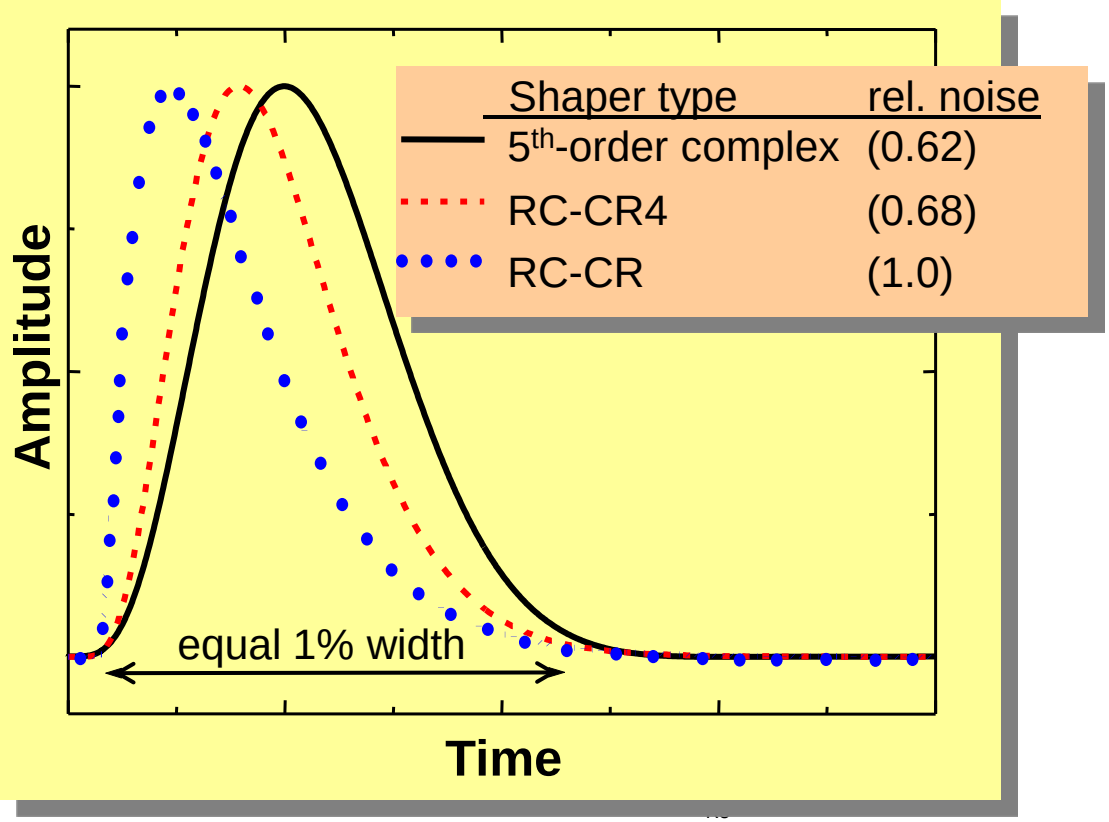
More symmetrical than CR-RC^n filter of same order for same peaking time

Noise weighting functions:

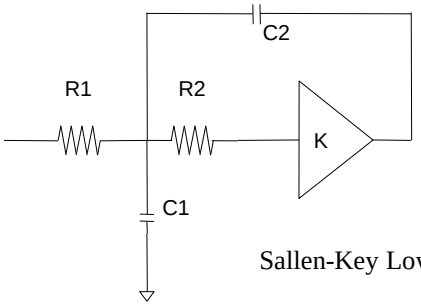
$I_{1,complex}/I_{1,CR\text{-}RC} = 1.18$ **series**

$I_{2,complex}/I_{2,CR\text{-}RC} = 0.81$ **parallel**

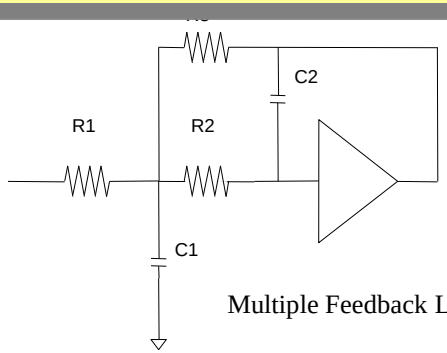
Shaper optimization



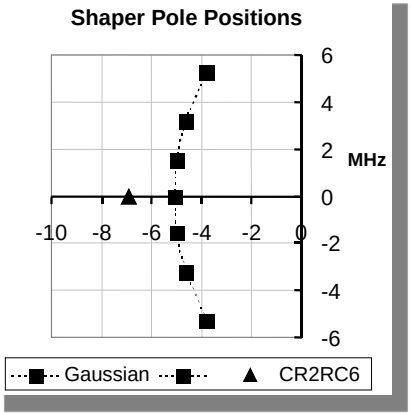
- For a given rate-handling capability, high-order shapers have lower noise.
- Adding an extra shaper stage can reduce noise more than putting the equivalent amount of power into the preamp.
- For a given shaper order, complex pole constellation using second- or third-order active filter topologies minimizes noise.



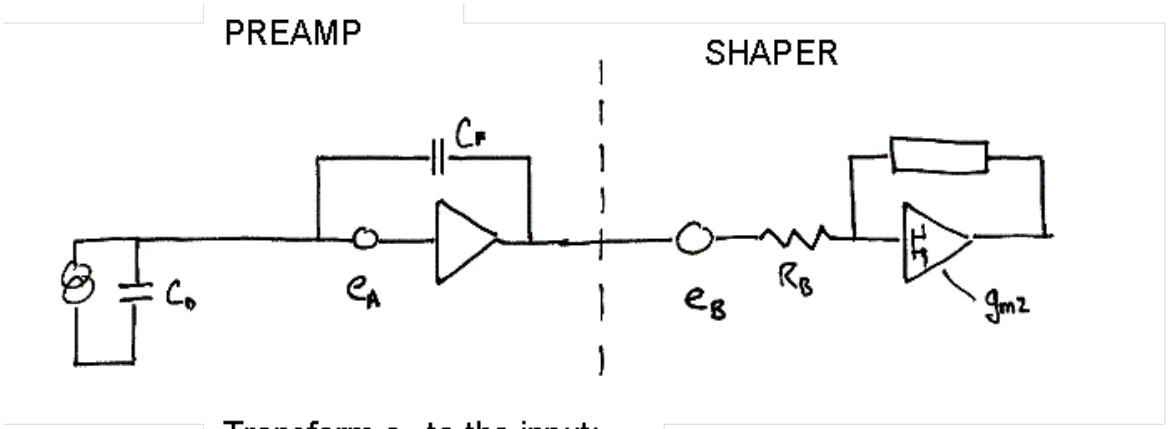
Sallen-Key Lowpass



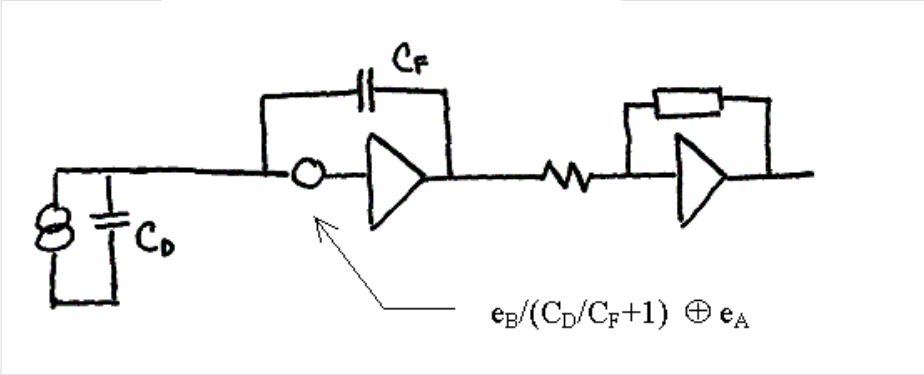
Multiple Feedback Lowpass



Second-stage noise



Transform e_B to the input:



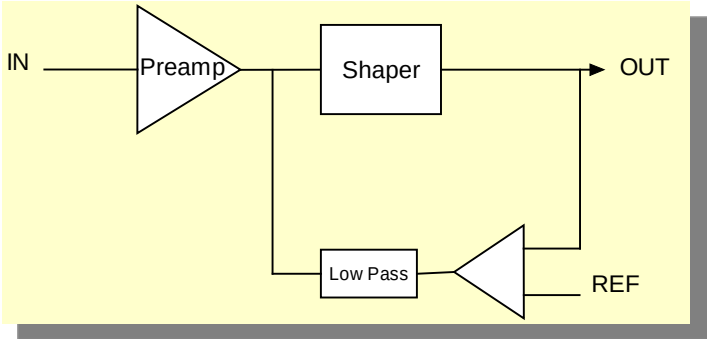
$$\frac{ENC_B}{ENC_A} = \frac{C_F}{C_D} \cdot \left(\frac{R_B}{R_A}\right)^{1/2}$$

Baseline stabilization

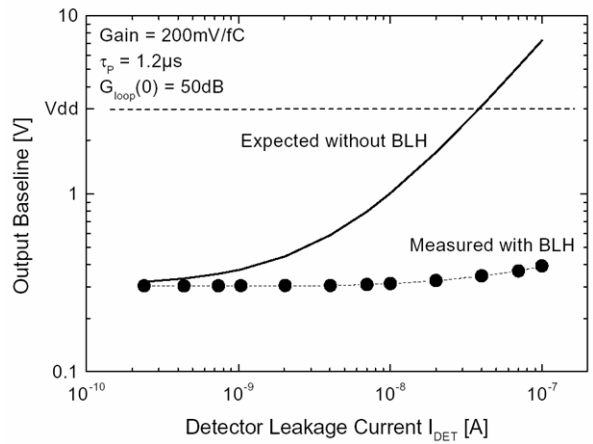
Baseline can move due to:

1. DC coupling to detector with variable leakage
2. Temperature and power supply drift
3. Rate fluctuations in a system with AC coupling

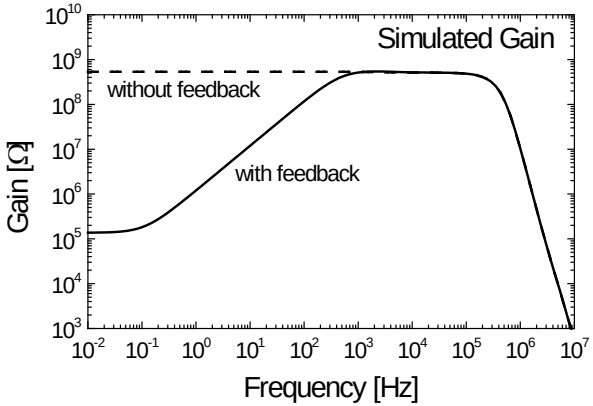
(1) and (2) can be prevented by low frequency feedback circuit:



Result:



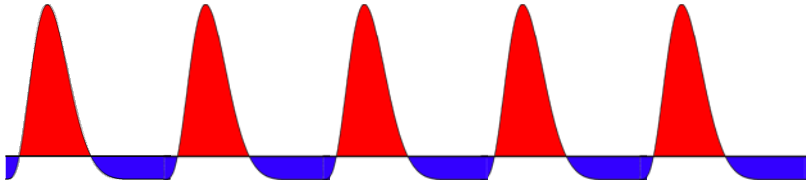
But this introduces unintended AC coupling:



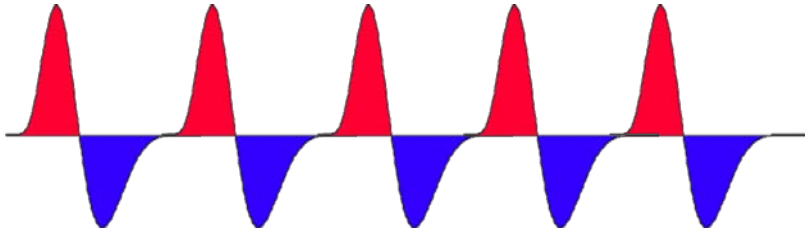
Compensate with nonlinear element or gating of the feedback circuit

Area balance after AC coupling

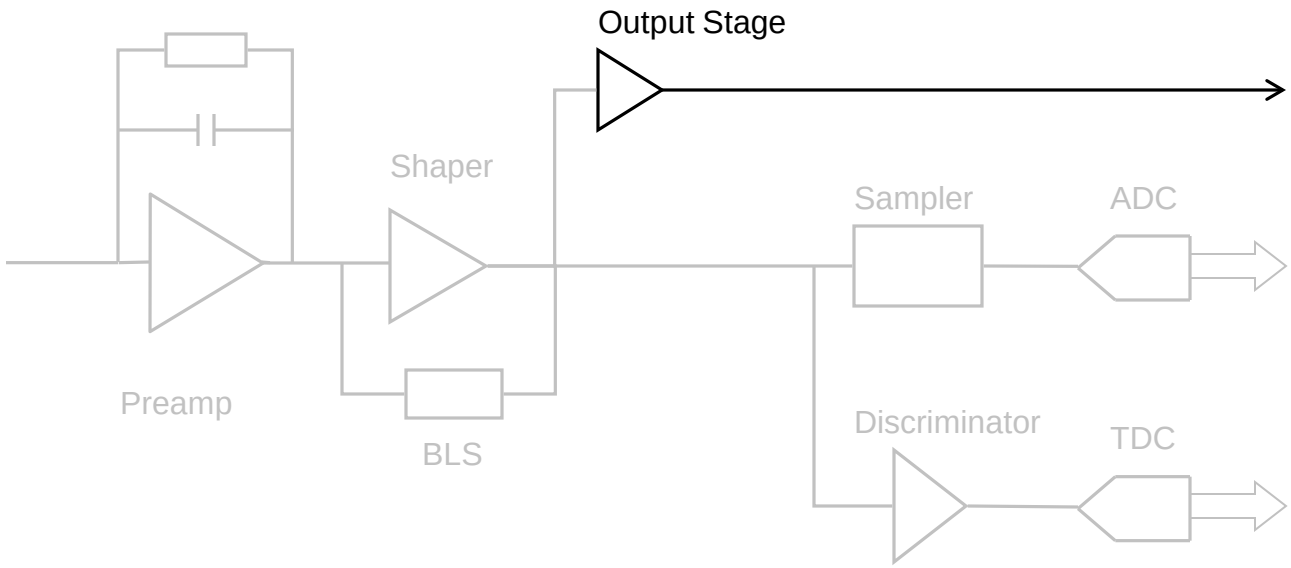
- Unipolar pulse:
- baseline displaced below 0
- instantaneous rate fluctuations cause baseline to wander



- Bipolar pulse:
- each pulse is area balanced, no detrimental effect of AC coupling
- penalty is higher noise, longer occupancy per pulse

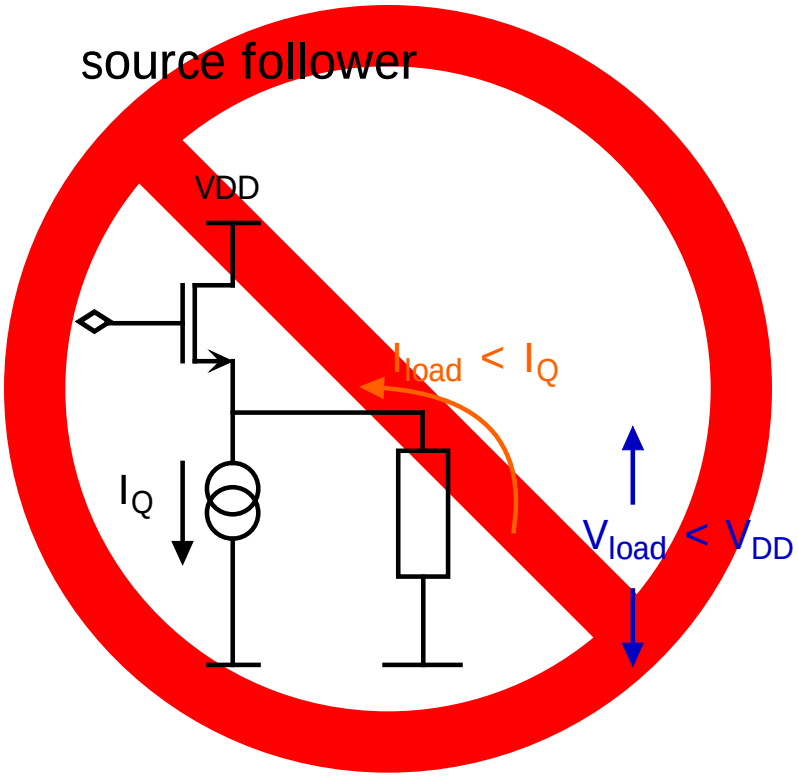


Output stage

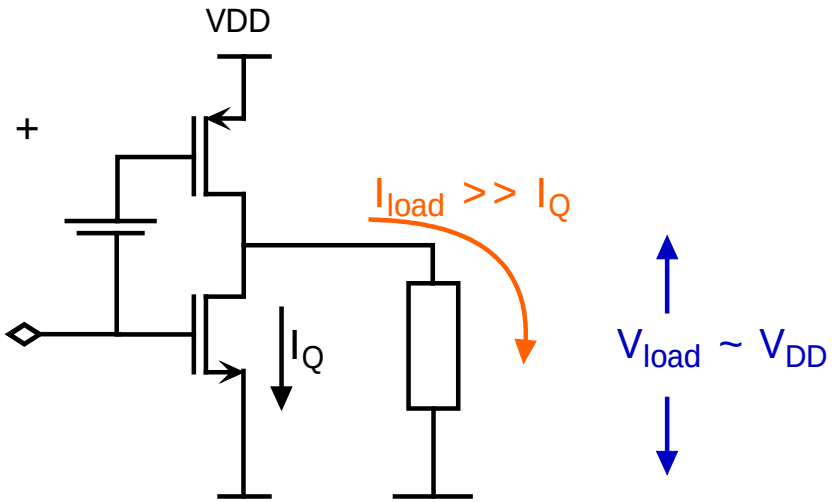


Output driver

source follower



class AB common source

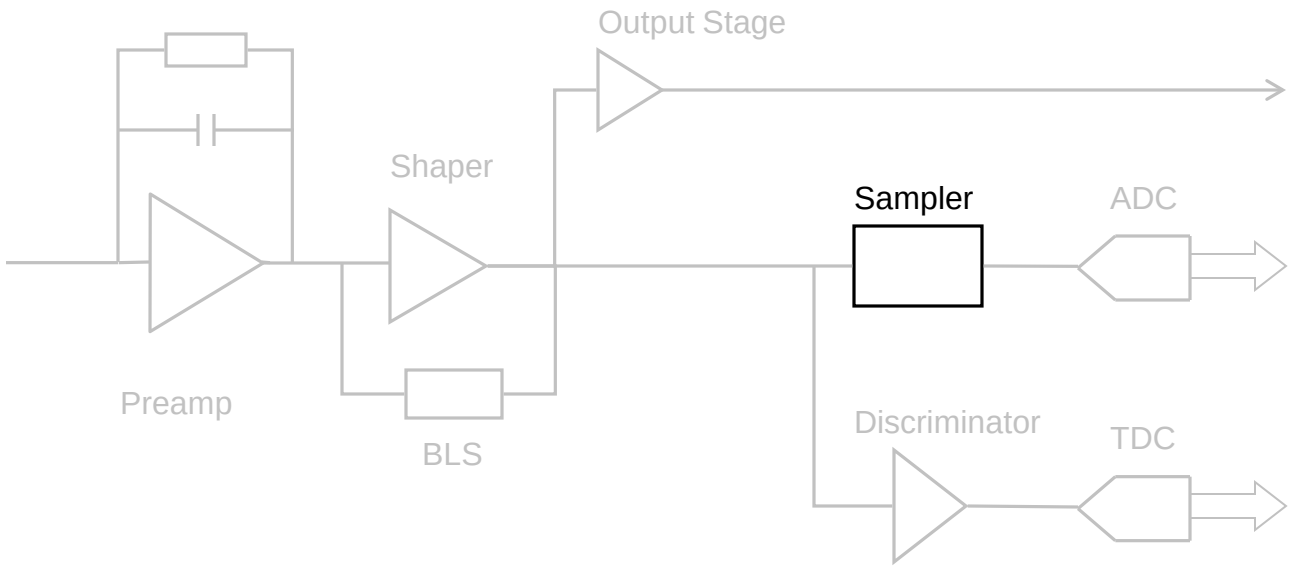


- class A: high standing current
- can't swing rail-to-rail

- class AB stage can source or sink currents >> quiescent current
- common-source stage can drive rail-to-rail

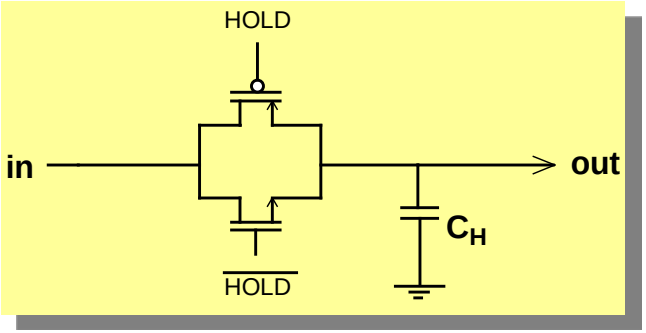
Hogervorst ref.

Analog sampling



Candidate sampling/memory cells in CMOS

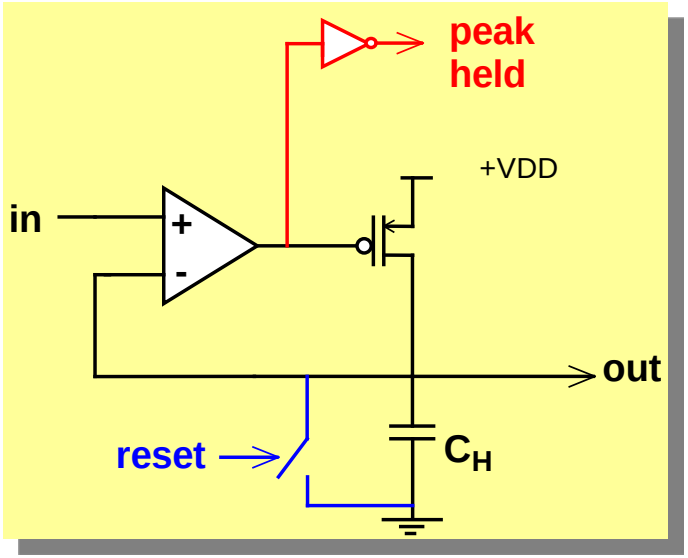
Sample/hold using switched capacitor



- small
- low-power

- timing of hold signal: needs CFD for walk-free operation
- switch charge injection
- poor drive capability: needs output amp

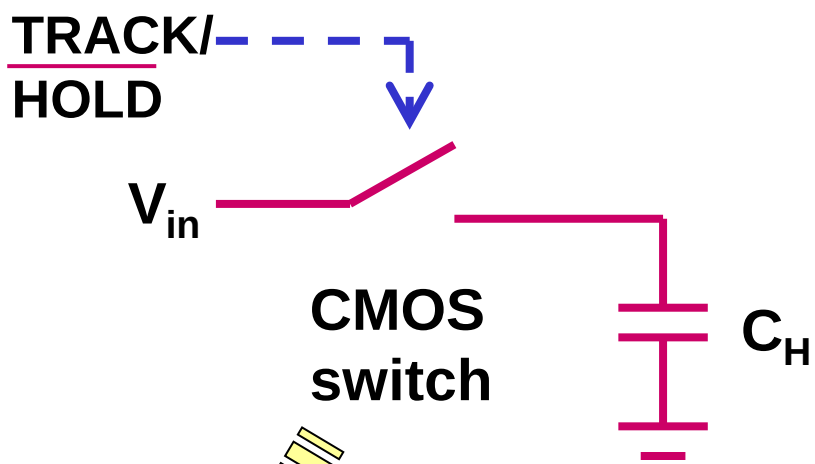
Peak Detector (PD)

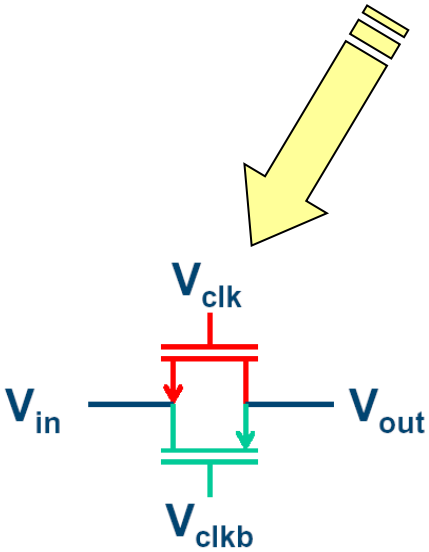


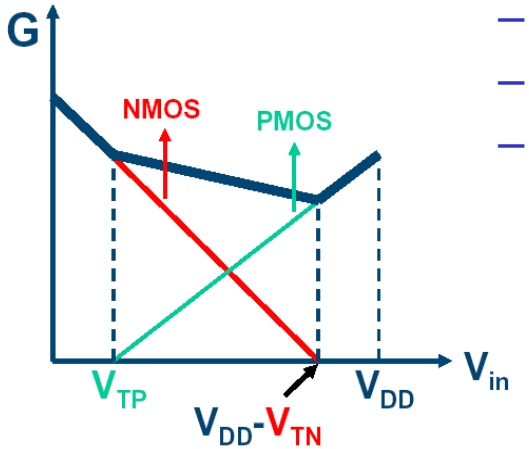
- self-triggered
- timing output
- feedback loop

- deadtime until readout reset
- poor drive capability
- accuracy impaired by opamp offsets, CMRR, slew rate

Switched-capacitor track-and-hold







CMOS switch:

- *low I_{off}*
- *high G_{on}, $0 < V_{sig} < V_{DD}$*

MOS/MIM capacitor:

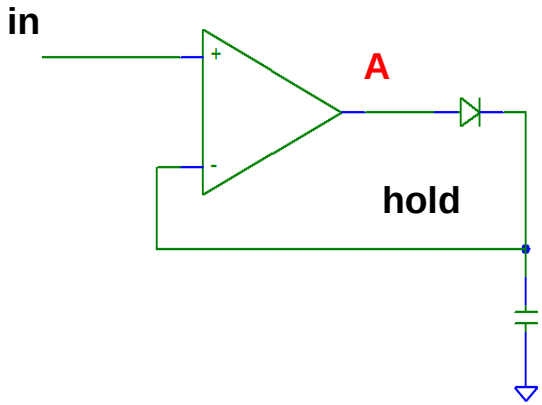
- *well-matched*
- *low leakage*
- *linear*

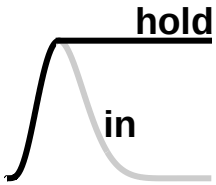
Design tradeoffs:

- *speed – droop rate*
- *speed – charge injection*
- *speed – clock feedthrough*
- *low voltage limits*

CMOS Peak Detector

Classical peak detector





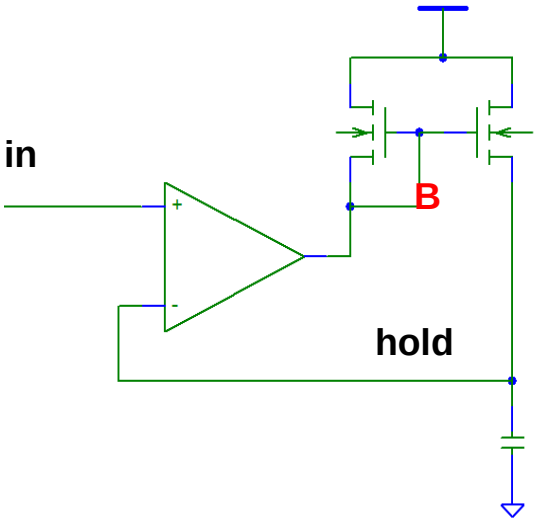
Diode replaced by current mirror acting as rectifying and loop-stabilizing element.

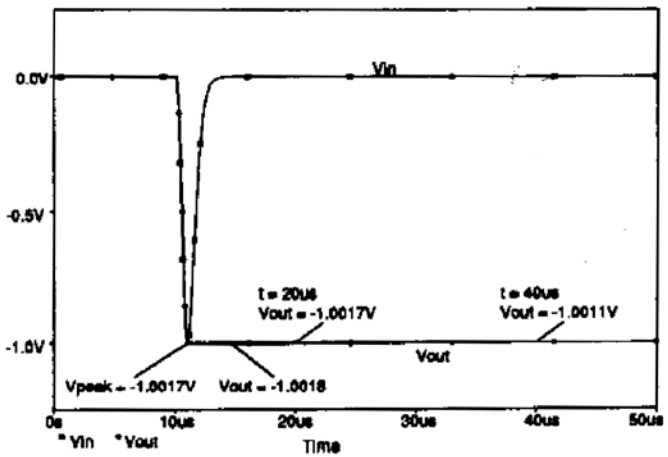
Reduced charge injection from sharp transient at node A(B).

$\Delta V_A = V_P$; $\Delta V_B = V_{th} << V_P$

Accuracy, speed, and dynamic range limited.

Improved CMOS version



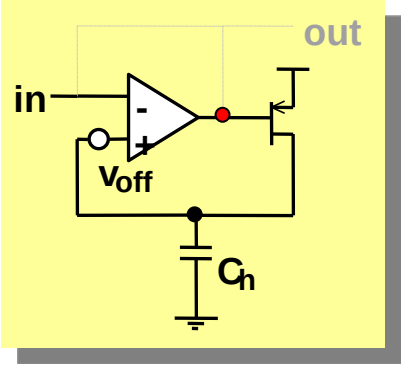


M. W. Kruiskamp, D. M. W. Leenaerts, IEEE Trans. Nuclear Sci., 41(1) 295 (1994)

The two-phase peak detector concept

Write phase

• behaves like classical configuration



Read phase

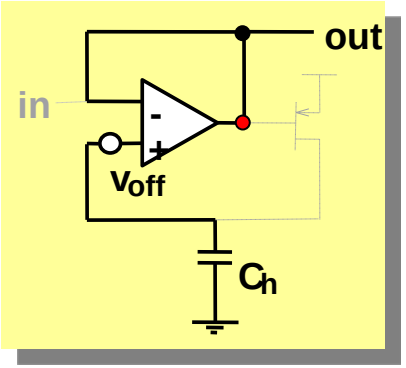
• op-amp re-used as buffer

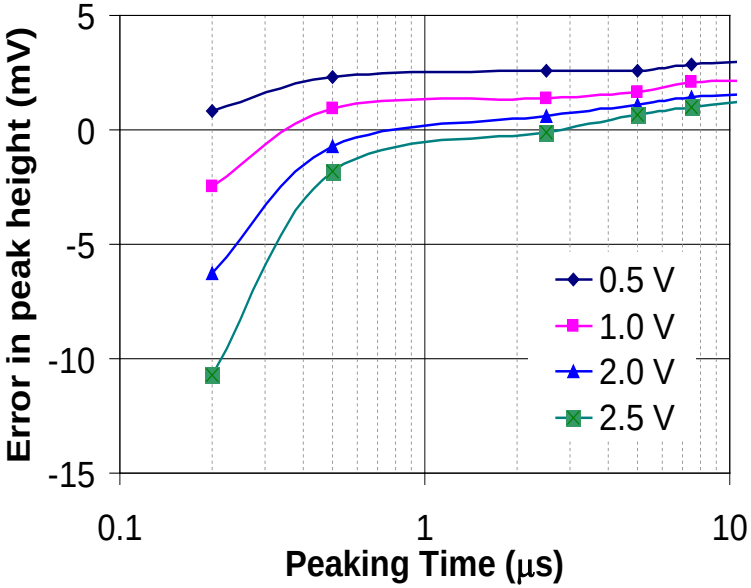
• **offset** and **CMMR errors canceled**

• enables **rail-to-rail** sensing

• good **drive capability**

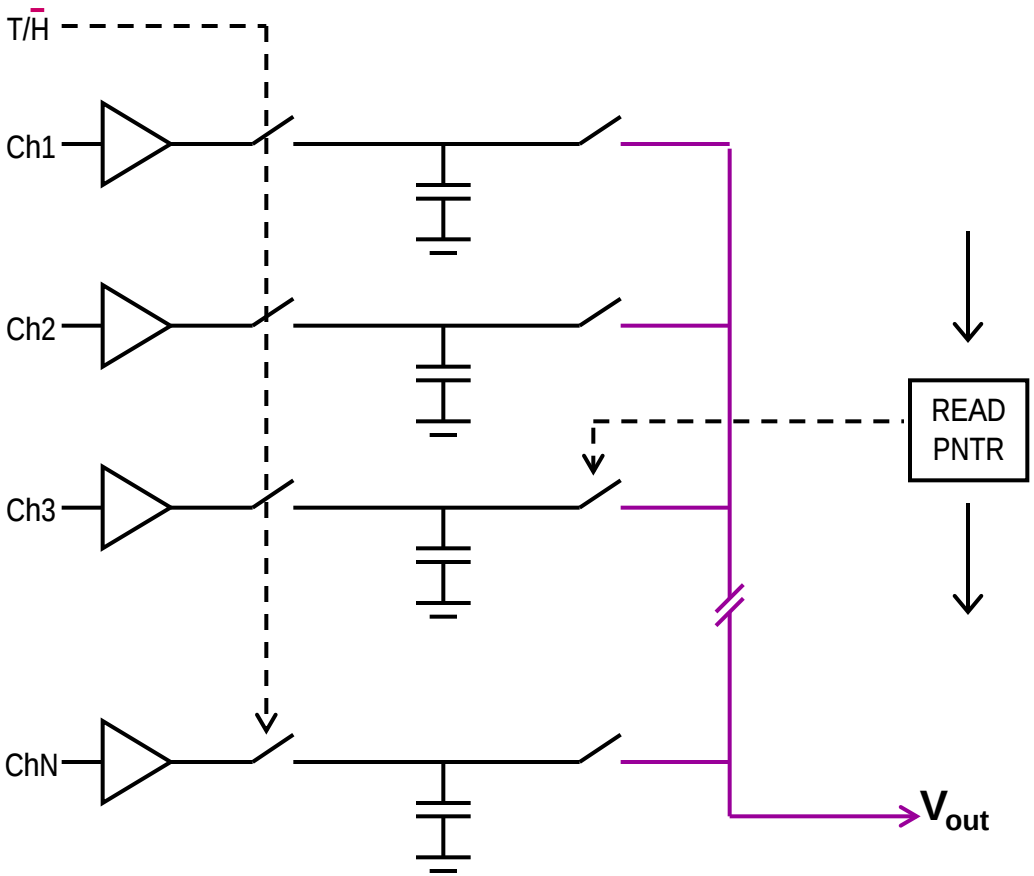
• **self-switching** (peak found)





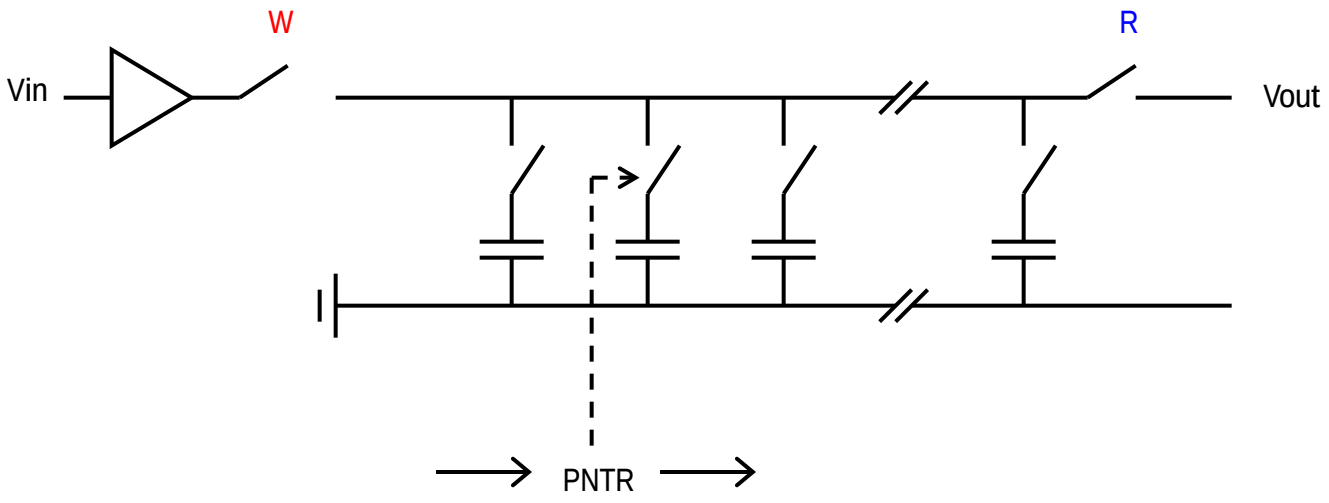
P. O'Connor, G. De Geronimo, A. Kandasamy,, IEEE Trans. Nucl. Sci. 50(4), 892 (2003)
G. De Geronimo, P. O'Connor, A. Kandasamy, Nucl. Instr. Meth. A484, 533 (2002)

Track/hold array + N-to-1 multiplexer

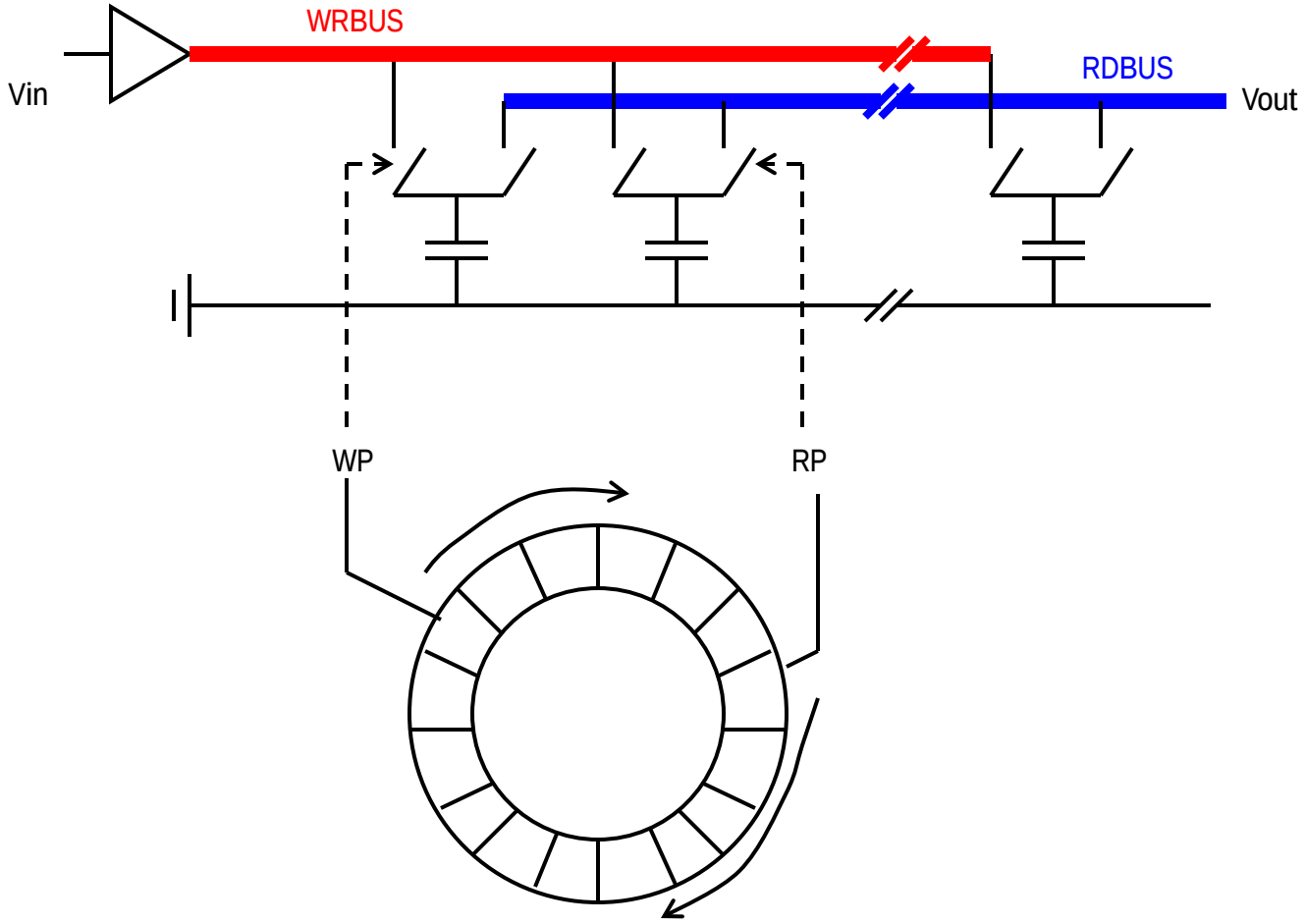


- tradeoff of multiplexing ratio, deadtime
- good channel-channel matching
- requires external signal to control track/hold

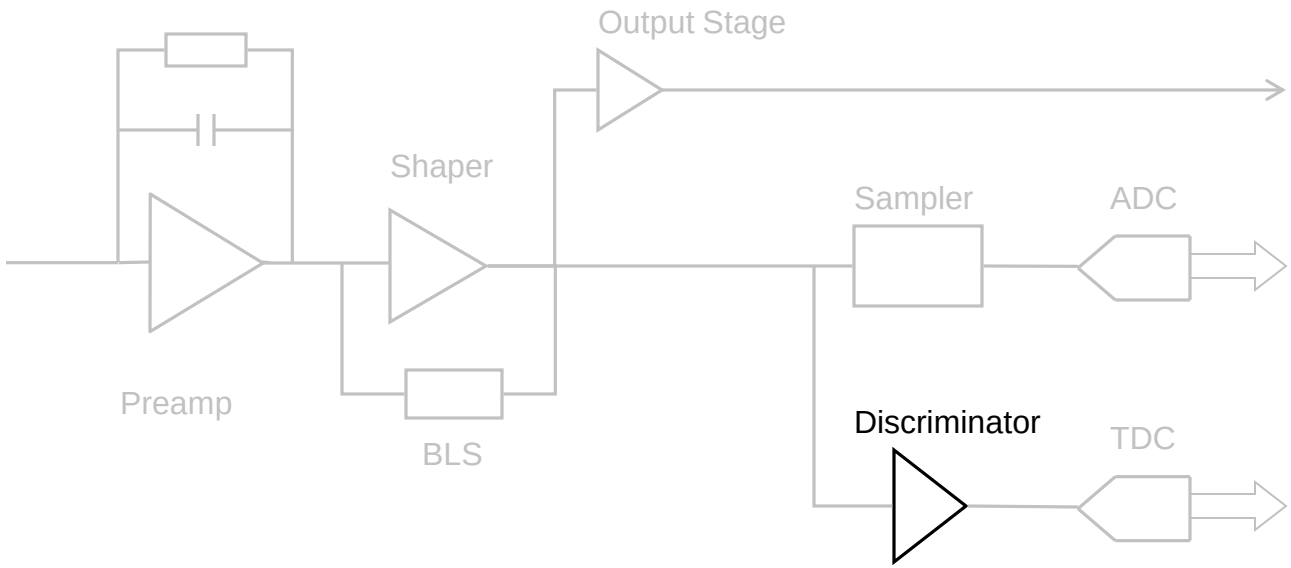
Switched-capacitor array waveform recorder



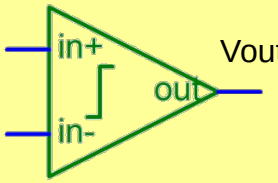
Deadtimeless SCA with simultaneous R/W



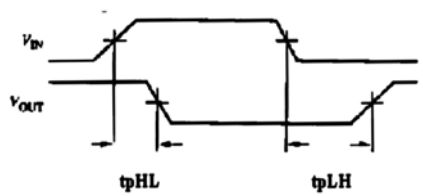
Discriminator

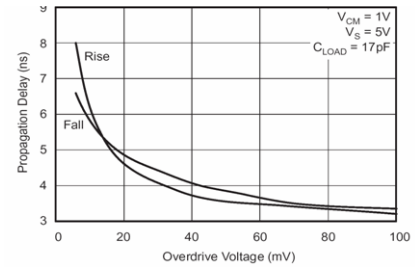


Discriminator properties and applications



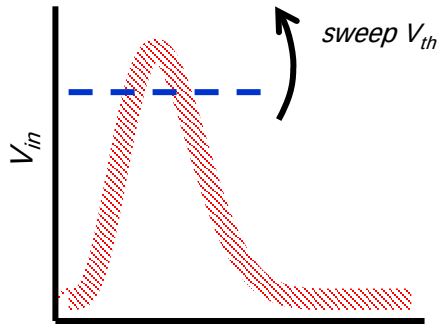
Vout = 1 if V(in+)>V(in-)
0 otherwise

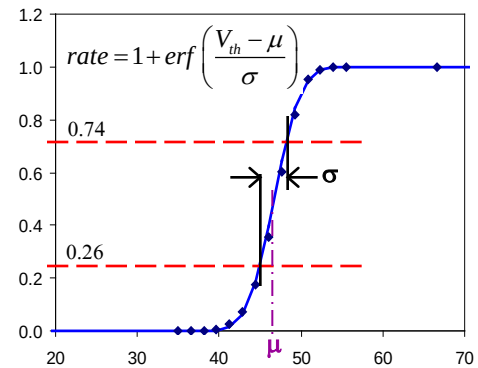




- Characteristics
  - *propagation delay*
    - vs. overdrive
    - vs. risetime (of input wfm)
    - vs. load capacitance
  - *hysteresis*
  - *recovery from saturation*

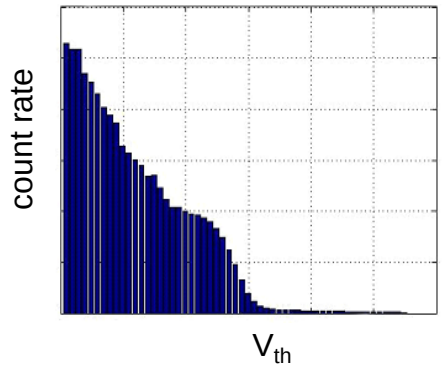
- Used for
  - *hit detection (YES/NO)*
  - *trigger*
  - *amplitude windowing*
  - *amplitude spectra (by threshold sweep)*
  - *time interval marker*

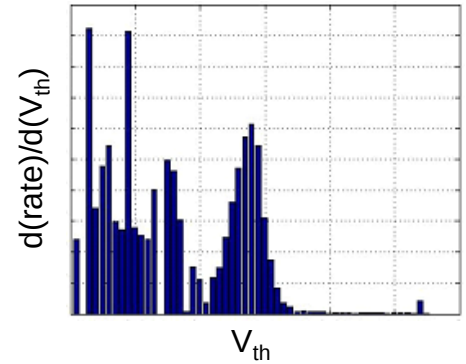




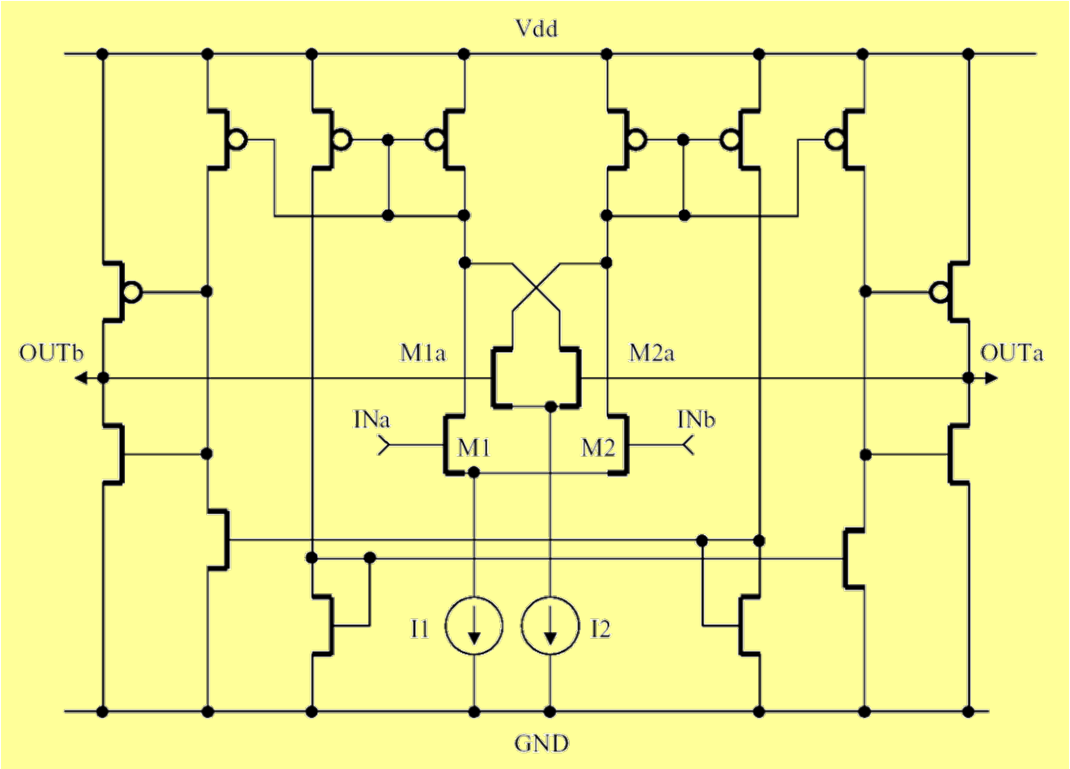
Noise hit rate in threshold detection:
System bandwidth B, rms noise σ ➔

$$f_{noise} \approx 0.6B \exp\left(-\frac{V_{th}^2}{2\sigma^2}\right)$$



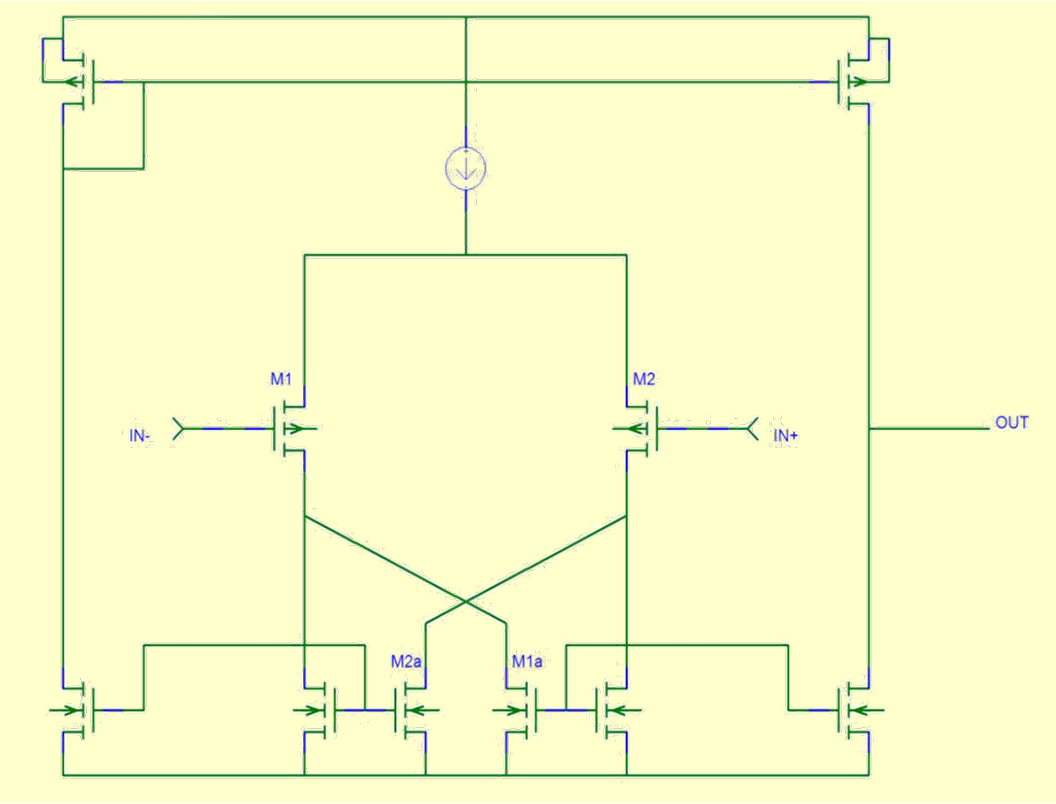


CMOS discriminator topologies (1)



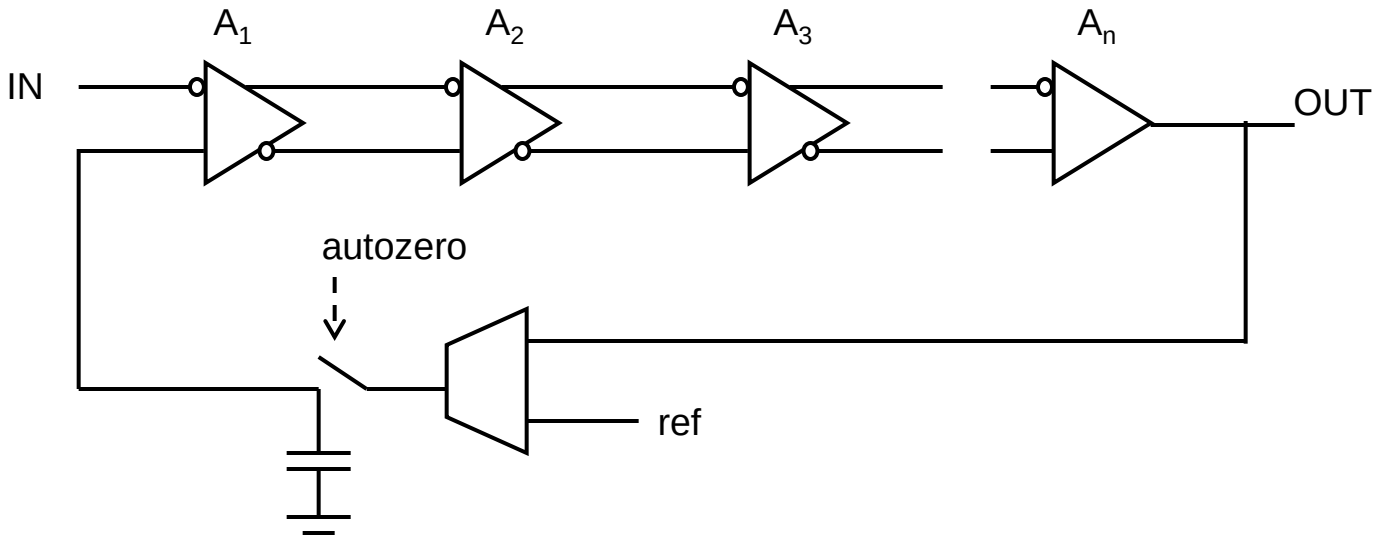
- Main differential pair M1-M2 plus dual current mirrors provide gain ~ 500
- Cross-coupled pair M1a, M2a provide positive feedback.
- Hysteresis level adjustable by I2/I1 ratio.
- Balanced, fully differential circuit less prone to feedback oscillation.

CMOS discriminator topologies (2)

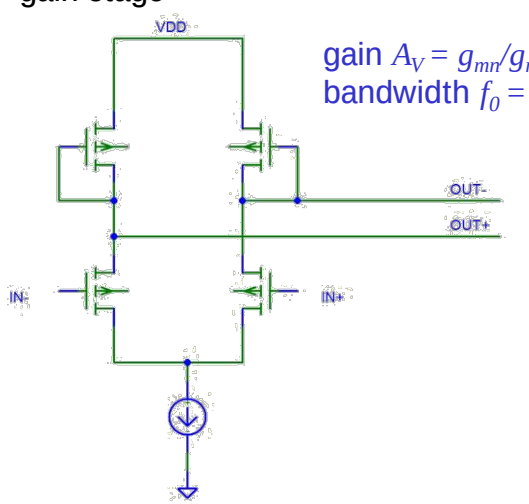


- Cross-coupled pair M1a, M2a provide positive feedback
- Hysteresis level adjustable by M1/M1a width ratio

Cascade topology



gain stage



gain $A_V = g_{mn}/g_{mp}$
bandwidth $f_0 = g_{mp}/2\pi C_{out}$

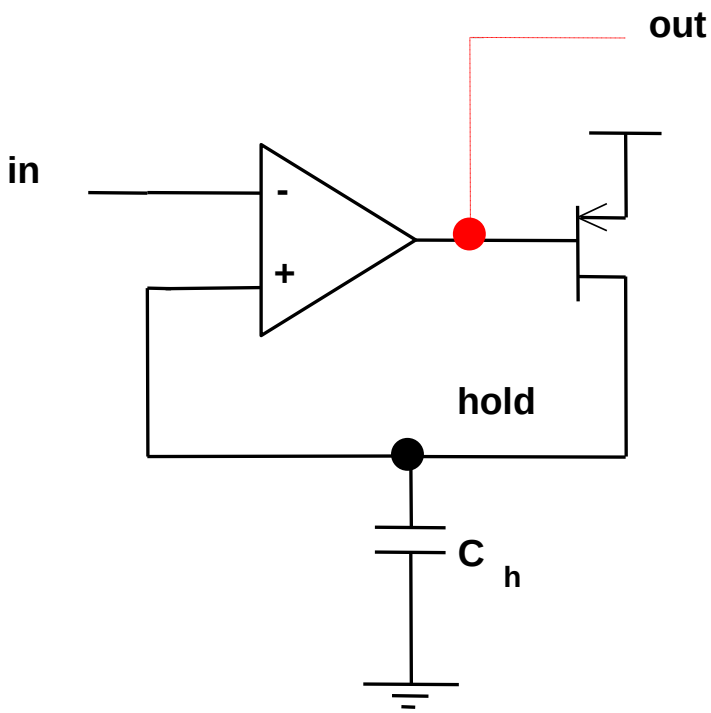
Overall gain A_V^n

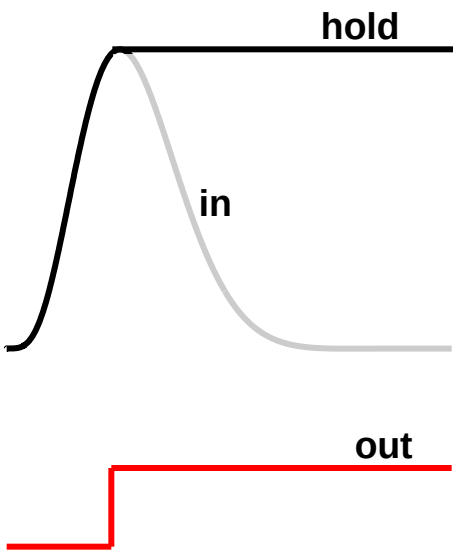
Overall BW $f_0\sqrt{2^{1/n}-1}$

- Cascade gain increases faster than bandwidth decreases as add more stages.
- Nonlinearities limit n to ~ 5 - 6 in practice.

M.L. Simpson et al., IEEE J. Solid-State Circuits 32(2), 1997 (198)
N. Paschalidis et al., IEEE Trans. Nuc. Sci. 49(3), 2002 (1156)

Peak detector as timing comparator

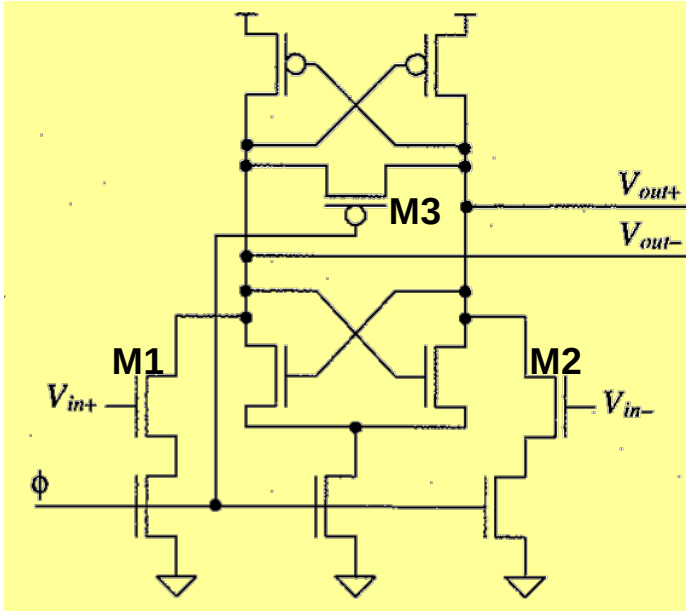




C_h may be precharged to threshold

V_{out} is free of time-walk

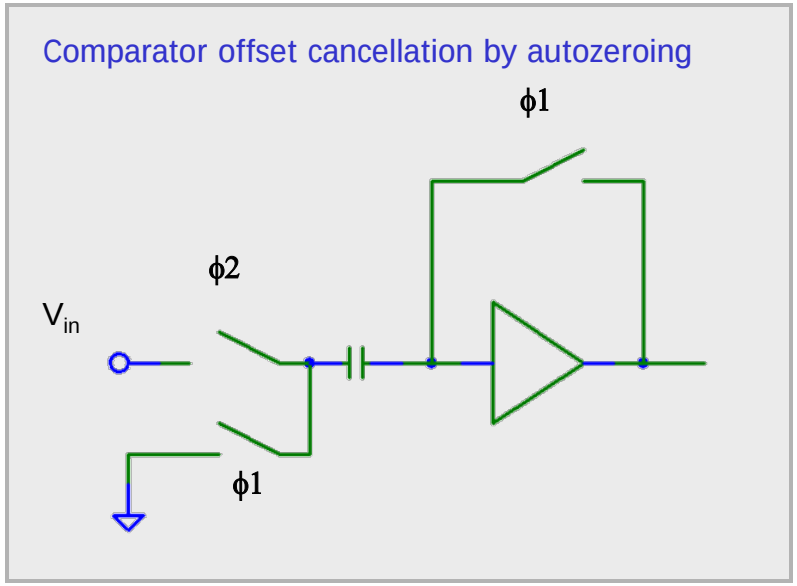
Clocked comparator



ϕ=0:
M3 holds latches in balanced condition

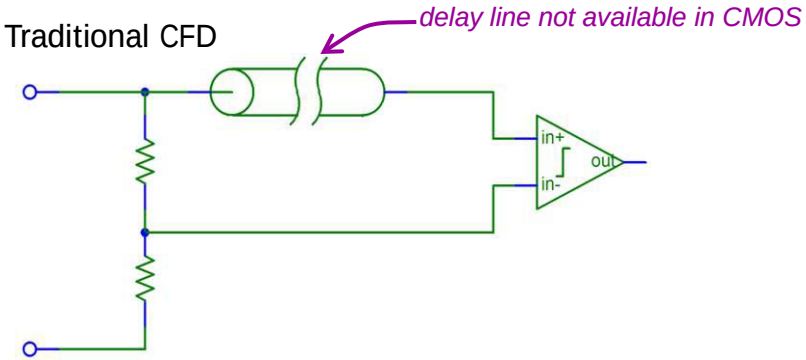
ϕ=1:
M3 OFF, M1/M2 unbalance latches, positive feedback gives rapid response

- This topology frequently used in ADCs.

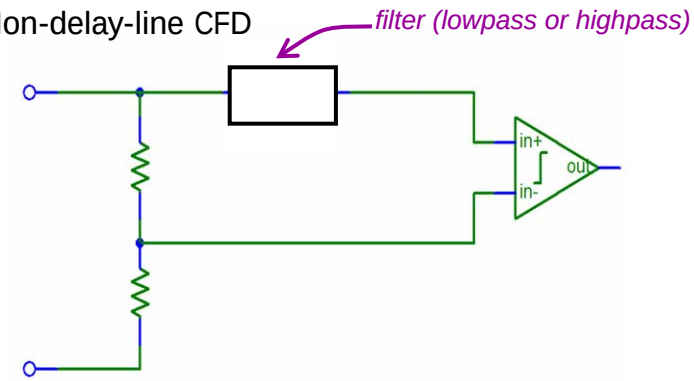


Non-delay-line constant fraction discriminators

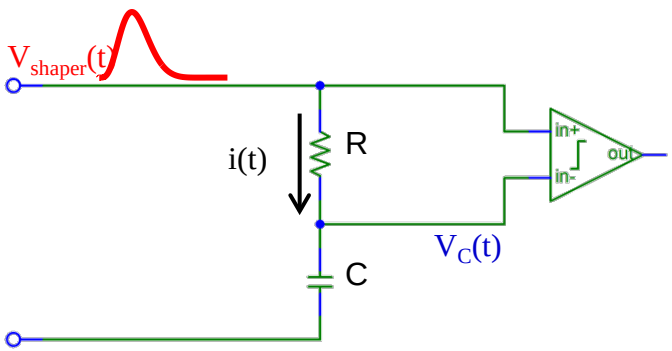
Traditional CFD

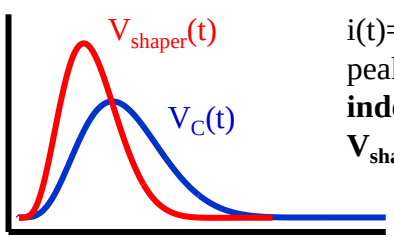


Non-delay-line CFD



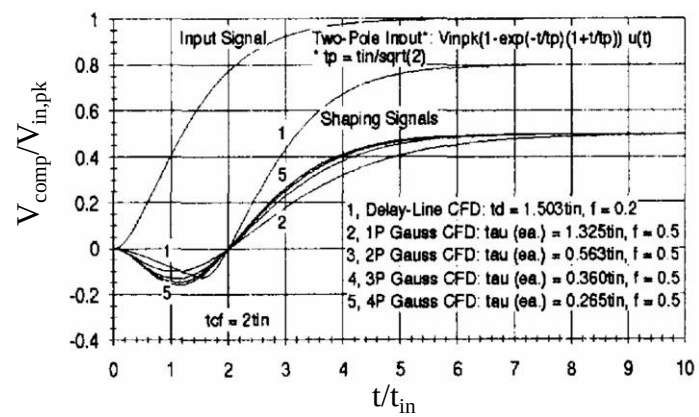
Simple monolithic implementation





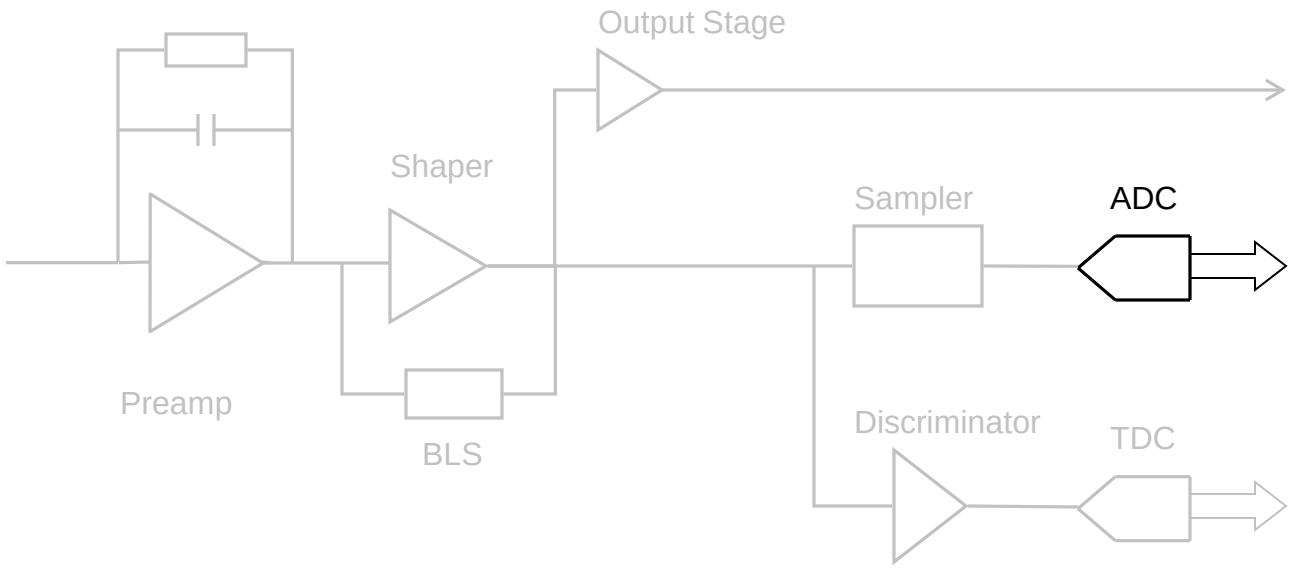
i(t)=0 when $dV_C(t)/dt=0$, i.e. at peak of lowpass waveform **independent of amplitude of $V_{shaper}(t)$**

Higher-order filter improves slope at zero-cross and leading-edge sensitivity

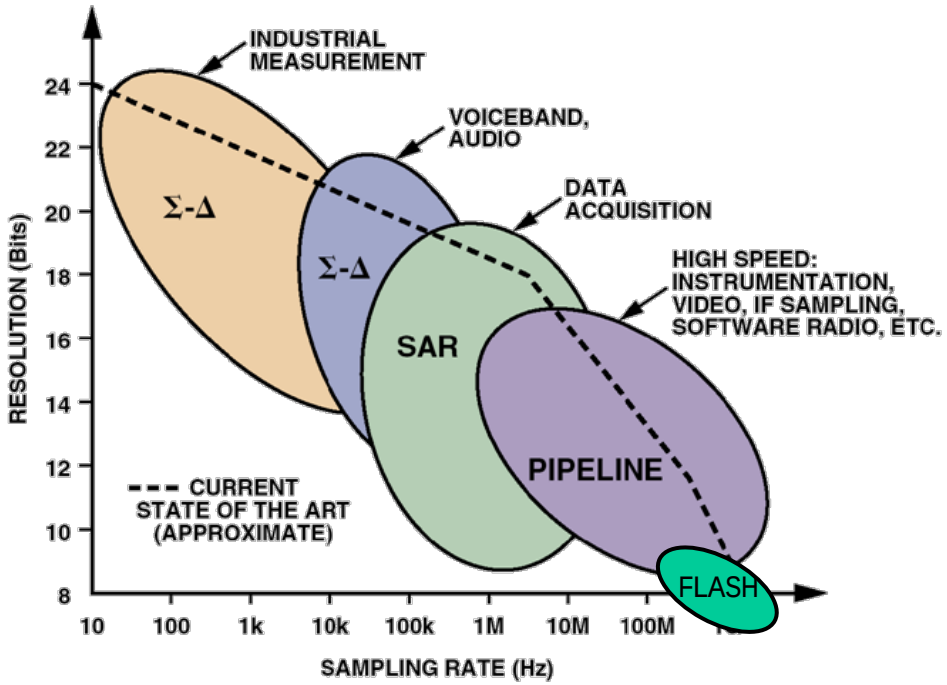


B.T. Turko, R.C. Smith, IEEE Trans. Nuc. Sci. 39(5), 1992 (1311)
C.H. Nowlin, Rev. Sci. Instr. 63(4), 1992 (2322)
D.M. Binkley, IEEE Trans. Nuc. Sci. 41(4), 1994 (1169)

Analog-to-digital converter (ADC)



ADC architectures

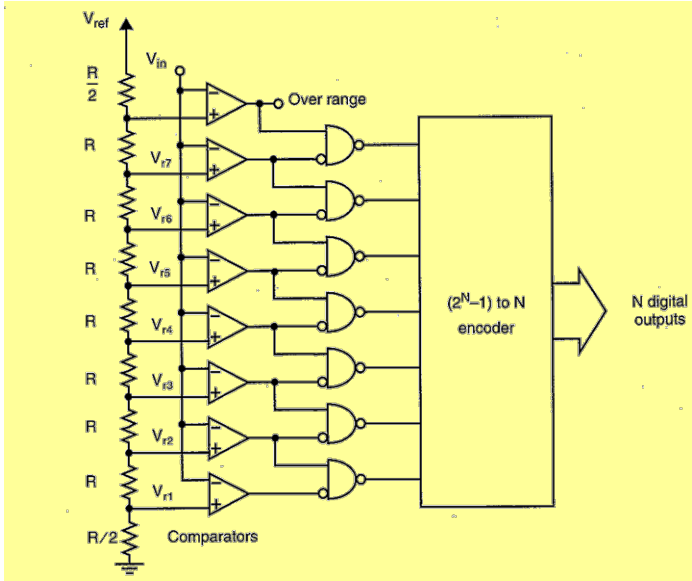


Tradeoffs:

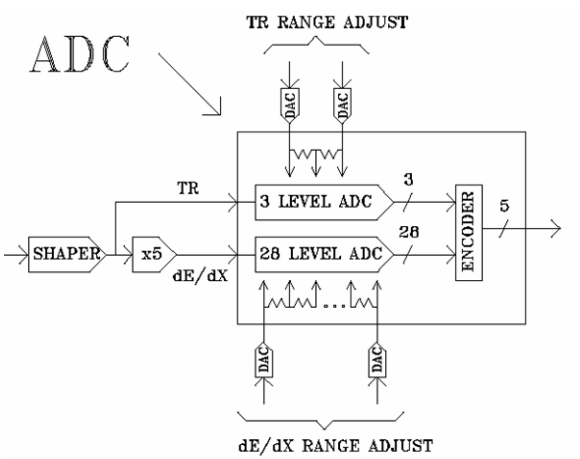
- speed
- power
- resolution

W. Kester, Analog Dialogue 39(2), 2005 (11)

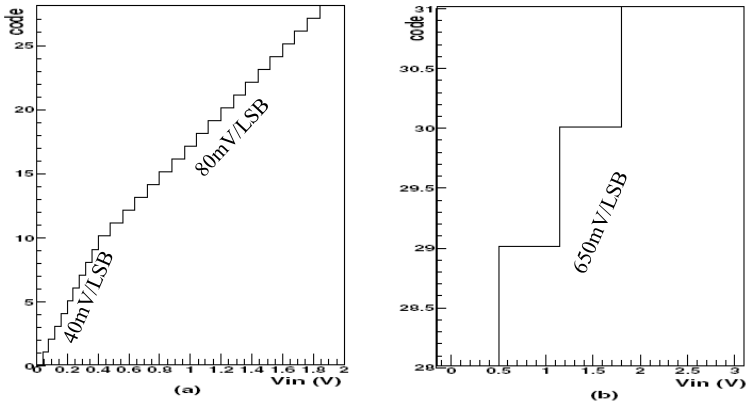
Flash converter



- N-bit converter requires 2^N-1 comparators and resistors
- Converts in one clock cycle (no latency)
- Comparator offset must be < $V_{FS}/(2^N)$
- Vin must be able to drive large dynamic load of comparator array
- Resistor string may be tapped for piecewise-linear transfer function

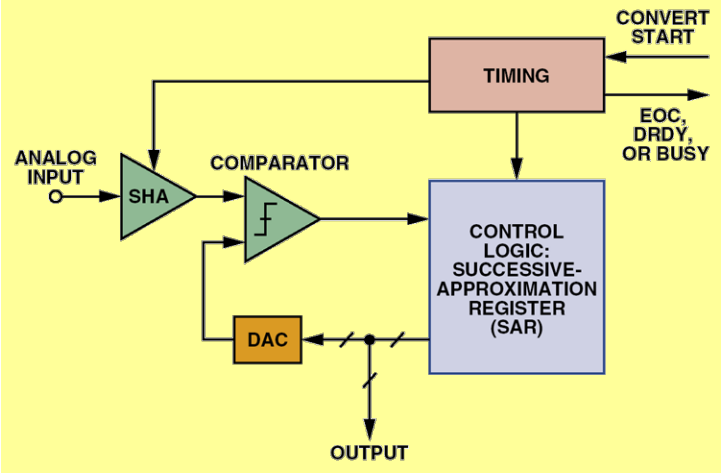


5 bit output
9 bit dynamic range



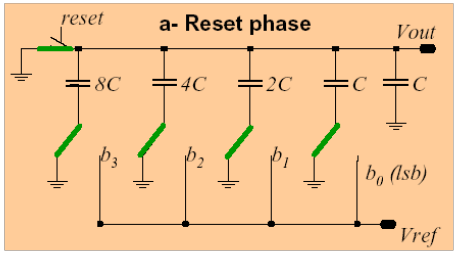
K. Barish et al., Nuclear Science Symposium Conference Digest IEEE, Nov. 2001, 604

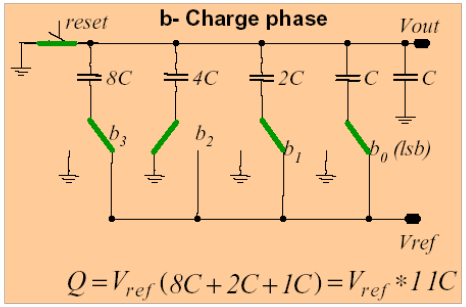
Successive Approximation (SAR) converter

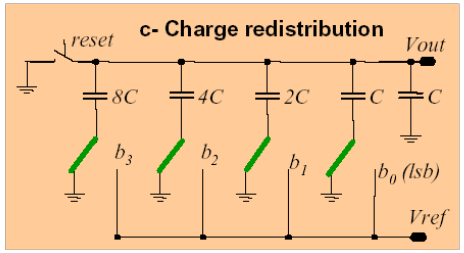


- Performs binary search using N-bit accurate DAC
- Charge-redistribution DAC gives 10 bit accuracy without calibration for typical 0.1% capacitor matching
- With digital autocalibration accuracy improves to 18-bit
- N-bit conversion requires N comparisons
- Sample-and-hold required at input so value to be converted does not change during the conversion time

Charge Redistribution DAC
Example: 4Bit DAC- Input Code 1011



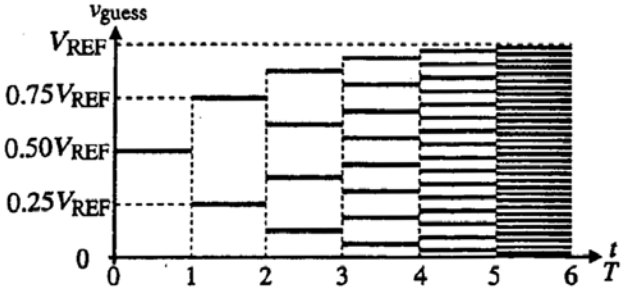




$$V_{ref} * 11C = V_{out} * 16C$$

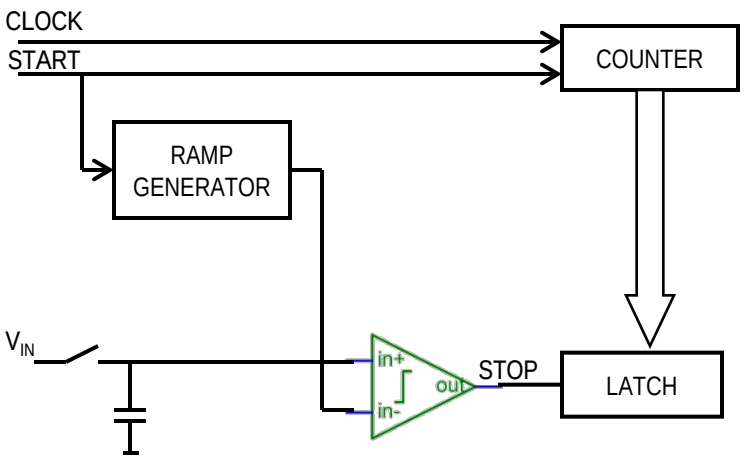
$$\rightarrow V_{out} = \frac{11}{16} V_{ref}$$

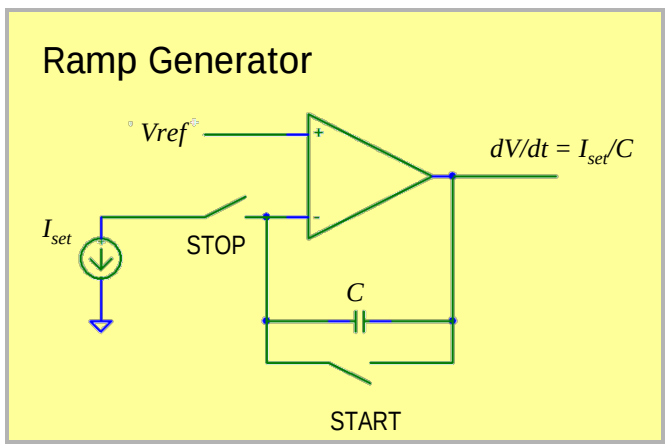
Binary search



In SAR converter, CDAC also combines functions of sample/hold and subtractor

Single-slope (Wilkinson) integrator

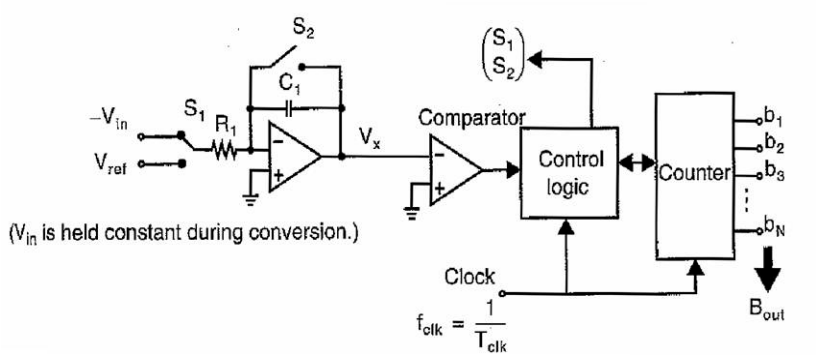


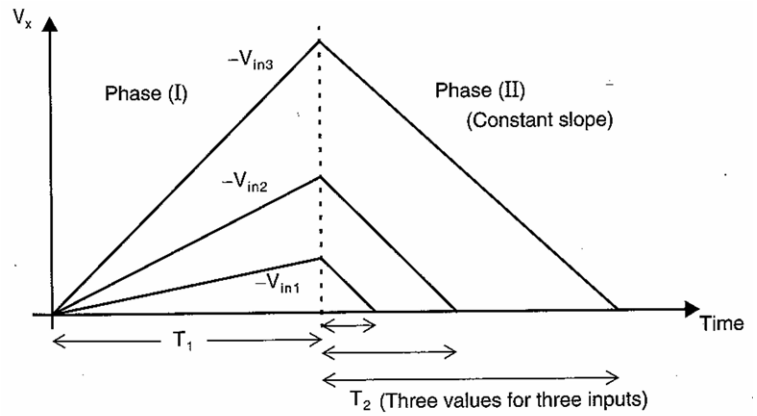


O. B. Milgrome, et al, "A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 4, pp. 771-5, 1992.

- Converts voltage into time interval
- N-bit conversion requires 2^N-1 clock cycles (worst case)
- Dual-edge clocked, Gray code counter improves speed performance
- Compact, low power
- Easily extended to multichannel systems
  - *counter, ramp generator common to all channels*
  - *Sample/hold, comparator, and output register per channel*

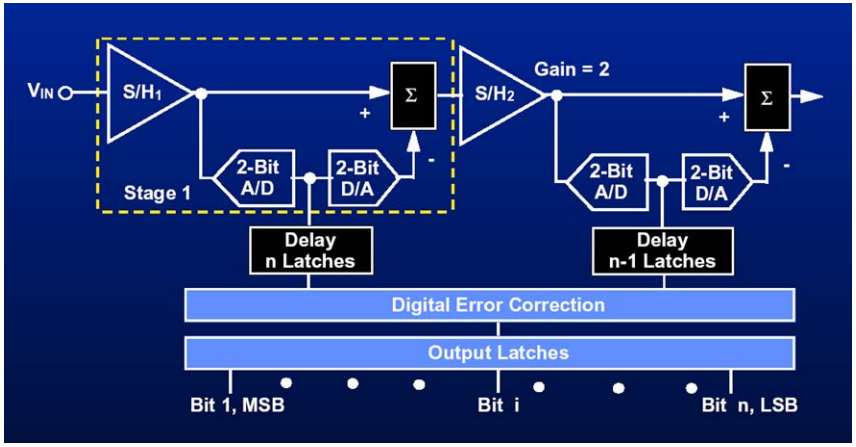
Dual-slope integrator





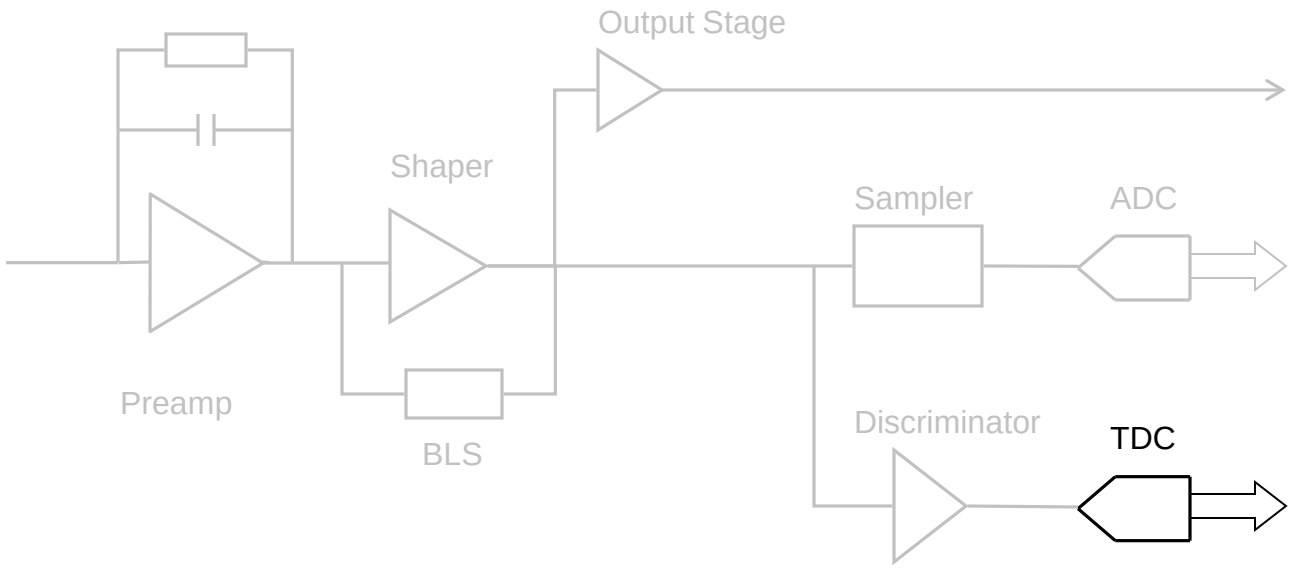
- Compare V_{in} to reference voltage by measuring time needed to charge/discharge C_1
- 2^N clock cycles per conversion, worst case
- Result independent of R_1,C_1, comparator offset
- Largely supplanted by oversampling Σ–Δ converters in most commercial markets

Pipeline converter

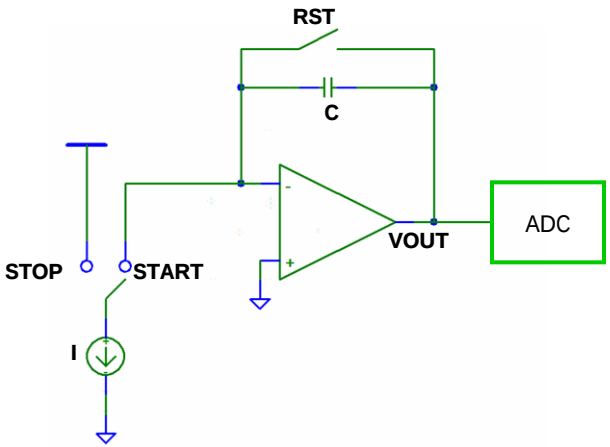


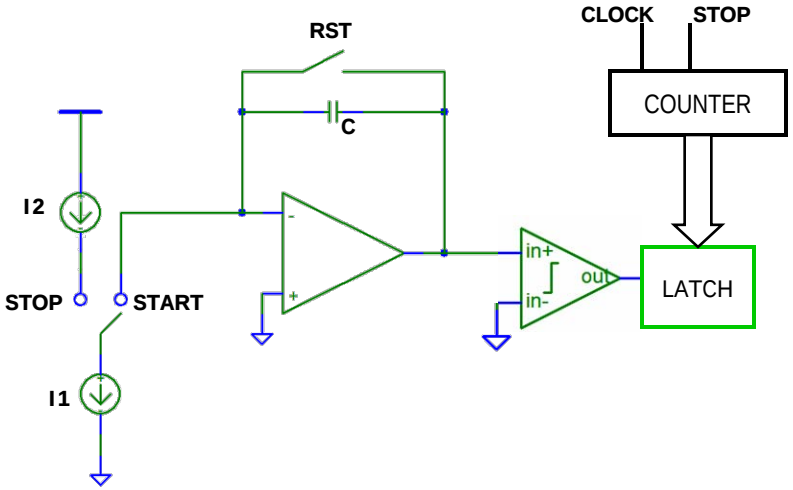
- Cascade of N stages, each stage consists of a sample/hold, low resolution ADC and DAC, summing amplifier with gain-of-2
- Each stage converts one bit and passes the residue on to the next stage
- N samples being simultaneously processed
- High throughput, moderate complexity, low power
- Only first stage needs full accuracy
- Sub-converter nonidealities can be removed by digital error correction
- Latency of N clocks between sample and valid data
- Minimum clock rate because of droop of internal S/H's
- Cannot be operated in burst mode

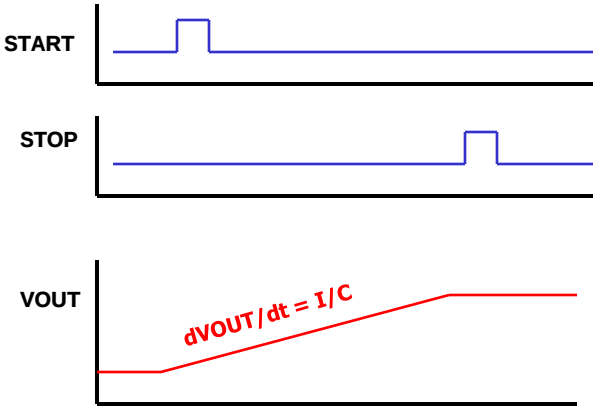
Time-to-digital converter (TDC)

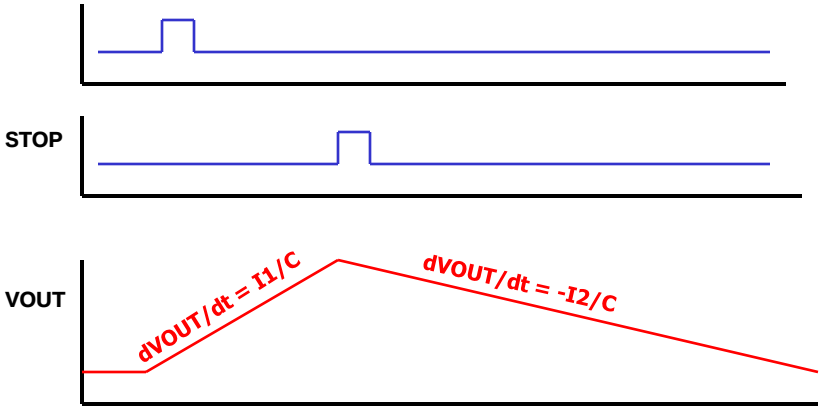


Time-to-amplitude converter (TAC)

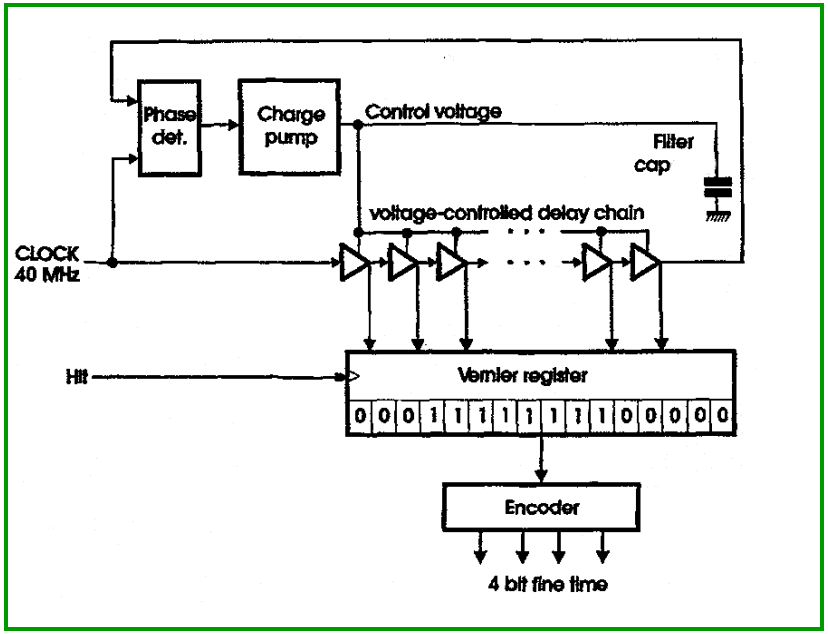






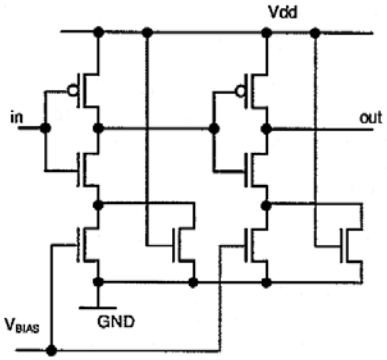


Delay-locked loop interpolator

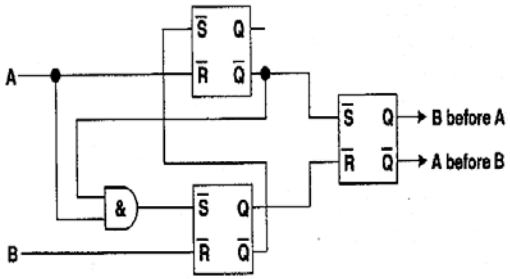


- Clock (START) signal propagated down a tapped, N-element delay chain
- Hit (STOP) freezes state of delay line
- Delay per stage stabilized to T_{ck}/N by phase-locking output to input, using voltage control of delay elements
- Resolution T_{ck}/N; dynamic range T_{ck}
- Extend dynamic range by coarse counter
- Mismatch of delay elements ➔ nonlinearity
- Long delay lines more nonlinear
- Easily extended to multichannel systems:
  - *DLL common to all channels*
  - *Latch, encoder per channel*

Variable delay element

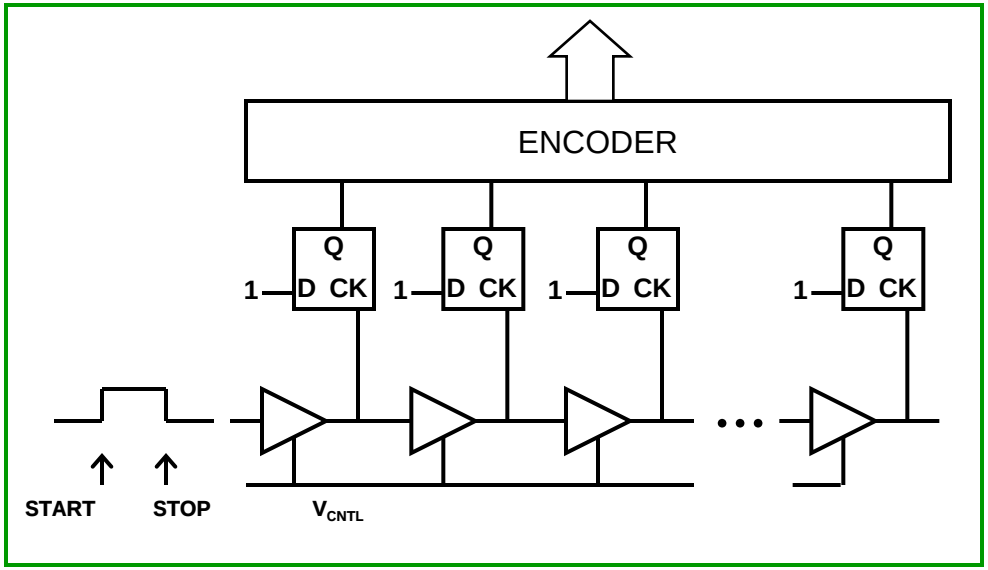


Phase detector



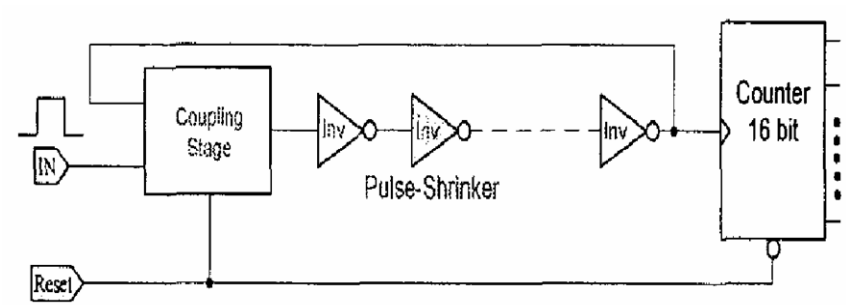
K. Barish et al., Nuclear Science Symposium Conference Digest IEEE, Nov. 2001, 604

Pulse-shrinking TDC



- Chain of pulse-shrinking elements
- Change of pulse width Δt per cell (stabilized)
- After n cells the pulse width shrinks to zero
- Cyclic version recirculates pulse through same shrinking element; count number of cycles until pulse vanishes
- Resolution LSB can be << t_{pd} of the technology
- Conversion time > time interval to be measured
- Both schemes can be combined with coarse counters to extend dynamic range

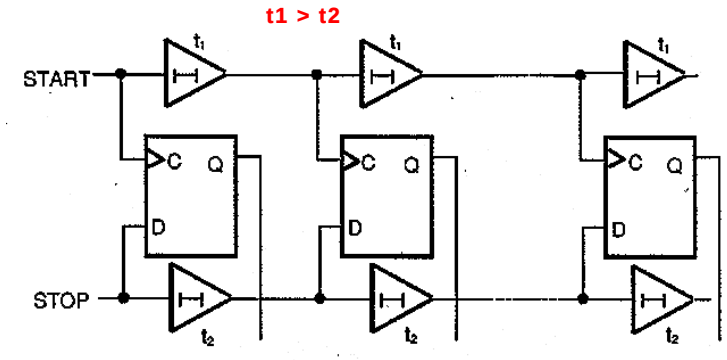
Cyclic version



E. Raisanen-Ruotsalainen, IEEE J. Solid State Circuits 30(9), 984 (1995)
S. Tisa et al., Proc. ISCAS 2003, p.465

Vernier techniques

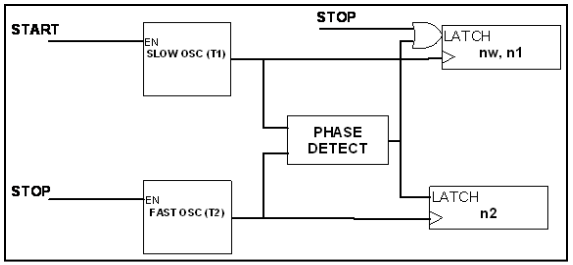
Vernier DLL

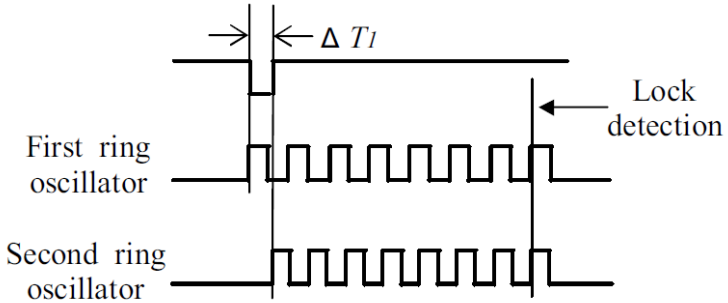


- START and STOP signals propagate down separate delay lines
- START chain has longer element delay than STOP
- Measure the stage where STOP catches up to START
- Stabilize by controlling *difference* t1-t2 so that N(t1-t2) = T_{ck}
- Resolution LSB can be << t_{pd} of the technology

P. Dudek, IEEE Trans. Solid-State Circuits 35(2), 240 (2000)

Two-ring oscillator





- START and STOP signals are used to enable triggerable oscillators having a small frequency difference
- START triggers the slower of the two oscillators, STOP triggers the faster one
- Resolution LSB is equal to the difference in period between the two oscillators T1-T2
- Counters record the number of periods of each oscillator between START and lock detection
- $\Delta T = (n_1 - n_2)T2 + n_1(T1-T2)$

Not in signal path, but important

- Power conditioning and distribution
- Bias circuits
- Electrostatic discharge protection
- Digital configuration switches
- Analog monitor
- DACs
  - *set comparator thresholds*
  - *trim channel-channel variations*
- Calibration pulser

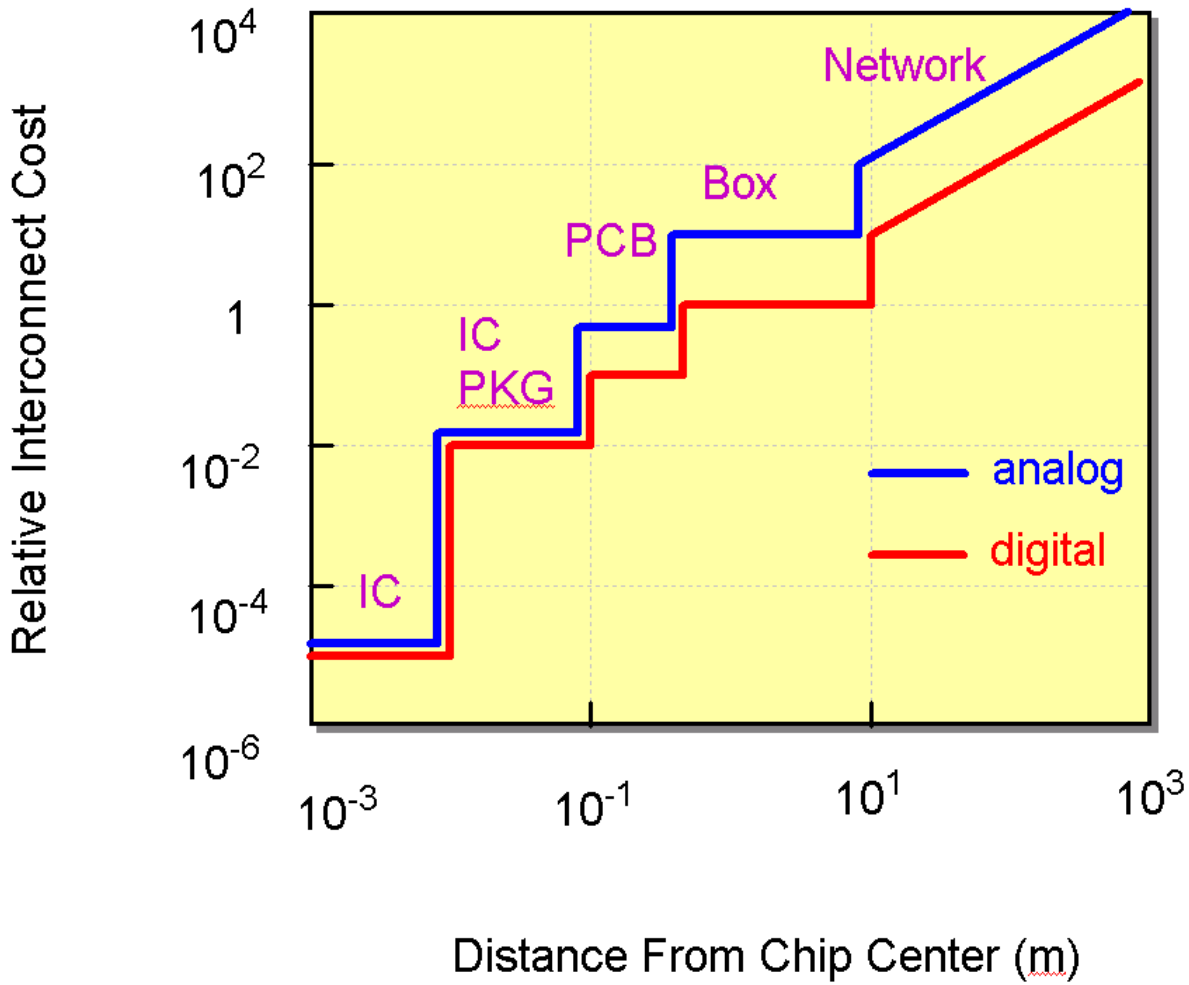
Packaging, Interconnect, and Systems Issues

Paul O'Connor, Brookhaven National Laboratory

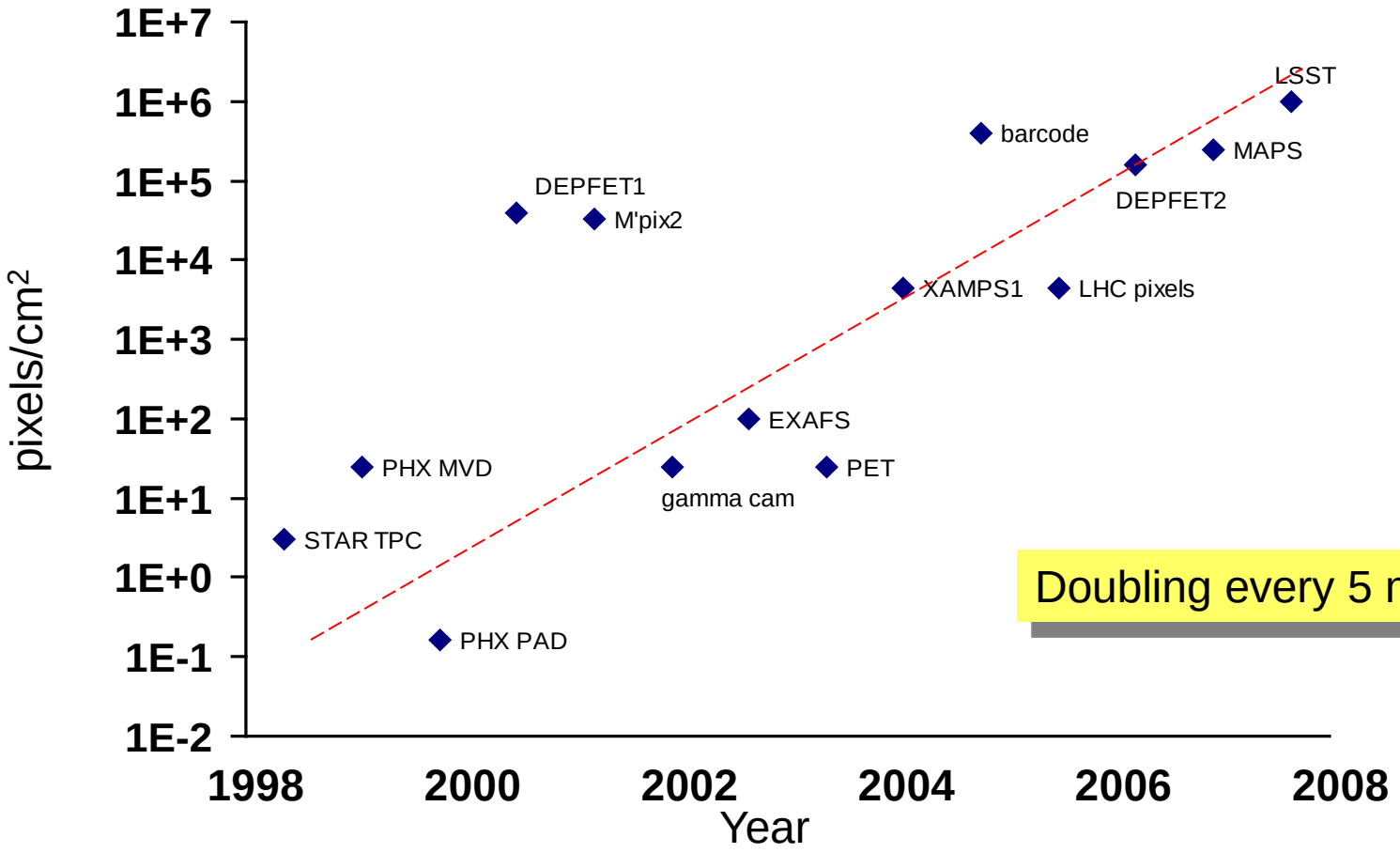
IEEE Nuclear Sciences Symposium/Medical Imaging Conference

October 30, 2010

Cost of interconnect



Pixel density



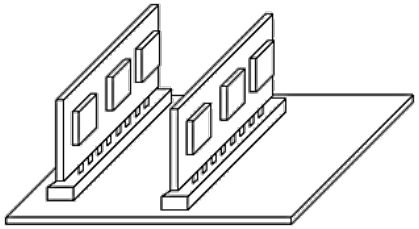
Doubling every 5 months

Interconnect issues in monolithic front ends

- Detector – Front End
  - Lowest possible capacitance for low noise
  - Maintain small form factor
  - Ease of assembly
- Front end – Data Acquisition
  - Analog processing to reduce the required level of digitization
    - *sampling*
    - *peak detection*
    - *multiplexing*
  - Efficient use of expensive “analog” interconnect

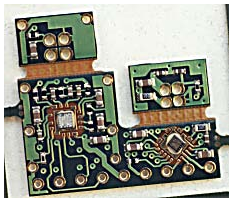
Detector – FE interconnect choices

- **board-to-backplane**
  - easy to test, repair
  - large boards possible
  - connector pins are failure points
  - coarse pitch and high capacitance (> 1pF)

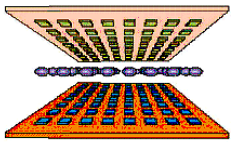


- **standard SMT package soldered to board (QFP or BGA)**
  - easy to test, difficult to repair
  - capacitance down to 0.2 pF for small packages
  - board area limited by reflow oven capacity

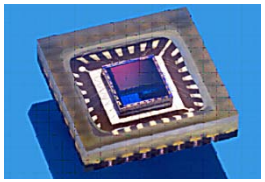
- **wirebonded chip-on-board**
  - difficult to test, assemble, and repair
  - board area limited by wirebonder
  - fragile
  - low capacitance (0.1 pF)



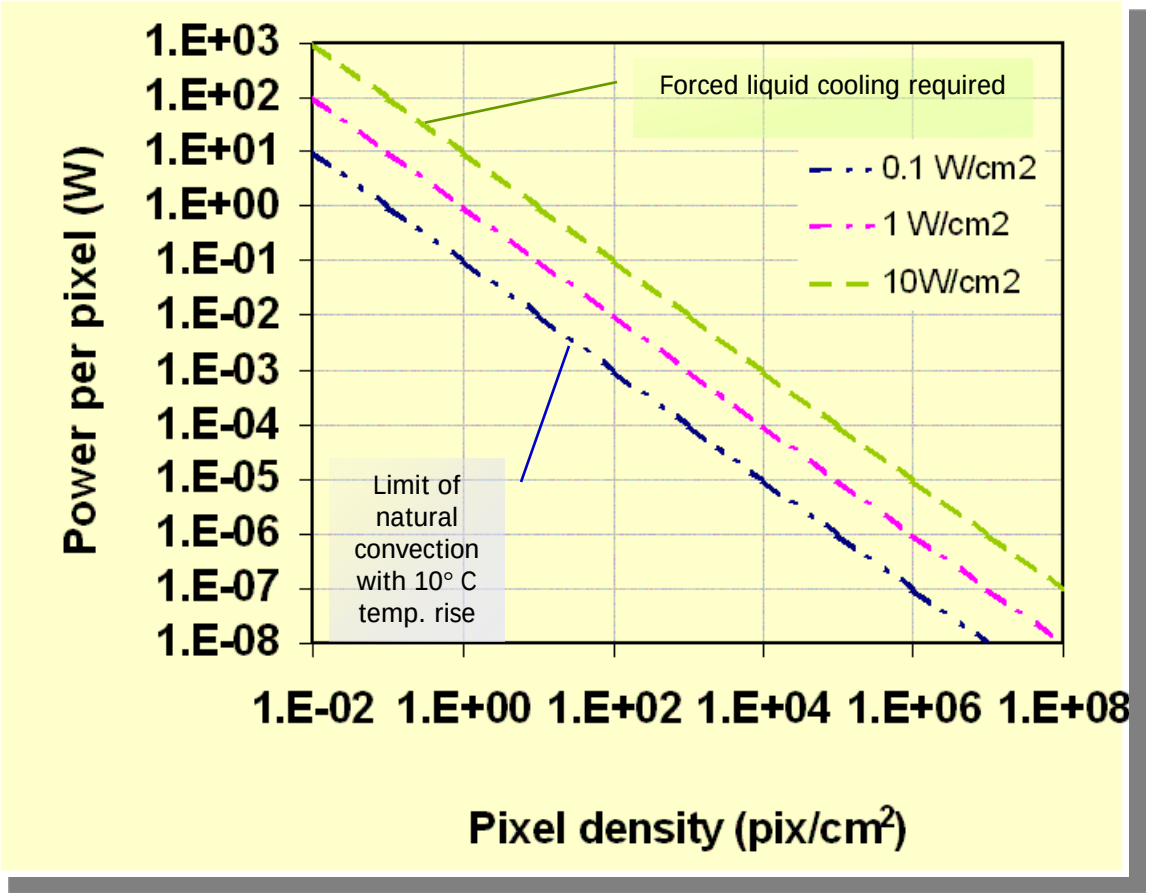
- **bump-bonded flip-chip**
  - can match pixels with pitch from ~30 – 1000 μm
  - difficult to test, assemble, and repair
  - circuitry has to fit in same area as pixel



- **monolithic detector/electronics**
  - interconnect is created as part of the detector fabrication process
  - ultra-low capacitance (few fF)

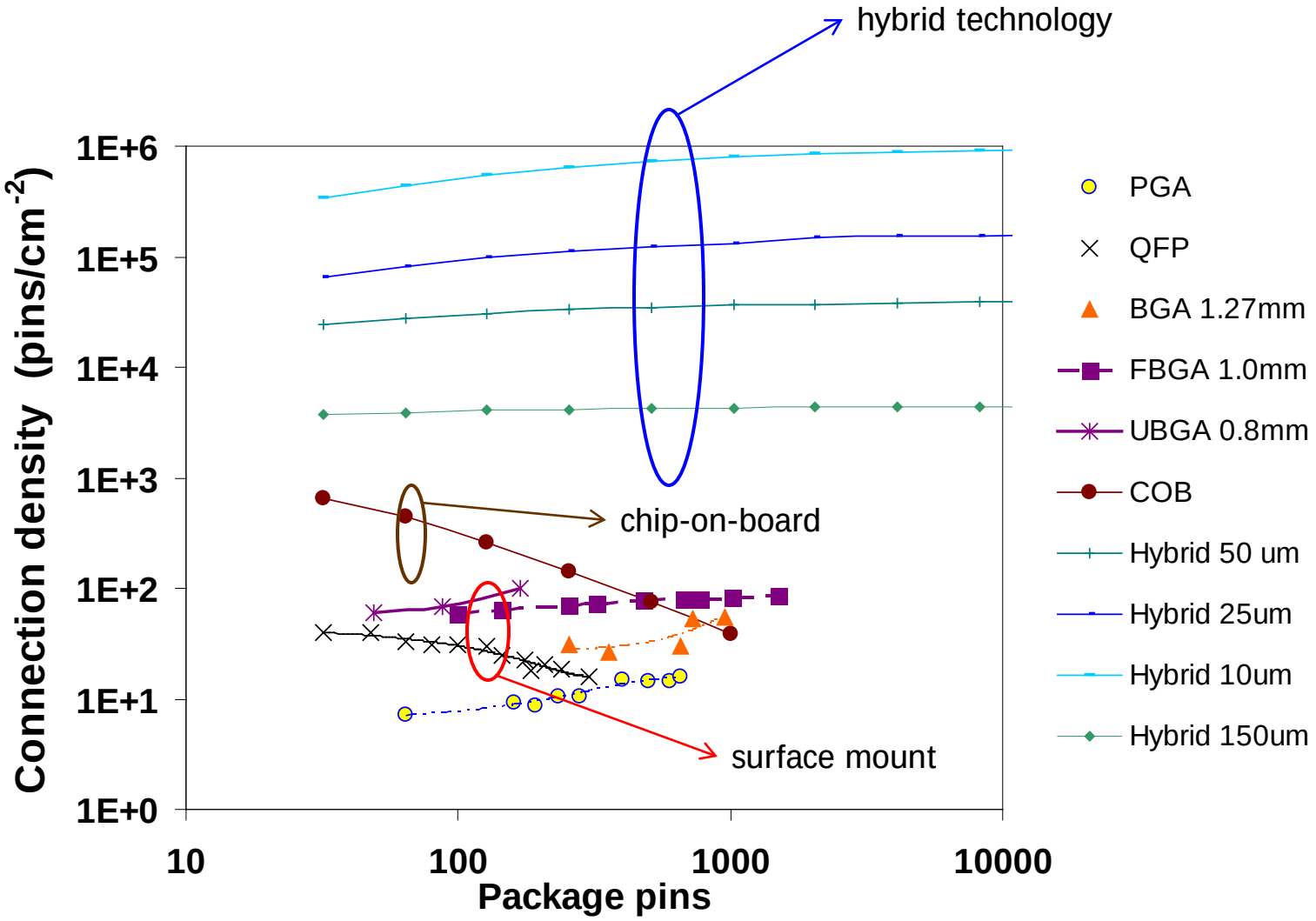


Power density



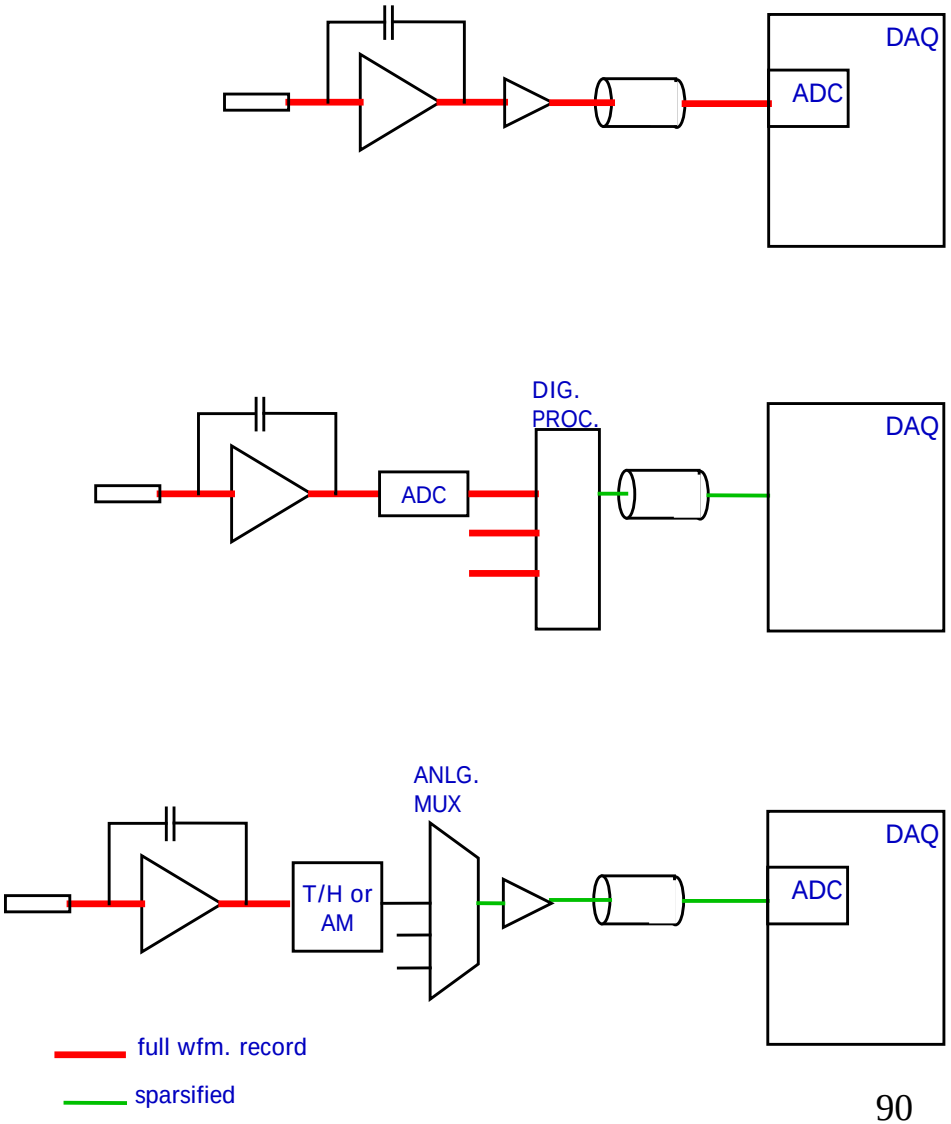
- On-detector power density is limited by cooling capability.
- Electronics for high-density detector must be extremely low power.

Packaging density

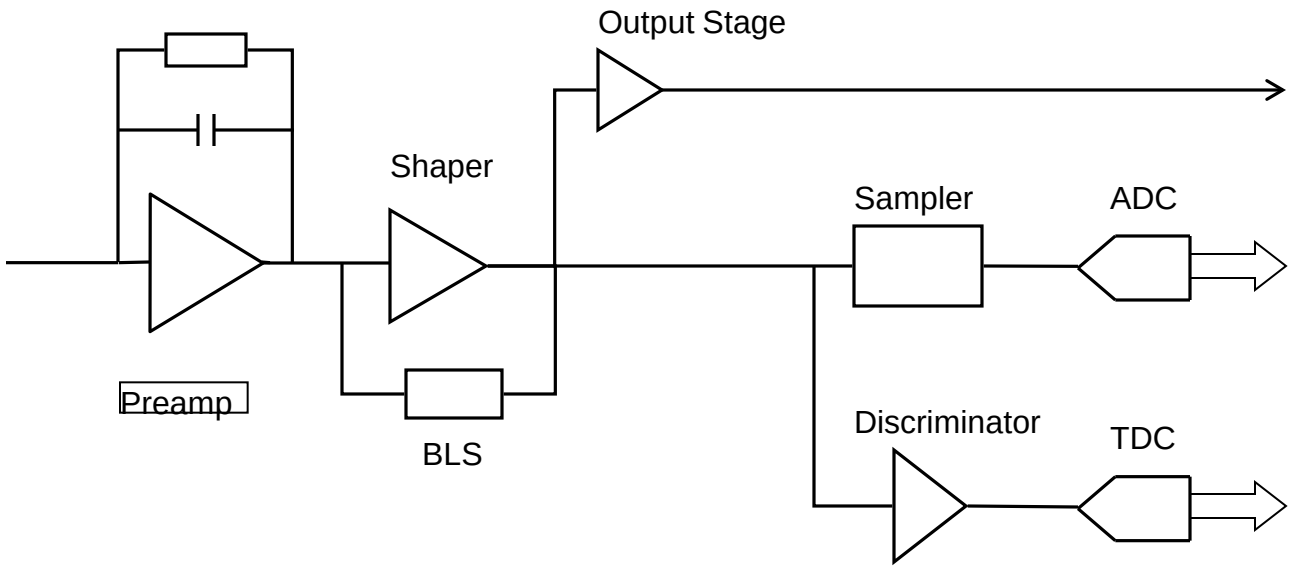


Front end – DAQ interconnect

- High bandwidth analog interconnect is expensive and bulky.
- Due to the low occupancy, this interconnect bandwidth is mostly wasted.
- Digitizing every channel is inefficient in a low-occupancy system.
- Existing approaches to sampling and multiplexing are inefficient:
  - *track/hold needs trigger, incurs deadtime during readout*
  - *analog memory (SCA) deadtimeless but needs trigger, multiple samples, no sparsification, complex controller*



Putting it all together



Power Efficient Architecture

- Highest power functions:
  - *charge preamplifier*
  - *analog line driver*
  - *ADC*

- Staying within a power budget and achieving maximum performance involves careful tradeoff.

Figure of merit for charge amplifiers and ADCs

$$FOM_{CSA} = \frac{P_d \cdot \tau_p}{Q_{\max} / \sigma_Q}$$

- Expresses the power cost of achieving SNR and speed
- Can be applied to front ends in any technology
- Corresponds to figure of merit for analog-digital converters:

$$FOM_{ADC} = \frac{P_d}{2^{ENOB} \cdot f_s}$$

Rule-of-thumb estimates

- Use FOM_{CSA} ~ 1pJ, calculate most quantities of interest.
- Given P_{max}, rate r, what is achievable SNR?

$$SNR = \frac{P}{FOM_{CSA} \cdot 10r}$$

  – *e.g.* P *=1mW,* r *=100kHz, SNR ~ 10^3*
- What power needed to get timing accuracy σ_t?

$$\sigma_t \approx \frac{\sigma_V}{dV/dt} \sim \frac{\tau_p}{SNR}; \quad P = \frac{FOM_{CSA}}{\sigma_t}$$

  – *e.g.* σ_t *=2ns,* P *~ 50μW*

Figure of merit for charge amplifiers (FOM_{CSA}) vs. detector capacitance

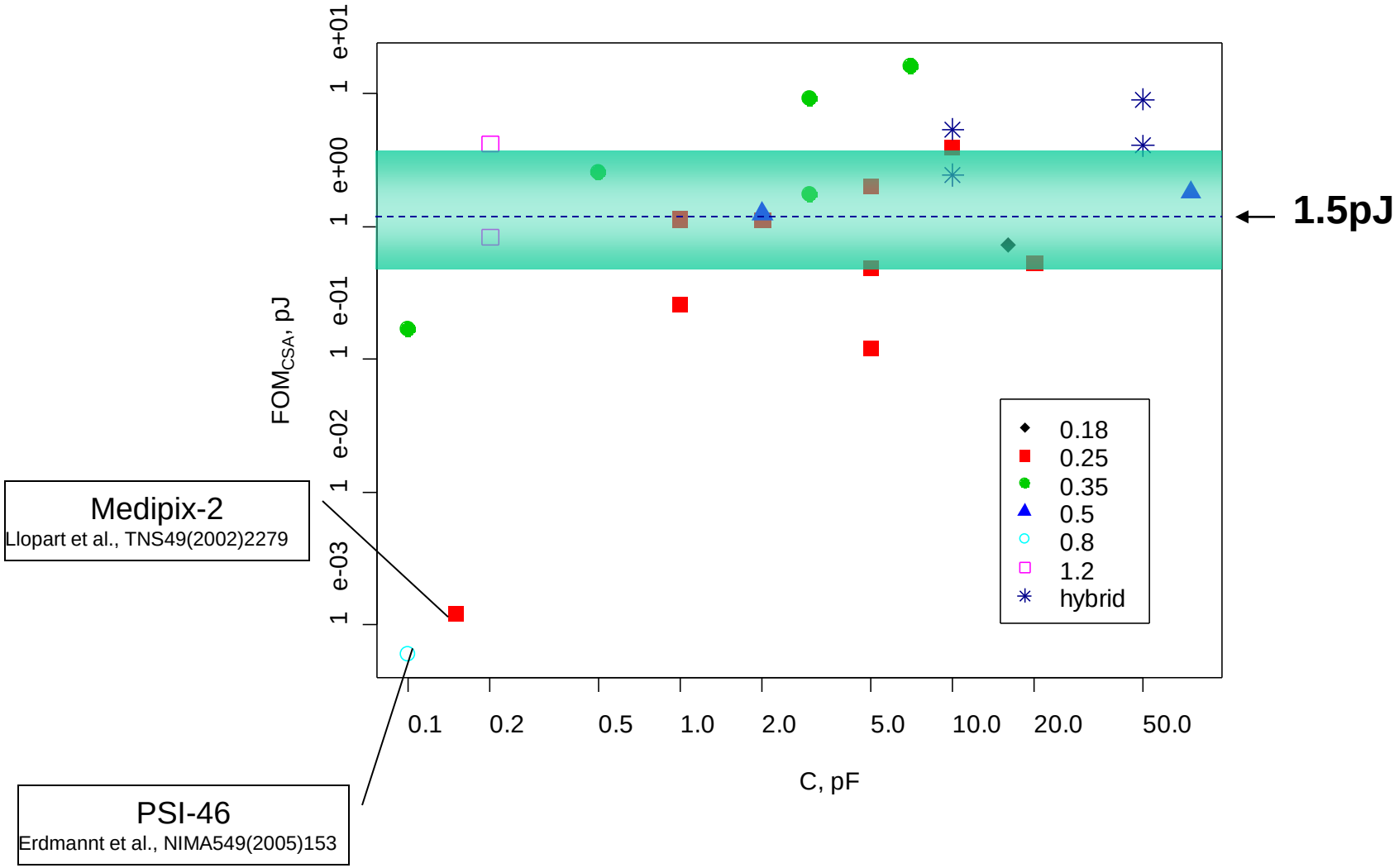
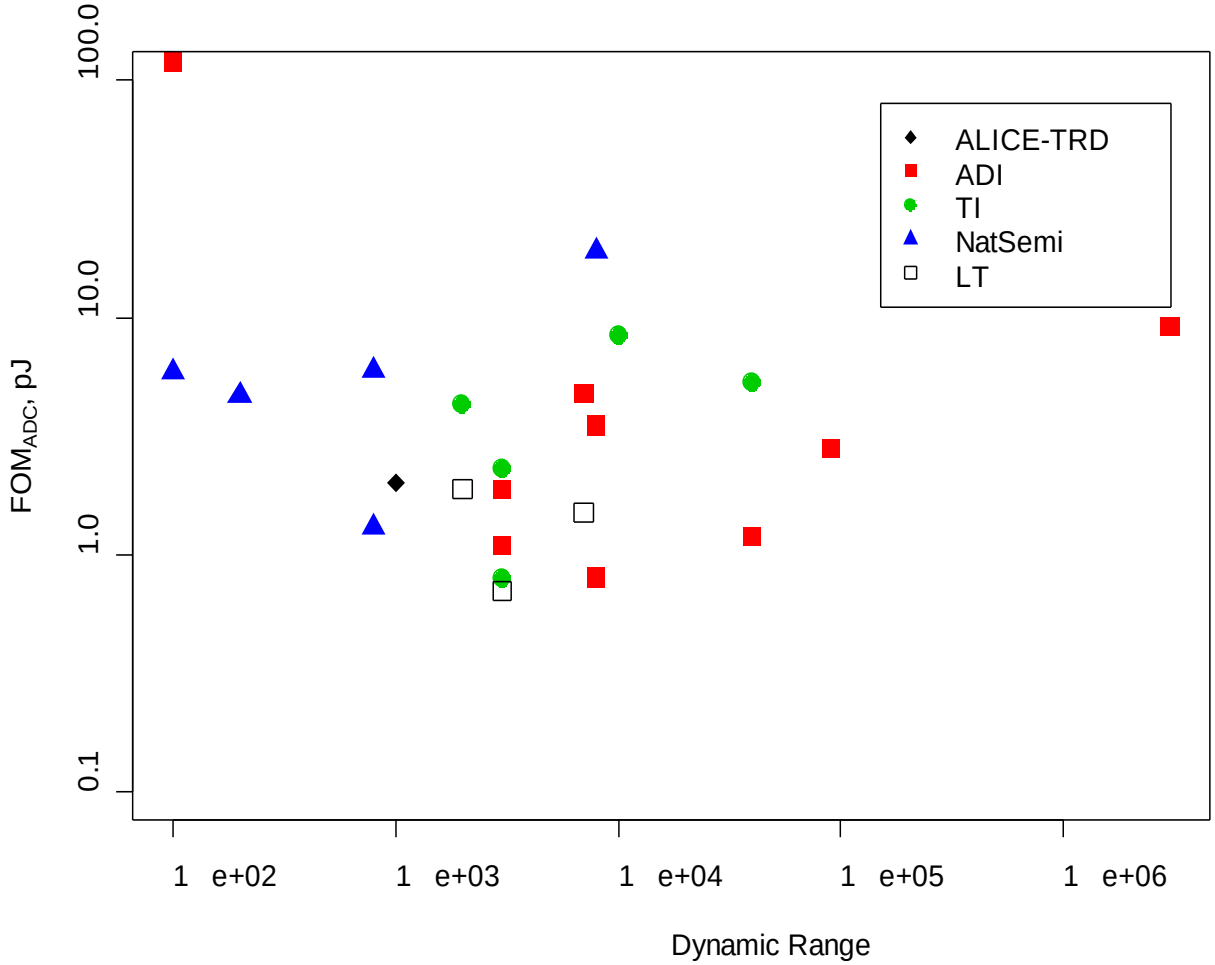


Figure of merit for ADCs (FOM_{ADC}) vs. dynamic range



Architecture choices

- Digital waveform recording of every channel requires ADC to have:
  - *same SNR as charge amplifier*
  - *sampling frequency 2X – 20X higher than analog bandwidth*
- **Guarantees** $P_{ADC} >> P_{CSA}$
- Better architecture: capture and buffer the analog information on the FEE ASIC, then steer samples to the ADC
- Switched capacitors or peak detectors can serve as the sampling cells
- Use analog buffers (memory) with simultaneous READ/WRITE to avoid deadtime

Example: TPC Digitization Power

- N_{pads} 8000
- $N_{timeslices}$ 500
- N_{voxels} 4×10^6
- t_{drift} 7μs
- f_{trig} 2kHz
- Occupancy 2%

- Digitization Energy (12 bit resolution):
  - *10^{-12} J/bit * 2^{12} * N_{voxels} = 16 mJ*
- Power (FADC):
  - *16mJ / 7μs = 2000W (250 mW/chan)*
- Power (buffer and readout at 2 kHz trigger rate):
  - *16mJ / 500μs = 30W (4 mW/chan)*

- ***Compare with <u>0.75mW/chan</u> for amplifier + <u>0.6mW/chan</u> for PD + TAC.***
- ***With sparsified readout of only occupied channels buffered in PD: P_{ADC} ~ 0.6W (75 μW/chan).***

Summary

- Modern IC technologies, optimized for digital performance, are challenging for analog design but offer exceptional integration density, speed, and radiation tolerance.
- Noise is limited by available power, detector properties, event rate, and the 1/f properties of the technology.
- In addition to optimizing the first transistor, choice of shaping function is also important in noise optimization.
- High-order shapers improve the power/noise tradeoff, and also improve pileup and charge collection performance.
- An empirical figure of merit for charge amplifiers, analogous to that for ADCs, can be used to guide design choices.
- Reducing the number of analog-to-digital conversions and minimizing off-chip analog signal transmission (where possible) improves noise by allowing power to be allocated to the front end.

Design Examples:

1. Time Projection Chamber (TPC) Readout:

   An example of Detector Signal Processing Design and System Fabrication

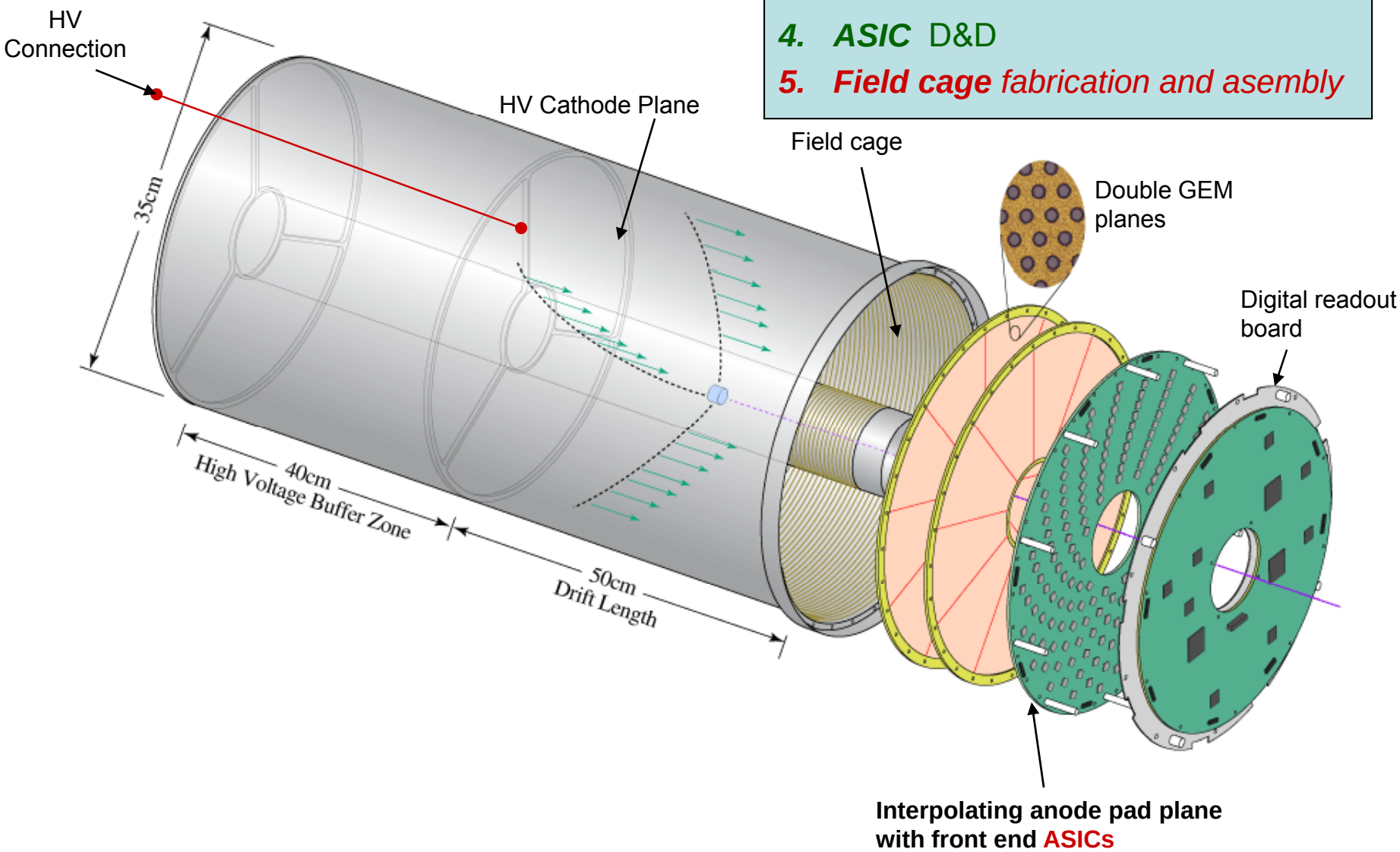
2. Examples of Low Noise ASICs

Veljko Radeka, BNL

NSS Short Course 2010

TPC Critical Technologies:

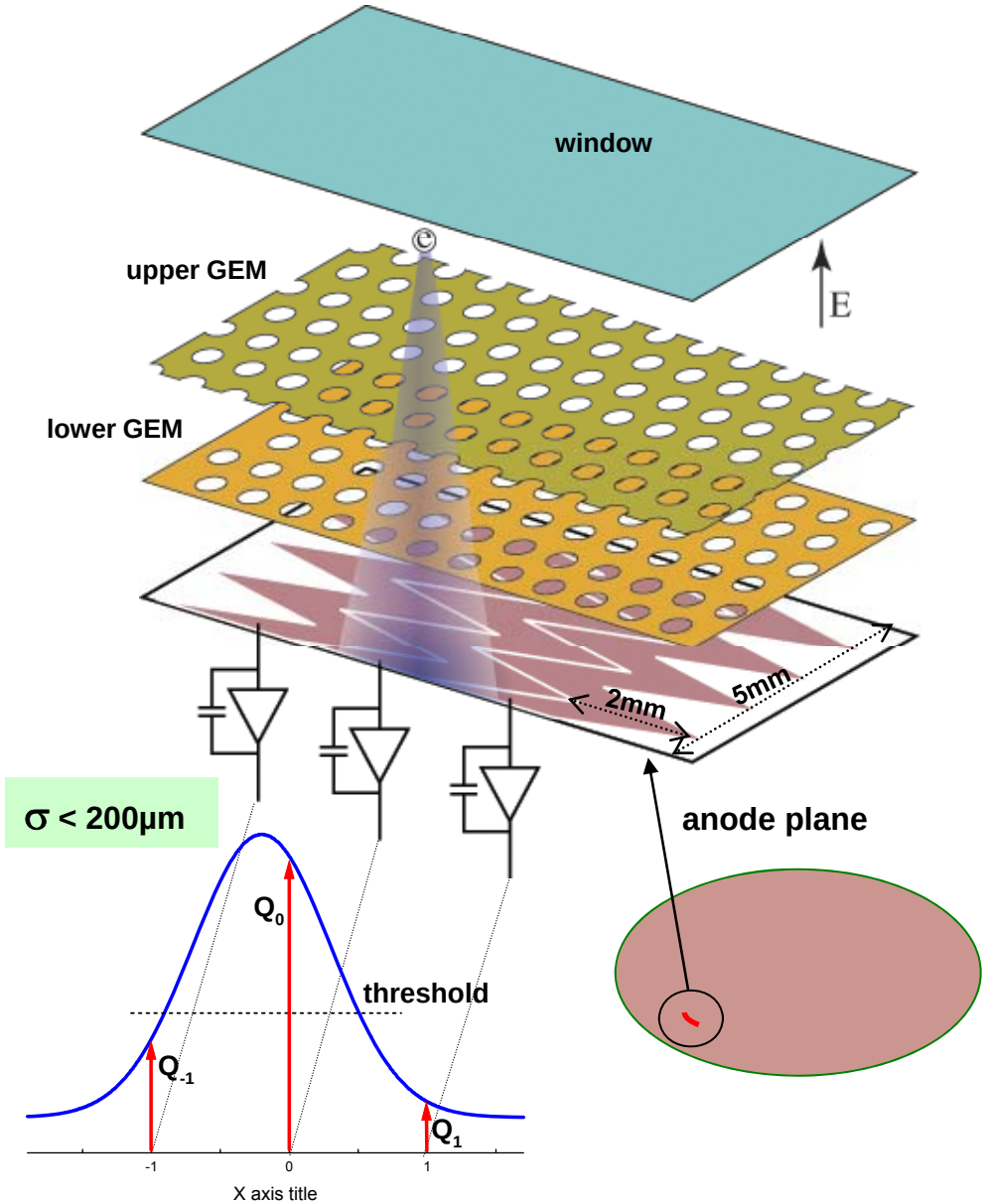
1. ***GEM*** *vs MWPC*
2. *Anode pad configuration -* ***chevron***
3. ***Anode pad – ASIC board topology and fabrication***
4. ***ASIC*** D&D
5. ***Field cage*** *fabrication and asembly*



TPC - Key Features and Parameters

- Designed for low rate (~kHz), low multiplicity environment: single sample per channel per trigger
- TPC Active Volume:
  Inner diameter ~9 cm; Outer diameter ~35 cm; Drift Length: 50 cm
- Double GEM amplification, ***gas gain <1000***
- Drift field ~ 600V/cm (30kV high voltage) max., total drift time ~ 5-7 μs.
- Interpolating zigzag anode pad plane, ~200 μm position resolution for stiff tracks; ***Pad density >10 times higher than in previous large TPCs***
- Readout channel count, ***7296***
- Customized ASICs, 32 channels per chip, 40mW per chip, ***10+6 W total***
- Electronic noise <***250e***, 500ns peaking time, single peak time and amplitude measurement, timing resolution ~ 5-15 ns
- 8 sets of ADCs digitize the sparsified and serialized data streams, worst case event processing time <0.5ms

Front-End Electronics Specifications



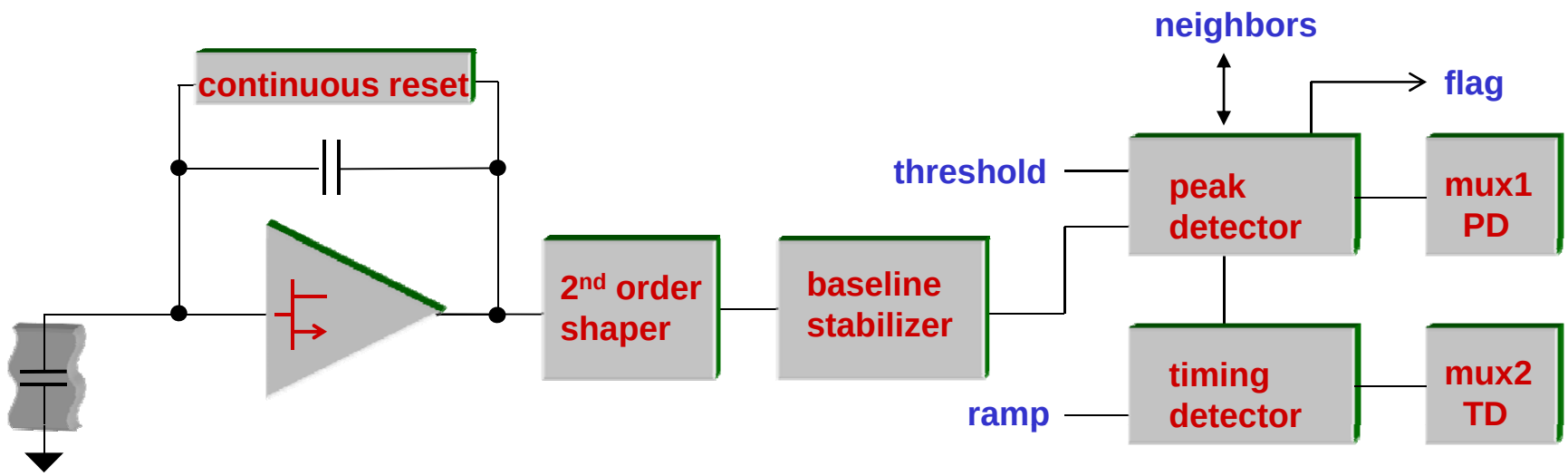
Tracking

- Rate: 2kHz
- Multiplicity: 3 tracks max
- Charge of triggered pad
- Charge of neighbor pads (centroid)
- Timing of triggered pad

Front-End Requirements

- **ENC < 250e⁻ rms** (S/N>100 at 4fC min)
- **Timing Res. < 20ns rms** (drift ~ 7μs)
- **Readout Time < 500μs** (all channels)
- **Power < 1.5mW** (<10W total)
- Preamplifier - shaper
- Pulse amplitude (peak detect) + analog memory
- Pulse timing (TAC) + analog memory
- Neighbor channel/chip logic
- Gain equalization +/- 30%, 3-bit
- Channel calibration capacitance
- Channel masking
- Analog monitor and analog buffer

ASIC Readout Channel - Block Diagram



INPUT n-MOSFET
- optimized for operating region
- ENC < 250 rms electrons
- NIM A480, p.713

CONTINUOUS RESET
- feedback MOSFET
- self adaptive
- low noise
- fully compensated
- US patents 5,793,254 & pend.
- NIM A421, p.322
- TNS 47, p.1458

SHAPER
- amplifier with passive feedback
- dual stage multiple feedback
- 2nd order, 600ns peaking time
- adjustable channel gain (3-bit)

BASELINE STABILIZER (BLH)
- band-gap referenced
- low-frequency feedback
- slew-rate limited follower
- high dc stability < 1mV
- low channel dispersion < 4mV
- TNS 47, p.818

PEAK DETECTOR
- two-phase configuration
- offset error cancellation
- high absolute accuracy < 0.2%
- US patent 6,512,399
- NIM A484, p.544

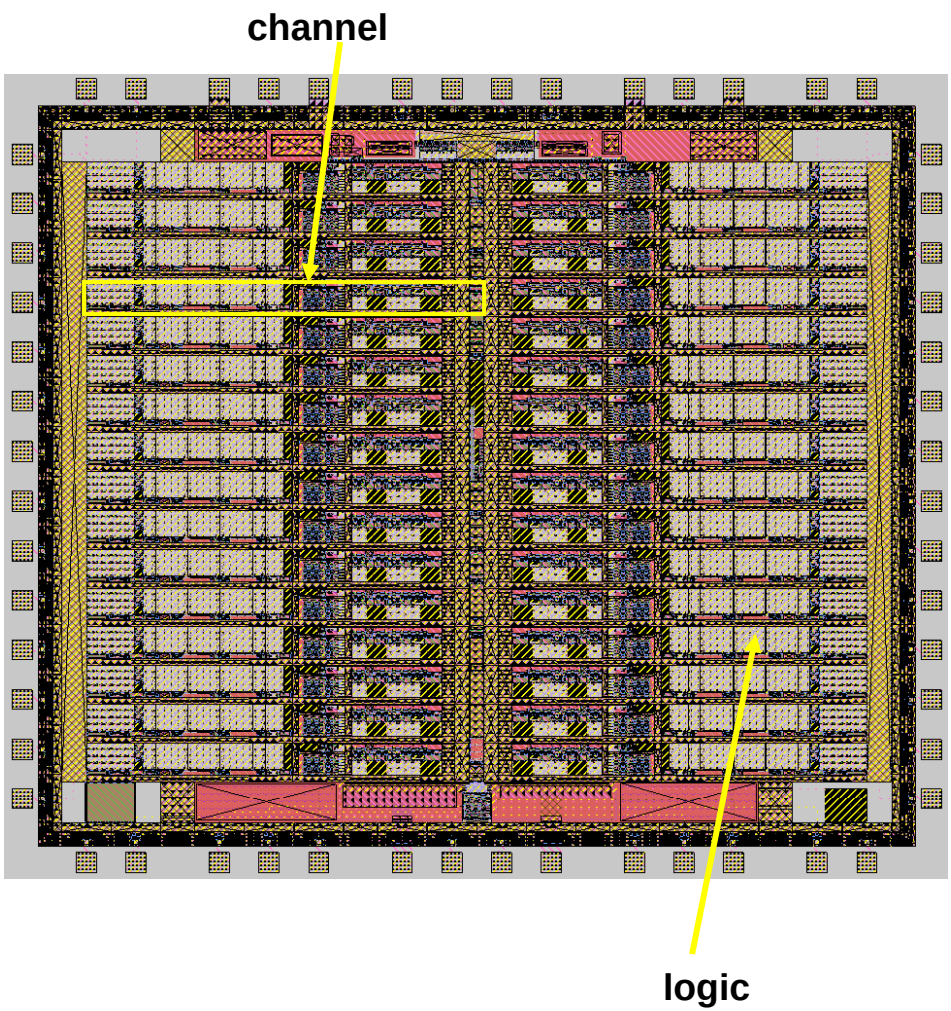
TIMING DETECTOR
- time-to-amplitude converter
- internal or external ramp
- two-phase configuration
- timing resolution < 20ns rms

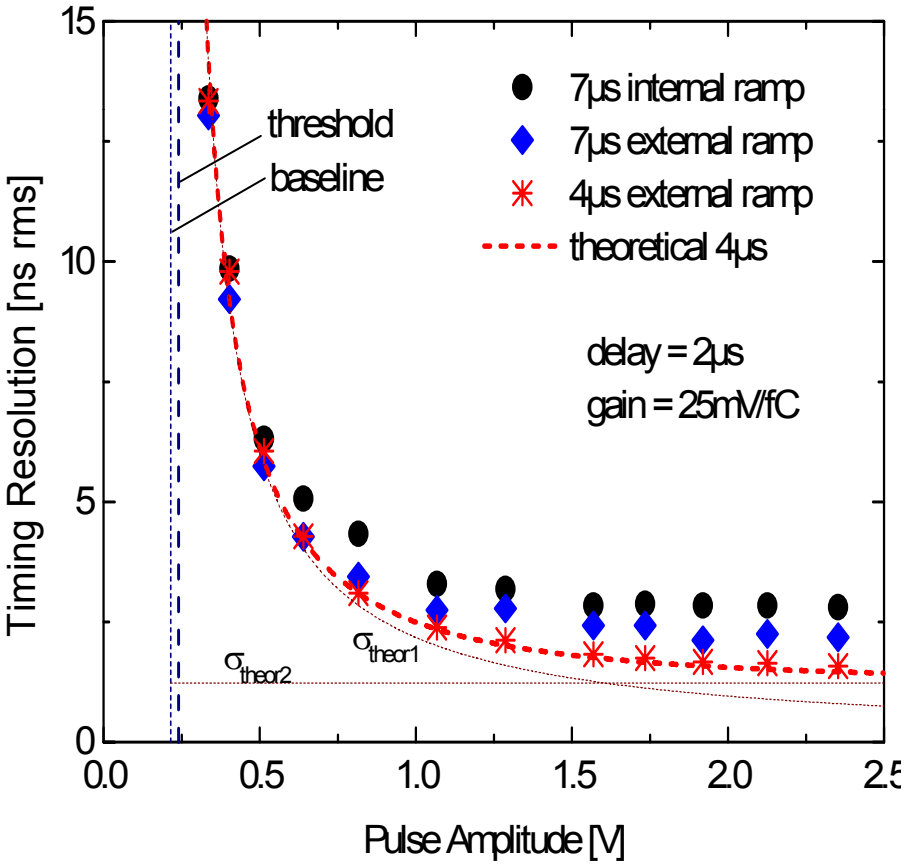
≈ 350 µW

≈ 900 µW

TPC ASIC Layout

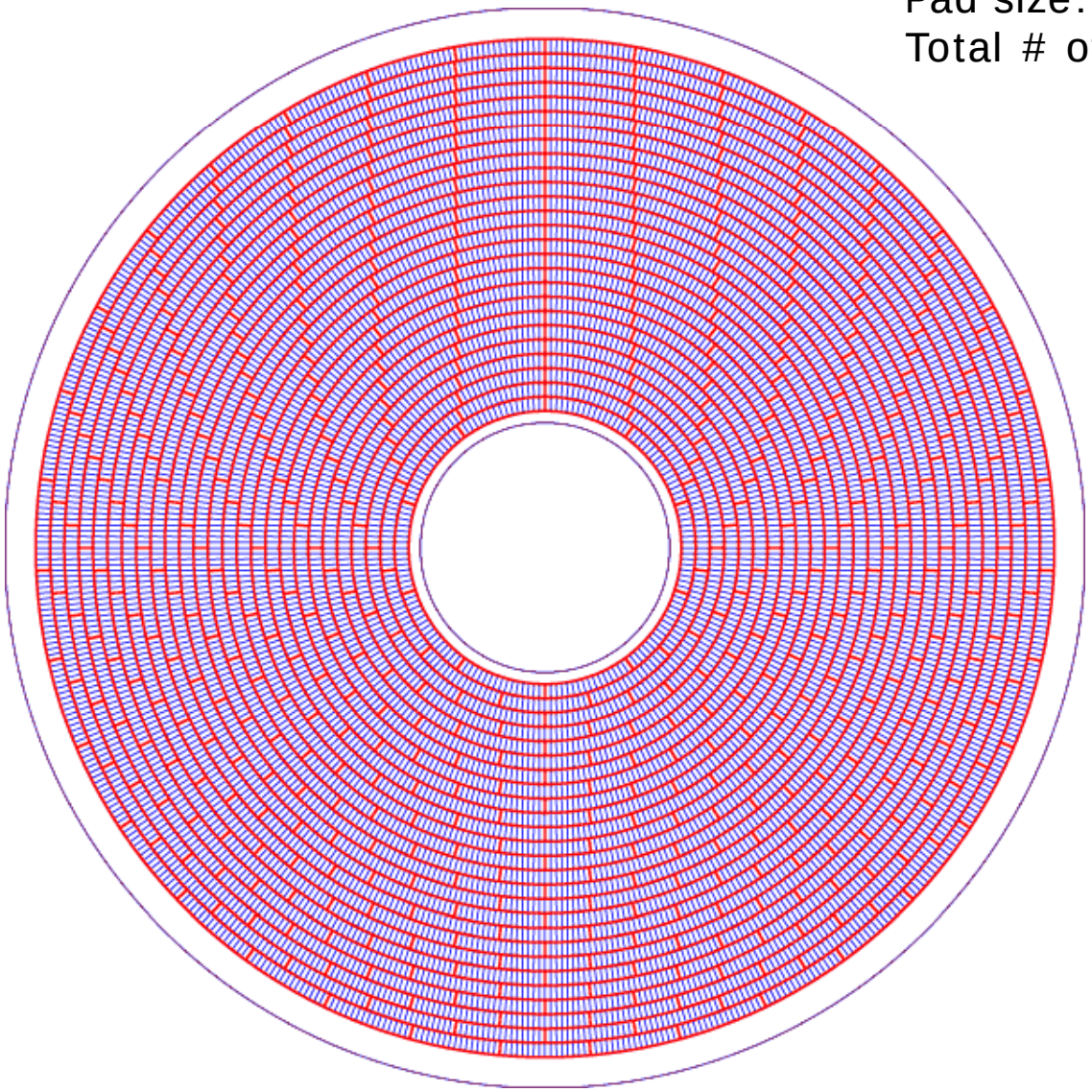
- TSMC 0.25µm
- 32 channels
- 3.1 x 3.6 mm² (~0.35 mm²/channel)
- 47k MOSFETs
- 1.2 mW/channel

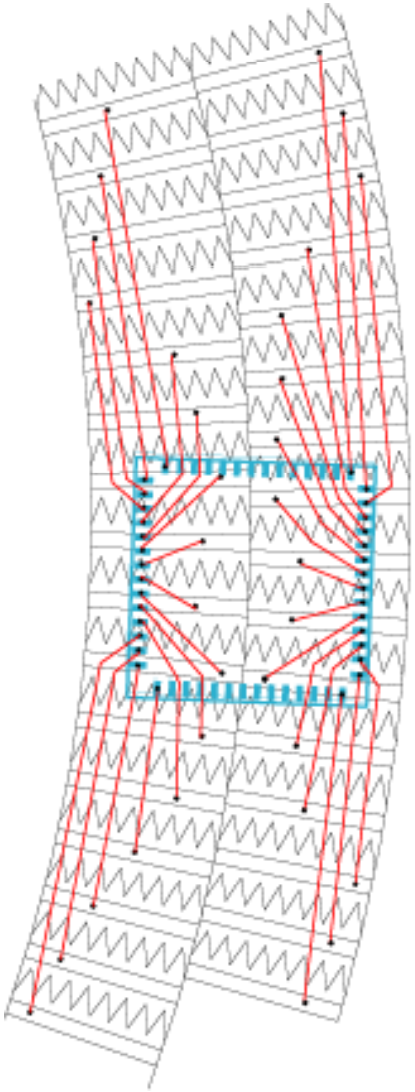




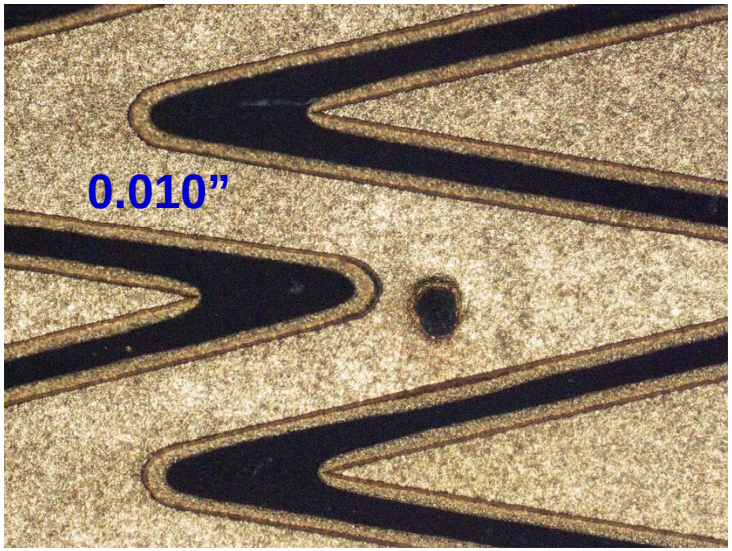
Layout of the Anode Pad Plane – Topology of the Readout Board

Pad size: ~2mmx5mm, 22 rows
Total # of Channels: ~ 7296

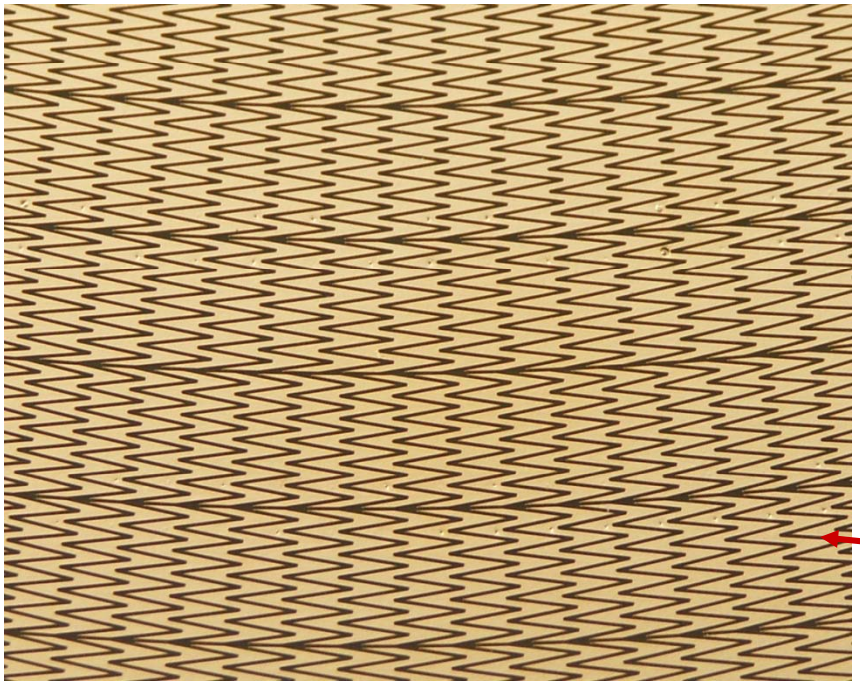




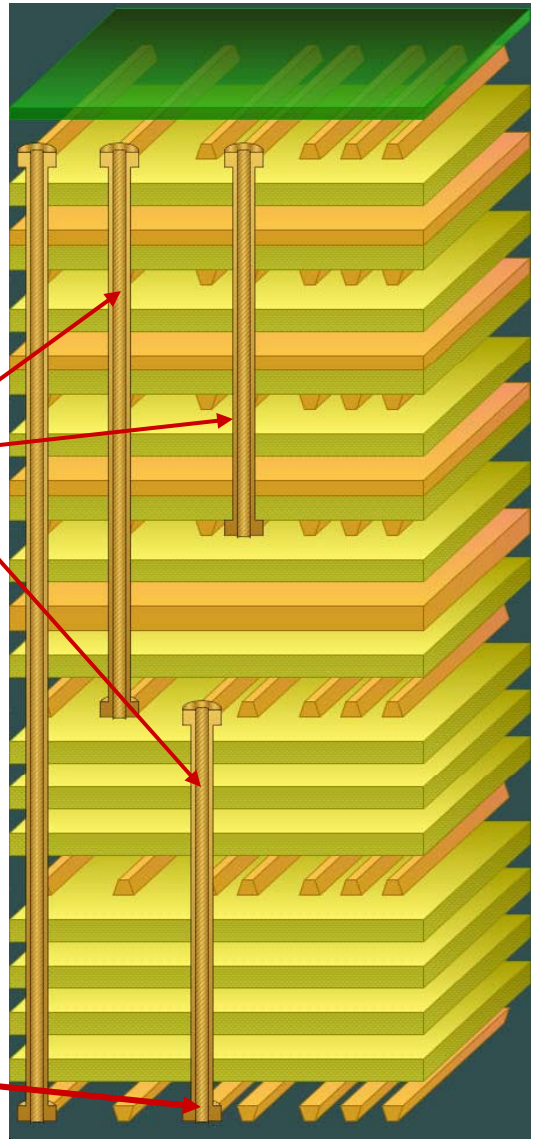
Anode Pad Plane – Asic Board: *A major topology and fabrication challenge (solved)*



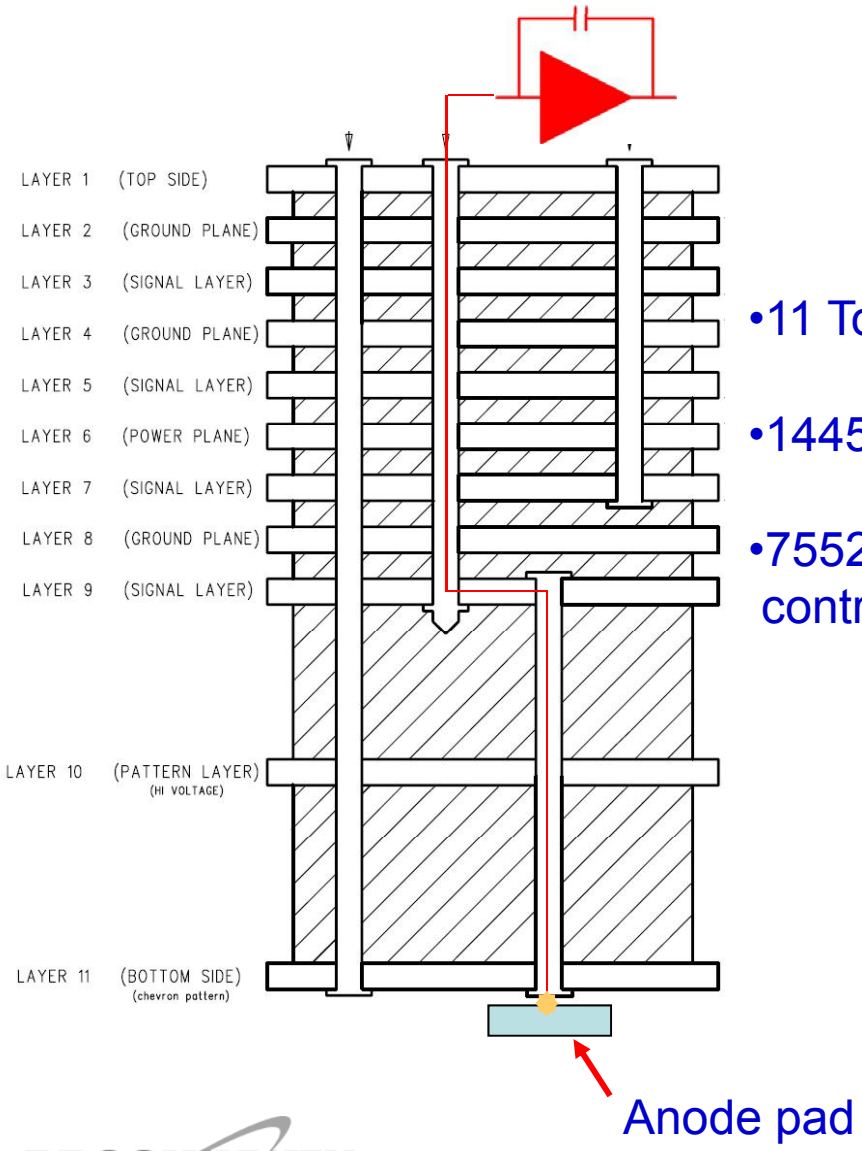
0.004”



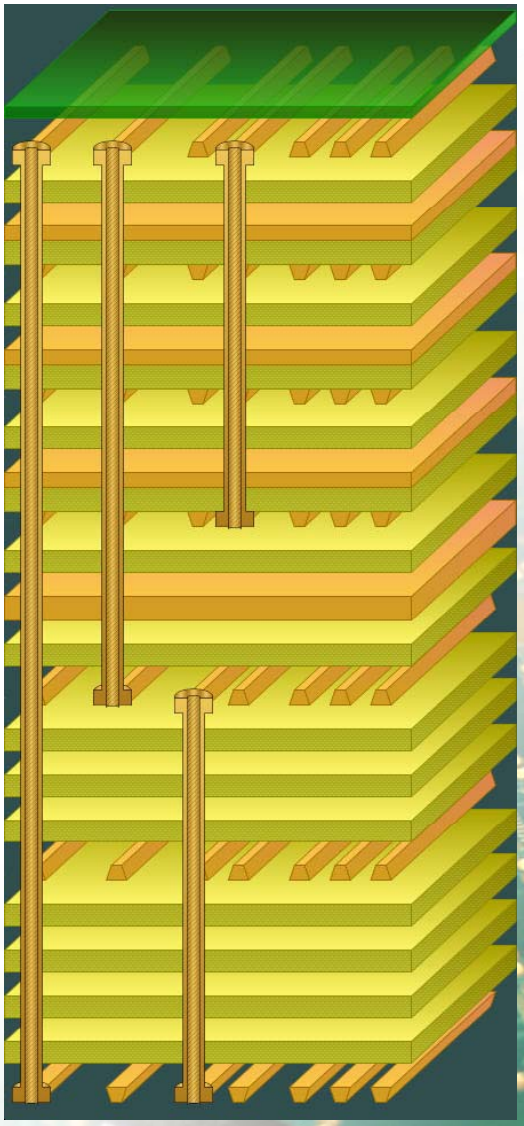
“Blind Vias”!



Board fabrication – Inner details



- 11 Total Layers
- 14459 Blind Vias
- 7552 Blind Vias with controlled depth drilling



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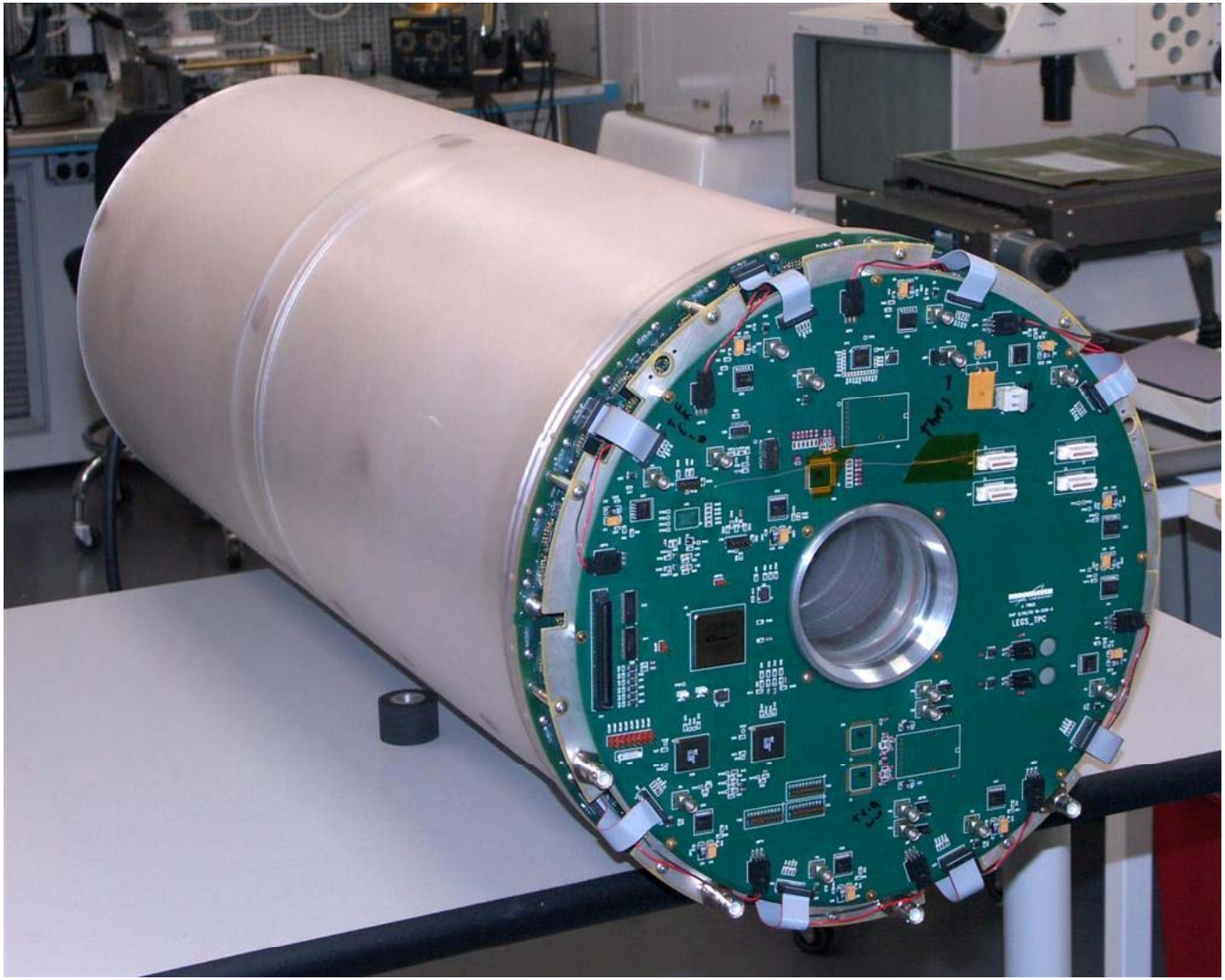
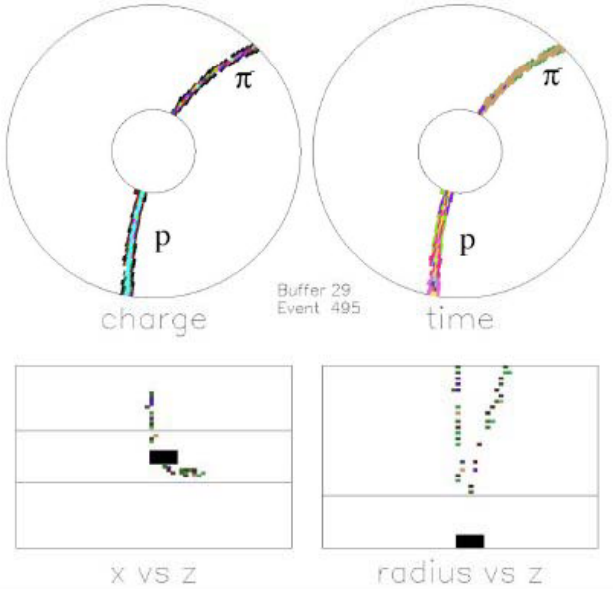
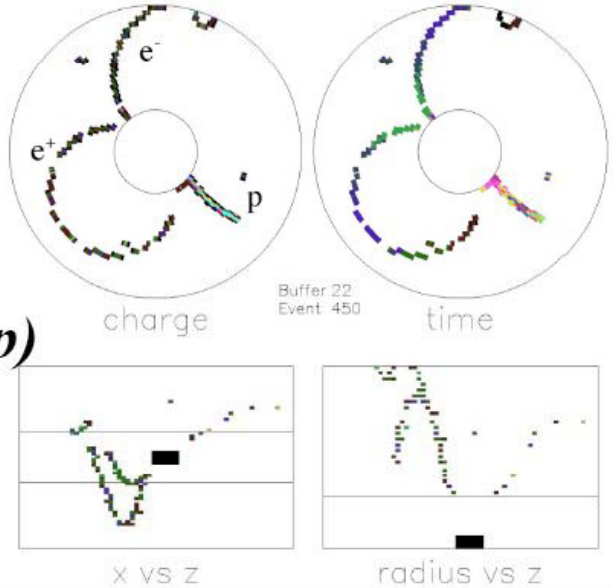

LEGS_TPC

Sample TPC events

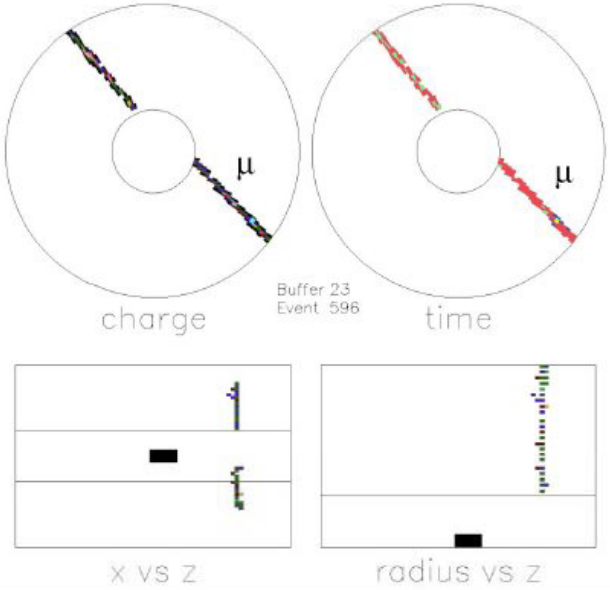
$\gamma\, n\ (p)$
$\downarrow$
$\pi^- p\ (p)$



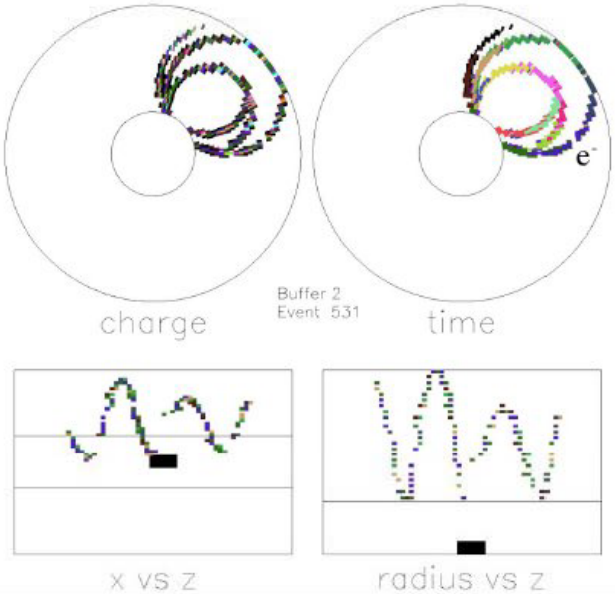
$\gamma\, n\ (p)$
$\downarrow$
$\pi^0 p\ (p)$
$\downarrow$
$\gamma(e^+e^-)\gamma p(p)$



Cosmic
μ



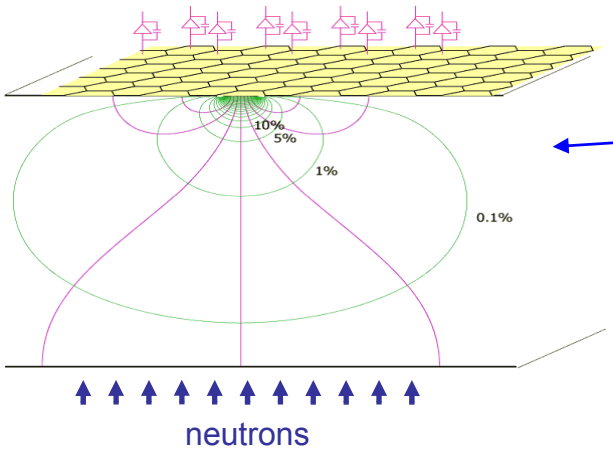
atomic
e^-
spiral



2. Examples of Low Noise ASICs

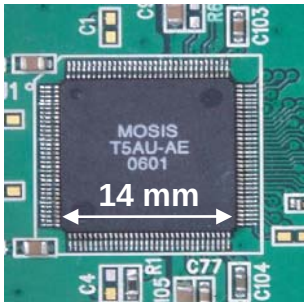
ASIC for Spallation Neutron Source Experiments

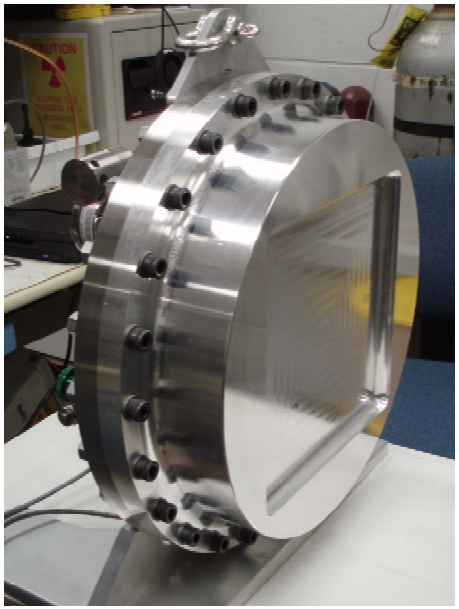
^{3}He detector for small angle neutron scattering experiments

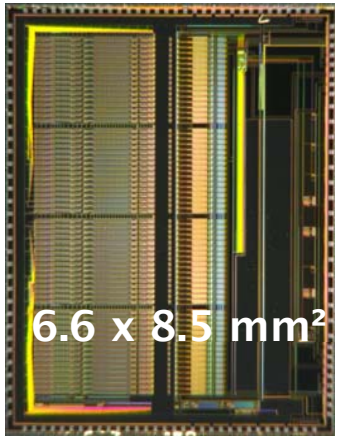


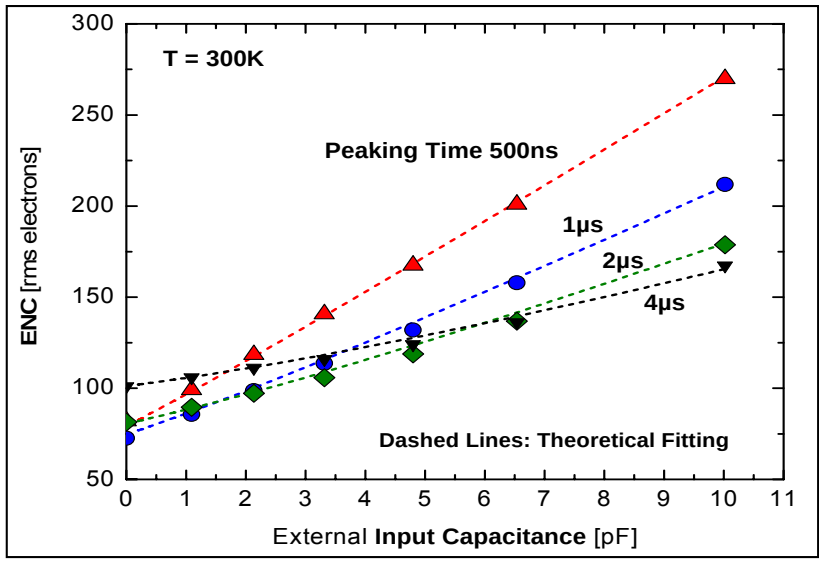
- Low-noise front-end with unity gas-gain
- Single-pad induction (small-pixel effect)
- ^{3}He pressure for max 3-pad charge sharing
- Full size: 196 x 196 pixel array (10^8 n/s)
- Pixel 25 mm², **5 pF**, rate 5 kHz / pixel

- 64 channels - **mixed signal**
- low-noise charge amp.
- peak detector, 6-bit ADC
- 18-bit timestamp
- **110 e$^-$ resol., 1.5 mW/ch.**
- sparse readout and FIFO
- 300,000 transistors





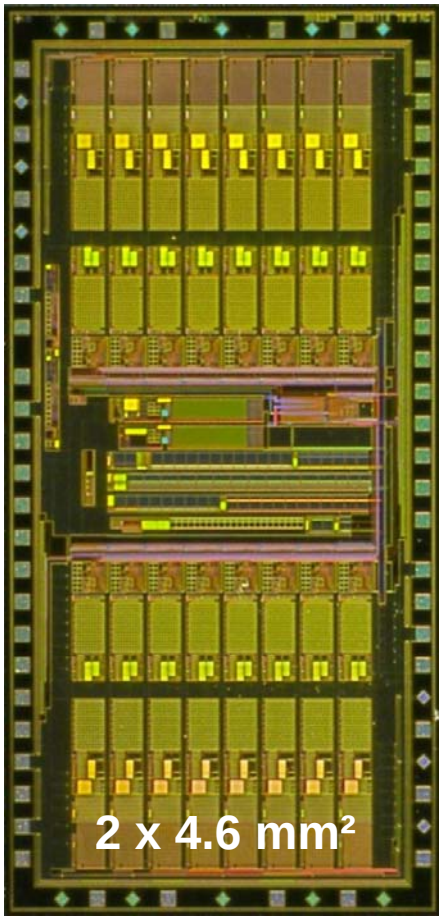




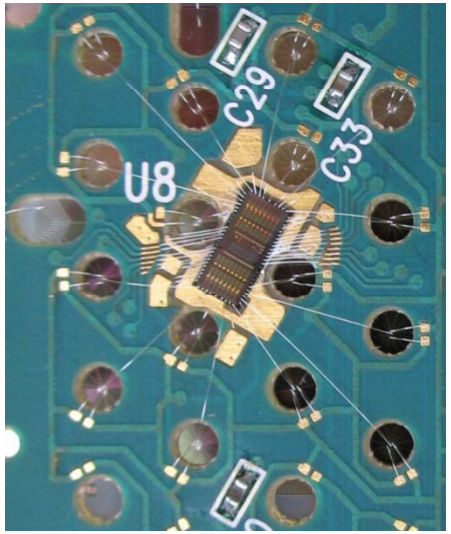
G. De Geronimo et al., IEEE TNS 54 (2007), collaboration with ORNL

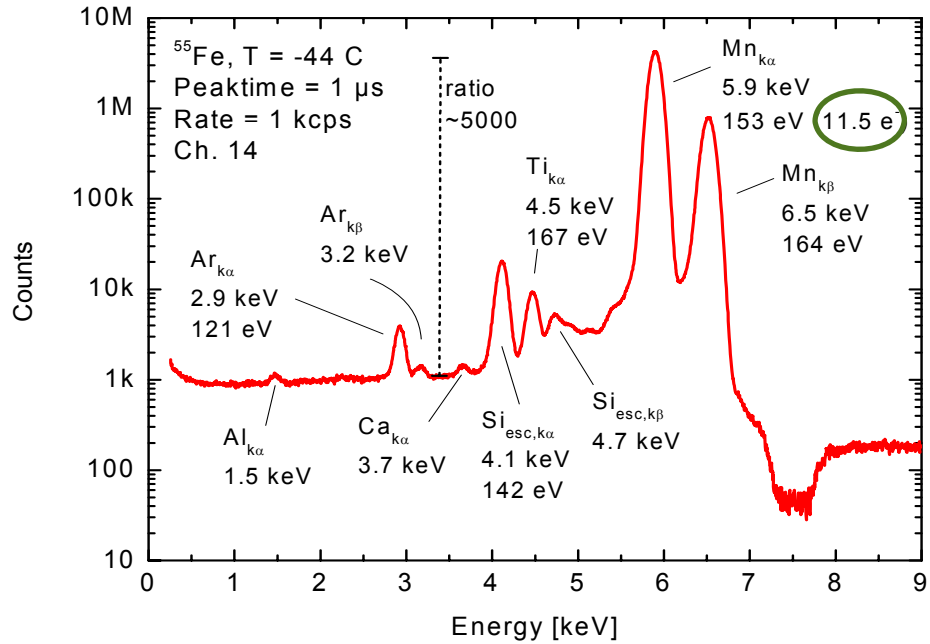
ASIC for High-Resolution X-ray Spectroscopy

- Collaboration with NASA at XRS for elemental mapping
- Based on Silicon Drift Pixels



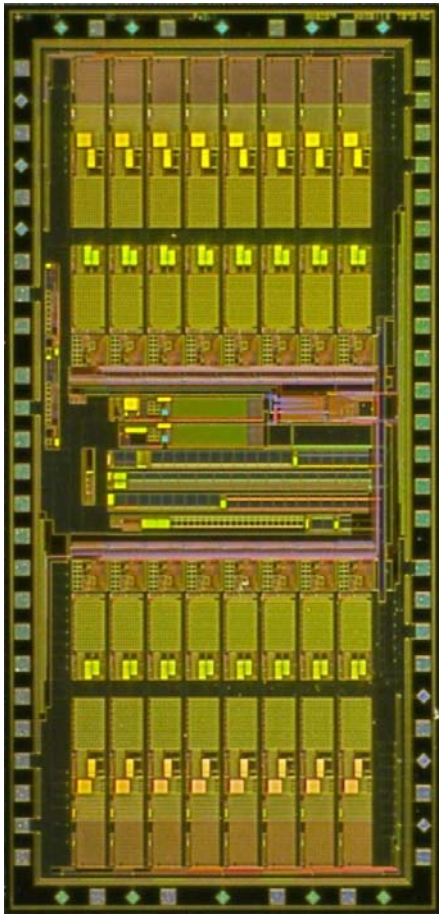
- 16 channels - **mixed signal**
- very low noise amplification
- **11 electrons** resolution
- Pixel **<1pF**
- **1.2 mW/channel**
- peak detection, sparse readout
- 30,000 transistors



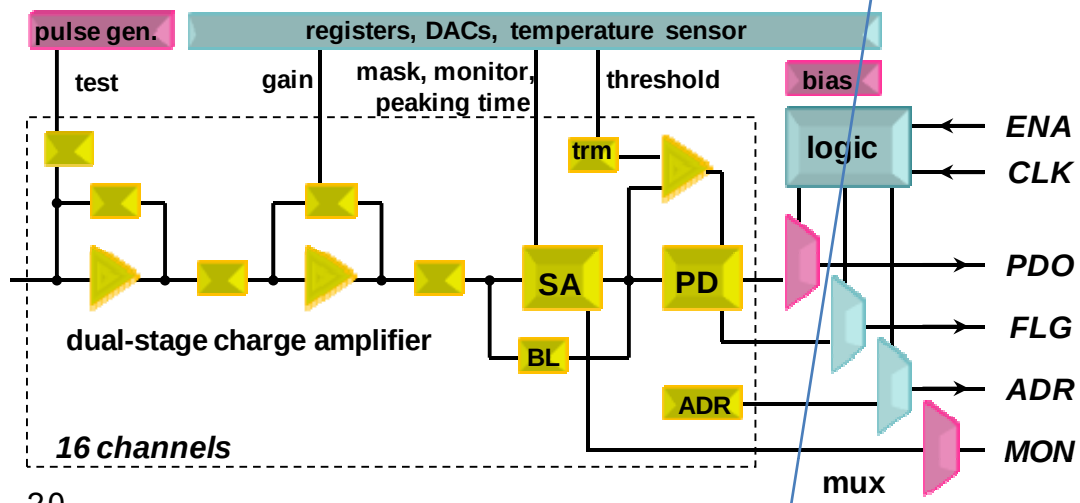


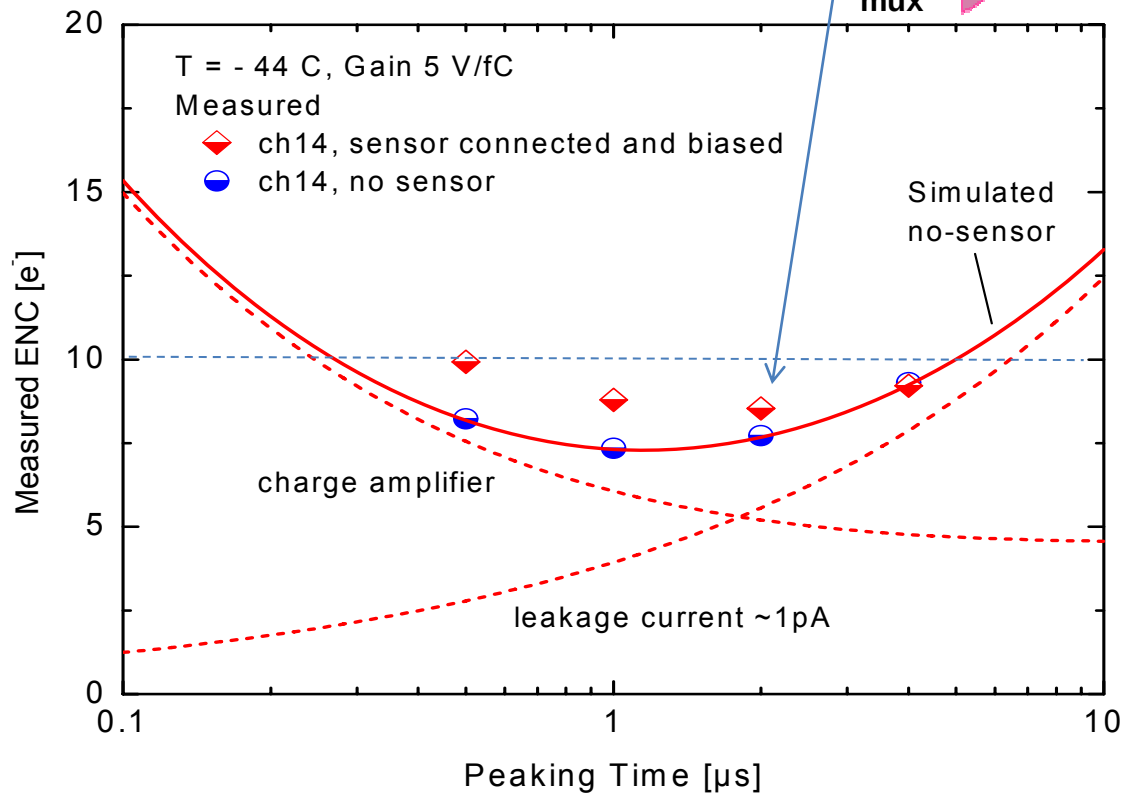
G. De Geronimo et al., IEEE TNS 55 (2008), collaboration with NASA

ASIC for high resolution X-Ray spectrometers → < 10 rms e

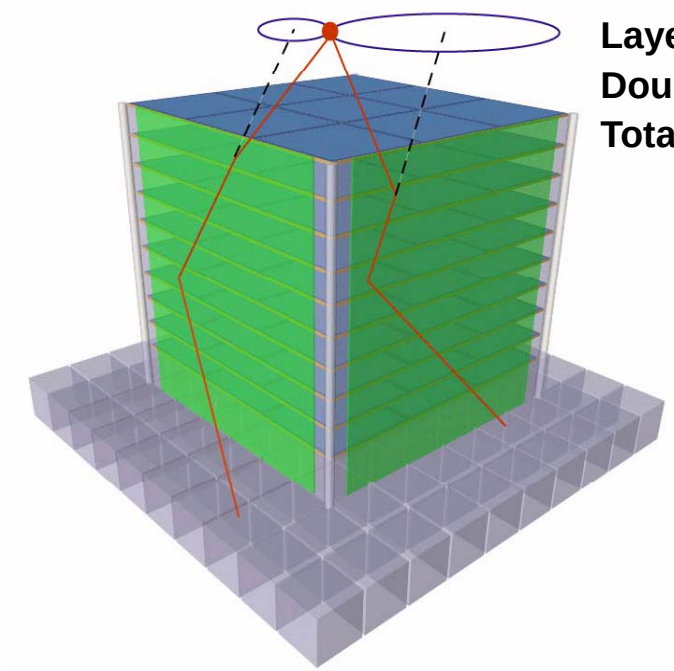


CMOS 0.25 µm
2.2 mm x 4.6 mm
1.2 mW/channel
NASA, NSLS

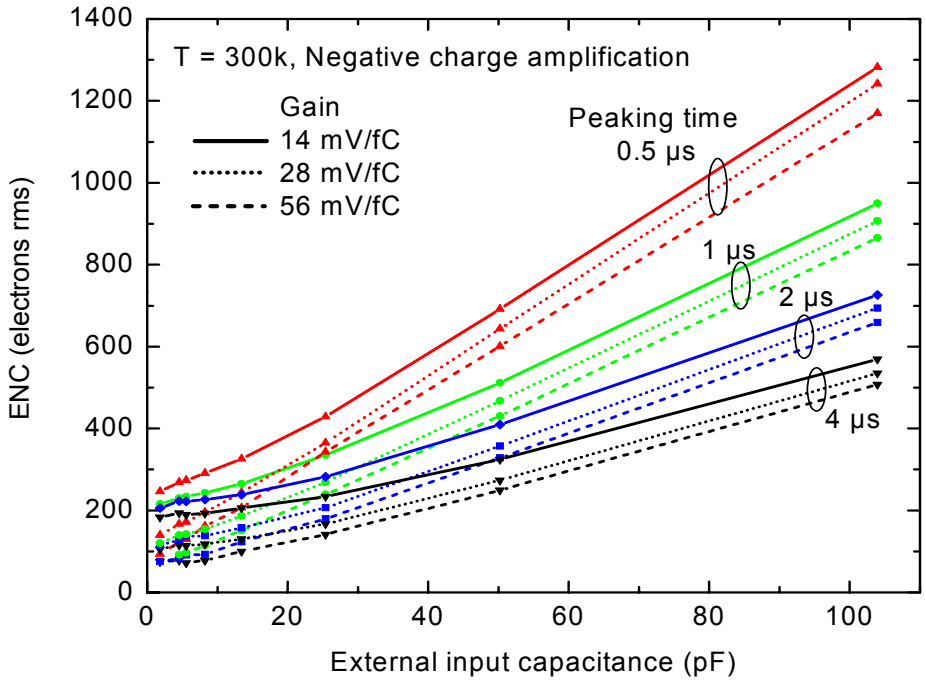


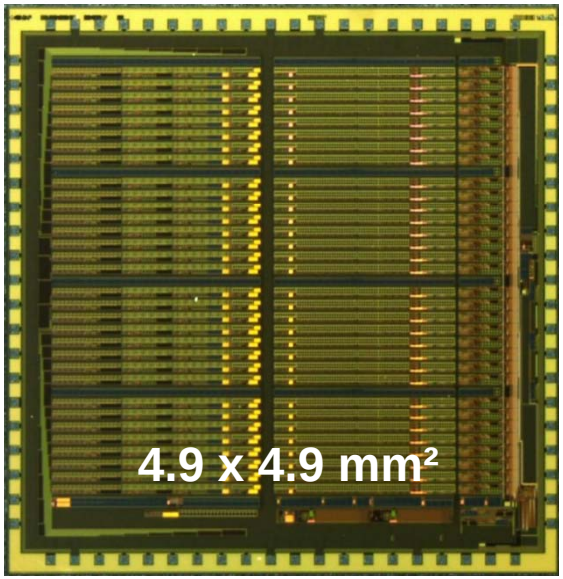


ASIC for Silicon Compton Telescope



Layers of 2 mm thick Si, 1x1 m²
Double sided orthogonal strips
Total strip length 30 cm (≈ 30pF)





- 32 channels - **mixed-signal**
- positive or negative low-noise charge amplification
- peak detection, sparse readout, multiplexing
- 65,000 transistors
- also used with CZT sensors for astronomy applications

G. De Geronimo et al., IEEE TNS 55 (2008), collaboration with U.S. Naval Research Laboratory (DoD)

Concluding Remarks

Detector concept ⟷ Readout Concept

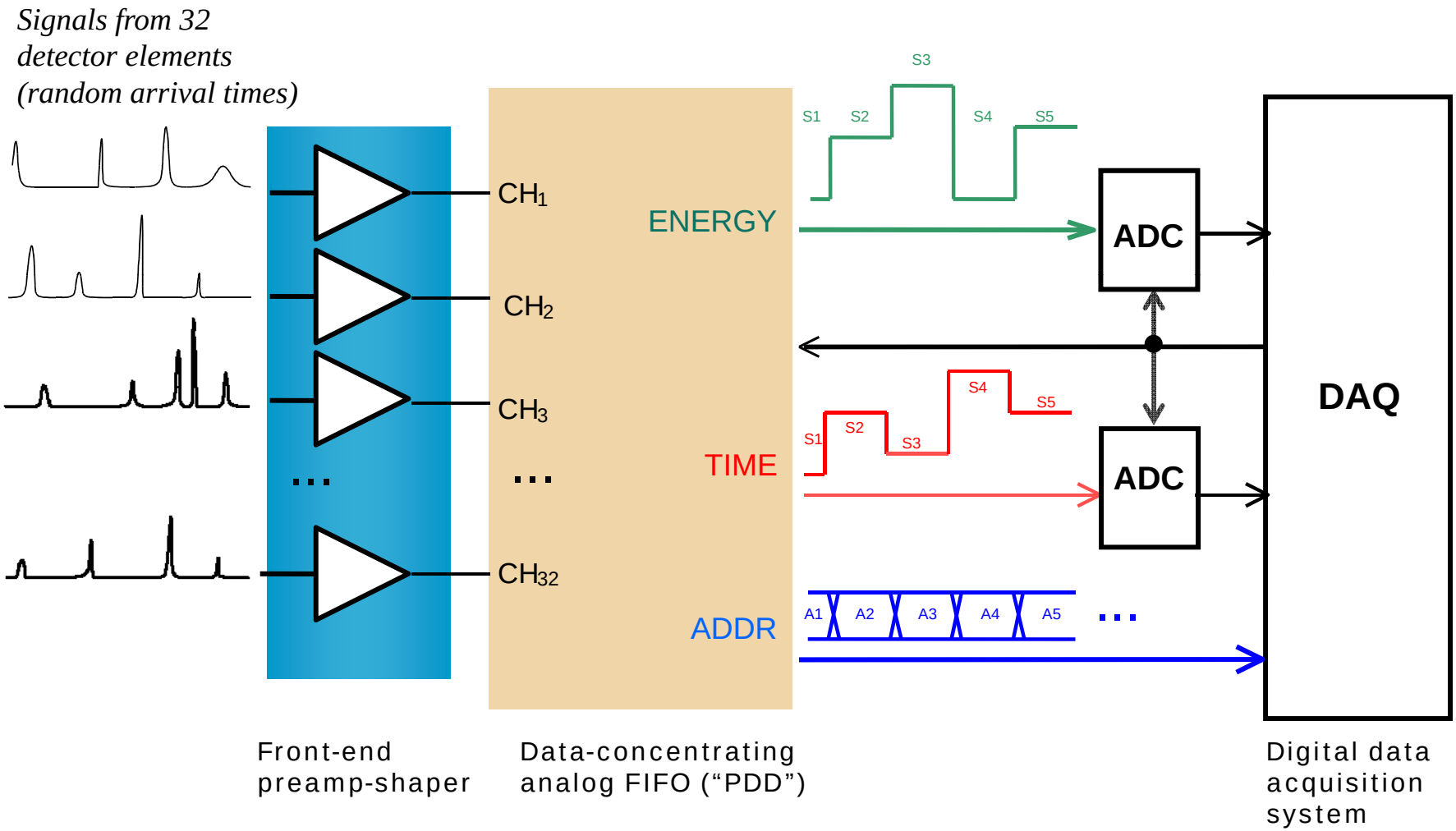
Electrode Design Interconnections Front end design	→	Capacitance Noise Power

Design Examples:

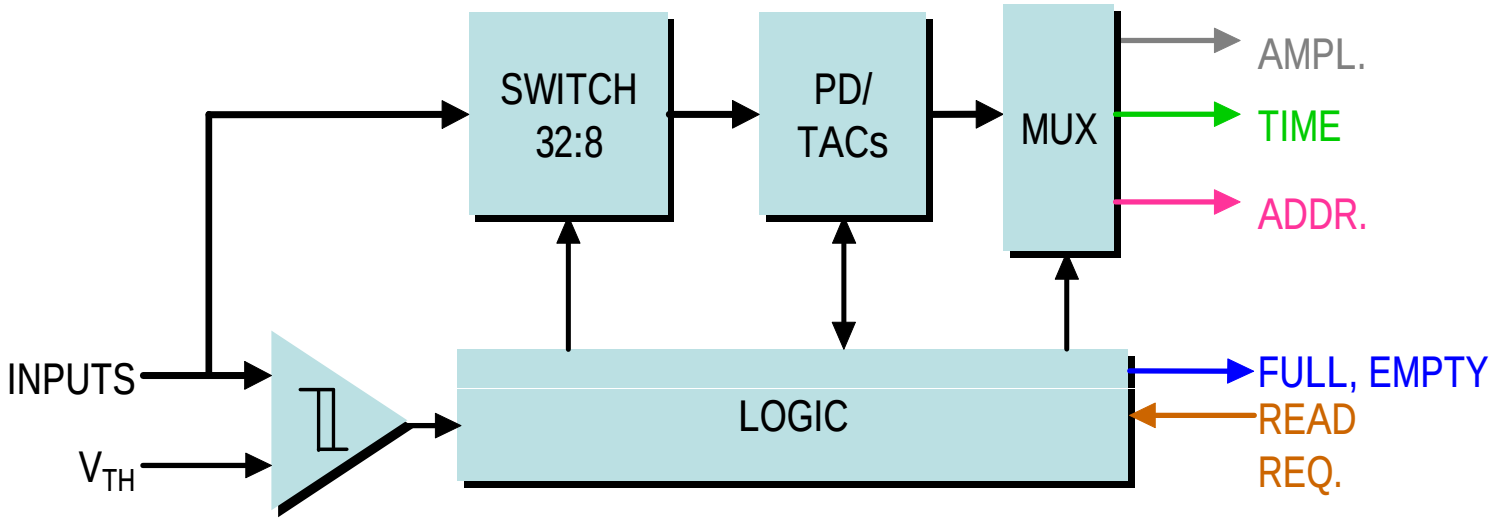
1. Multichannel pulse measurement with analog data concentration and derandomization

2. Readout ASIC for miniaturized PET tomograph

1. Multichannel pulse measurement with analog data concentration



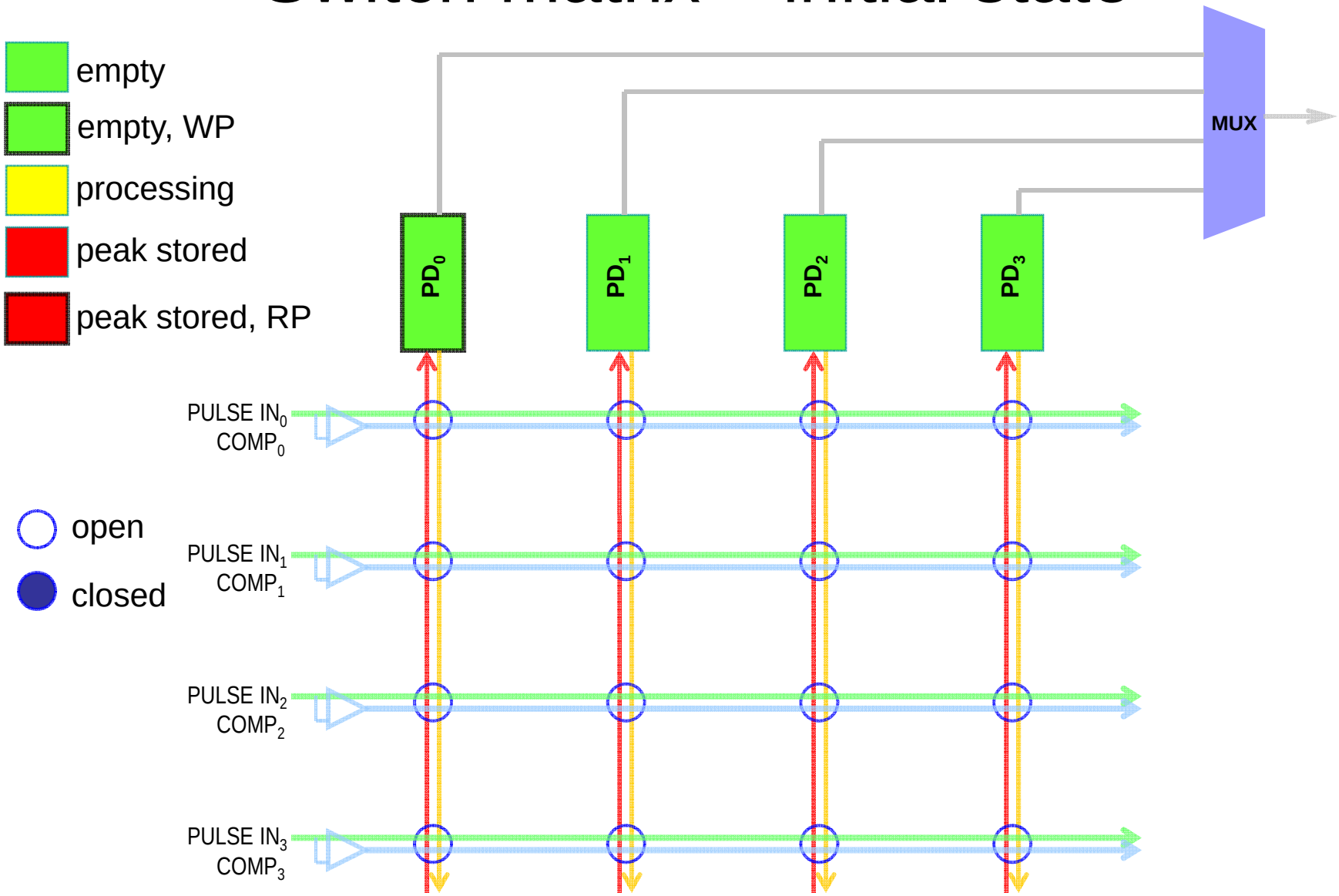
PDD ASIC Block Diagram



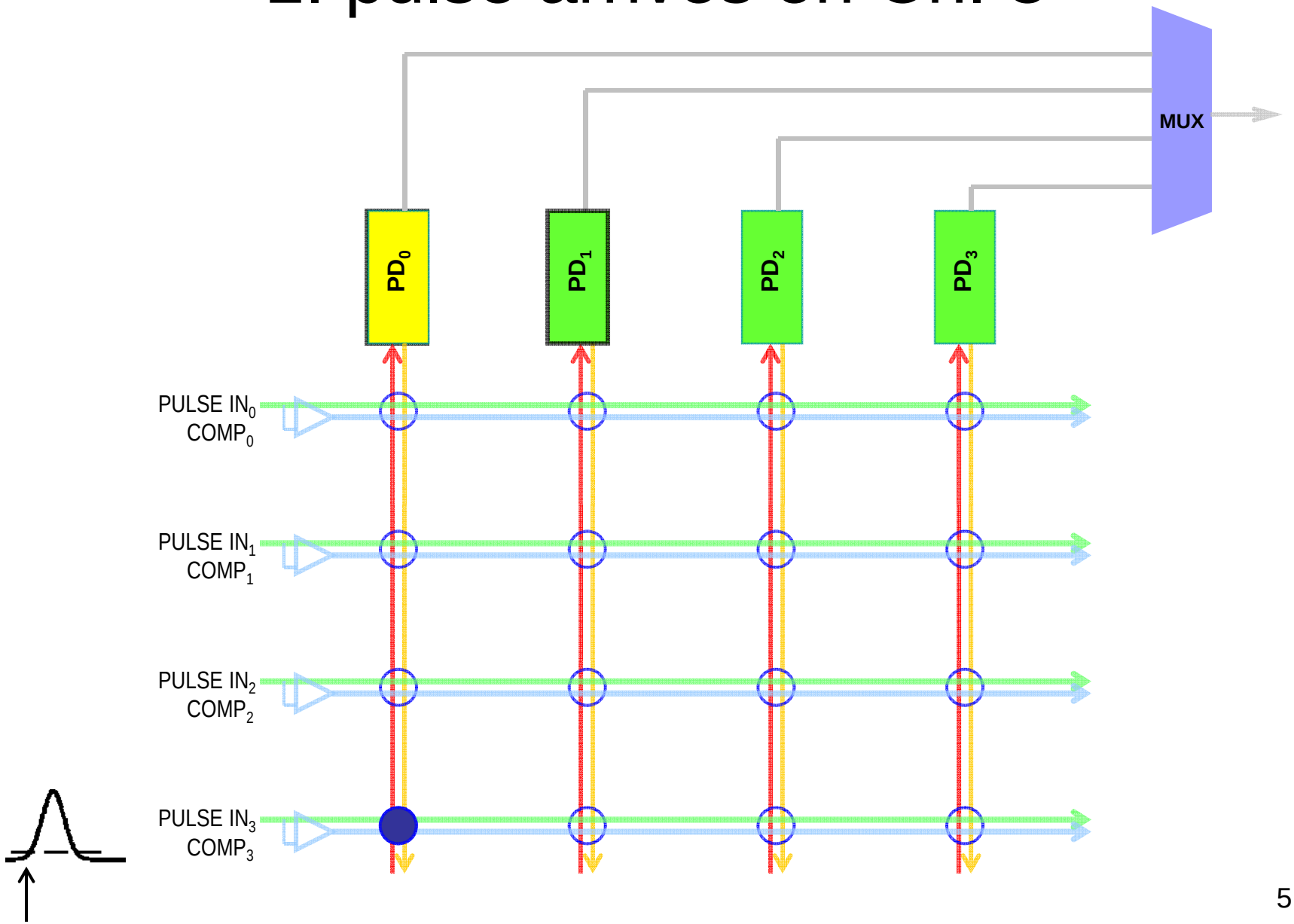
- ***Self-triggered and self-sparsifying***
- ***Simultaneous amplitude, time, and address measurement for 32 input channels***
- ***Set of 8 peak detectors act as derandomizing analog memory***
- ***Rate capability improvement over present architectures***
- ***High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)***
- ***Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel***
- ***Low power (3 mW per channel)***

P. O'Connor, G. De Geronimo, A. Kandasamy, *Amplitude and time measurement ASIC with analog derandomization: first results*, IEEE Trans. Nucl. Sci. 50(4), pp. 892-897 (Aug. 2003).

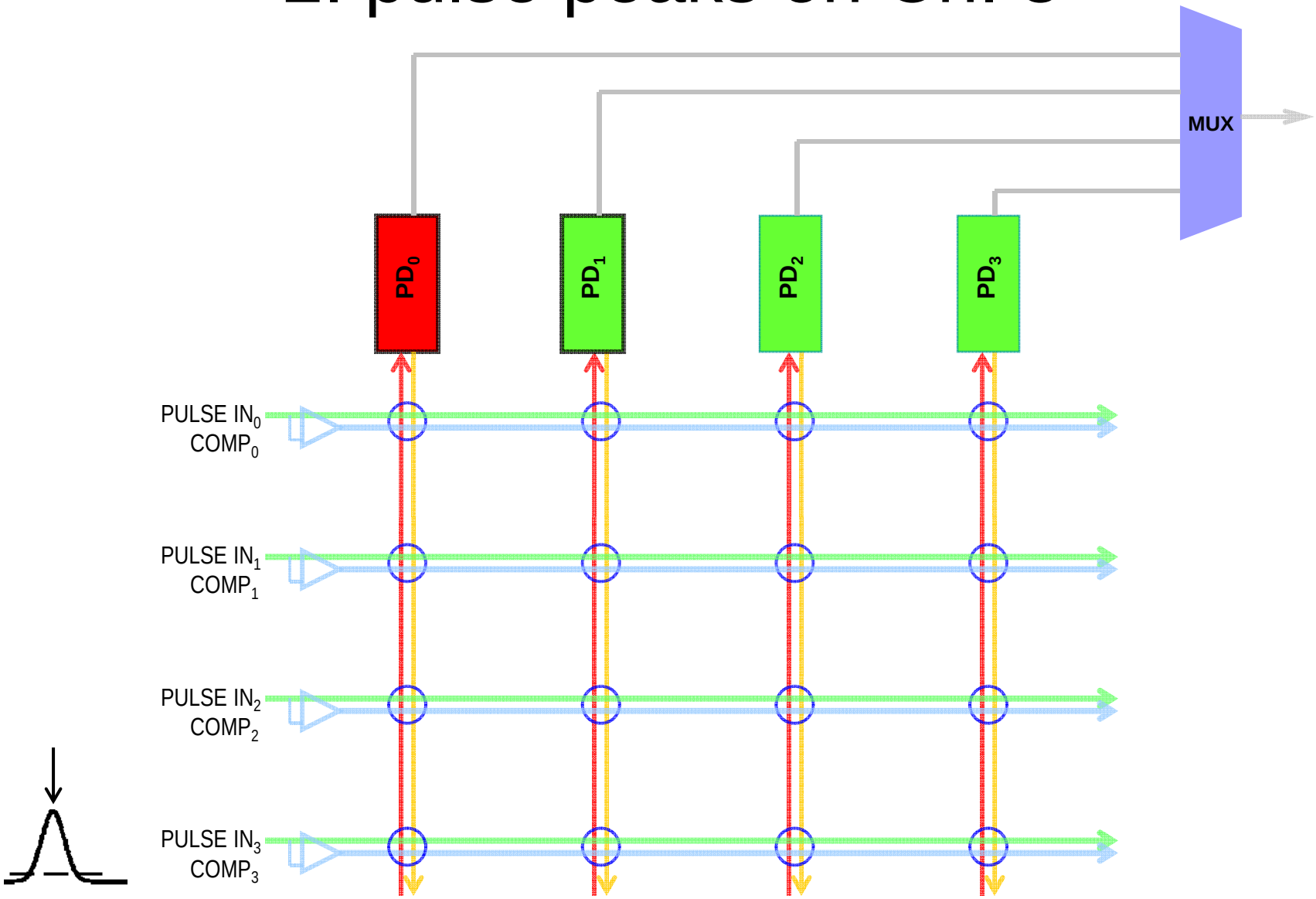
Switch matrix – initial state



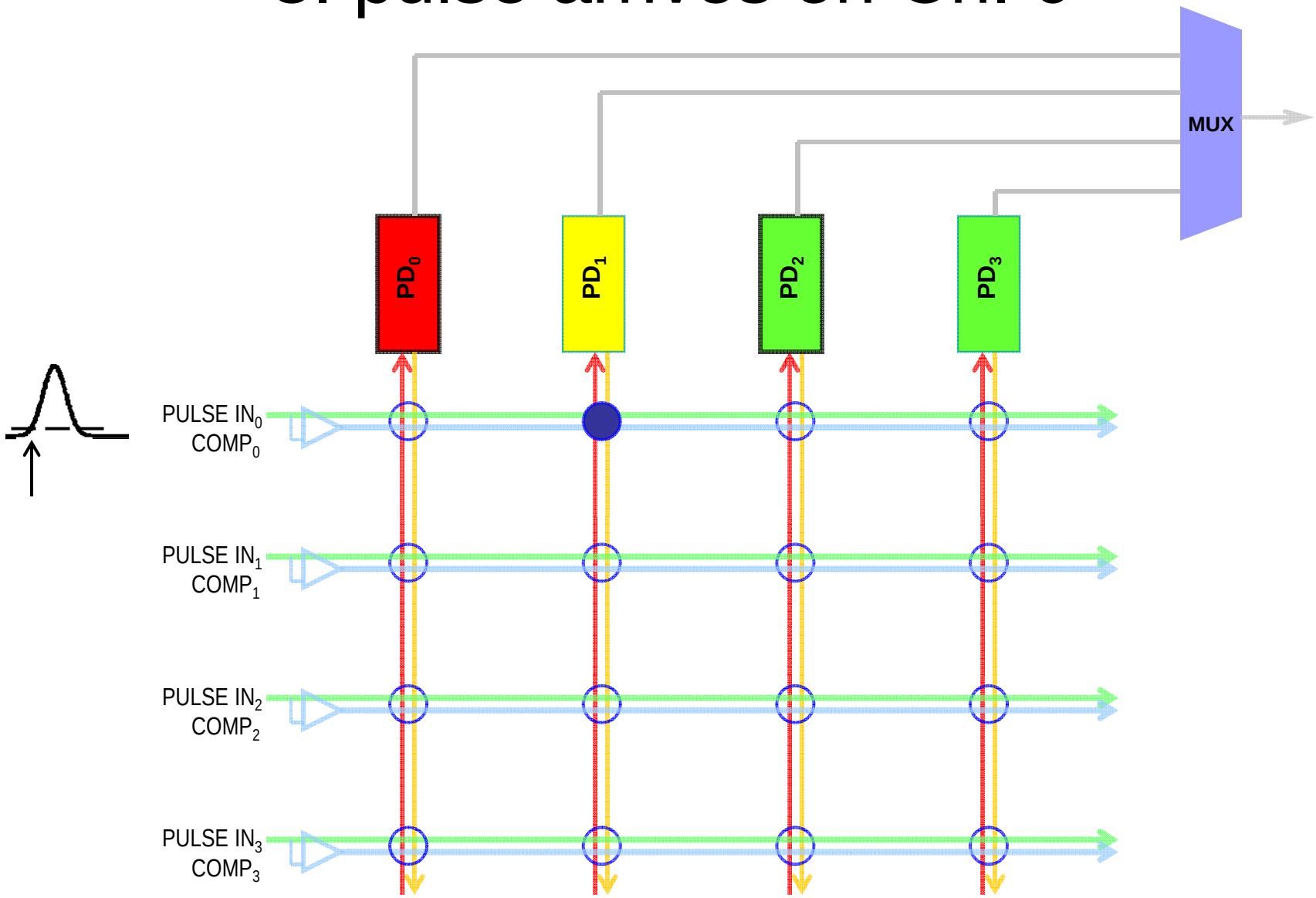
1. pulse arrives on Ch. 3



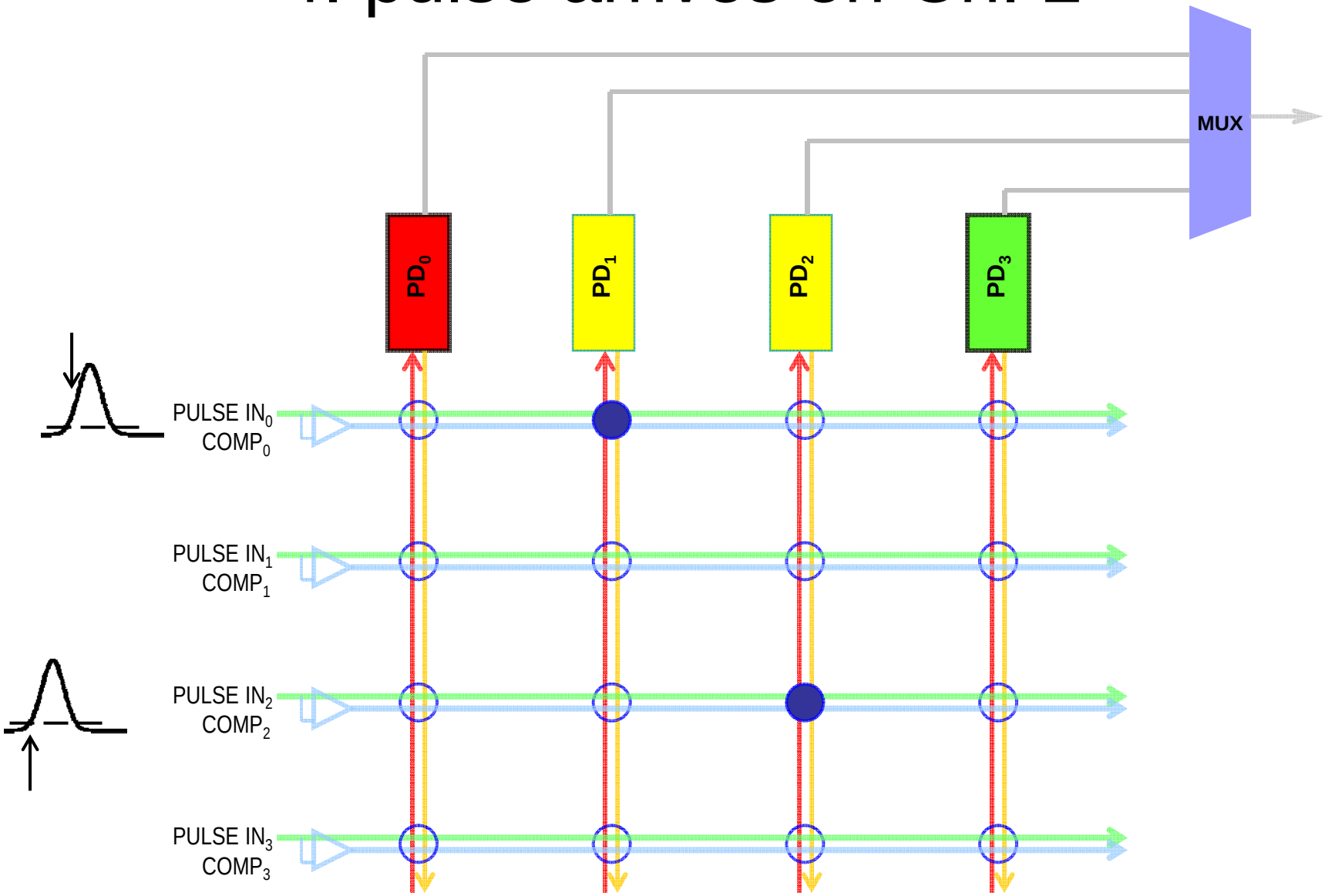
2. pulse peaks on Ch. 3



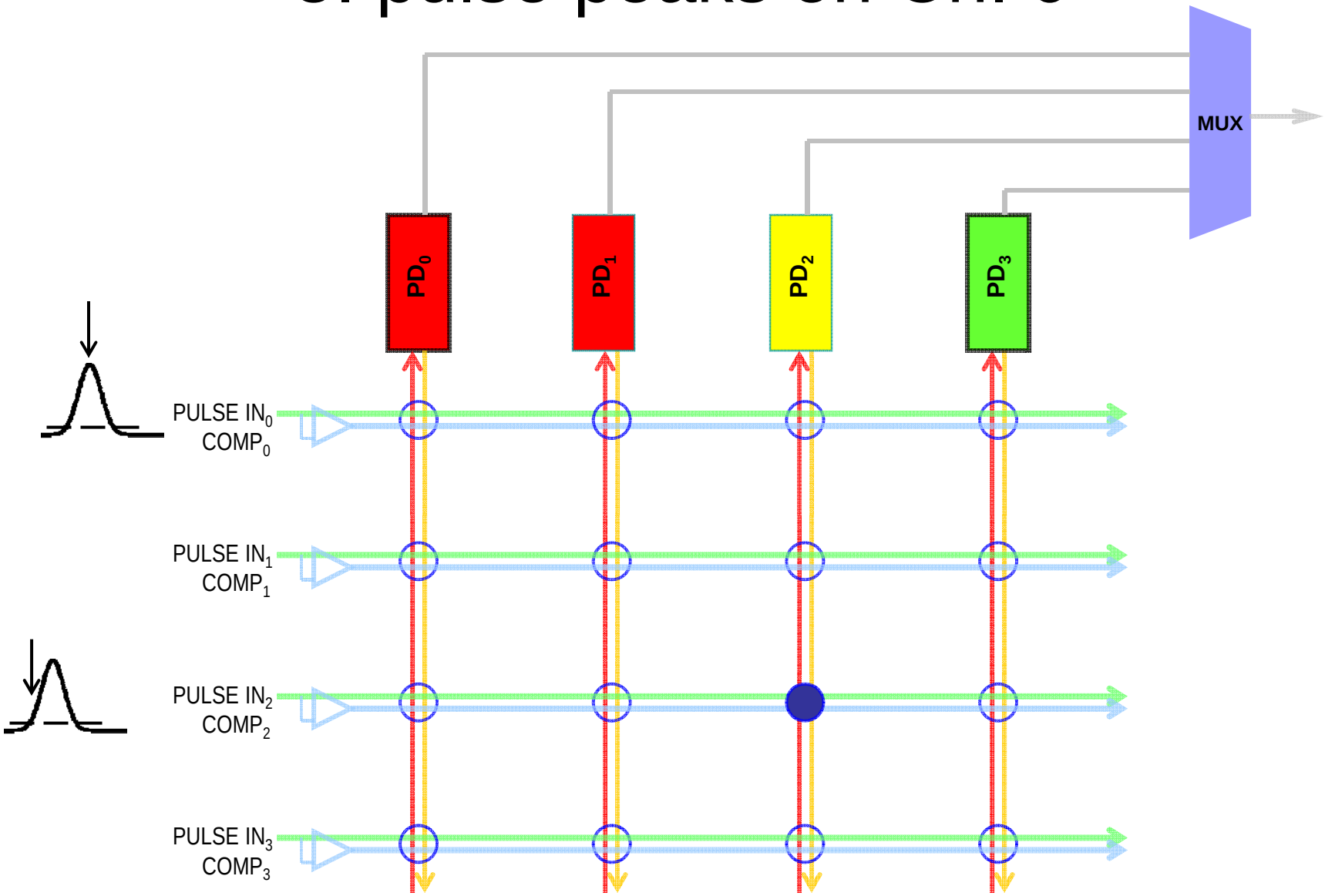
3. pulse arrives on Ch. 0



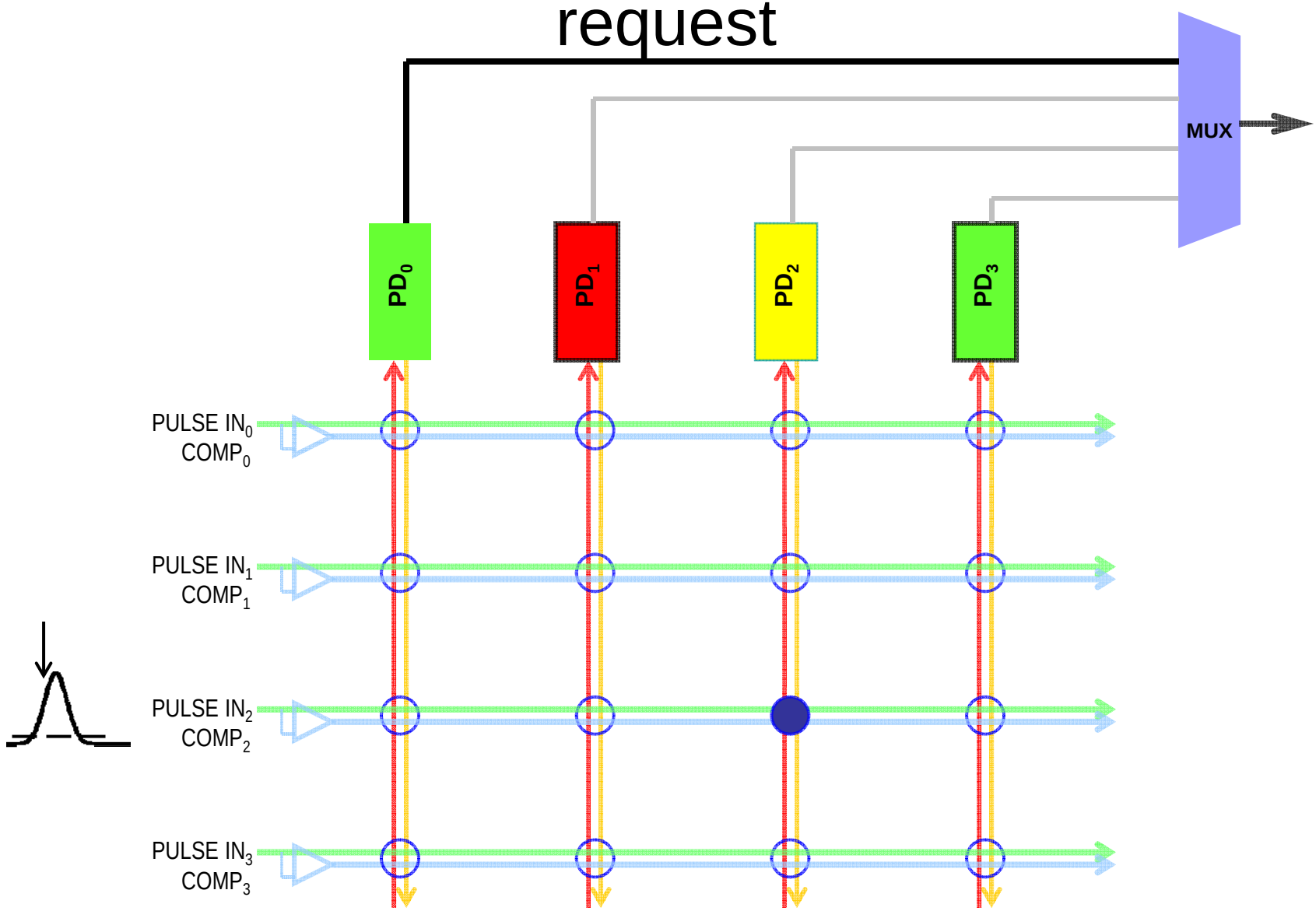
4. pulse arrives on Ch. 2



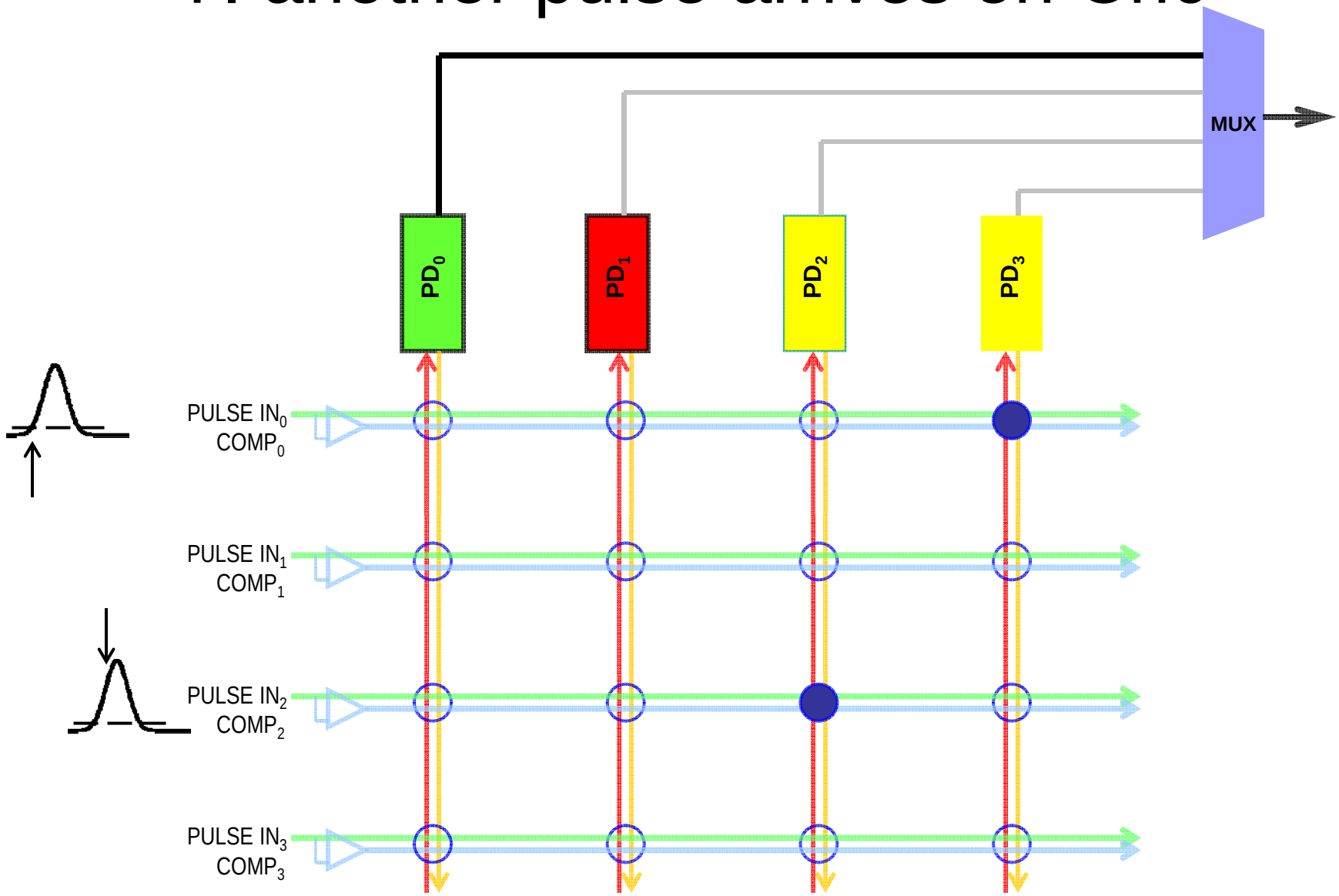
5. pulse peaks on Ch. 0



6. PD_0 read out in response to external read request

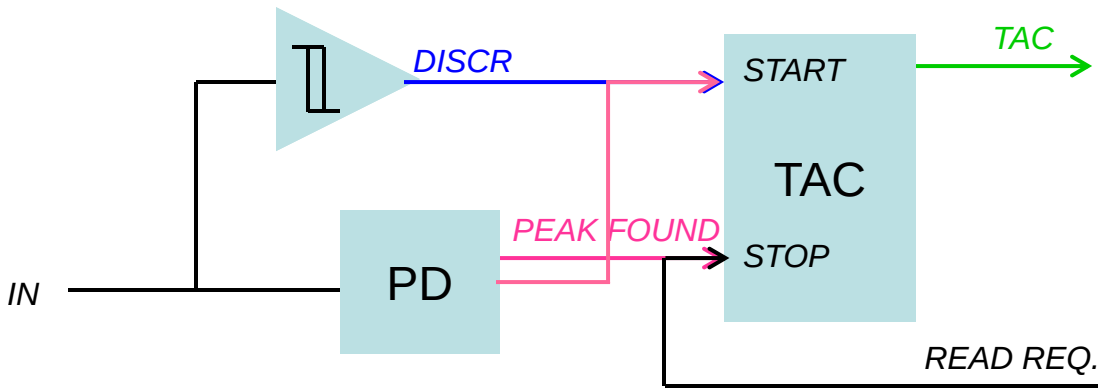


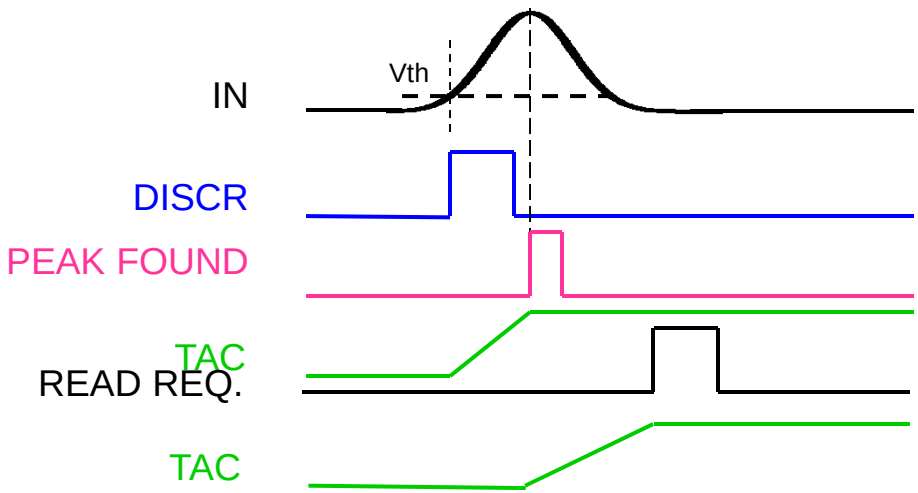
7. another pulse arrives on Ch0



Quad-mode Time-to-Amplitude Converter

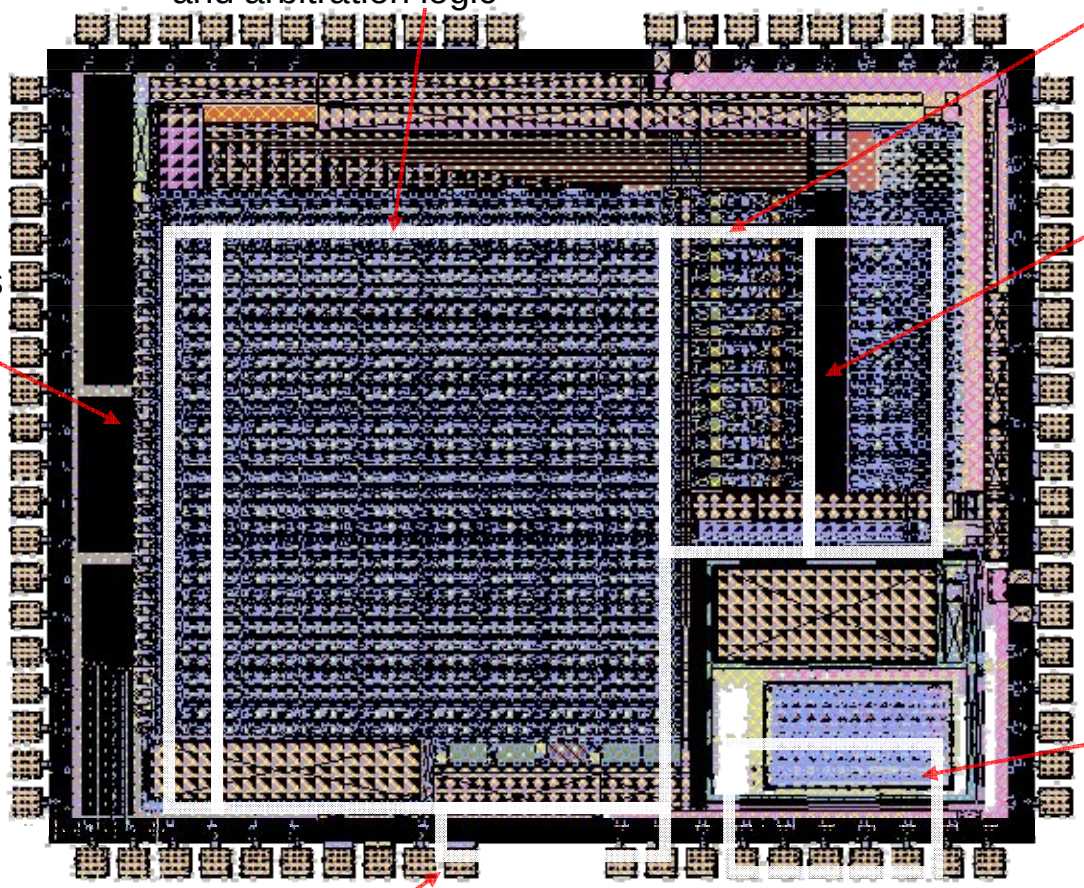
MODE 1
MODE 2





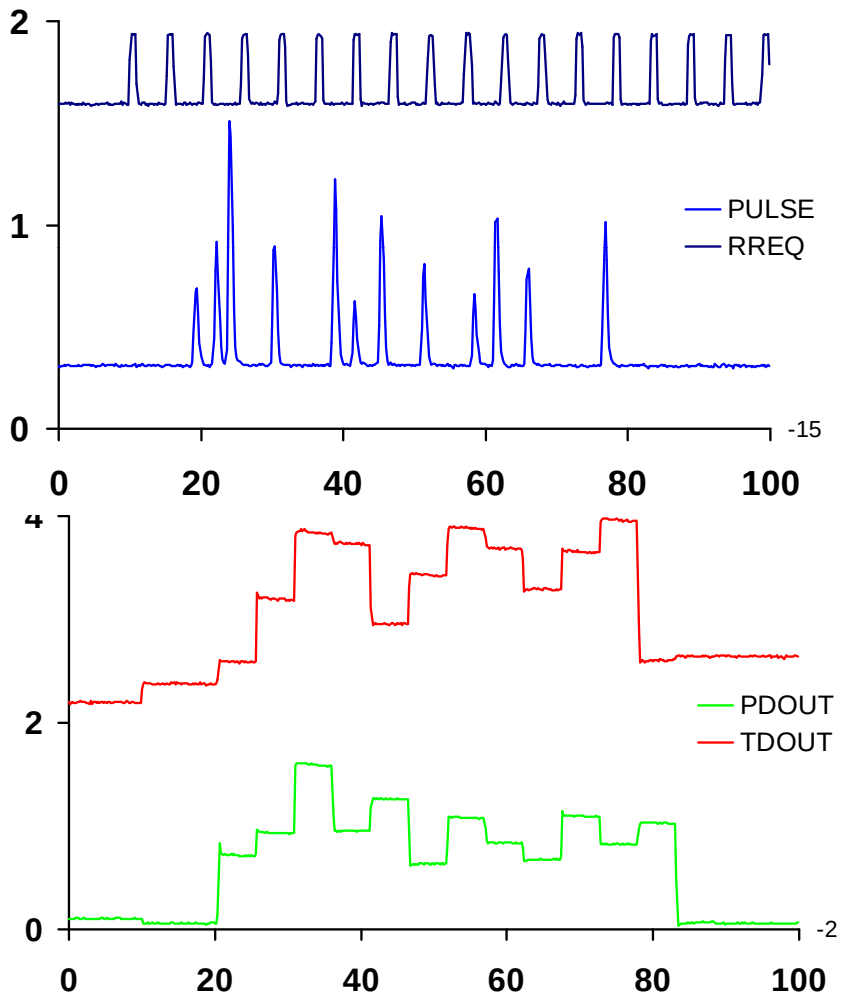
1. risetime
2. peak-RR
3. TOT
4. lead-RR

PDD layout



size : 3.6 x 3.2 mm²
technology: 0.35µm CMOS
DP4M

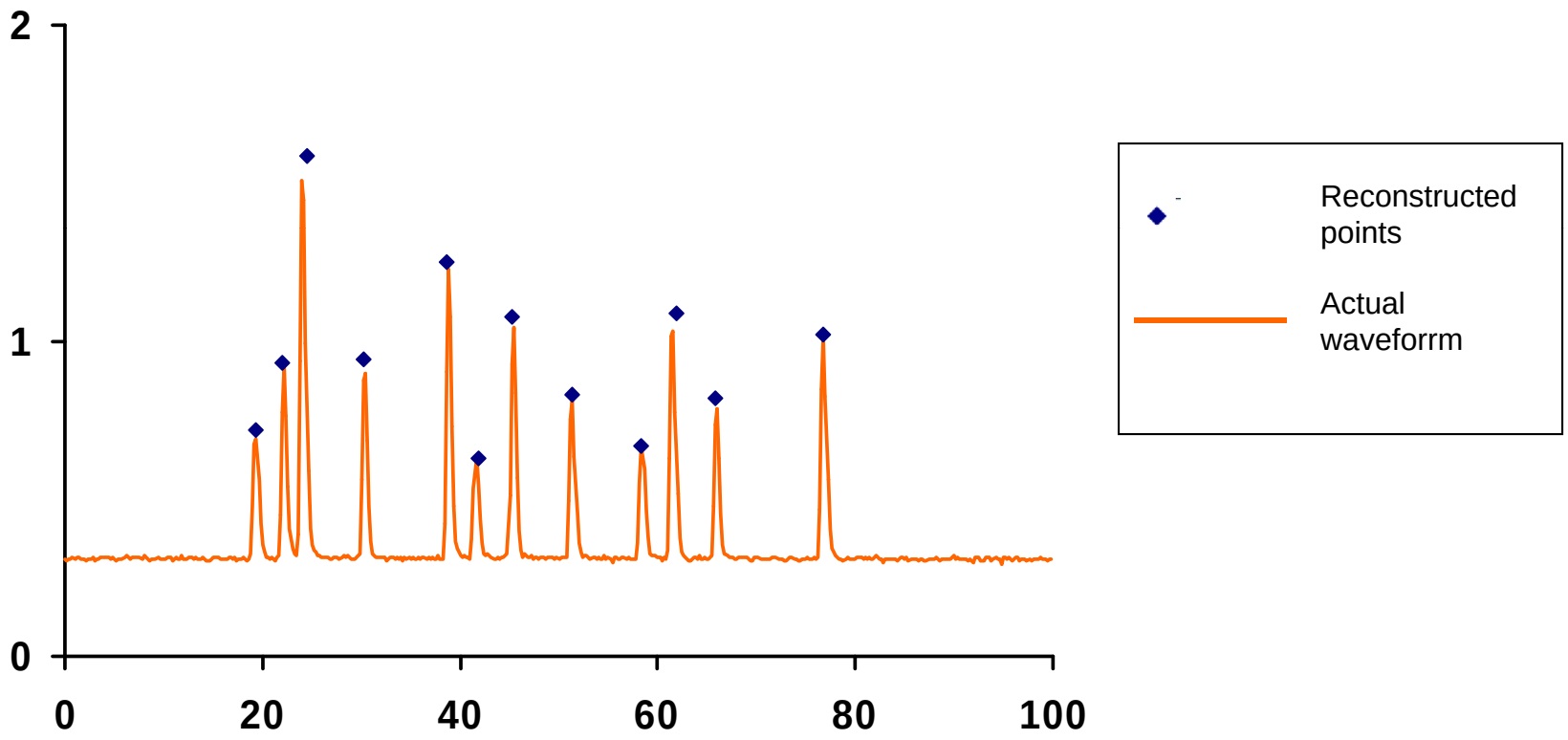
Reconstruction of peak height and time



ASIC Inputs

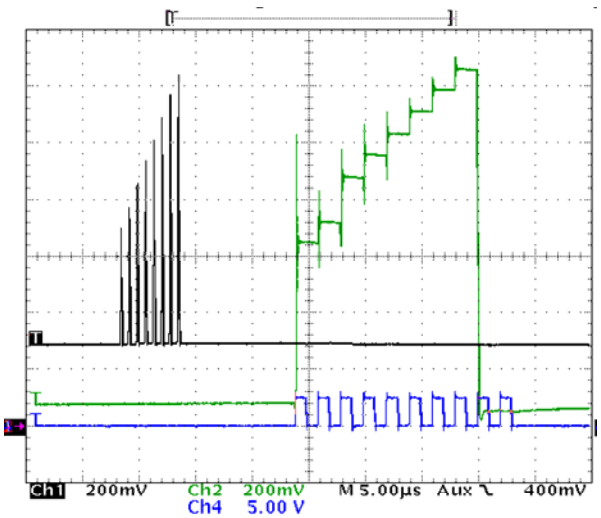
ASIC Outputs

Reconstruction of peak height and time



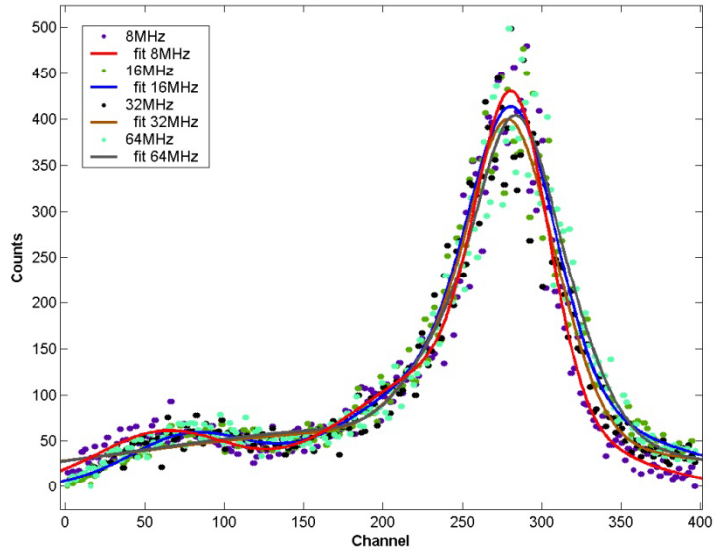
High rate capability

Fast pulses, high rate



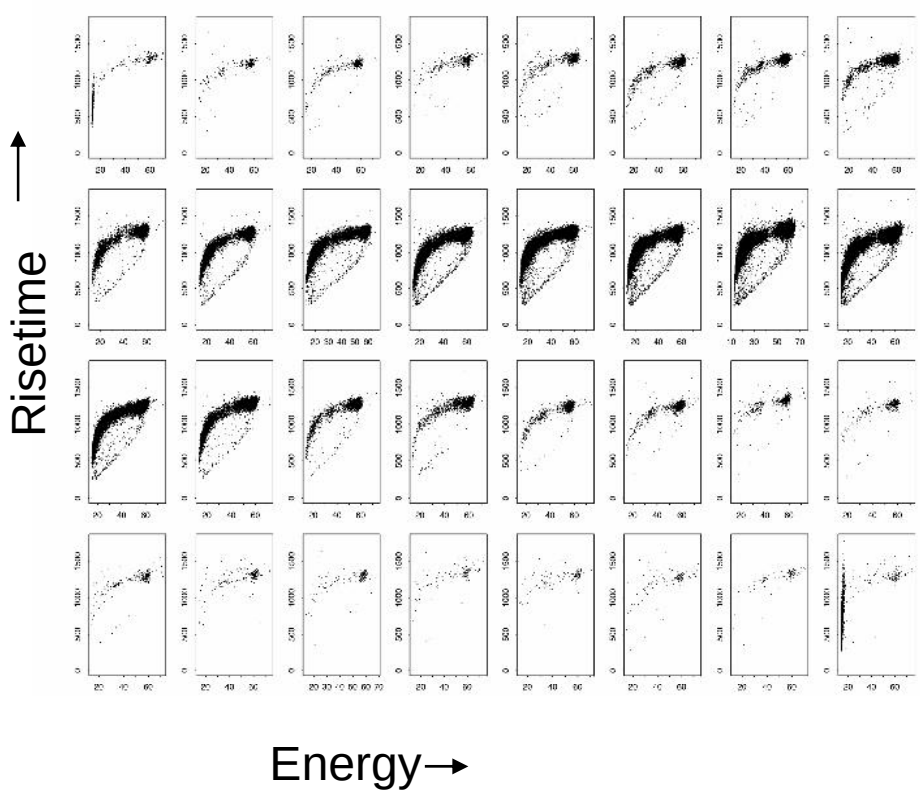
Black – pulse input
Blue – Read Request
Green – PD output

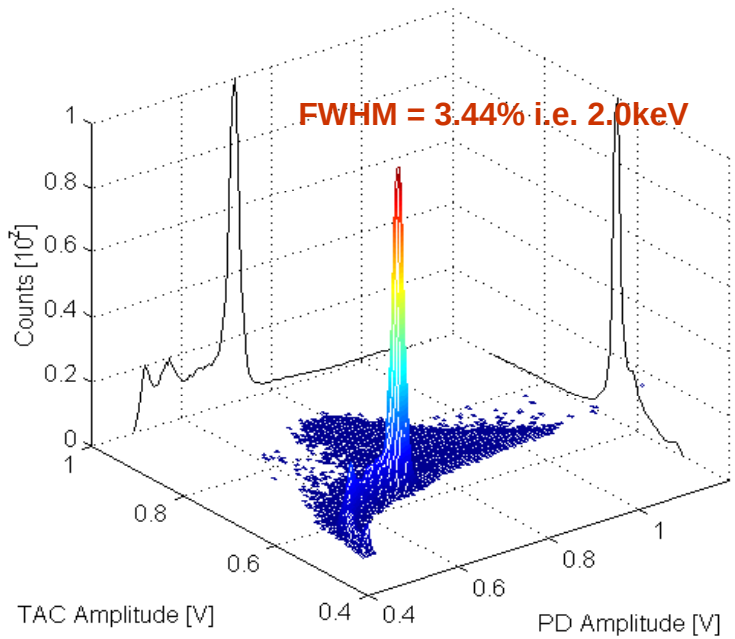
- Input pulses:
  - 30 ns peaking time
  - 1.6 MHz rate
- Readout rate 500 kHz



- 32 CZT sensors, 7x3x7mm^3
- ^{241}Am source, overall rate ~ 8MHz
- Shaper peaking time 600ns
- Rate of read request varied from 8 MHz to 64 MHz
- No peak shift or FWHM degradation seen
- Settling time of output mux ~ 10ns

Biparametric spectra



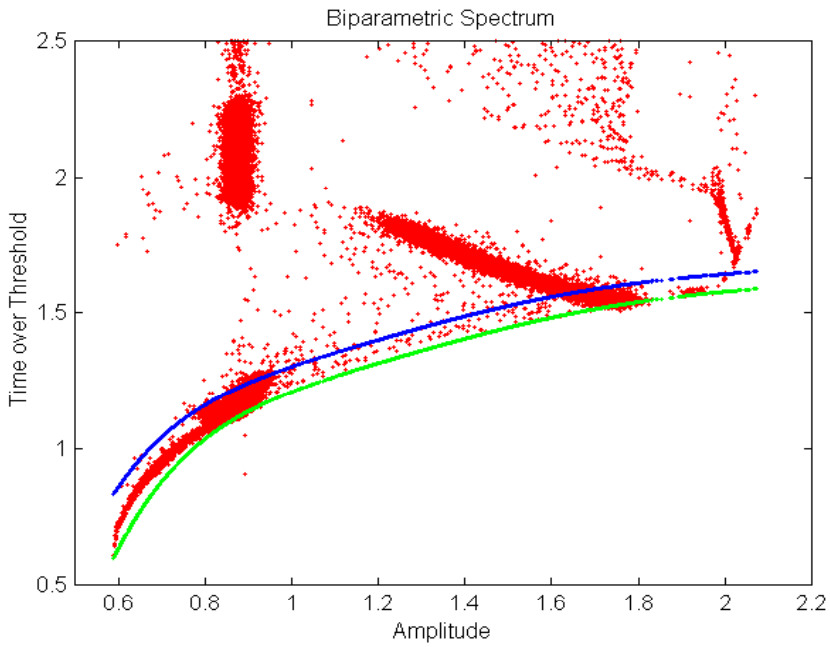


- **Detector: eV Products CZT Pixellated Linear Array of 32 elements 16x3x3 mm^3 biased at 900V**
- **Source: 2 x 8mCi ^{241}Am**
- **FE: t_p = 400ns, gain=200mV/fC**
- **Event Rate: 4.5MCounts/s overall, 210kCounts/s on the single pixel**

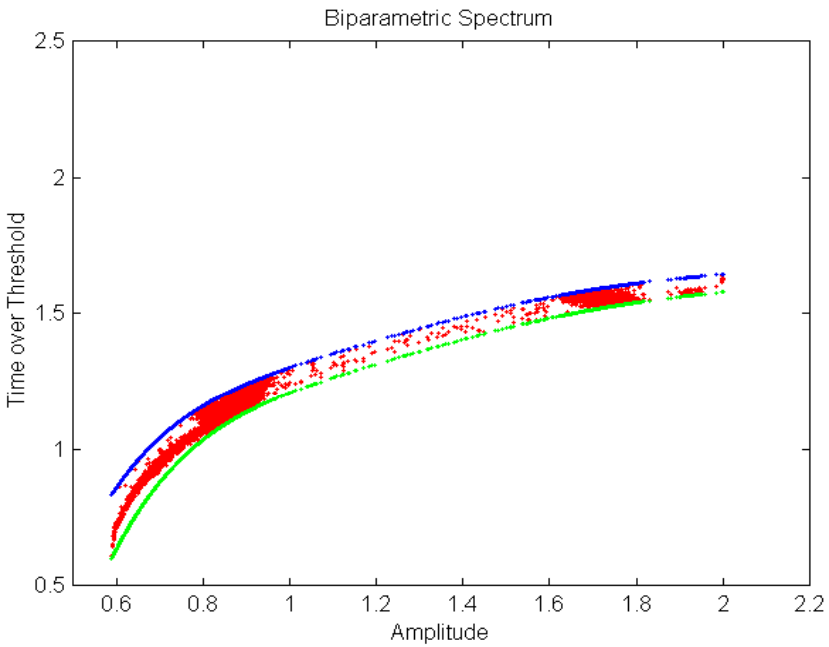
Time-Over-Threshold Measurement for pile-up rejection

Experiment Setup

- Array of 1mm x 1mm silicon diodes, built on a fully-depleted 400um high-resistivity wafer and cooled at ~ -54 ˚C
- 8keV X-ray monochromatic collimated 10umx10um beam from NSLS focused on the center of one pixel
- FE with 2us peaking time



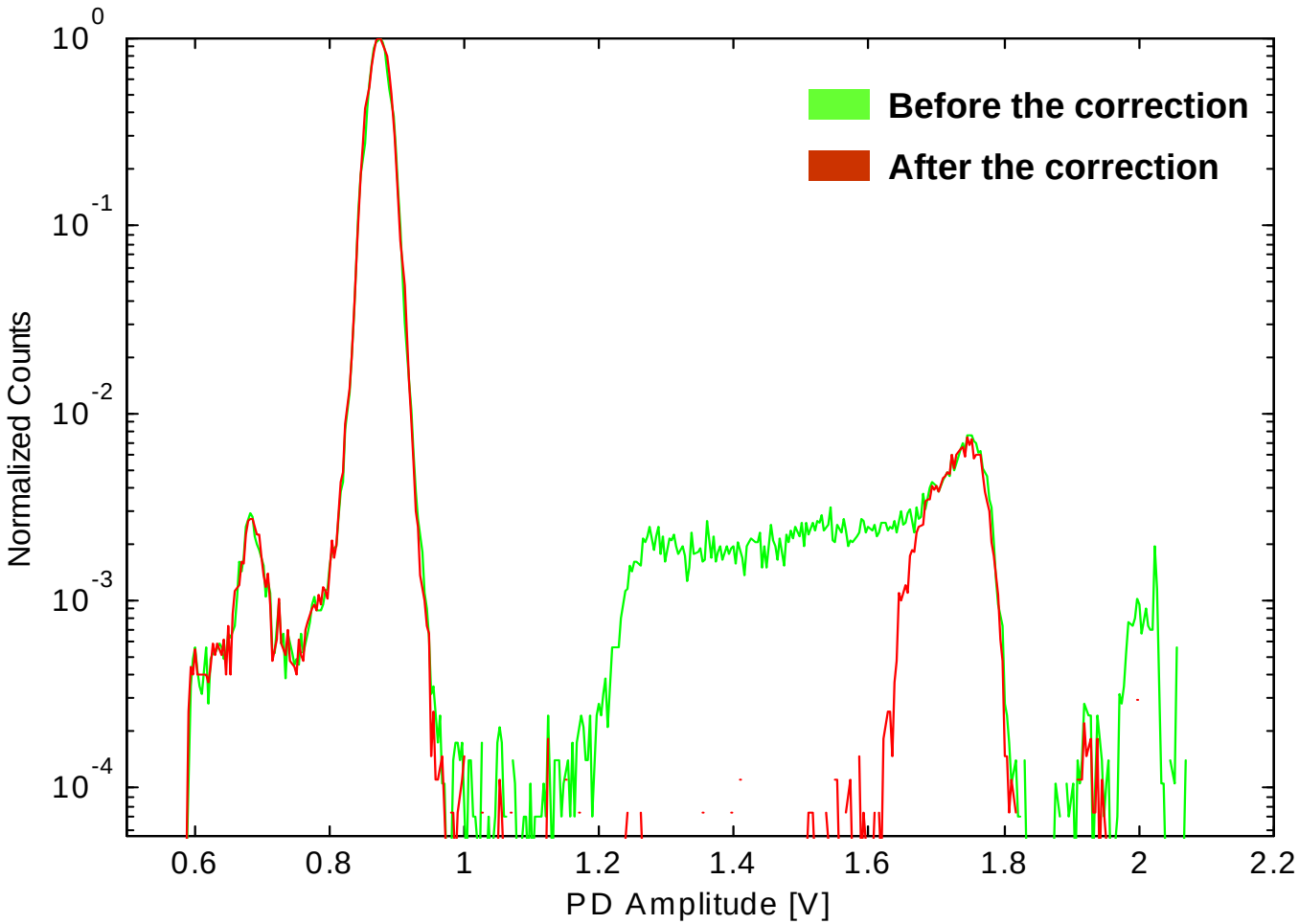
Before The Correction



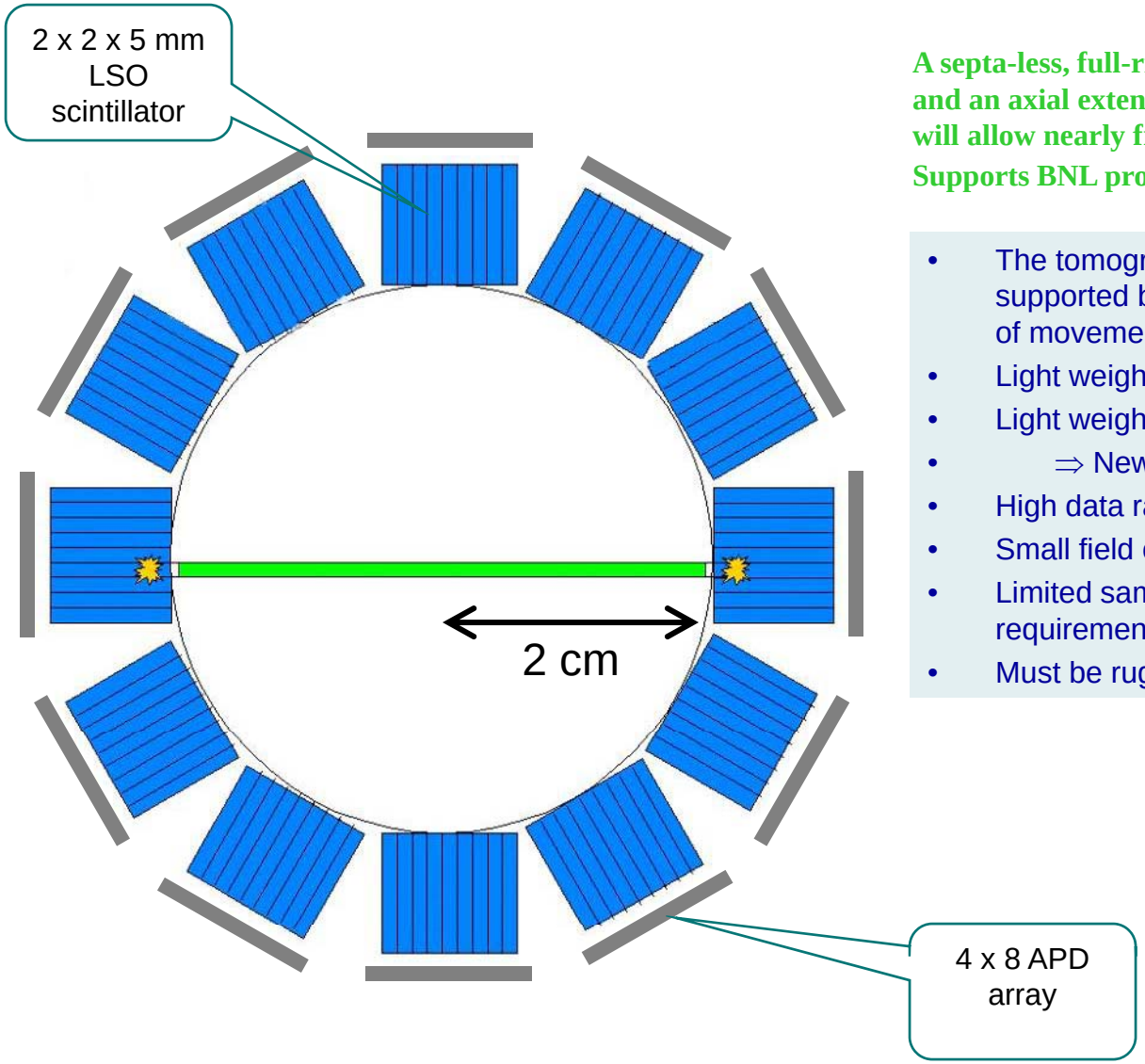
After The Correction

Time-Over-Threshold Measurement for pile-up rejection

Pulse Height Spectra Comparison

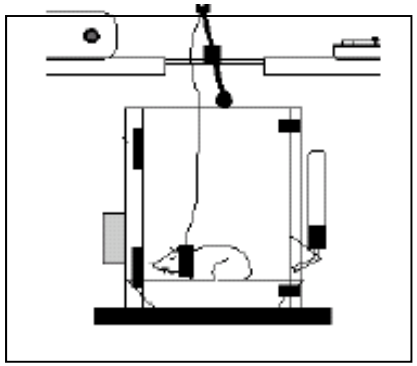


2. RatCAP – Rat Conscious Animal PET

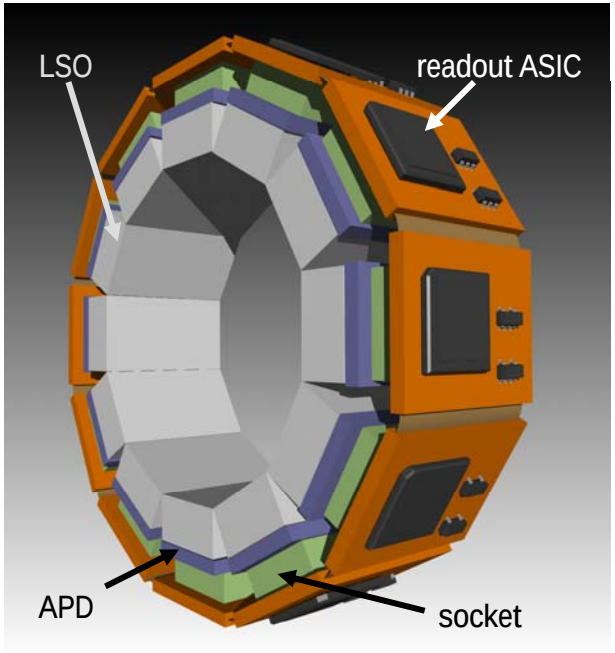


A septa-less, full-ring tomograph with a diameter of 4 cm and an axial extent of 2 cm, suspended by a tether, which will allow nearly free movement of the awake animal. Supports BNL program in addiction research.

- The tomograph ring must be light enough to be supported by the rat and allow reasonable freedom of movement
- Light weight detectors (~ 150 g total weight)
- Light weight electronics with low power dissipation
- ⇒ New custom ASIC
- High data rates and large singles background
- Small field of view and large parallax effects
- Limited sampling due to space and weight requirements
- Must be rugged enough withstand activity of the rat

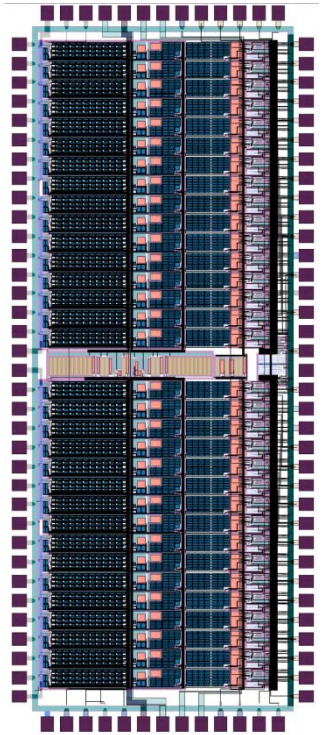


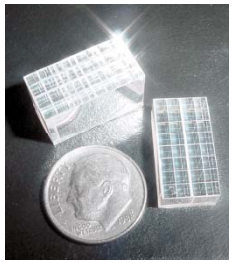
Electronics for a mobile, miniature animal PET tomograph



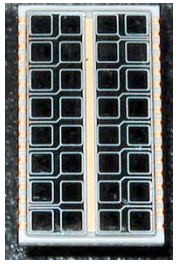
Mockup of the portable ring on the head of a rat

- 0.18 μm CMOS
- 1.5 mW/channel
- 32 channel ASIC
- Preamplifier + shaper + timing discriminator
- address encoding
- serialized output



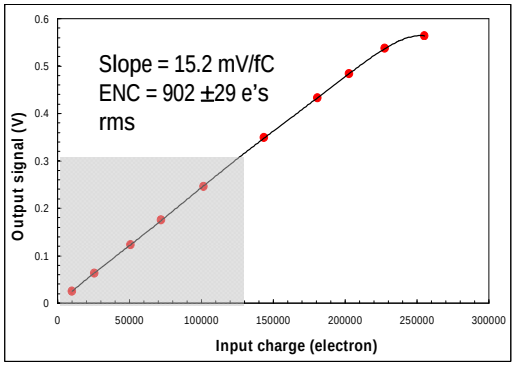


LSO scintillator

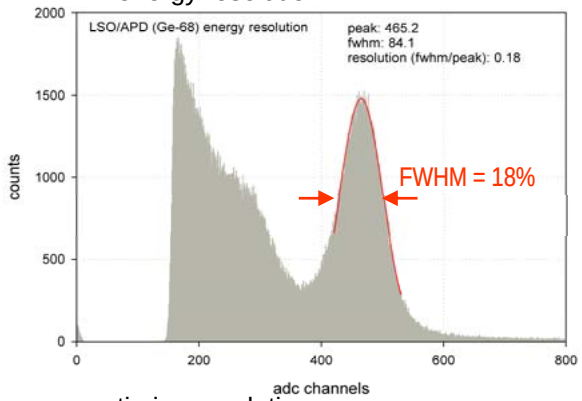


APD array

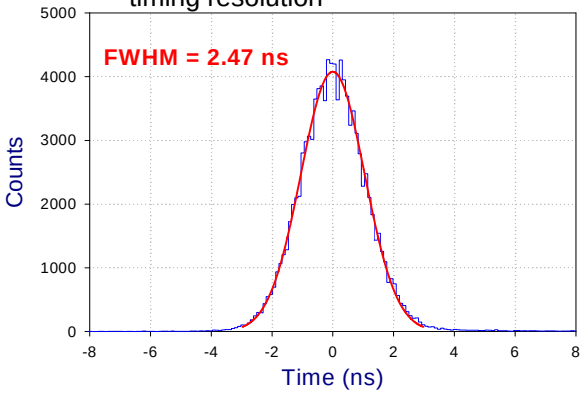
linearity



energy resolution



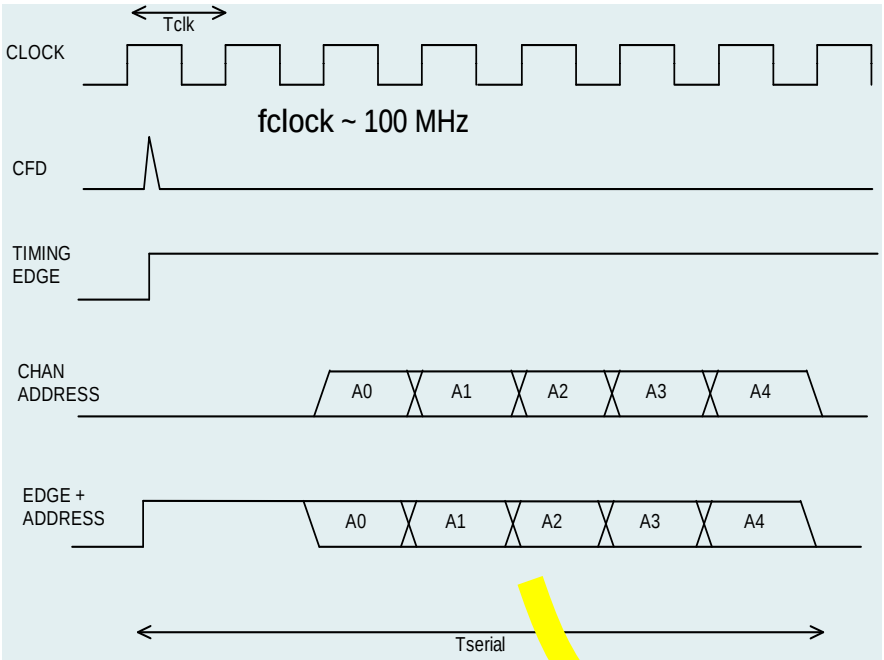
timing resolution

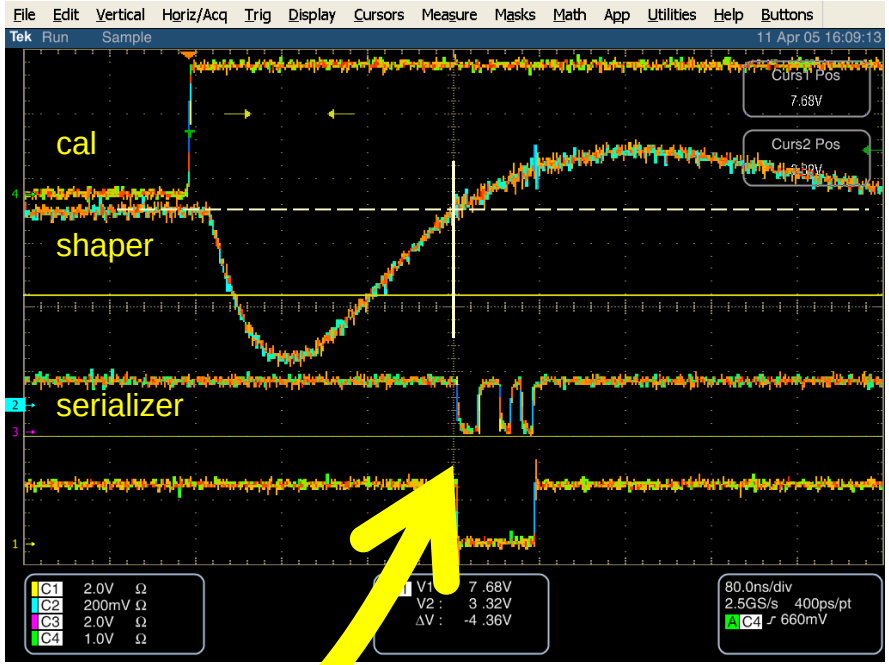


ASIC preamplifier with CFD vs. BaF_2/PMT

RatCAP ASIC address serializer

- 384 channels on ring make it impossible to bring all signals off detector.
- Analog pulse height information is not saved, lower level discriminator only.
- Discriminator pulse is encoded to give 5 bit address
- Leading edge of encoded serial pulse train gives time information

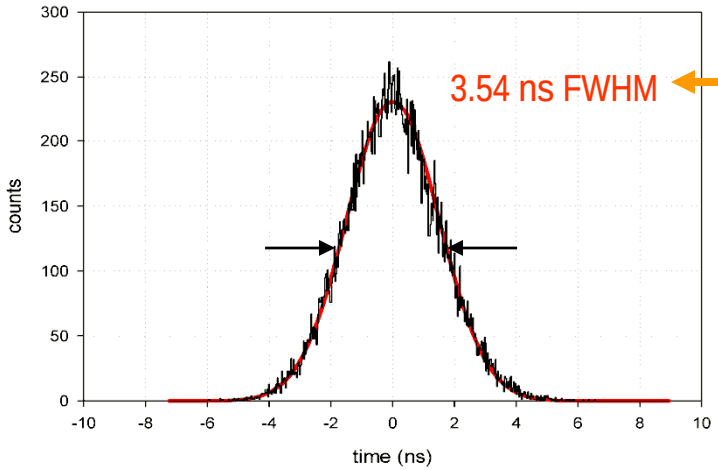




J.-F. Pratte et al., *Front End Electronics for the RatCAP mobile animal PET scanner*, IEEE Trans. Nucl. Sci. 51(4), pp. 1318-1323 (Aug. 2004).

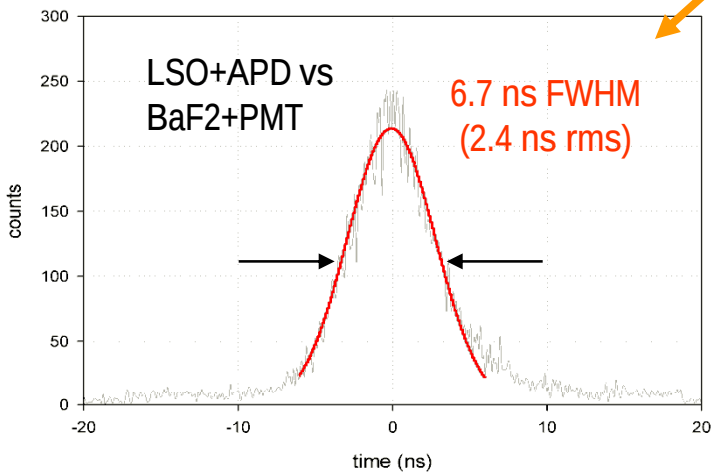
ASIC Performance - Timing Resolution

Preamp/Shaper + ZCD

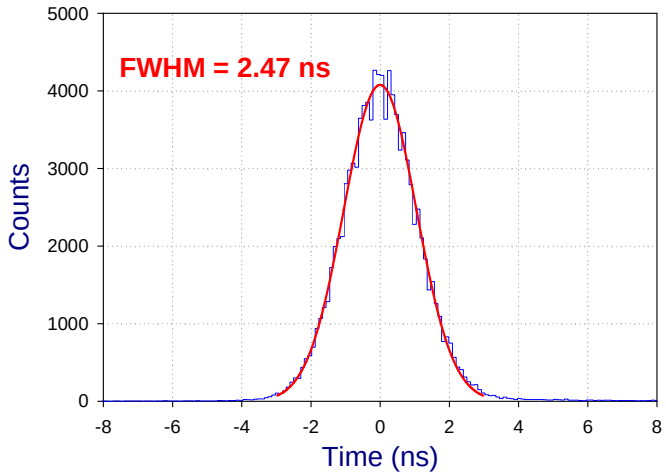


Electronic Timing Resolution at 511 keV equivalent energy

Coupled to LSO/APD with 511 keV γ's timed against a BaF_2 scintillator w/PMT

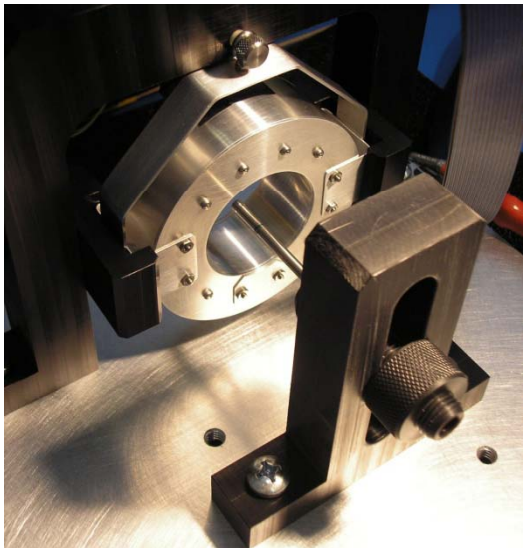


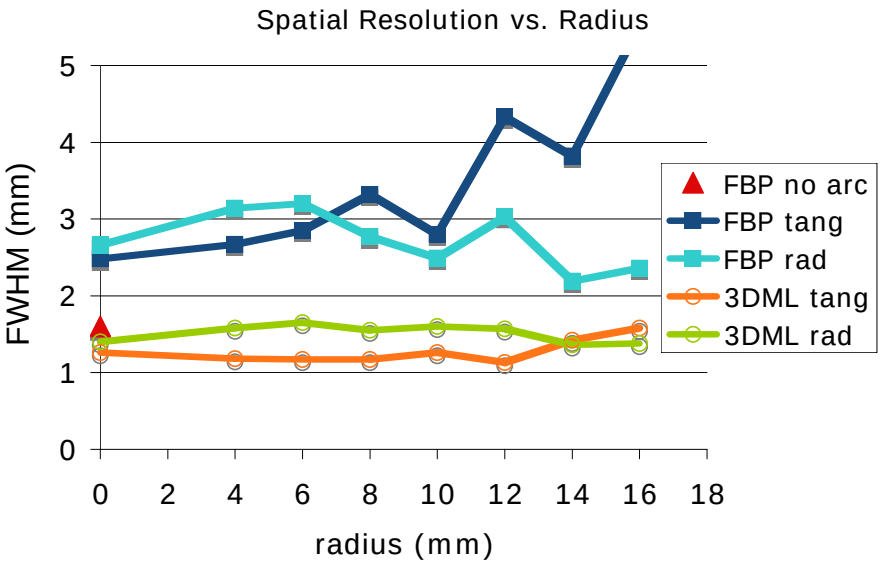
Same with CFD



Spatial Resolution

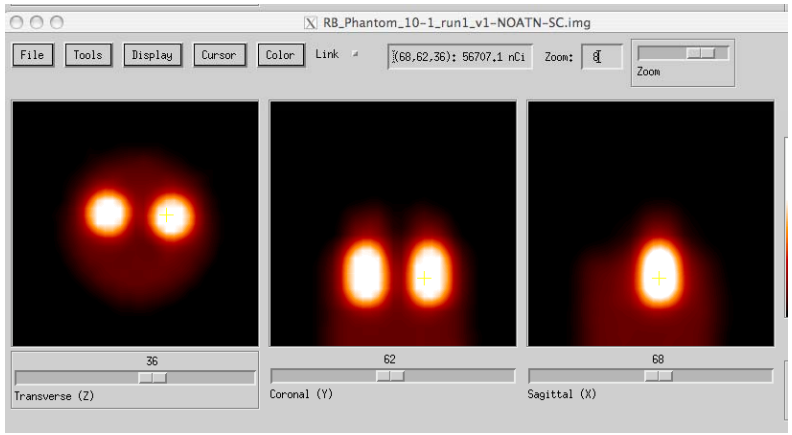
- ^{68}Ge point source
  - ~1 mm dia.
  - r = 0-16 mm
- 2D FBP
  - sinogram arc correction by linear resampling
  - ramp filter
- 3D Monte Carlo MLEM
  - 50 iterations
- Note:
  - arc correction parameters to be optimized
  - point source size NOT deconvolved

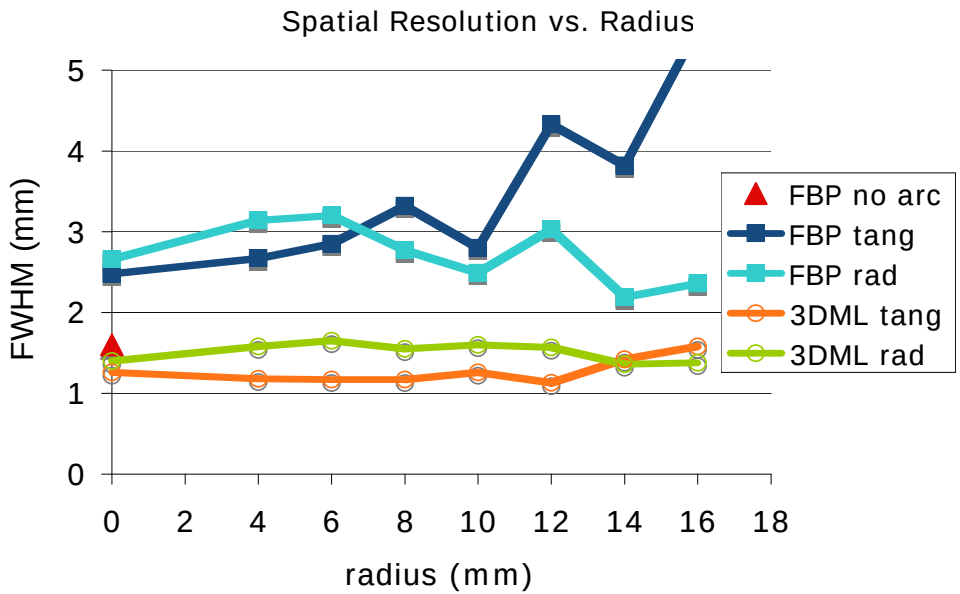




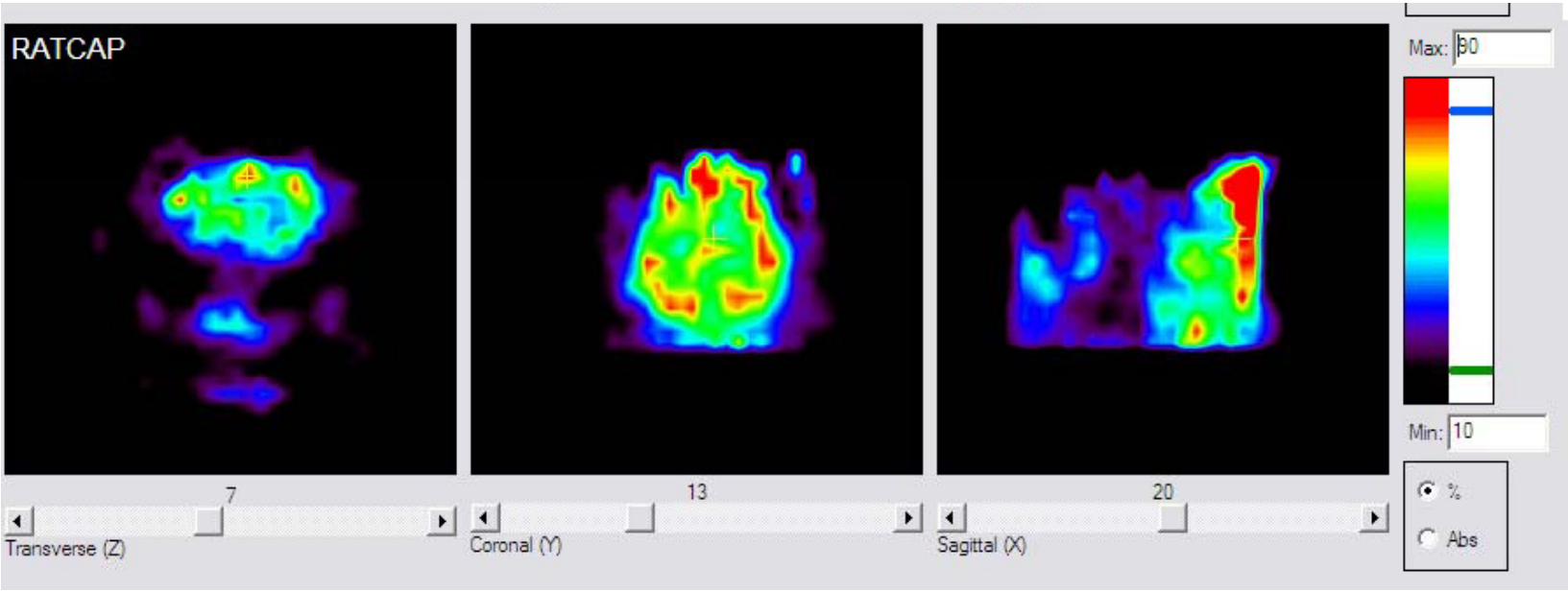
First Phantom Data

- Rat striatum phantom
  - 3.4:1 ratio
  - RatCAP
    - MLEM
    - 25 iterations
    - post-smoothing with 2 mm FWHM Gaussian

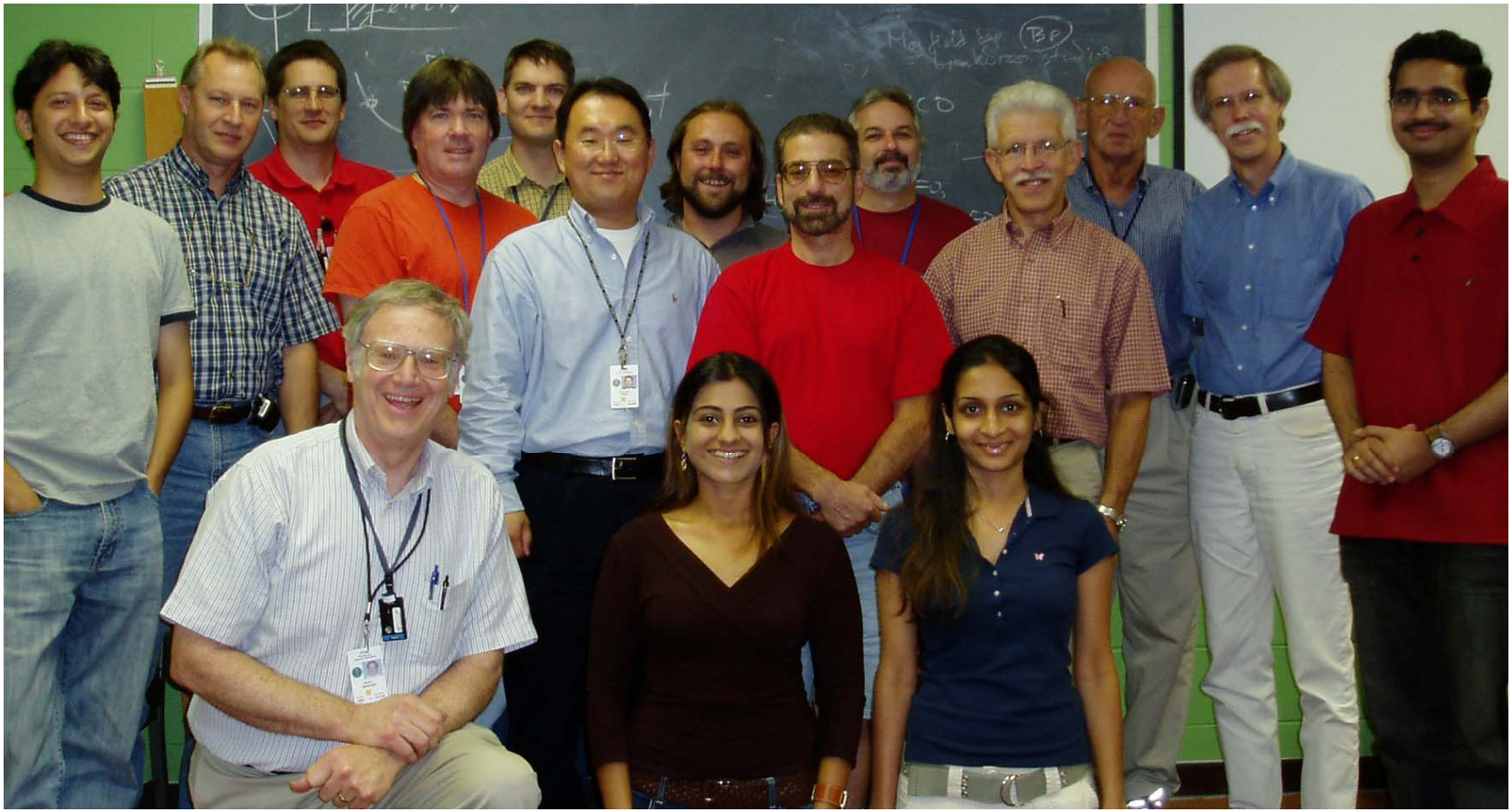




First conscious rat brain image



Thanks!



BNL RatCAP team