Time Projection Chamber (TPC) Readout:
An example of Detector Signal Processing Design and System Fabrication

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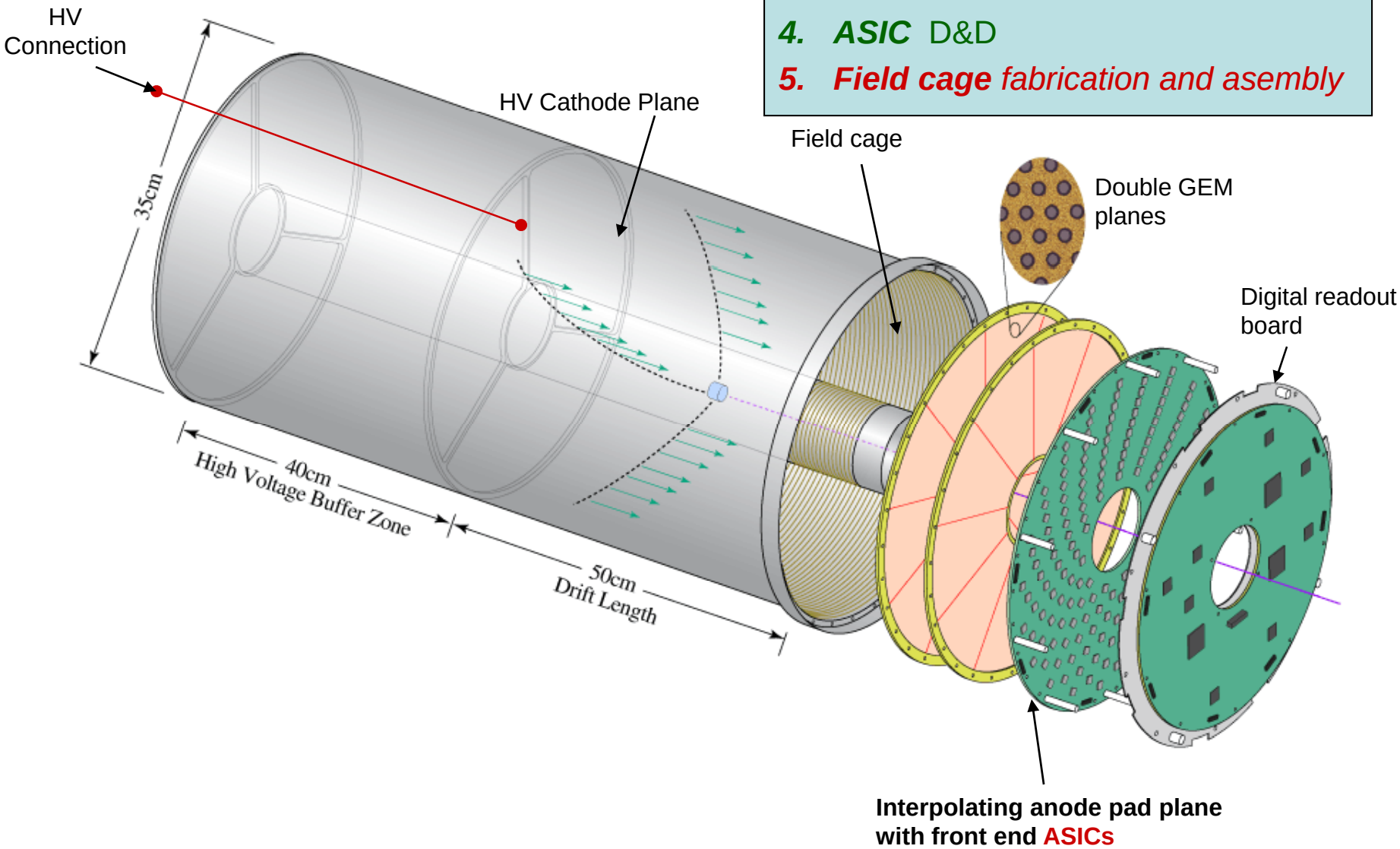
NSS Short Course 2009

TPC Critical Technologies:

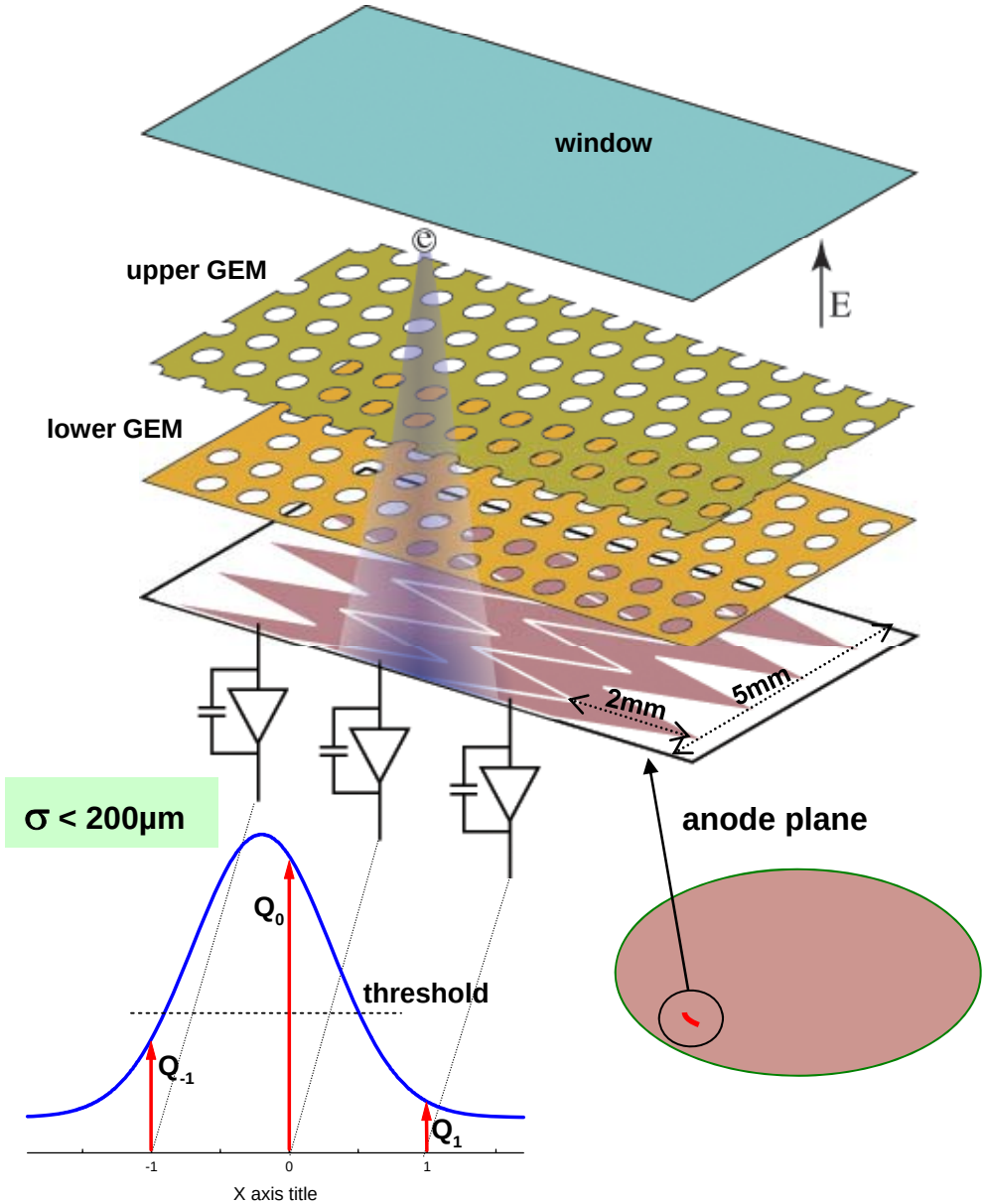
1. ***GEM*** *vs MWPC*
2. *Anode pad configuration -* ***chevron***
3. ***Anode pad – ASIC board topology and fabrication***
4. ***ASIC*** D&D
5. ***Field cage*** *fabrication and asembly*



TPC - Key Features and Parameters

- Designed for low rate (~kHz), low multiplicity environment: single sample per channel per trigger
- TPC Active Volume:
  Inner diameter ~9 cm; Outer diameter ~35 cm; Drift Length: 50 cm
- Double GEM amplification, ***gas gain <1000***
- Drift field ~ 600V/cm (30kV high voltage) max., total drift time ~ 5-7 μs.
- Interpolating zigzag anode pad plane, ~200 μm position resolution for stiff tracks; ***Pad density >10 times higher than in previous large TPCs***
- Readout channel count, ***7296***
- Customized ASICs, 32 channels per chip, 40mW per chip, ***10+6 W total***
- Electronic noise <***250e***, 500ns peaking time, single peak time and amplitude measurement, timing resolution ~ 5-15 ns
- 8 sets of ADCs digitize the sparsified and serialized data streams, worst case event processing time <0.5ms

Front-End Electronics Specifications



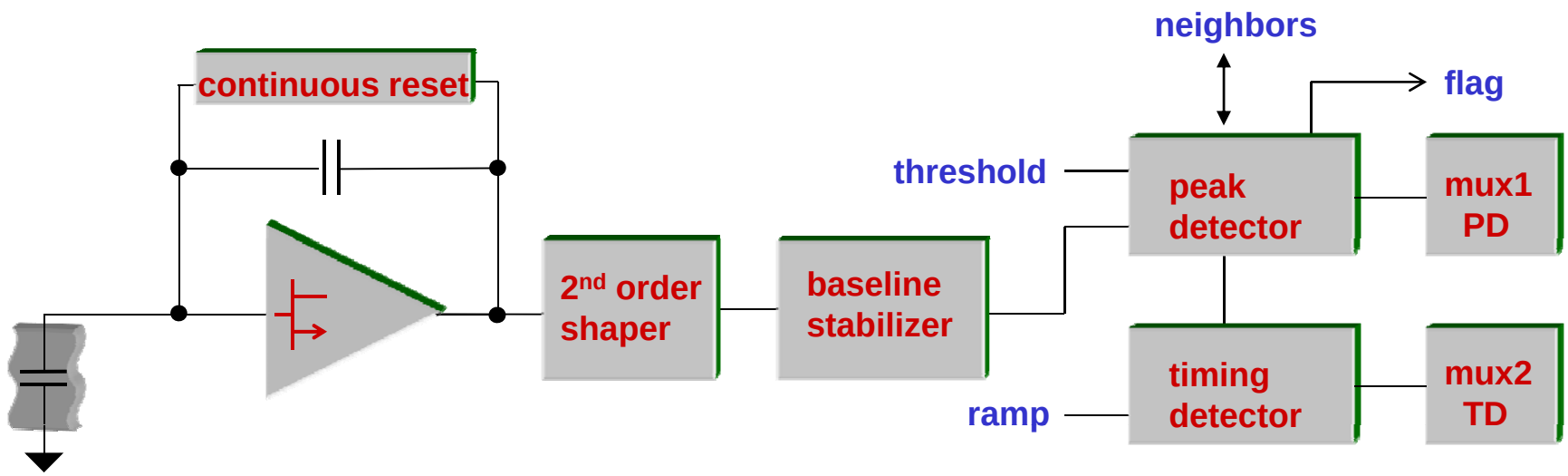
Tracking

- Rate: 2kHz
- Multiplicity: 3 tracks max
- Charge of triggered pad
- Charge of neighbor pads (centroid)
- Timing of triggered pad

Front-End Requirements

- **ENC < 250e⁻ rms** (S/N>100 at 4fC min)
- **Timing Res. < 20ns rms** (drift ~ 7μs)
- **Readout Time < 500μs** (all channels)
- **Power < 1.5mW** (<10W total)
- Preamplifier - shaper
- Pulse amplitude (peak detect) + analog memory
- Pulse timing (TAC) + analog memory
- Neighbor channel/chip logic
- Gain equalization +/- 30%, 3-bit
- Channel calibration capacitance
- Channel masking
- Analog monitor and analog buffer

ASIC Readout Channel - Block Diagram



INPUT n-MOSFET
- optimized for operating region
- ENC < 250 rms electrons
- NIM A480, p.713

CONTINUOUS RESET
- feedback MOSFET
- self adaptive
- low noise
- fully compensated
- US patents 5,793,254 & pend.
- NIM A421, p.322
- TNS 47, p.1458

SHAPER
- amplifier with passive feedback
- dual stage multiple feedback
- 2nd order, 600ns peaking time
- adjustable channel gain (3-bit)

BASELINE STABILIZER (BLH)
- band-gap referenced
- low-frequency feedback
- slew-rate limited follower
- high dc stability < 1mV
- low channel dispersion < 4mV
- TNS 47, p.818

PEAK DETECTOR
- two-phase configuration
- offset error cancellation
- high absolute accuracy < 0.2%
- US patent 6,512,399
- NIM A484, p.544

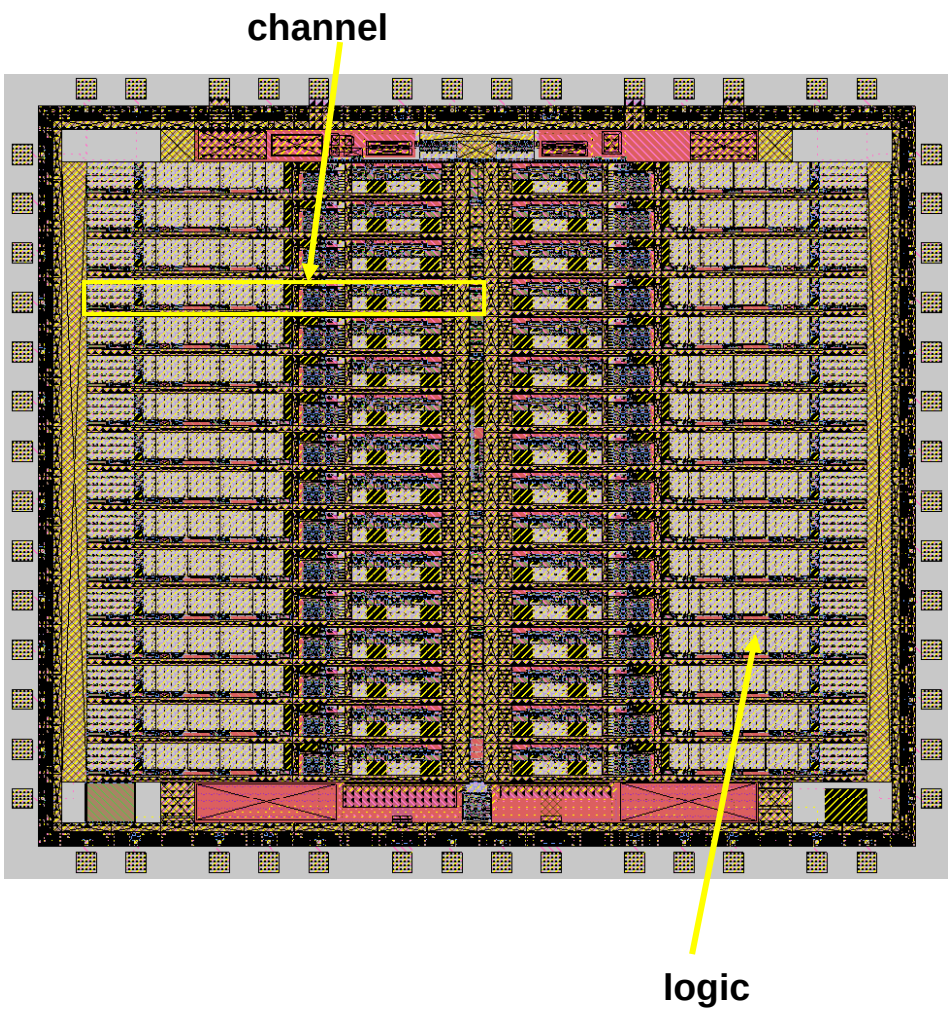
TIMING DETECTOR
- time-to-amplitude converter
- internal or external ramp
- two-phase configuration
- timing resolution < 20ns rms

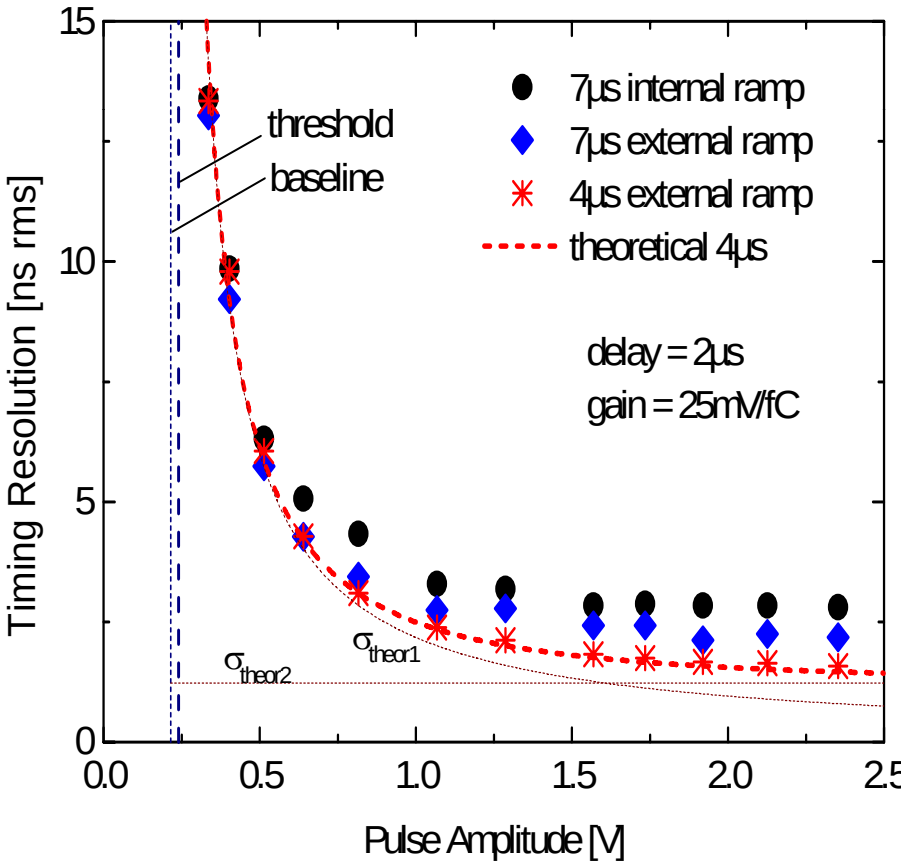
≈ 350 µW

≈ 900 µW

TPC ASIC Layout

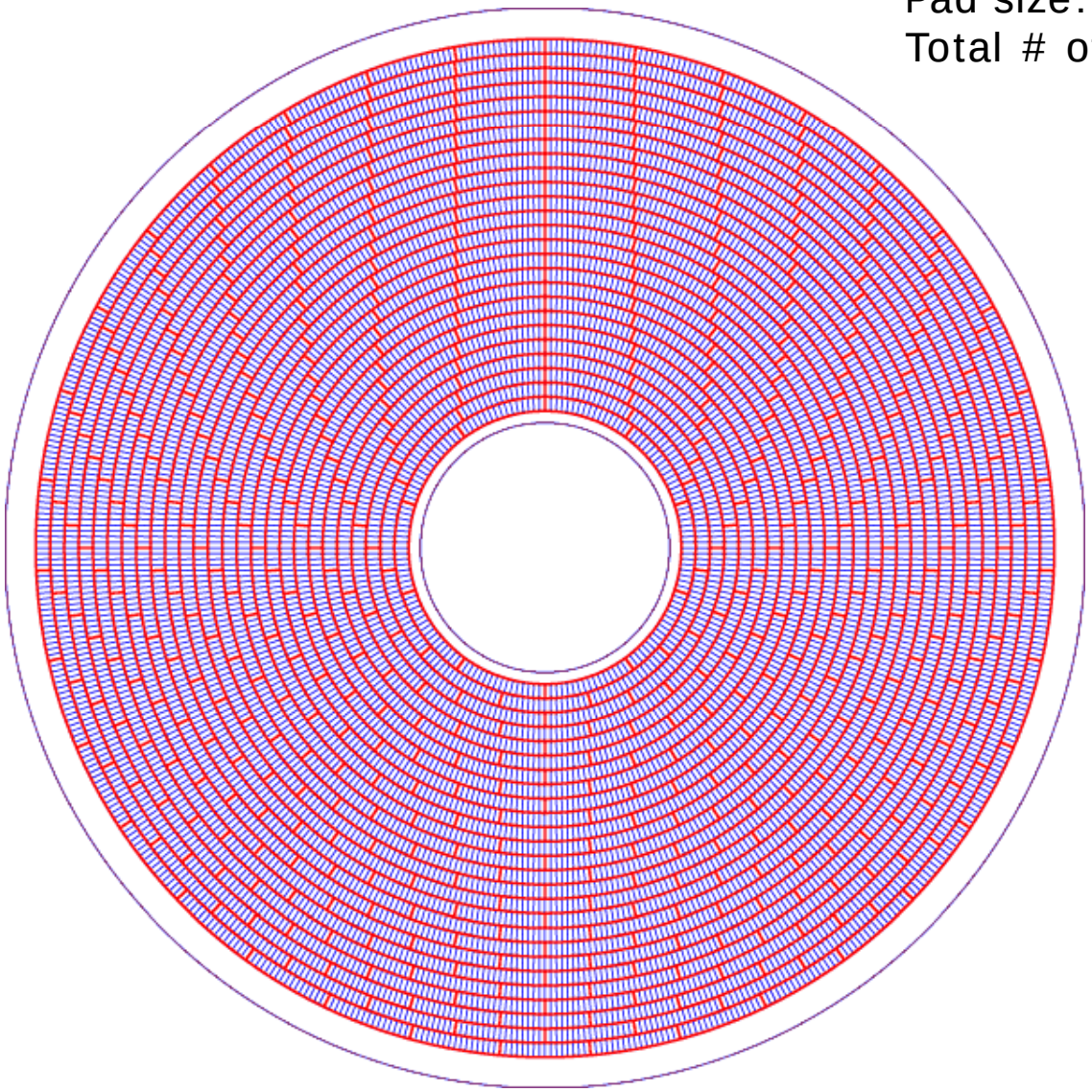
- TSMC 0.25µm
- 32 channels
- 3.1 x 3.6 mm² (~0.35 mm²/channel)
- 47k MOSFETs
- 1.2 mW/channel

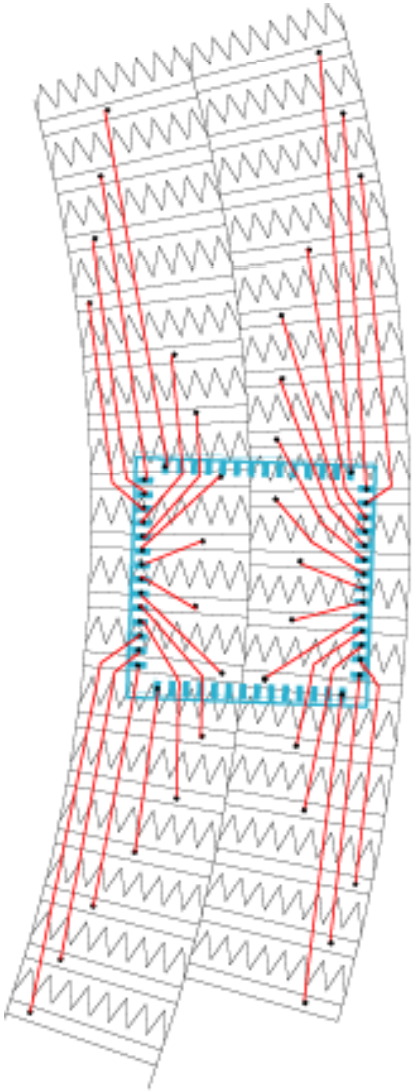




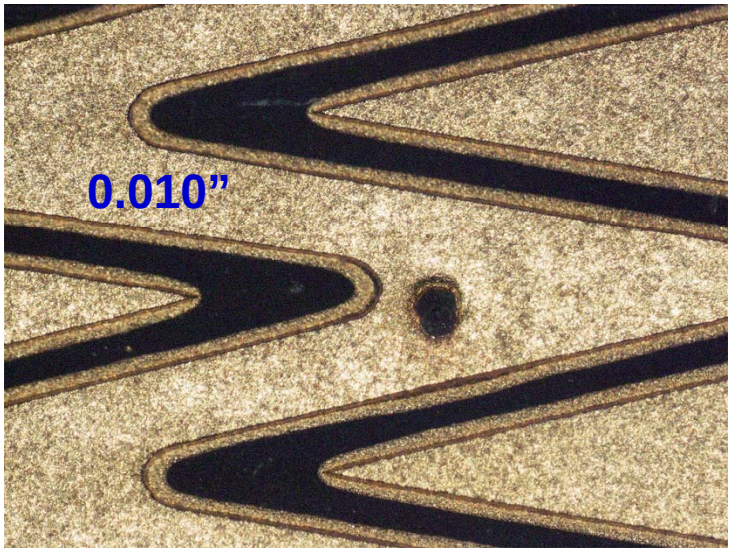
Layout of the Anode Pad Plane – Topology of the Readout Board

Pad size: ~2mmx5mm, 22 rows
Total # of Channels: ~ 7296





Anode Pad Plane – Asic Board: *A major topology and fabrication challenge (solved)*



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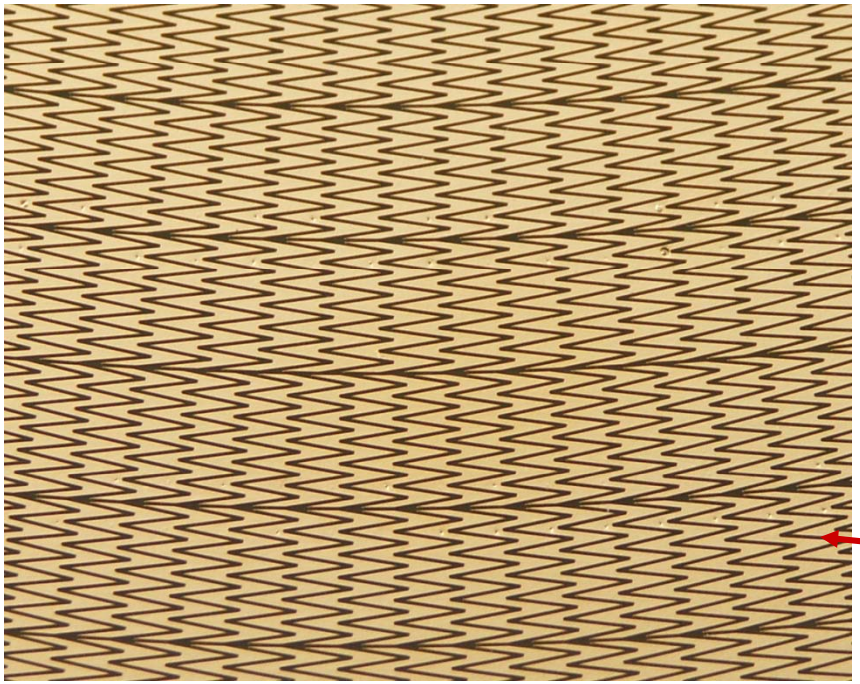
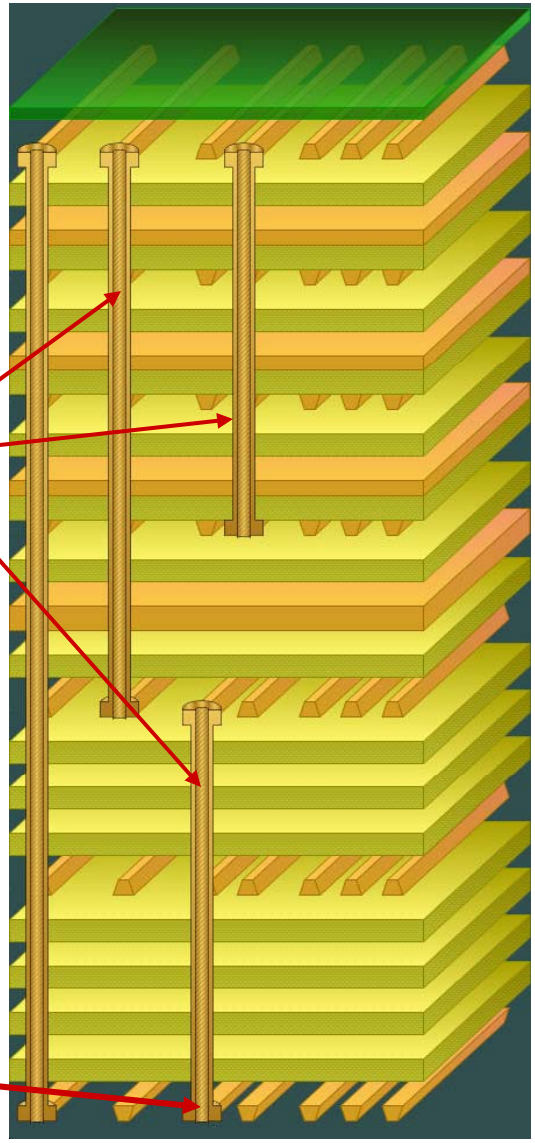
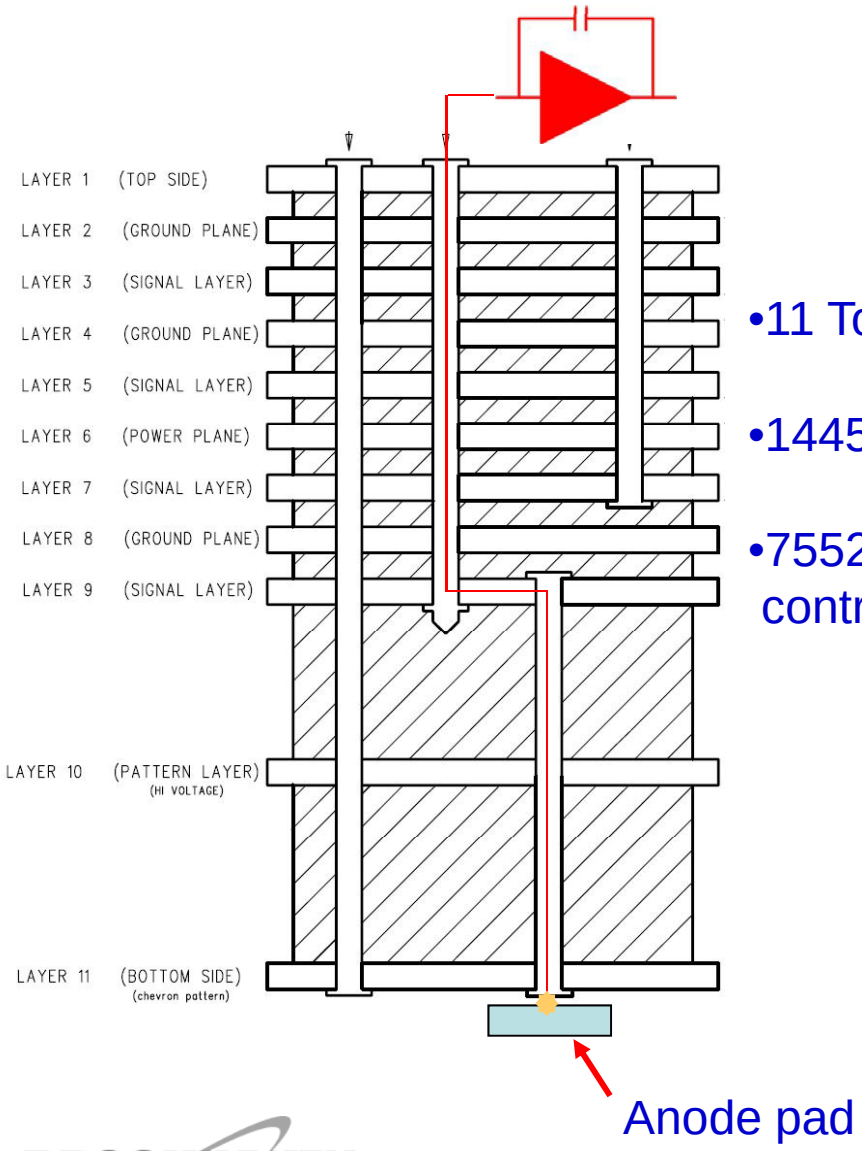


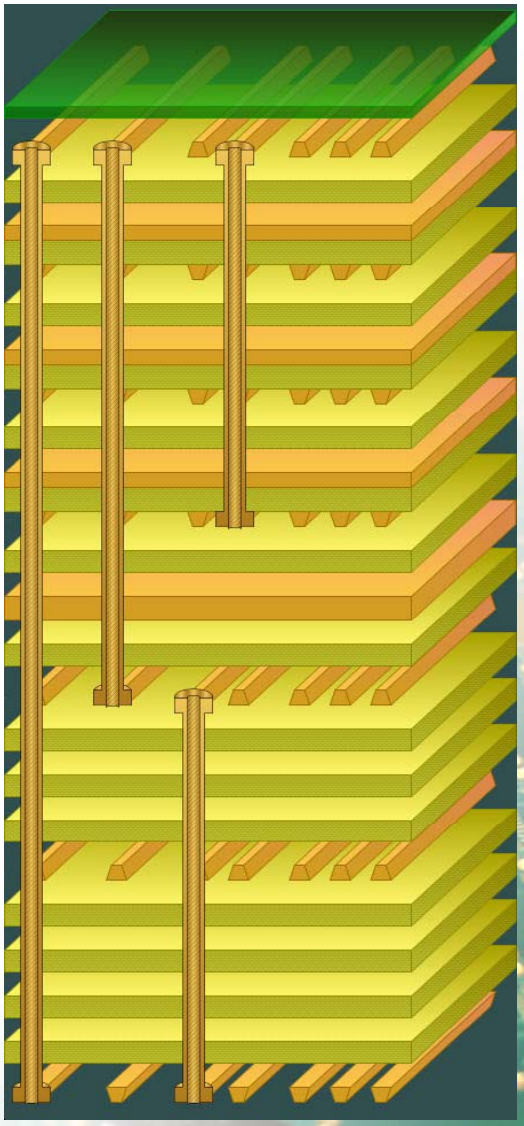
“Blind Vias”!



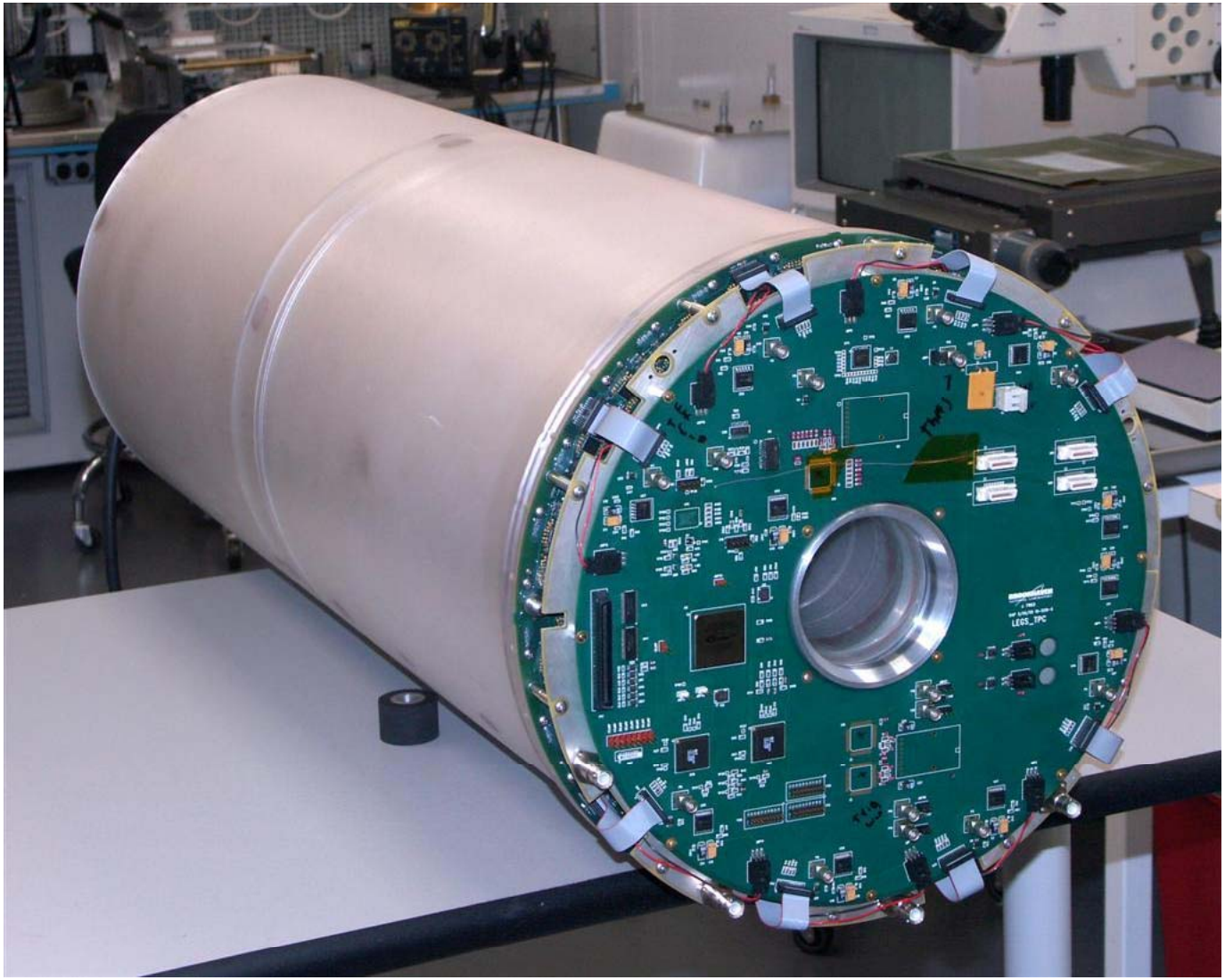
Board fabrication – Inner details



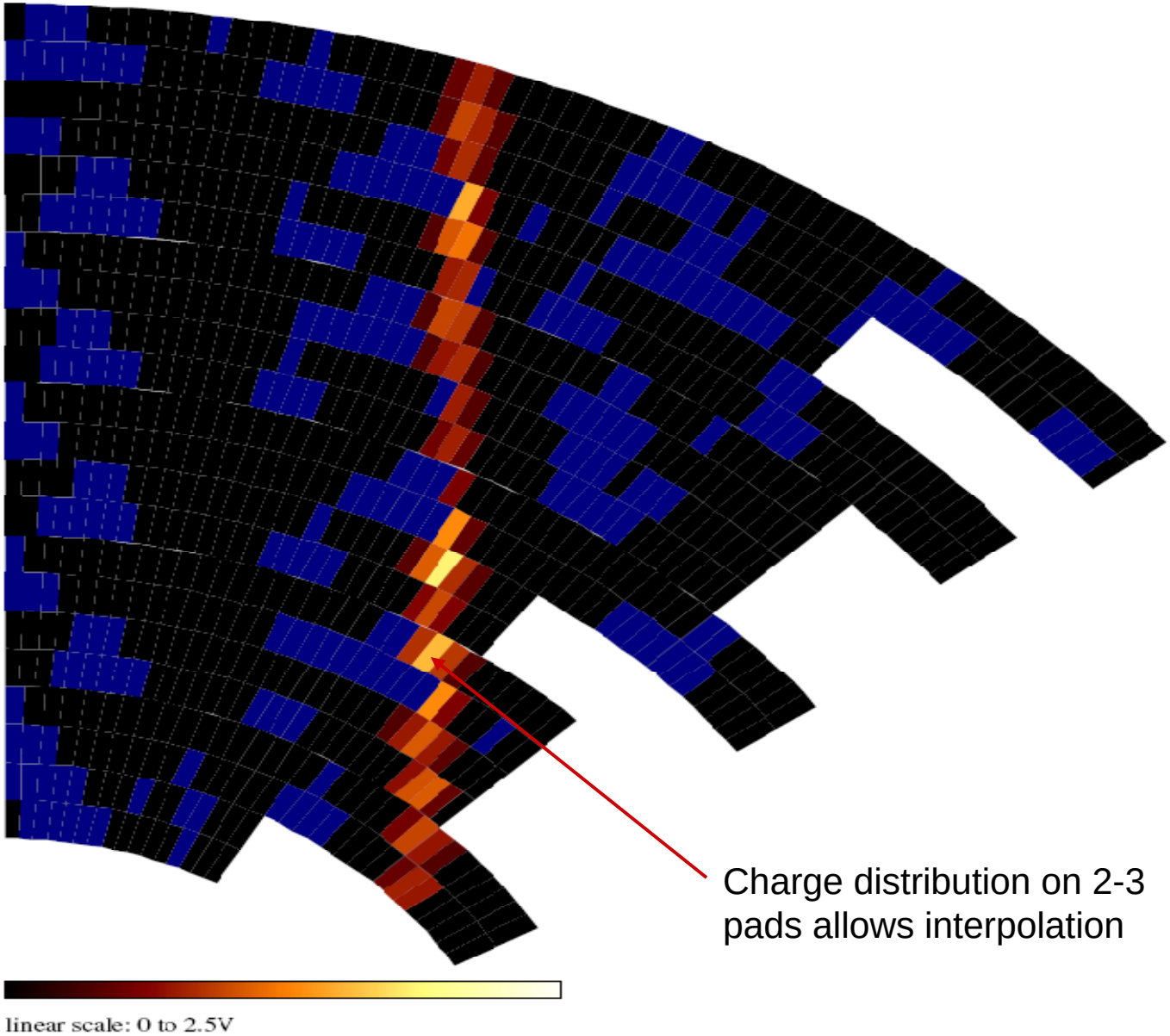
- 11 Total Layers
- 14459 Blind Vias
- 7552 Blind Vias with controlled depth drilling



BROOKHAVEN NATIONAL LABORATORY


LEGS_TPC

Prototype (short) chamber tests with cosmic rays



Concluding Remarks

Detector concept ⟷ Readout Concept

Electrode Design Interconnections Front end design	→	Capacitance Noise Power