Integrated Circuit Front Ends for Nuclear Pulse Processing

2014 IEEE Nuclear Science Symposium & Medical Imaging Conference

Short Course Schedule

8:30 a.m.	Welcome – Paul O'Connor
8:40 a.m.	Detector Signal Processing (Part I) – Veljko Radeka
10:00 a.m.	Break
10:20 a.m.	Detector Signal Processing (Part II) – Veljko Radeka
11:00 a.m.	Semiconductor Technology and Elementary Circuit Configurations (Part I) – C. de la Taille
12:00 p.m.	Lunch
1:10 p.m.	Semiconductor Technology and Elementary Circuit Configurations (Part II) – C. de la Taille
2:00 p.m.	Analog Circuit Design (Part I) – Paul O'Connor
3:00 p.m.	Break
3:15 p.m.	Analog Circuit Design (Part II) – Paul O'Connor
4:15 p.m.	Low-temperature CMOS – Veljko Radeka
4:40 p.m.	Design Examples
5:15 p.m.	Discussion period

DETECTOR SIGNAL PROCESSING

Veljko Radeka

DETECTOR SIGNAL PROCESSING

Veljko Radeka - radeka@bnl.gov

1.Signal Formation and Ramo's Theorem

2. Noise Generation Mechanisms

- Generation of noise spectra
- Random telegraph Noise (RTS) and 1/f noise

3.Equivalent Noise Charge (ENC) Calculation

- ENC calculation in time and frequency domains
- Simple ENC calculation for series and parallel noise
- ENC Calculation for *1/f* noise
- 1/f noise parameters and noise corner frequency for *1/f* vs. white noise

4.Signal Processing, i.e., "filtering" or "pulse shaping“

- Weighting function of the whole detector readout system
- Correlated and uncorrelated sampling
- Optimum weighting functions

5. Charge Amplifier Configuration

Transfer of charge from detector to amplifier

6. Total Fluctuations on a Capacitance and Charge Measurement Sensitivity

"kTC noise" and correlated sampling

7. Noise from Dielectrics

8. References on Signal Processing for Radiation Detectors

9. Concluding remarks

Appendix

A.1 Noise calculation: Time domain and Frequency domain
A.2 Parallel Noise in devices with Avalanche Gain
A.3 Noise Figure and Noise Temperature
A.4 Noise in Resistors at Different Temperatures and "Electronic Cooling" by Feedback
A.5 Zero-crossing statistics of noise
A.6 Autocorrelation function as a diagnostic tool

1. Signal Formation and Ramo's Theorem

Induced Current and Charge

W. Shockley, J. Appl. Phys. 9 (1938) 635.

S. Ramo, Proc. IRE, 27(1939) 584

Weighting field

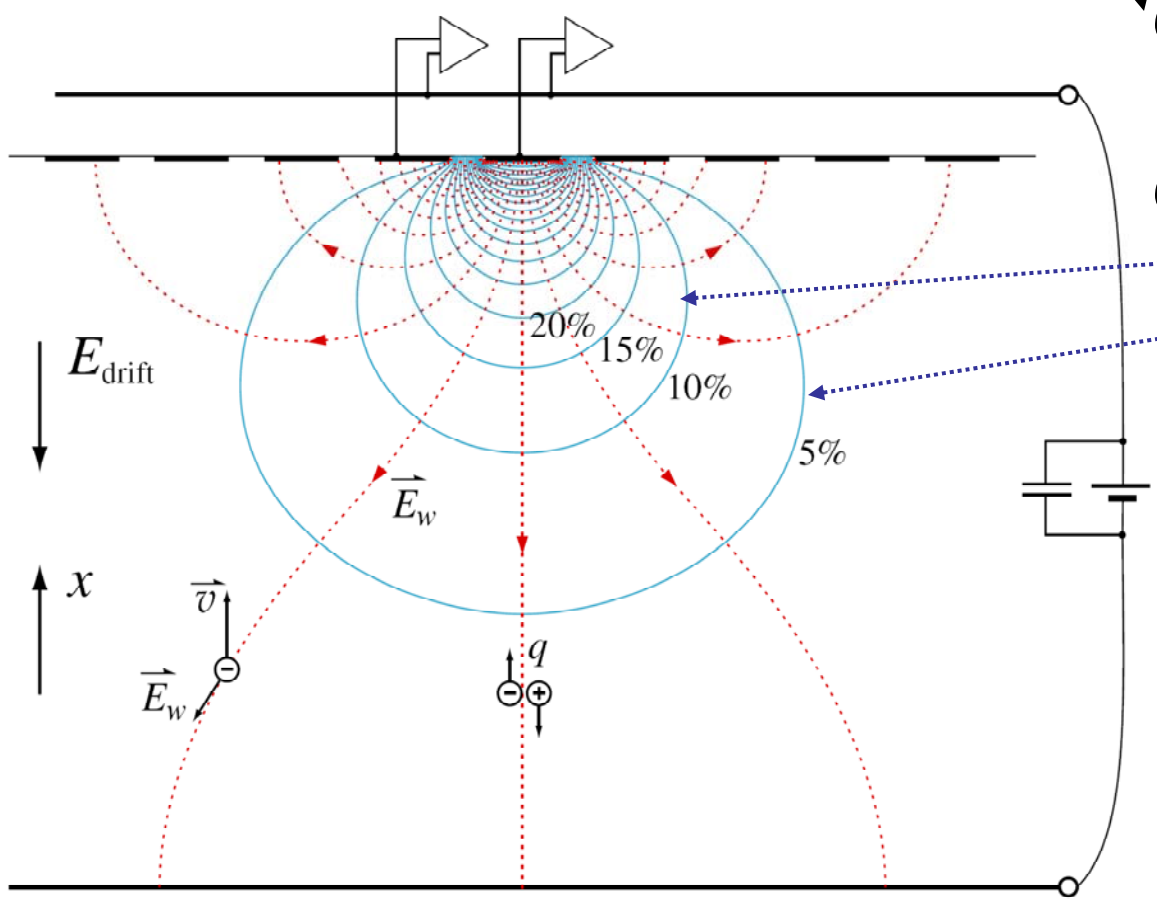
Velocity

$$i = -q\vec{E}_w \bullet \vec{v}$$

$$v = dx/dt$$

$$Q_s = \int i dt = +q\int \vec{E}_w d\vec{x}$$

$$Q_s(1,2) = q\left(V_{w2} - V_{w1}\right)$$



Weighting potentials

Shockley–Ramo theorem:

$$i = -q\vec{E}_w \bullet \vec{v}$$

$$v = dx/dt$$

Shockley–Ramo theorem states that the ***scalar product*** of the ***weighting field*** *vector* dependent on the instantaneous position of the charge cluster and *the* ***instantaneous (drift) velocity*** of the same, ***multiplied by the total charge*** of the cluster produces ***the induced current*** into a particular electrode.

The ***weighting field*** is created (imagined) in the chamber when a unity potential is applied only to that electrode while keeping all others grounded.

The ***weighting field*** is determined by the electrode geometry and is obtained by solving (usually numerically) the equation,

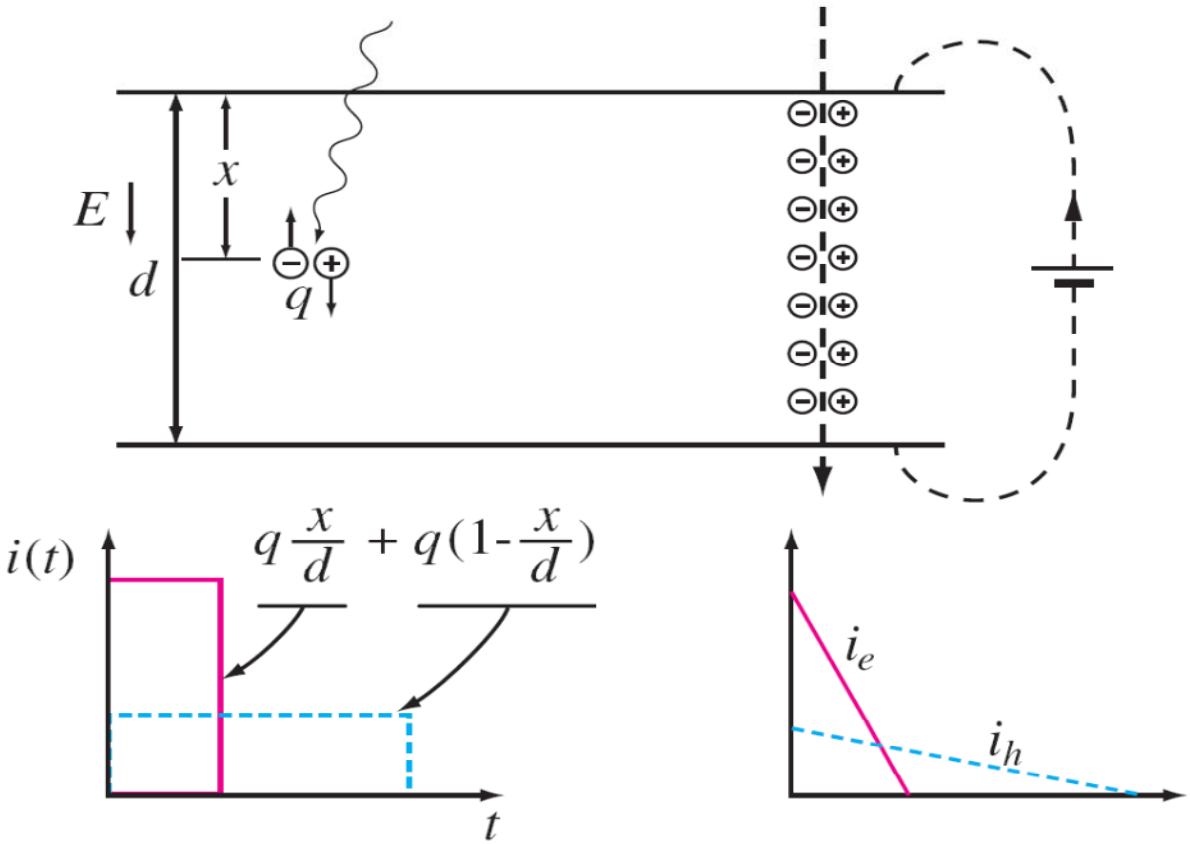
$$div\,\vec{D} = 0, \quad where \quad \vec{D} = \varepsilon\vec{E}$$

The ***physical ("operating") electric field*** is obtained by solving,

$$div\,\vec{D} = \rho$$

where ρ is charge density in the interelectrode space.

The Simplest Case: Induced Currents in Continuous Planar Electrodes for Localized and Extended Ionization in Semiconductor, Gas and Liquid Detectors



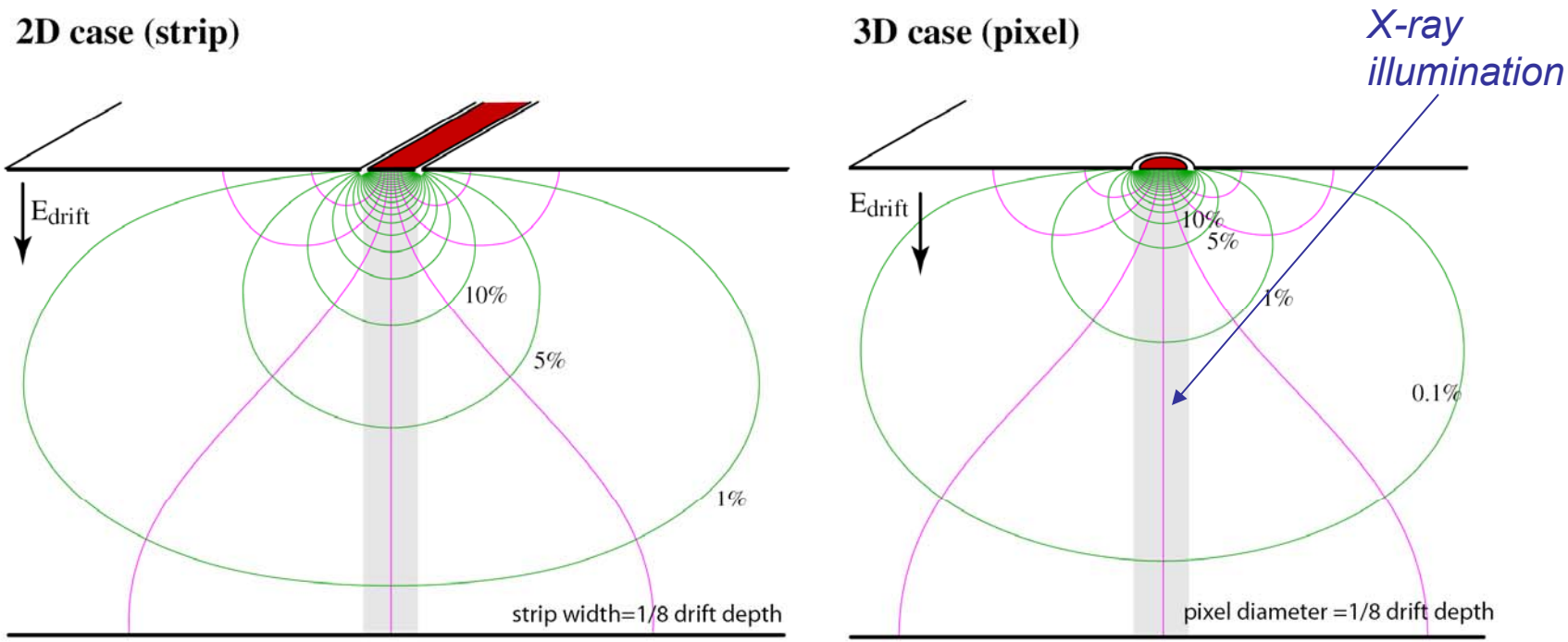
$$E_w = \frac{1}{d}$$

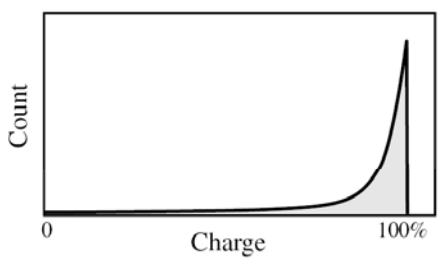
Carrier drift velocity

$$i = q \cdot \frac{v}{d} = \frac{q}{t_d}$$

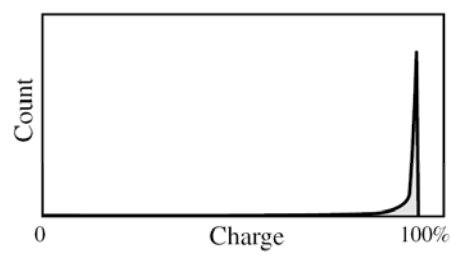
Carrier transit time

Weighting Potential and Pulse Height Distribution for Strips vs Pixels

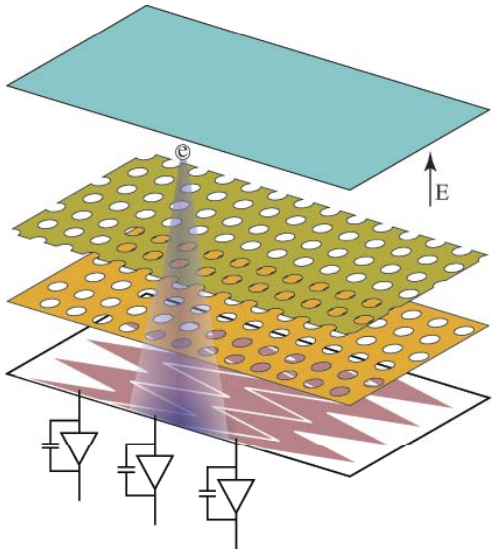


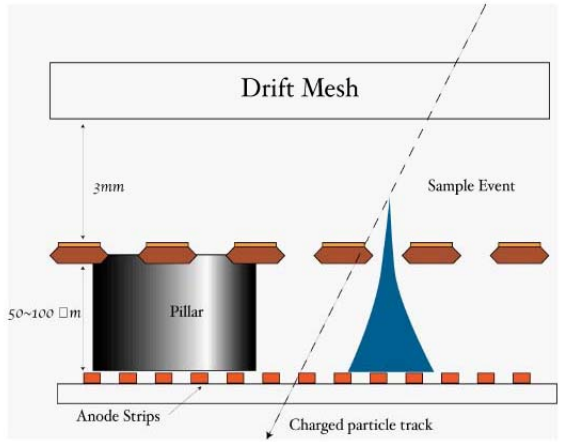


Comparison of their theoretical induced charge pulse height distributions. Assuming an ionization event creates a point charge, and the absorption probability is constant along the depth.

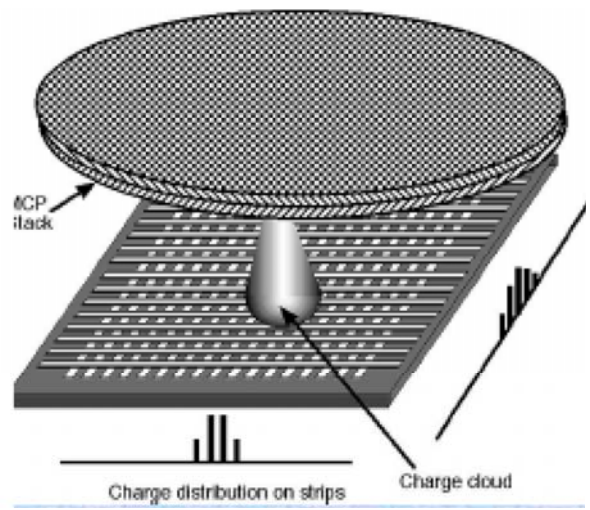


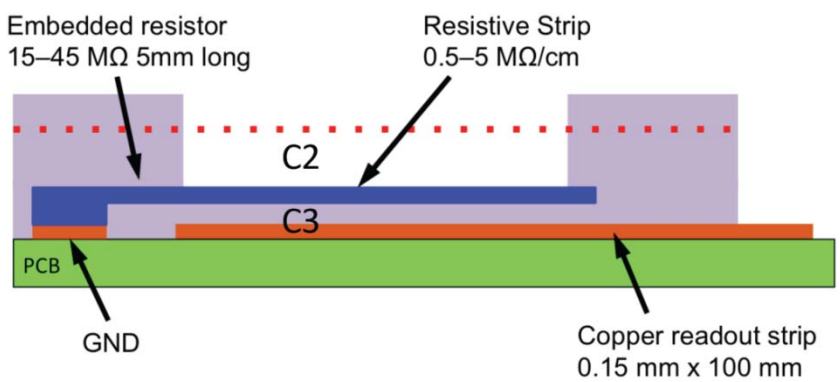
Charge collection and signal formation in GEM (Gas Electron Multiplier), Micromegas (MICROMEsh GAseous Structure) and MCP (Micro-Channel Plate) based detectors.

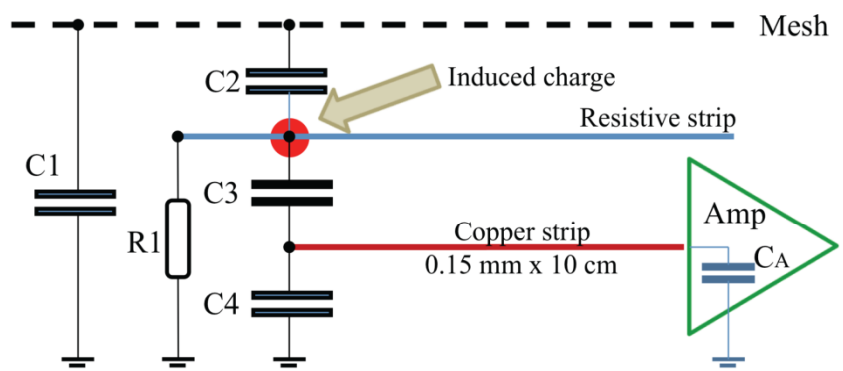




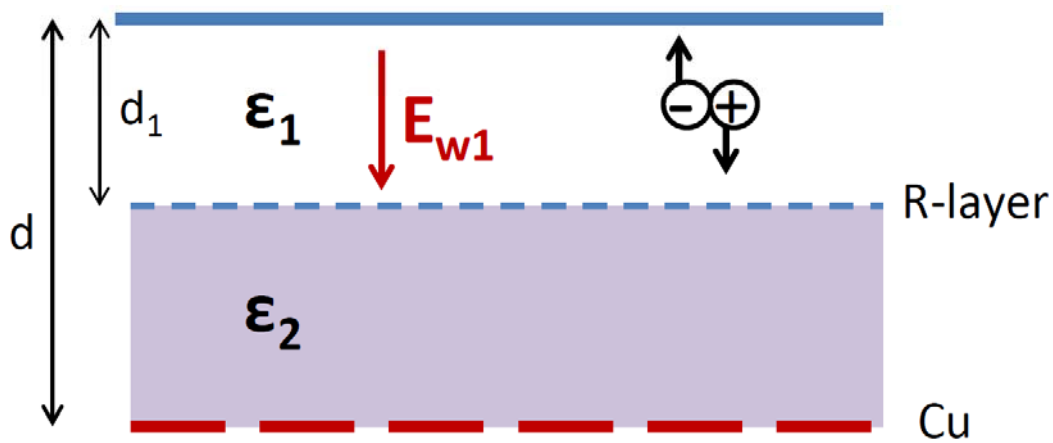
MCP (from B. Feller)







Weighting Field and Induced Charge with a Dielectric in the Interelectrode Gap



$$\frac{E_{w1}}{(1/d)} = \left[\frac{\varepsilon_1}{\varepsilon_2} + \frac{d_1}{d_2}\left(1 - \frac{\varepsilon_1}{\varepsilon_2}\right)\right]^{-1}$$

For: $\frac{\varepsilon_1}{\varepsilon_2} = \frac{1}{4};\ \frac{d_1}{d} = \frac{1}{2} \rightarrow E_{w1} = \frac{1.6}{d}$

$$\frac{\varepsilon_1}{\varepsilon_2} = 1;\ \frac{d_1}{d} = \frac{1}{2} \rightarrow E_{w1} = \frac{1}{d}$$

Induced charge on Cu is *0.8* with dielectric layer, instead of 1.0 without.

Notes on Weighting Field - Potential and Induced Signals

- *Note that the **(operating) electric field** and the **weighting field** are distinctly different.*
- The (operating) electric field determines the charge trajectory and velocity.
- The (fictitious) weighting field depends only on geometry and determines how charge motion couples to a specific electrode.
- *Only in 2-electrode configurations are the operating electric field and the weighting field of the same form.*
- Because the weighting potential is strongly peaked near the signal electrode, most of the charge is induced when the moving charge is near the signal electrode.
- As a result, the signal charge is due to the charge terminating on the signal (measurement) electrode.
- In general, if moving charge does not terminate on the measurement electrode, signal current will be induced, but the current changes sign and integrates to zero.
- The exception is, if the measurement (observation; integration) time is shorter than the charge transit time, a net charge will be observed on the electrodes other than the electrode where the charge is eventually collected, thus resulting in *crosstalk by charge induction*.
- There are *two types of crosstalk* on the detector, *by charge induction* and *by capacitive coupling* among the electrodes.

2. Noise mechanisms

Noise Spectra Origin and Transformation

Impulse Response — Transfer Function

$$h(t) \overset{\mathcal{F}}{\Leftrightarrow} H(j\omega)$$

Random sequence of impulses → "white" noise:

W_0= const.

$$W(\omega) = W_0 \left| H(j\omega) \right|^2$$

Relaxation process → Lorentzian spectral density:

$$W(\omega) = W_0 \left(1 + \omega^2 \tau^2\right)^{-1}$$

$$\frac{1}{\tau} e^{-\frac{t}{\tau}} \Leftrightarrow \frac{1}{1 + j\omega\tau}$$

Random walk → ***1/ω²*** noise:

$$W(\omega) \simeq W_0 \left(const / \omega^2\right)$$

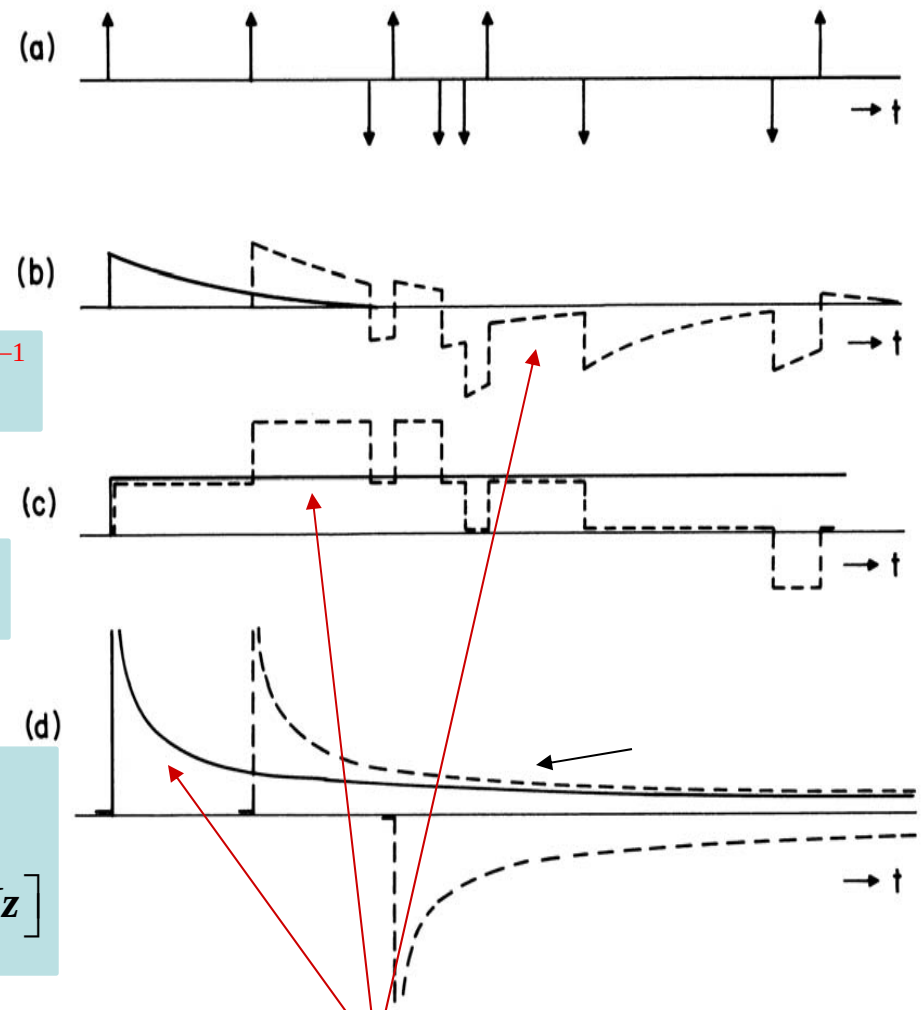
$$U(t) \Leftrightarrow 1/j\omega$$

"1/f " *noise*:

$$W(\omega) = W_0 \left(const / |\omega|\right)$$

$$v_n^2(f) = A_f / f \qquad \left[V^2/Hz\right]$$

$$U(t)/t^{1/2} \Leftrightarrow 1/(j\omega)^{1/2}$$



White noise ⊗ ***transforming filter =***

Shot Noise and Thermal Noise Spectral Densities and Variance Calculation

- Noise spectral density for ***shot noise*** (Poisson sequence of impulses each carrying charge ***q***, at a mean rate ***n***):

$$W_0 = i_n^2 = 2\bar{n}q^2 = 2qI_0 \quad \left[A^2/Hz\right]$$

- Noise spectral density for ***thermal noise*** (also known as Johnson-Nyquist noise):

$$W_0 = v_n^2 = 4k_BTR \quad \left[V^2/Hz\right]$$

- The above equation is a good approximation at any practical radio frequency (i.e. frequencies below about 1THz at T=300K). In the general case, which includes up to optical frequencies, the power spectral density of the voltage across the resistor *R*, in V^2/Hz is given by:

$$W_0 = v_n^2 = \frac{2Rhf}{e^{\frac{hf}{k_BT}} - 1} \qquad \frac{hf}{k_BT} \ll 1$$

- ***Campbell's theorem*** (from the principle of superposition):

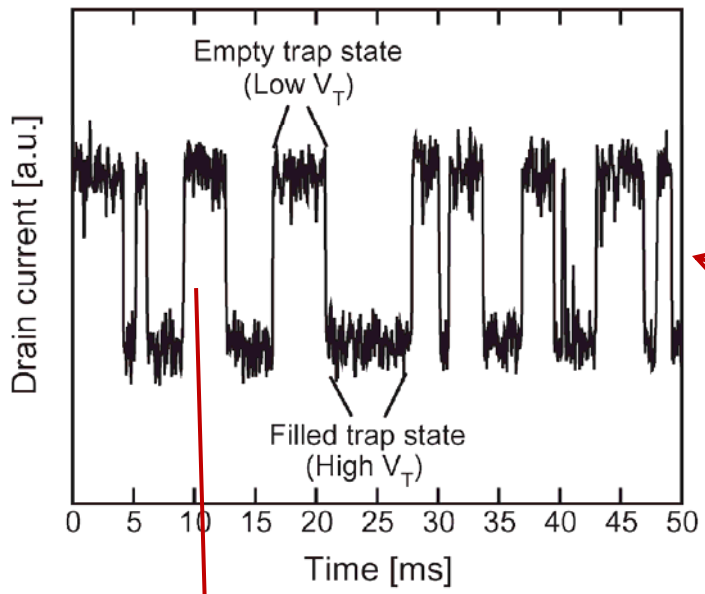
$$\sigma^2 = \bar{n}q^2 \int_{-\infty}^{\infty} h^2(t)dt$$

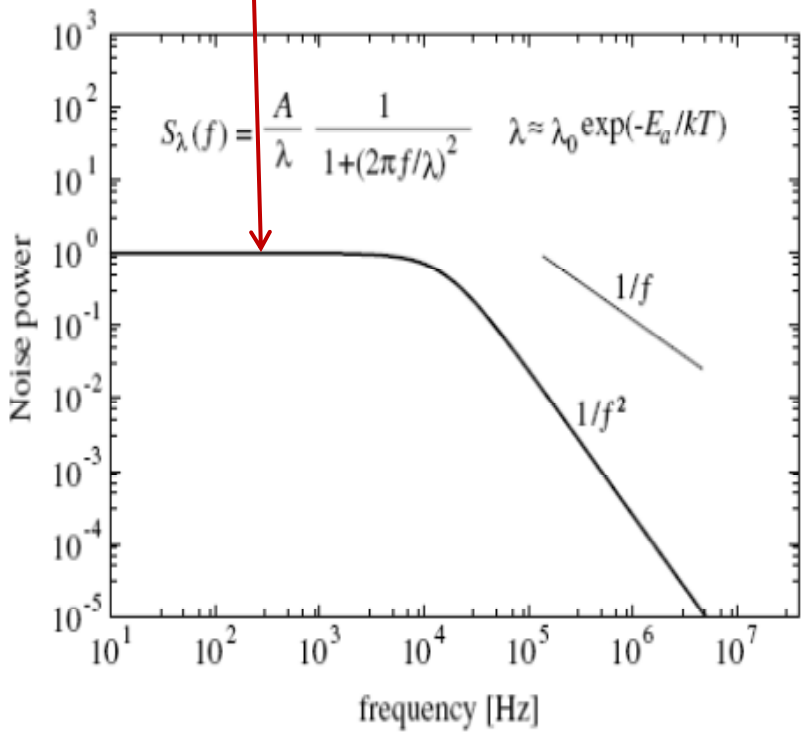
- From Parseval's theorem, noise <u>*variance*</u> ("power") can be expressed in both ***frequency*** and ***time domains***:

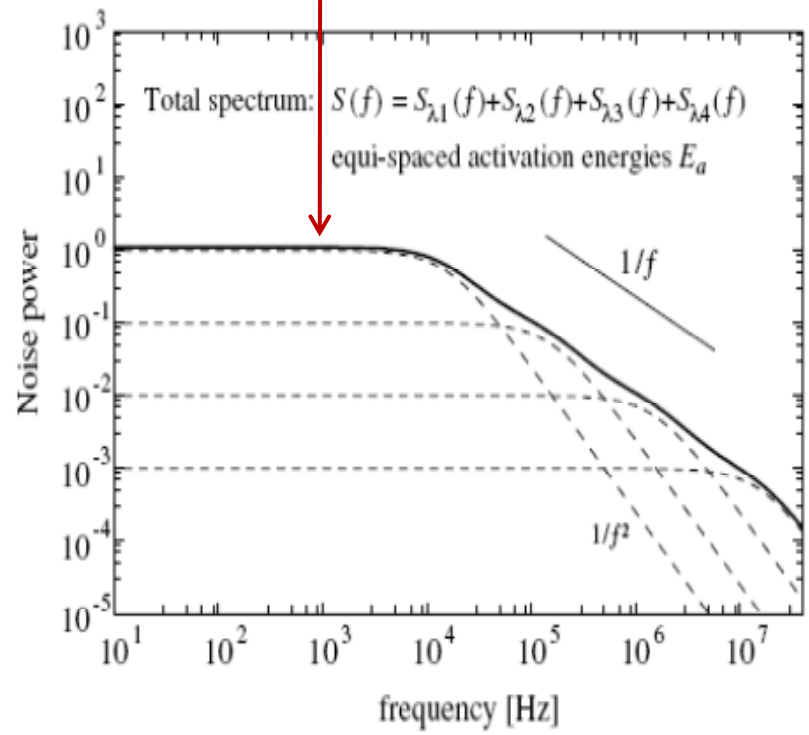
$$\sigma^2 = \bar{n}q^2 \int_{-\infty}^{\infty} h^2(t)dt = 2\bar{n}q^2 \int_{0}^{\infty} \left|H(\omega)\right|^2 df$$

Low frequency Noise: Trapping Noise – from RTS (Random Telegraph Noise to *1/f* Noise

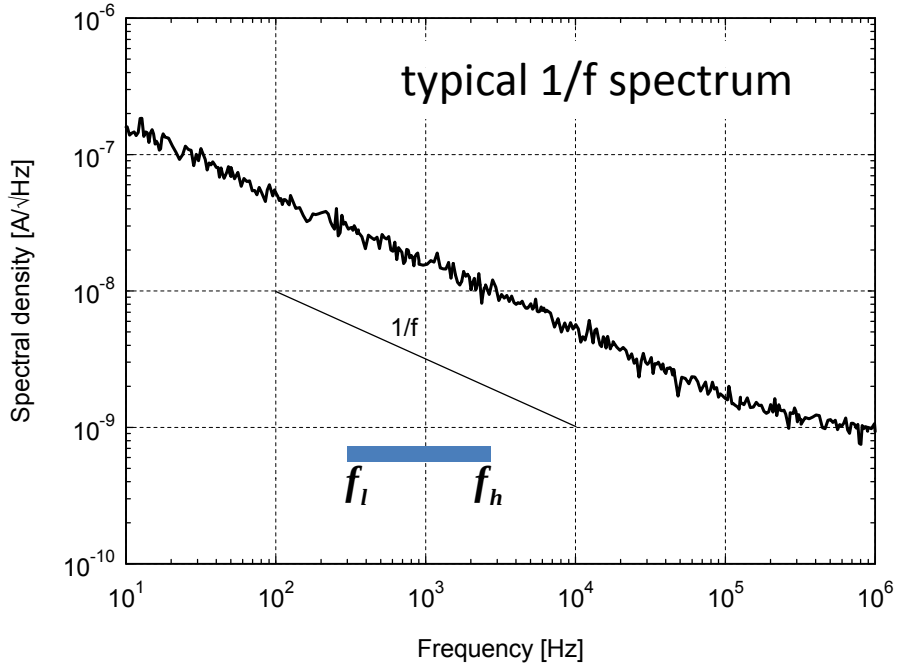
- Single trap → Lorentzian spectrum
- Distribution of traps → *1/f* spectrum







"Self-similarity" of 1/|*f*| Noise (scaling invariance)



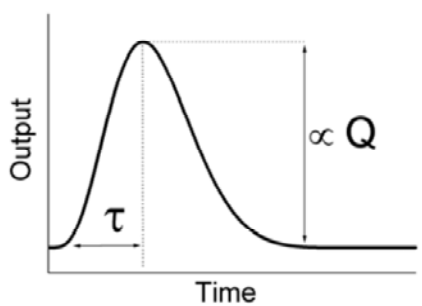
$$\sigma(f_l, f_h) \propto \left(\ln \frac{f_h}{f_l}\right)^{1/2} \quad rms$$

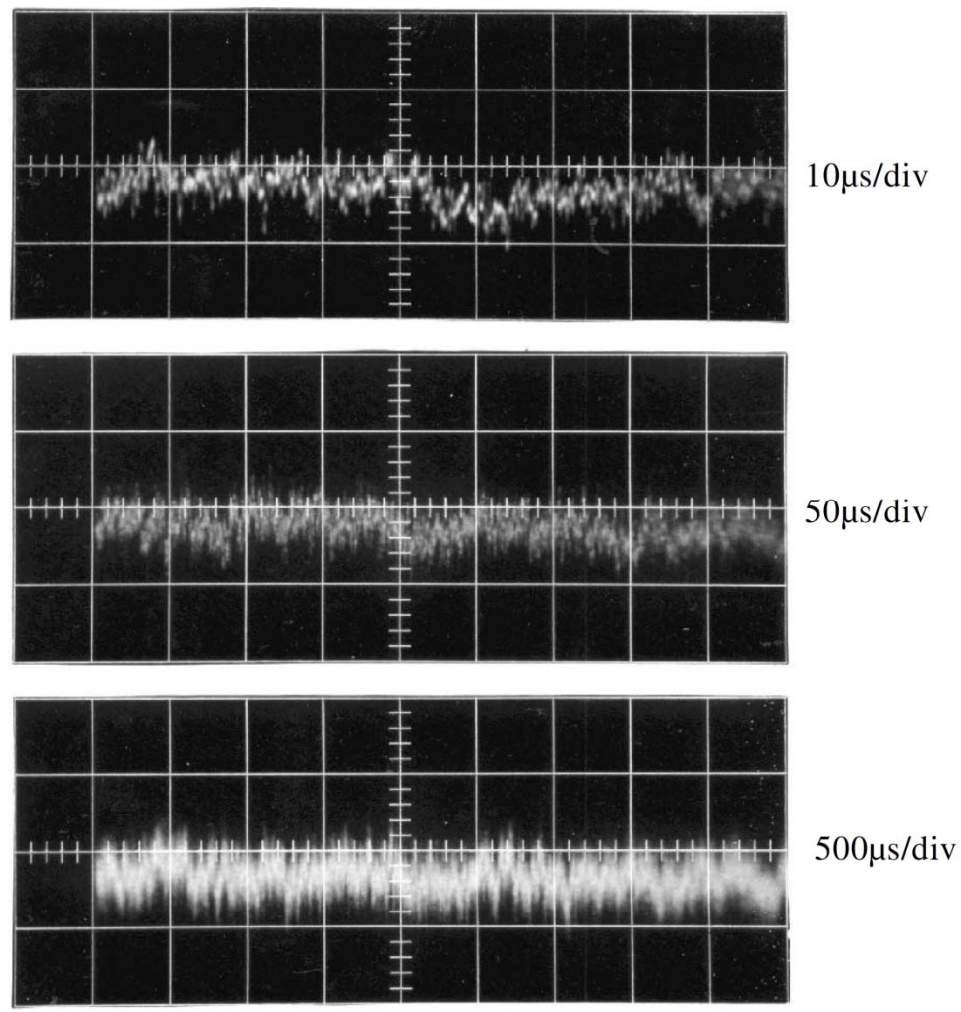
Variance (noise power):

$$\sigma(f_l, f_h)^2 = \int_{f_l}^{f_h} \frac{A_f}{f} df = A_f \ \ln \frac{f_h}{f_l}$$

$\sigma(f_l, f_h)$ constant for same ratio f_h/f_l

i.e., independent of shaping (peaking time) $\boldsymbol{\tau}$

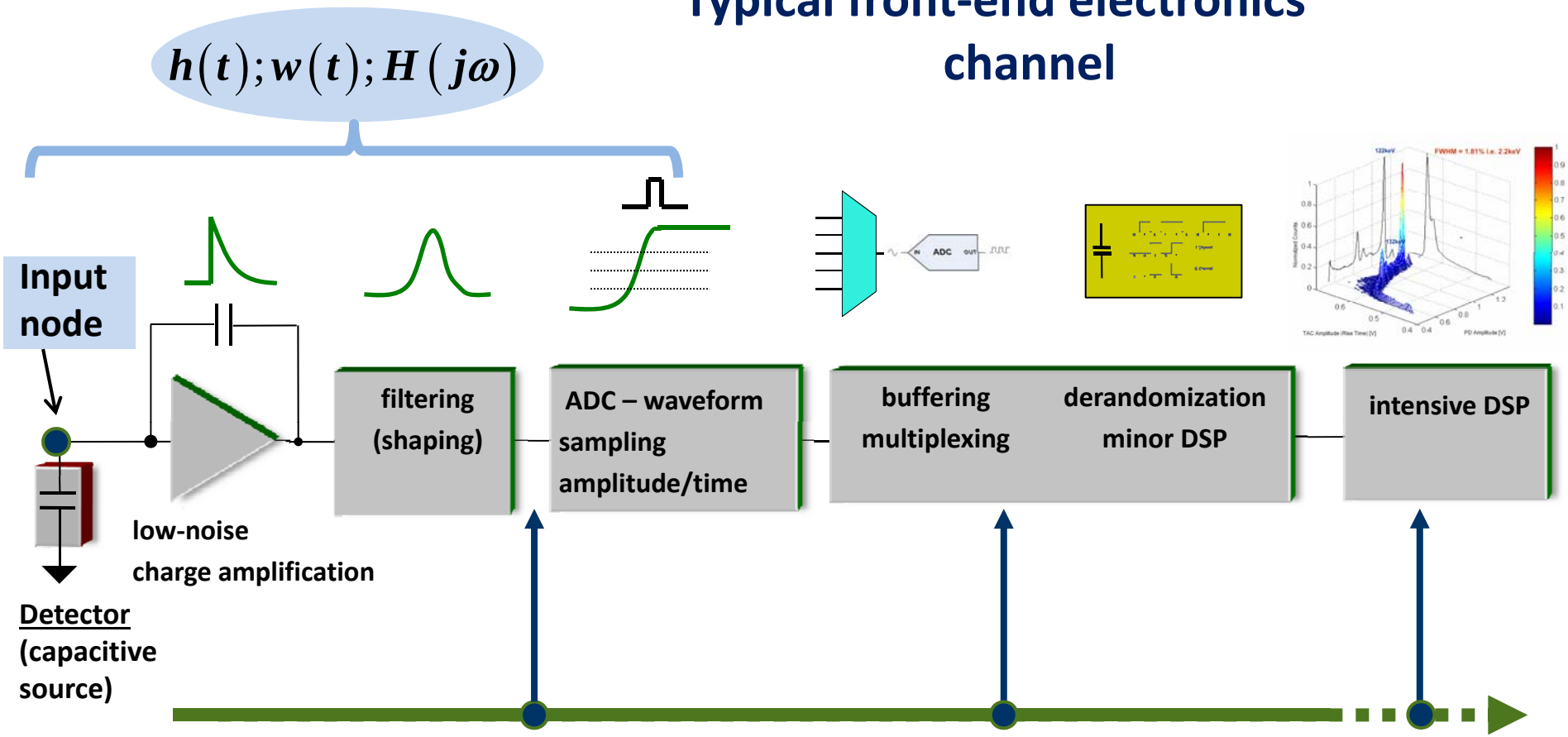


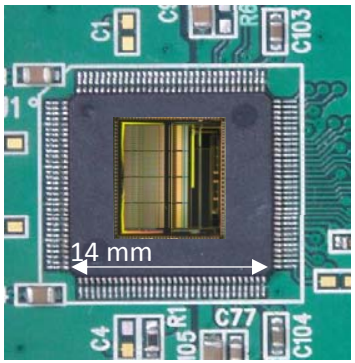


1/|*f*| noise — different time scales

3. Equivalent noise charge (ENC) calculation

Typical front-end electronics channel





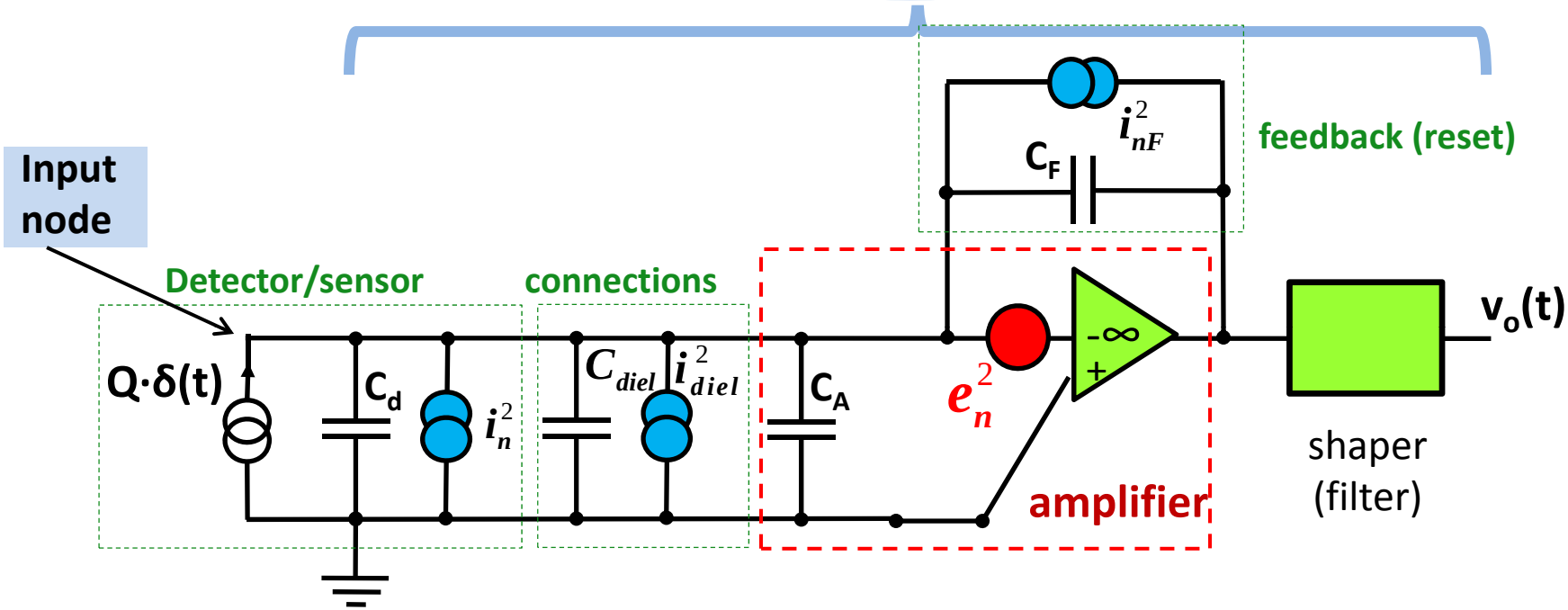
year 2000
- 500 nm technology
- 16,000 transistors
- 16 channels
- analog

year 2010
- ~ 180 nm technology
- ~ 1M transistors
- ~ 100 channels
- analog and digital (mixed-signal)

year 2013
- ≤ 130 nm technology
- >> 1M transistors
- >> 100 channels

Noise Sources in Detector-Amplifier

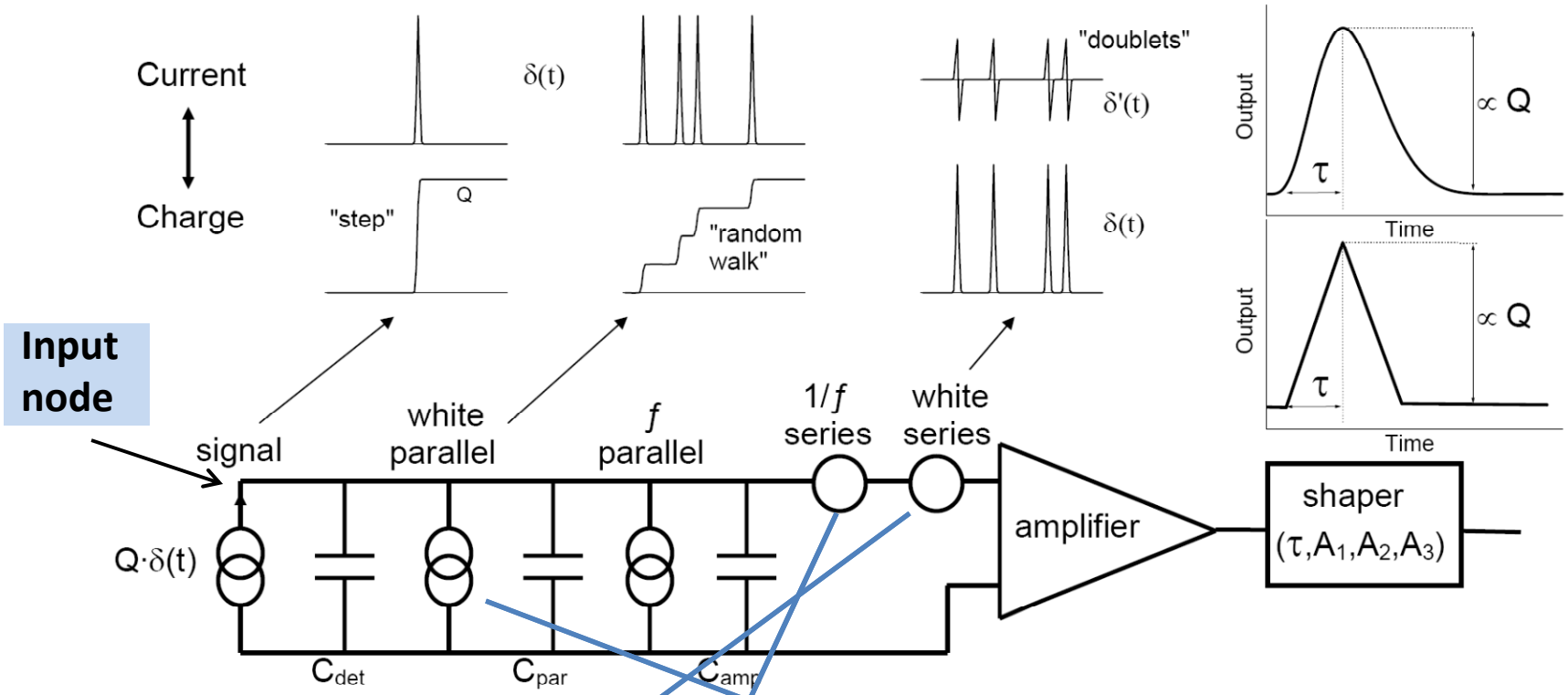
Overall system processing function: $h(t); w(t); H(j\omega)$



Dominant noise sources are from the components and circuits **directly connected to the input node**. Noise sources from the rest of the signal processing chain should be made negligible.

- i_n^2 arises in the sensor, e.g., from the leakage (dark) current; i_{nF}^2 may arise in feedback circuit
- i_{diel}^2 thermal fluctuations in dielectrics (dielectric loss noise, Lecture 6).
- e_n^2 **noise associated with gain mechanism in the input transistor (known as "*series white noise*").**
  (*1/f* eq. noise voltage generator in series with e_n^2 not shown for simplicity)

Noise Sources and Spectral Densities in Charge Amplifiers



$$v_n^2 = e_n^2 + \frac{2\pi A_f}{\omega} + 2q_e I_0 \frac{1}{C_{in}\omega^2}$$

$$i_{neq}^2 = v_n^2 \omega^2 C_{in}^2 = \omega^2 C_{in}^2 e_n^2 + 2\pi C_{in}^2 A_f \omega + 2qI_0$$

Noise spectral density:

Voltage: $e_n \left[nV/Hz^{1/2} \right]$

Current: $I_0 \left[fA, pA, nA, \ldots \right]$

Looking at the system in ***frequency domain****:

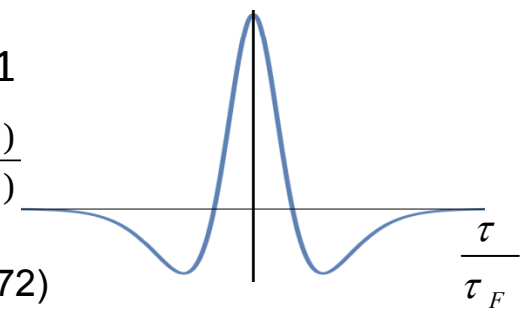
Equivalent input noise **current** x Anti-aliasing transfer function → **voltage** noise output

***Noise correlation function is in *time domain* (slides).**

Output noise correlation function

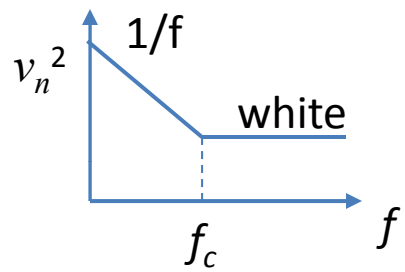
$$K_{out}(\tau) = \frac{1}{\pi}\int_0^\infty W_{out}(\omega)\cos(\omega\tau)d\omega$$

$$k(\tau) = \frac{K_{out}(\tau)}{K_{out}(0)}$$

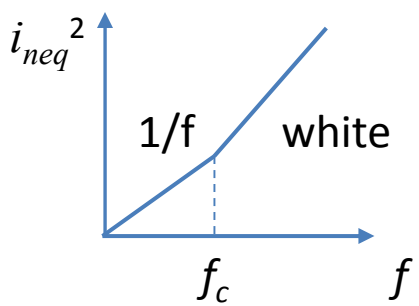


(see slides 70-72)

"Series"Noise in 1st transistor



Equivalent input noise **current** spectrum

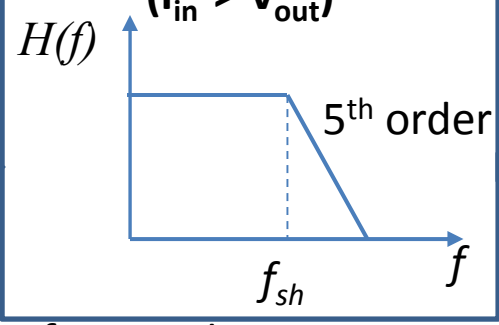


$i_{neq}^2 = v_n^2\omega^2C_{in}^2$

(see slide 19)

Analog front-end transfer function

(I_{in}-> V_{out})

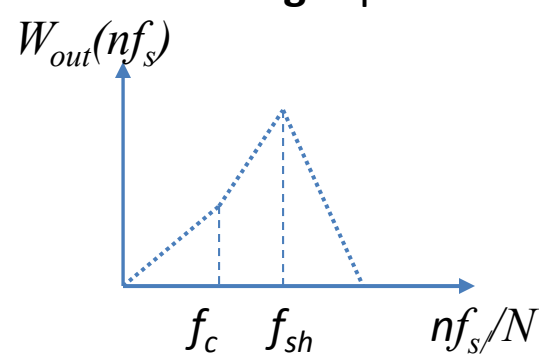


f_{sh} ~ 250 kHz @ 1µs,

and ~ 83 kHz @ 3 µs

(see slide 39)

Anti-aliasing filter output noise **voltage** spectrum



Equivalent Noise Charge (ENC) – Integrals and Coefficients A1, A2, A3

$$ENC^2 = \frac{1}{2\pi}\int_0^\infty i_{neq}^2 \left|H(\omega)\right|^2 d\omega = \frac{1}{2\pi}\int_{-\infty}^\infty \left(\tfrac{1}{2}\right) i_{neq}^2 \left|H(\omega)\right|^2 d\omega$$

$$ENC^2 = \tfrac{1}{2} e_n^2 C_{in}^2 I_1 + \pi C_{in}^2 A_f I_2 + q I_0 I_3 = \tfrac{1}{2} e_n^2 C_{in}^2 \frac{A_1}{\tau} + \pi C_{in}^2 A_f A_2 + q I_0 A_3 \tau$$

$$I_1 = \int_{-\infty}^\infty \left[w'(t)\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^\infty \left|H(j\omega)\right|^2 \omega^2 d\omega = \frac{A_1}{\tau}$$

Series white

$$I_2 = \int_{-\infty}^\infty \left[w^{(1/2)}\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^\infty \left|H(j\omega)\right|^2 \omega\, d\omega = A_2$$

1/f

$$I_3 = \int_{-\infty}^\infty \left[w(t)\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^\infty \left|H(j\omega)\right|^2 d\omega = A_3 \tau$$

Parallel white

Time domain (weighting function)

Frequency domain (transfer function)

Noise Calculation: Time Domain and Frequency Domain

- For <u>time invariant</u> systems impulse response <u>h(t)</u> and weighting function <u>w(t)</u> are interchangeable for noise calculations.

From Parseval's theorem, noise variance can be expressed as:

$$\sigma^2 = \bar{n}\, q^2 \int_{-\infty}^{\infty} h^2(t)dt = 2\,\bar{n}\, q^2 \int_{o}^{\infty} |H(\omega)|^2\, df$$

Campbell's theorem

Also: $\sigma^2 = W_o \int_{o}^{\infty} |H(\omega)|^2\, df$

Thus noise spectral density: $W_o = 2\,\bar{n}\, q^2 = 2q_eI_o$ for shot noise
(similarly $W_o = 4kT/R$ for thermal noise)

<u>Parallel noise integral</u>:

I_2 $$\overline{ENC_p^{\,2}} = \tfrac{1}{2} W_{op} \int_{-\infty}^{\infty} h^2(t)dt = W_{op} \int_{o}^{\infty} |H(\omega)|^2 df$$

parallel noise (current) spectral density = W_{op}

<u>Series noise integral</u>:

I_1 $$\overline{ENC_s^{\,2}} = \tfrac{1}{2} W_{os}\, C_{in}^{\,2} \int_{-\infty}^{\infty} h'^2(t)dt = W_{os}C_{in}^{\,2} \int_{o}^{\infty} \omega^2 |H(\omega)|^2\, df$$

series noise (voltage) spectral density, $W_{os} = \overline{e_n^{\,2}} = 4kTR_s$

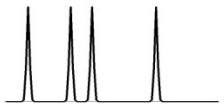
(since $\int_{-\infty}^{\infty} h'^2(t)dt = 2\int_{o}^{\infty} \omega^2 |H(\omega)|^2\, df$)

- For <u>time variant</u> systems, noise is calculated using <u>weighting function</u> and time domain relations.

ENC Calculation in Time domain: *Weighting Function Role*

$\delta'(t)\ C_{in}$ white "series" noise

$$ENC_S^2 = \frac{1}{2}\overline{e_n^2}\ C_{in}^2 \overbrace{\int [w'(t)]^2 dt}^{I_1}$$



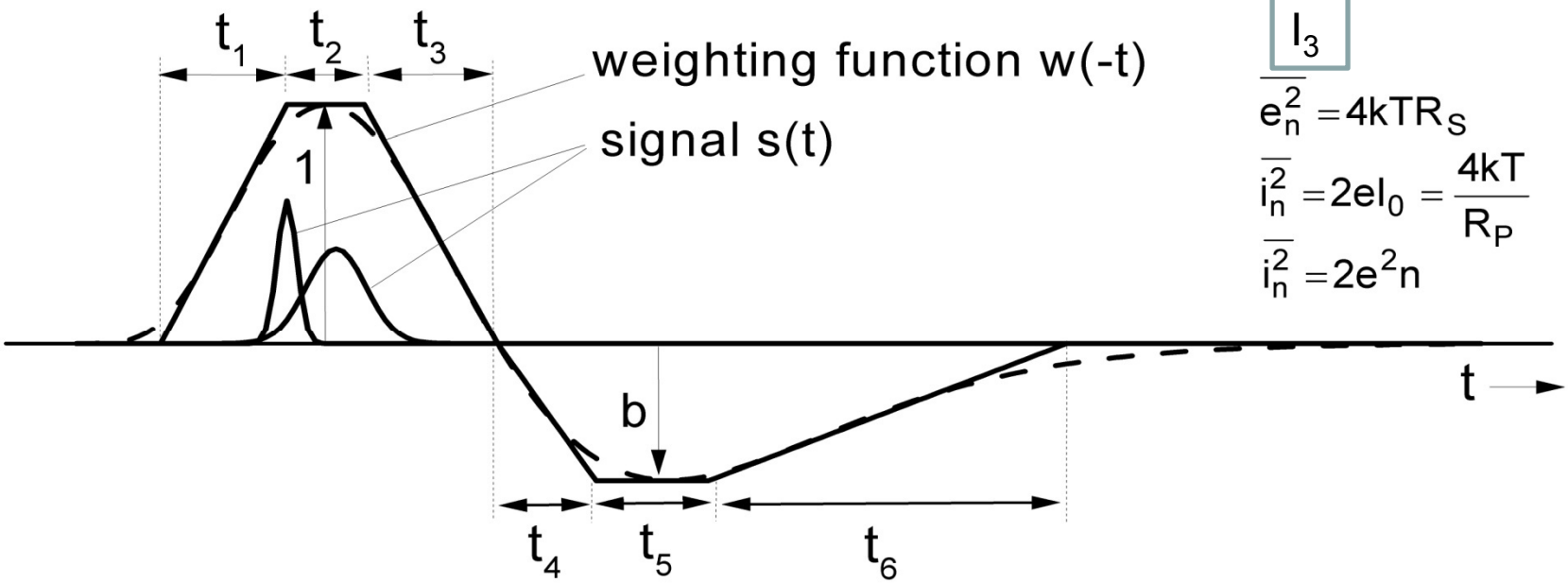
$\delta(t)$ white "parallel" noise

$$ENC_P^2 = \frac{1}{2}\overline{i_n^2} \underbrace{\int [w(t)]^2 dt}_{\boxed{I_3}}$$

$$\overline{e_n^2} = 4kTR_S$$

$$\overline{i_n^2} = 2eI_0 = \frac{4kT}{R_P}$$

$$\overline{i_n^2} = 2e^2 n$$



$$I_1 = \frac{1}{t_1} + 0 + \frac{1}{t_3} + b^2\frac{1}{t_4} + 0 + b^2\frac{1}{t_6}$$

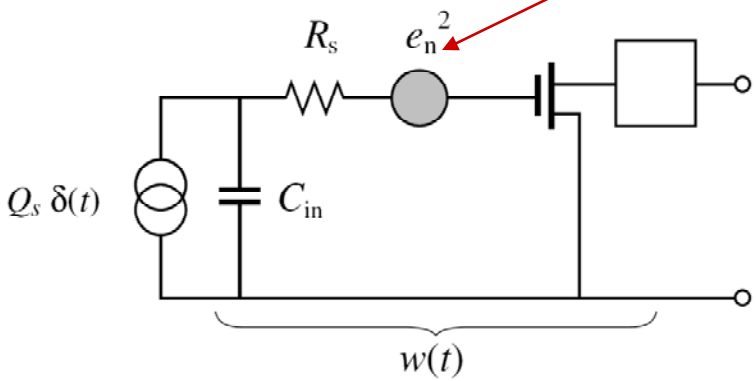
$$\boxed{I_3} = \frac{t_1}{3} + t_2 + \frac{t_3}{3} + b^2\frac{t_4}{3} + b^2 t_5 + b^2\frac{t_6}{3}$$

ENC Calculation in Time Domain

V.R., Ann. Rev. 1988
R. Wilson, Phil. Mag., 1950

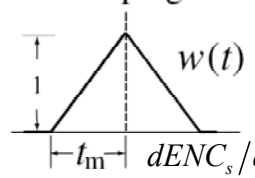
Simple ENC Calculation for ***Series*** White Noise

$$ENC_s^2 = \tfrac{1}{2}\, 4kTR_s C_{in} \bullet I_1$$



$$A_1 = I_1 t_m = 2$$

Shaping:



$$dENC_s / dC_{in} = e_n / t_m^{1/2} \quad [\ ]$$

$$I_1 = \int_{-\infty}^{\infty} w'^2(t)\,dt = 2/t_m$$

(for 5th order semi-gaussian $I_1 = 2.2$)

$$ENC_s = e_n C_{in} / t_m^{1/2}$$

Noise slope:

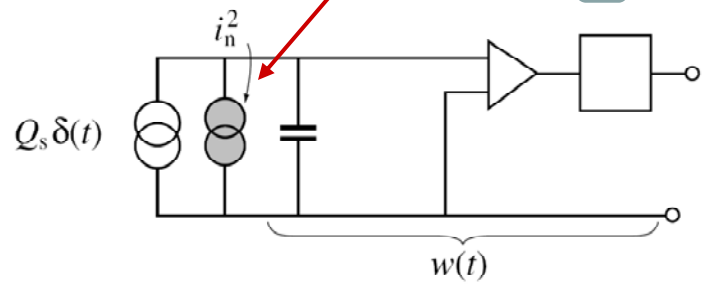
$e_n = 1\ \text{nV/Hz}^{1/2}$
$C_{in} = 1\ \text{pF}$
$t_m = 1\ \mu\text{s}$

$\rightarrow ENC_s \approx 6$ rms e $\rightarrow \Delta ENC_s / \Delta C_{in}$

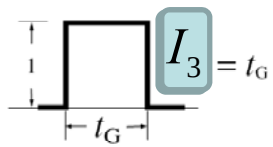
e_n = series noise (voltage) spectral density [V/Hz$^{1/2}$]
$e_n C_{in}$ = series noise (charge) spectral density [e/Hz$^{1/2}$]

Simple ENC Calculation for ***Parallel*** White Noise

$$ENC_p^2 = \tfrac{1}{2}\, \underbrace{2\, eI_o}_{i_n^2} \bullet I_3 \qquad I_3 = \int_{-\infty}^{\infty} w^2(t)\,dt$$



1. Assume a gated integrator for $w(t)$:



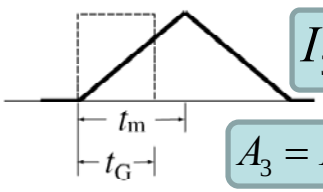
$I_3 = t_G$

$$ENC_p = (eI_o t_G)^{1/2} = (e^2 n t_G)^{1/2} = e(nt_G)^{1/2} = e\, n_G^{1/2}$$

$$ENC_p / e = n_G^{1/2} \quad \text{[rms e]}$$

1 nA in 1μs → $n_G = 6250$ e, $ENC_p = 79$ rms e

2. Triangular weighting function (similar to semi-gaussian)



$I_3 = \frac{2}{3} t_m$

$$ENC_p / e = (2nt_m/3)^{1/2}$$

equal ENC_p for: $t_G = 2t_m/3$

$$A_3 = I_3 / t_m = 2/3$$

3. Resistor noise = shot noise: $4kT/R_p = 2\, eI_o$

for $R_p I_o = 50$ mV at 293K

Calculation of ENC for 1/f Noise

From slides 14, 15:

$$ENC_f^2 = \pi C_{in}^2 A_f A_2$$

$$A_2 = I_2 = \int_{-\infty}^{\infty} \left[w^{(1/2)}(t) \right]^2 dt$$

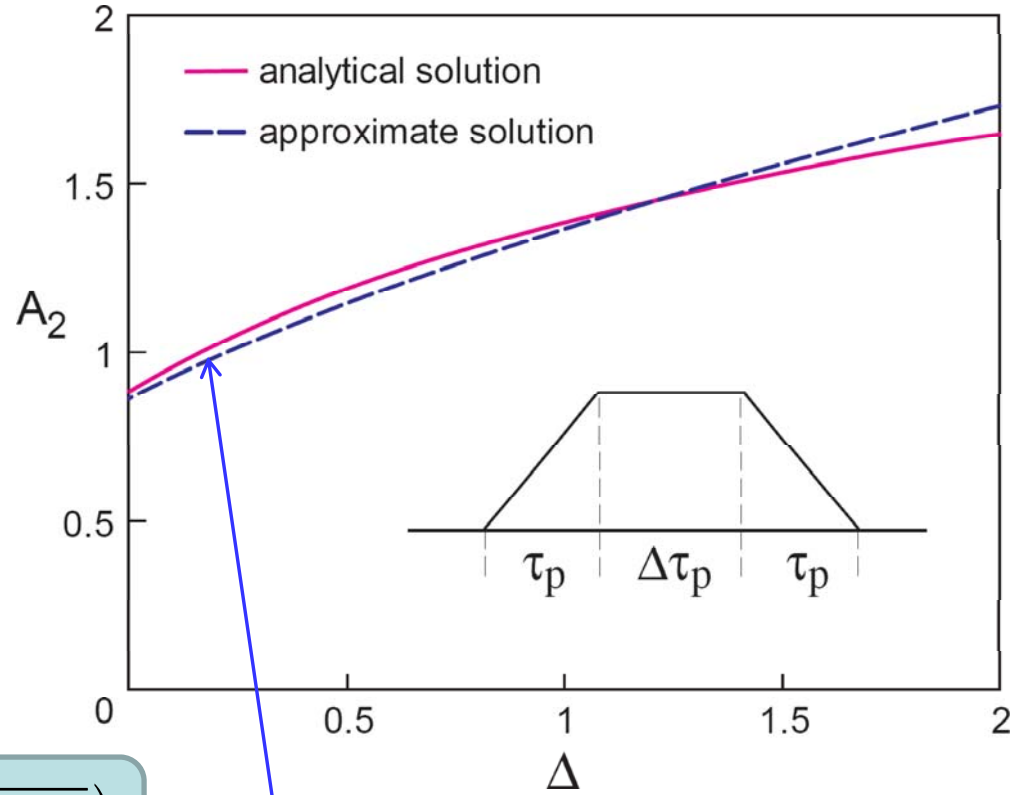
It can be shown that:

$$A_2 \le \left(A_1 A_3 \right)^{(1/2)}$$

($w^{(1/2)}$=fractional order derivative)

An approximation for practical purposes (*ENC_f to 10%):*

$$A_2 \approx 0.75 \left(A_1 A_3 \right)^{1/2}$$



$$\boxed{ENC_f^2 = \pi C_{in}^2 A_f A_2 \approx \pi C_{in}^2 A_f \left(0.75 \sqrt{A_1 A_3} \right)}$$

Transistor technology constant (~independent of transistor size) :

$$\boxed{K_f = A_f C_{gs}} \qquad \left[\left(V^2 \right) \left(As/V \right) \right] = \left[VAs \right] = \left[Joule \right]$$

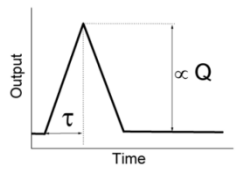
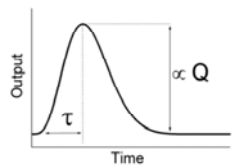
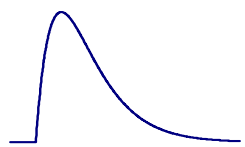
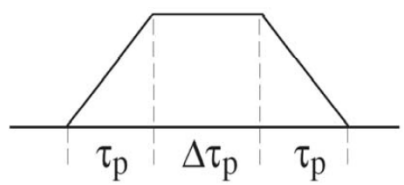
Trapezoidal weighting function (e.g., dual slope integrator):

$$A_1 = 2$$

$$A_3 = \left(\Delta + 2/3 \right)$$

$$A_2 \approx 0.75 \left[2 \left(\Delta + 2/3 \right) \right]^{1/2}$$

Weighting Function Noise Coefficients

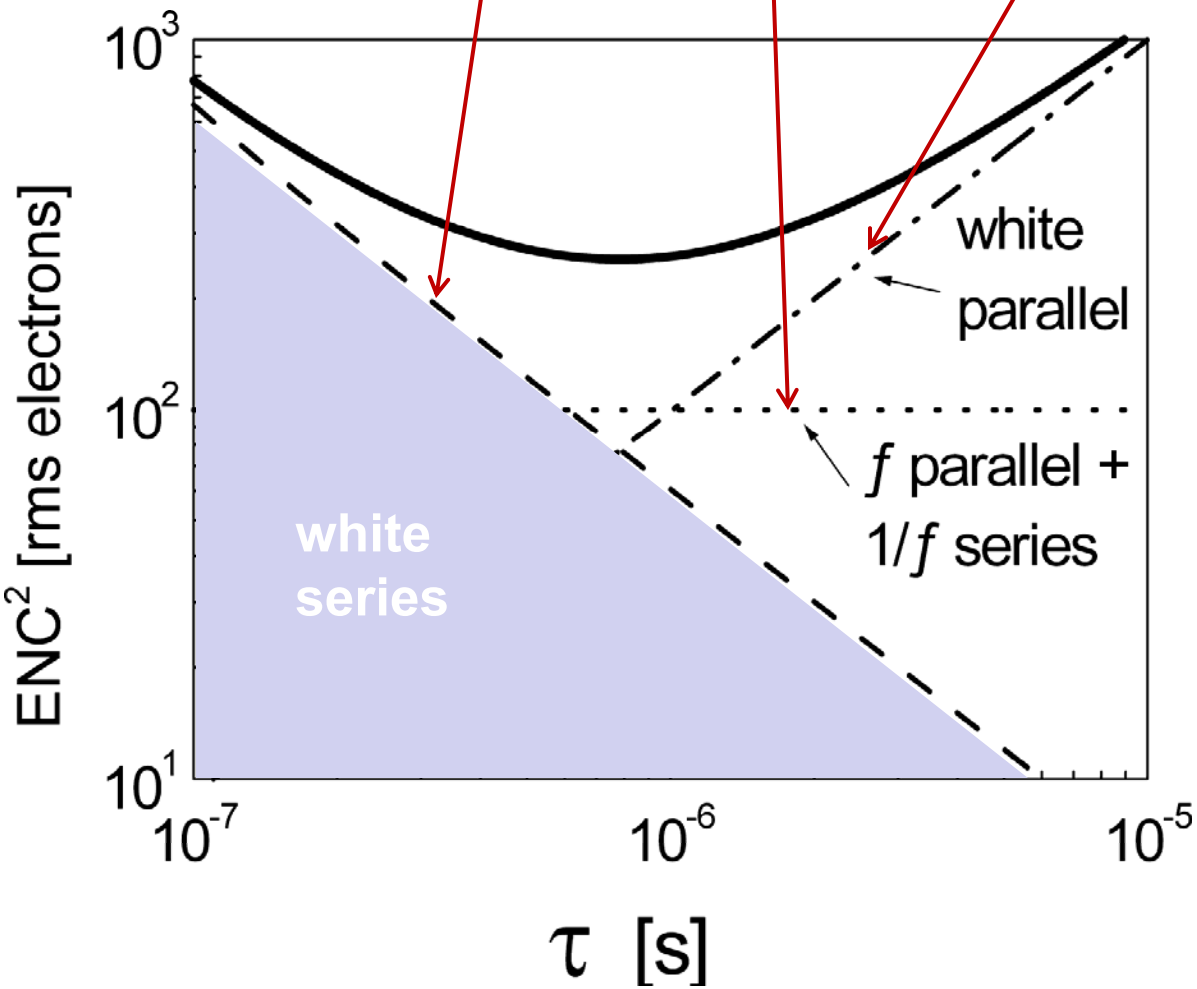
Weighting function	Series white A_1	Parallel white A_3	Series *1/f* $A_{2(calc)}$	Series 1/f $A_{2(approx)} \approx 0.75(A_1A_3)^{1/2}$
triangle 	2	2/3	0.88	.87
semi-gaussian 4th order 	2.04	0.90	1.04	1.01
CR-RC 	1.85	1.85	1.18	1.39
trapezoidal Δ=1 	2	1.67	1.38	1.37

$$ENC^2 = \tfrac{1}{2} e_n^2 C_{in}^2 \frac{A_1}{\tau} + \pi C_{in}^2 A_f A_2 + q I_0 A_3 \tau$$

ENC vs shaping (peaking time):

$$ENC^2 \approx \frac{e_n^2 C_{in}^2}{\tau} + \pi C_{in}^2 A_f + qI_0 \tau$$

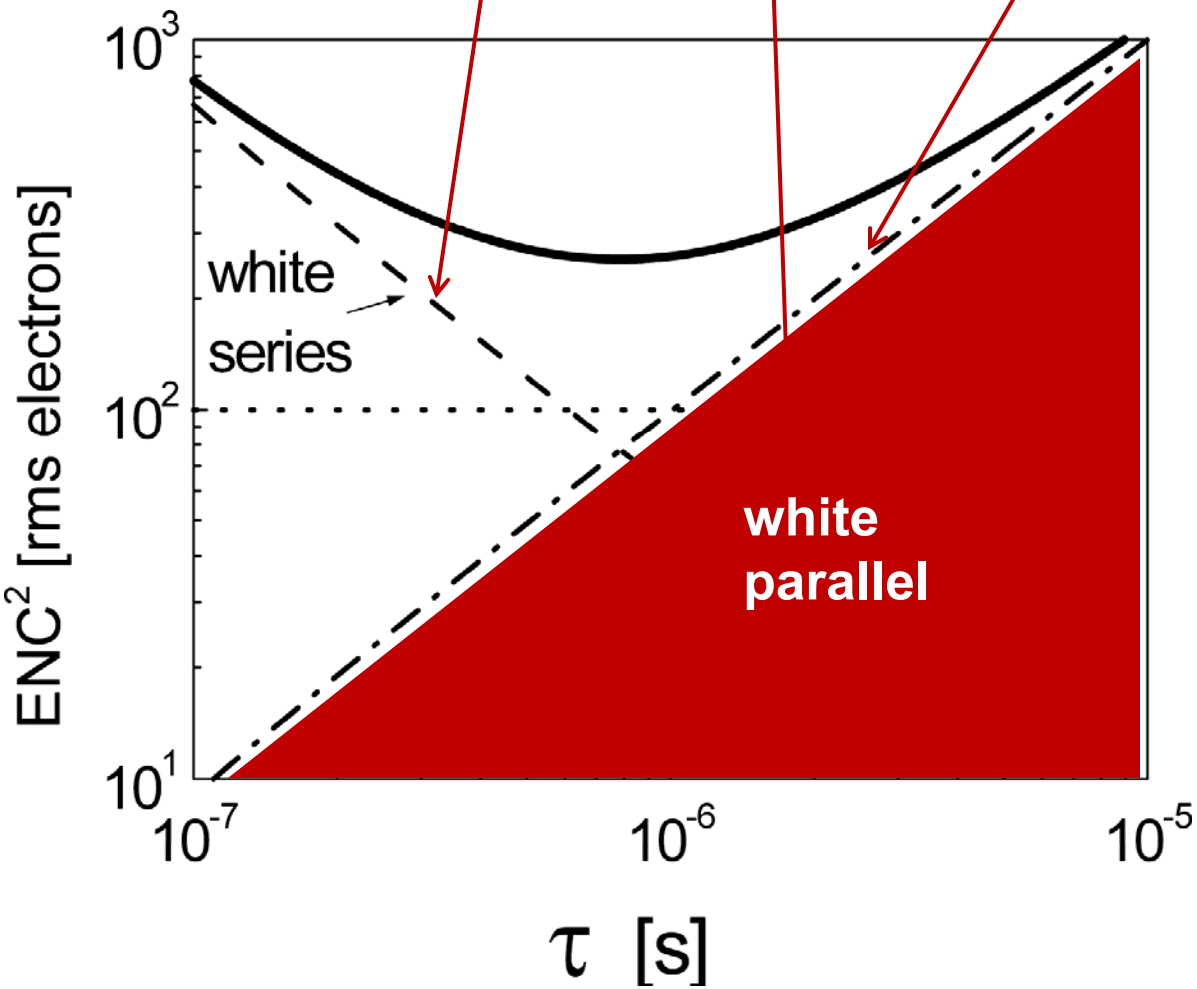
(Semigaussian 4th order)



ENC vs shaping (peaking time):

$$ENC^2 \approx \frac{e_n^2 C_{in}^2}{\tau} + \pi C_{in}^2 A_f + qI_0 \tau$$

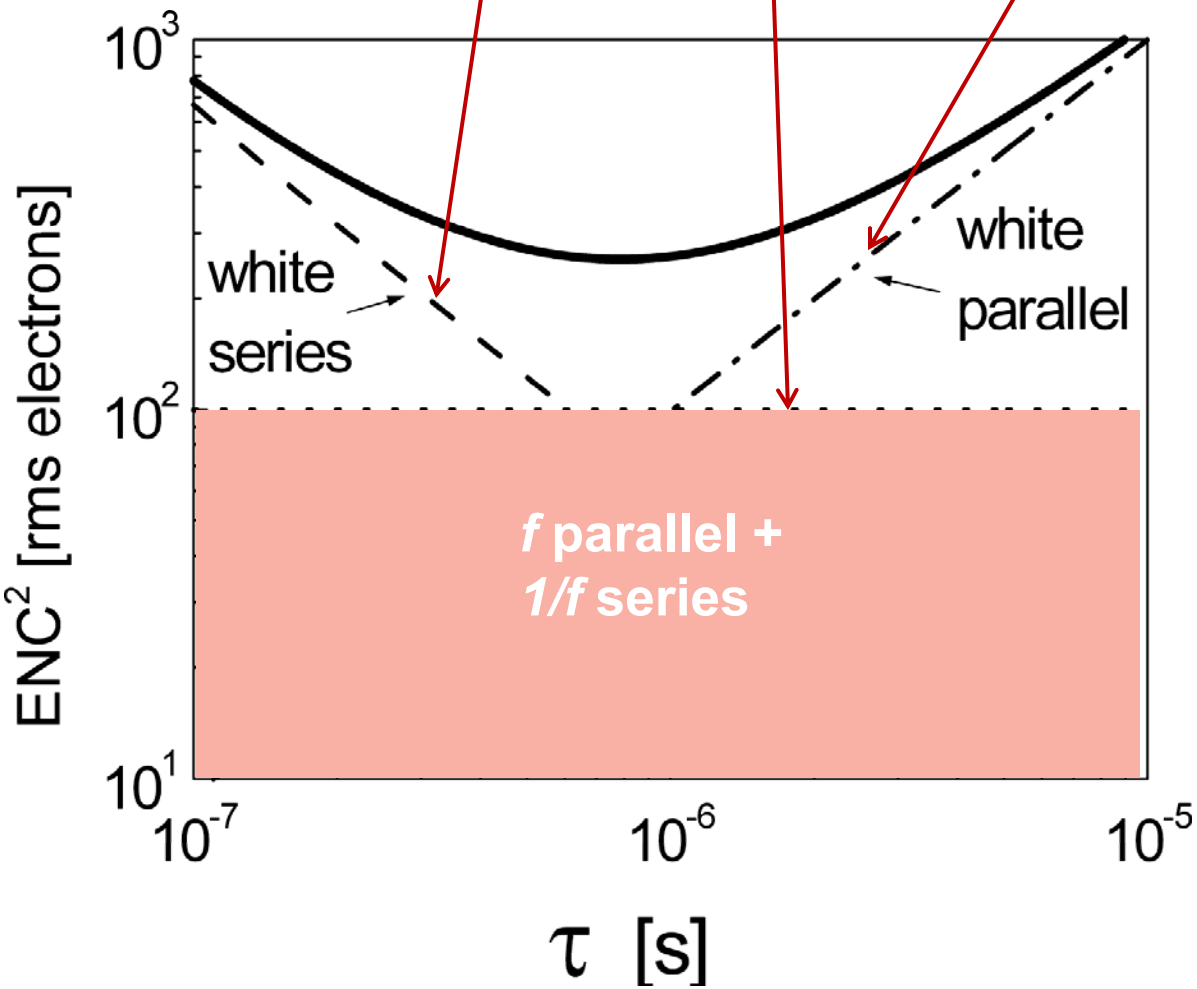
(Semigaussian 4th order)



ENC vs shaping (peaking time):

$$ENC^2 \approx \frac{e_n^2 C_{in}^2}{\tau} + \pi C_{in}^2 A_f + qI_0 \tau$$

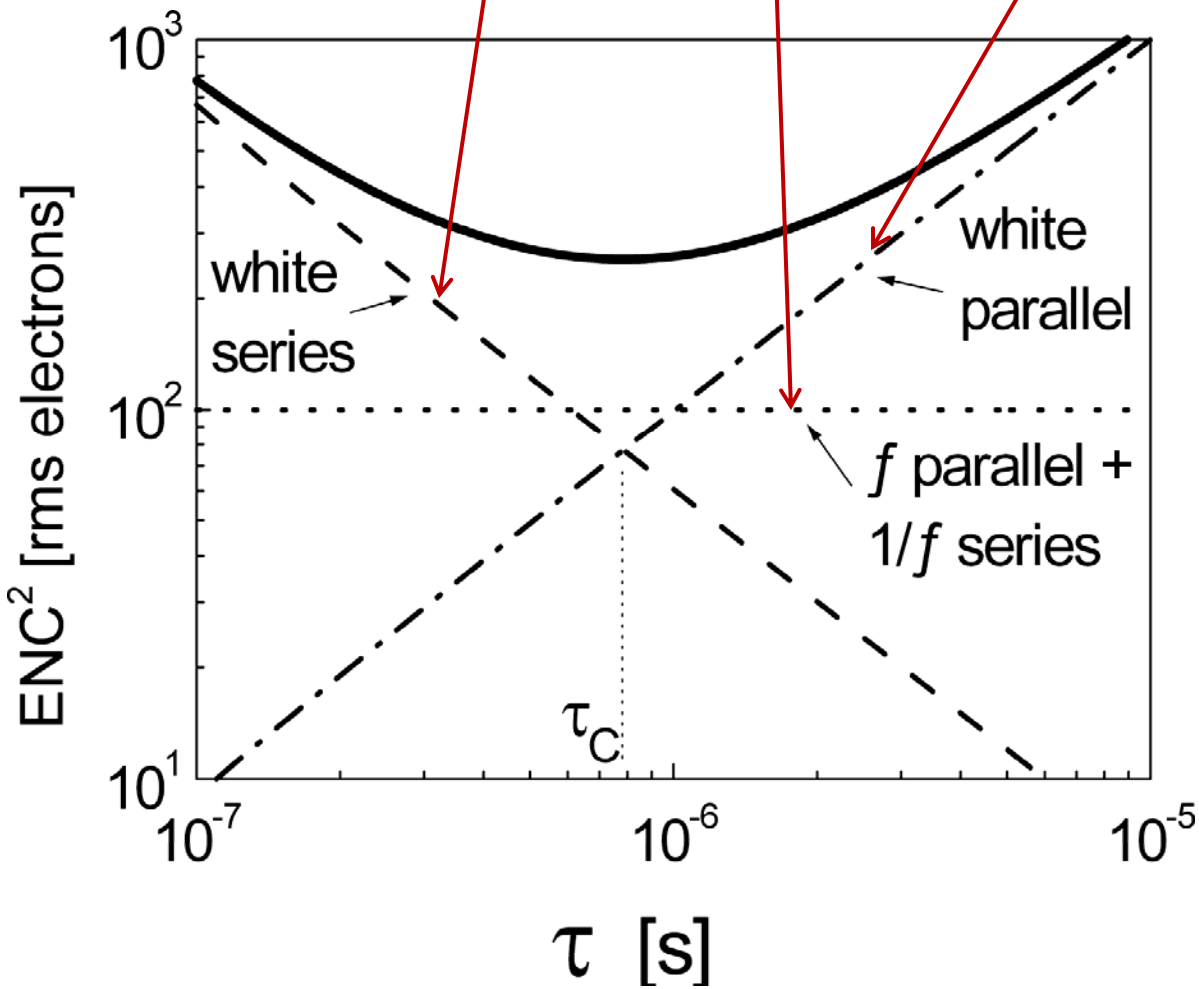
(Semigaussian 4th order)



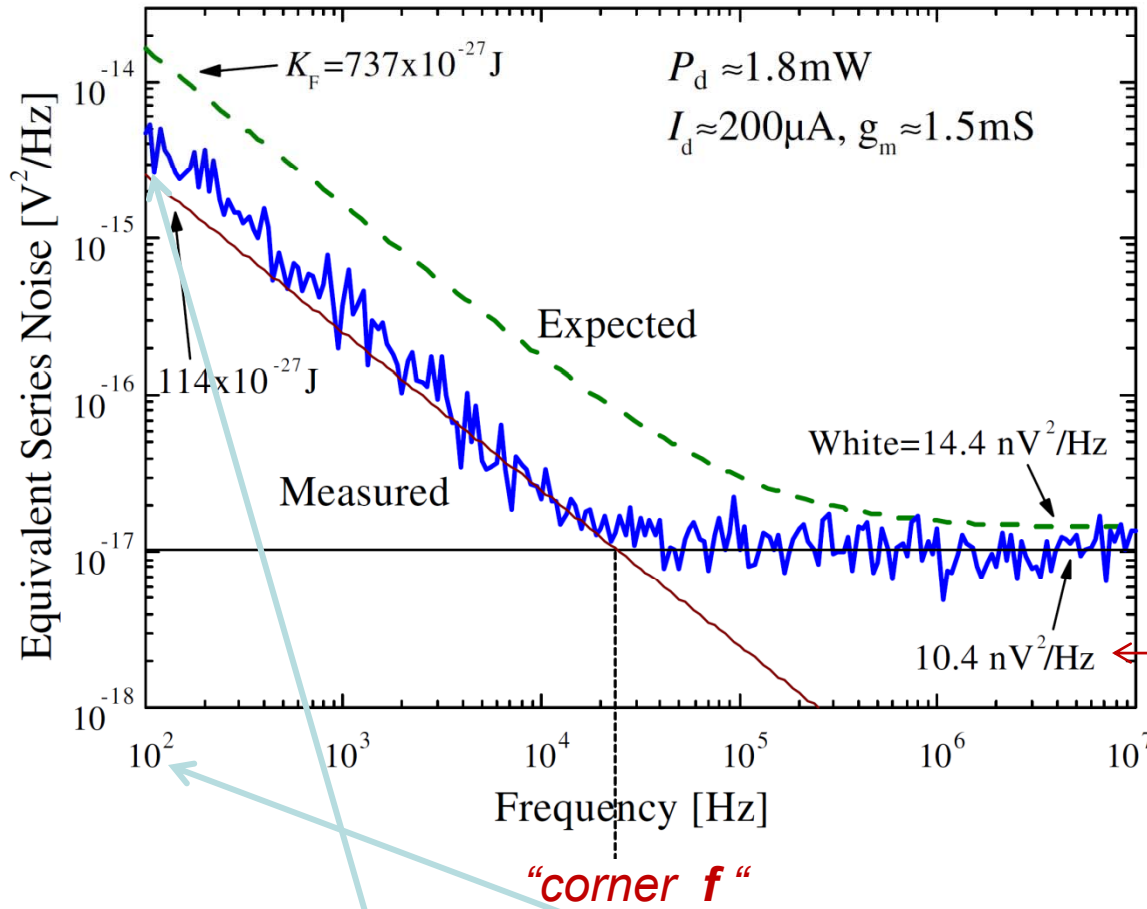
ENC vs shaping (peaking time):

$$ENC^2 \approx \frac{e_n^2 C_{in}^2}{\tau} + \pi C_{in}^2 A_f + qI_0 \tau$$

(Semigaussian 4th order)



1/f **Noise parameters**: *corner frequency, "technology constant" K_f and "measurement constant" A_f*



Measure:

$$\frac{K_f}{C_{ox}WLf} = \frac{A_f}{f} = v_n^2 \quad \left[(rms\ volts)^2\right]$$

$$K_f = (C_{ox}WL)A_f \left[joules\right]$$

$3nV/Hz^{1/2}$

$$e_n^2 = \gamma 4kT/g_m \ ; \gamma \simeq 2/3$$

"corner f "

$$K_{fN} \sim 10K_{fP}$$

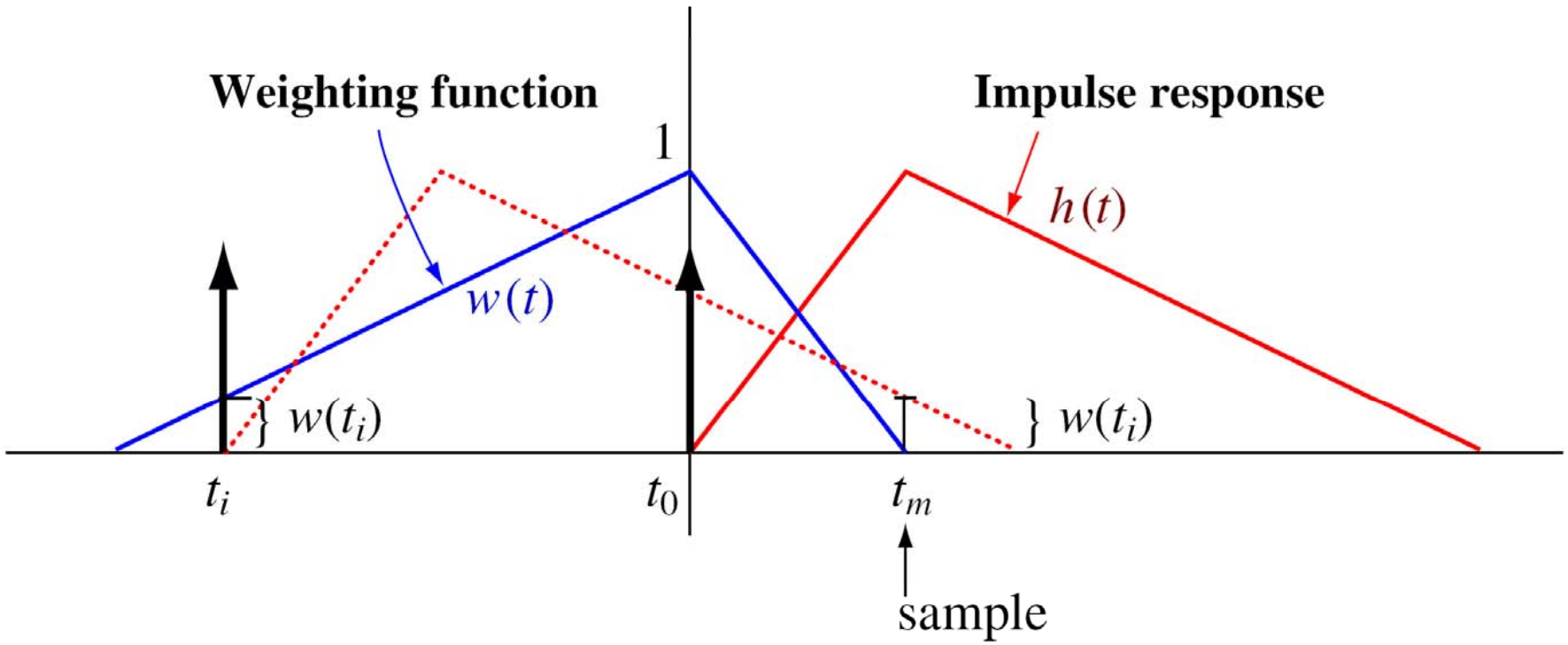
$$K_{fN} \sim 10^{-25} J$$

$$K_{fJFET} \sim 10^{-27} J$$

$$A_f = v_n^2 f \approx (3x10^{-15-} V^2/Hz)\cdot(10^2 Hz) = 3x10^{-13} V^2$$

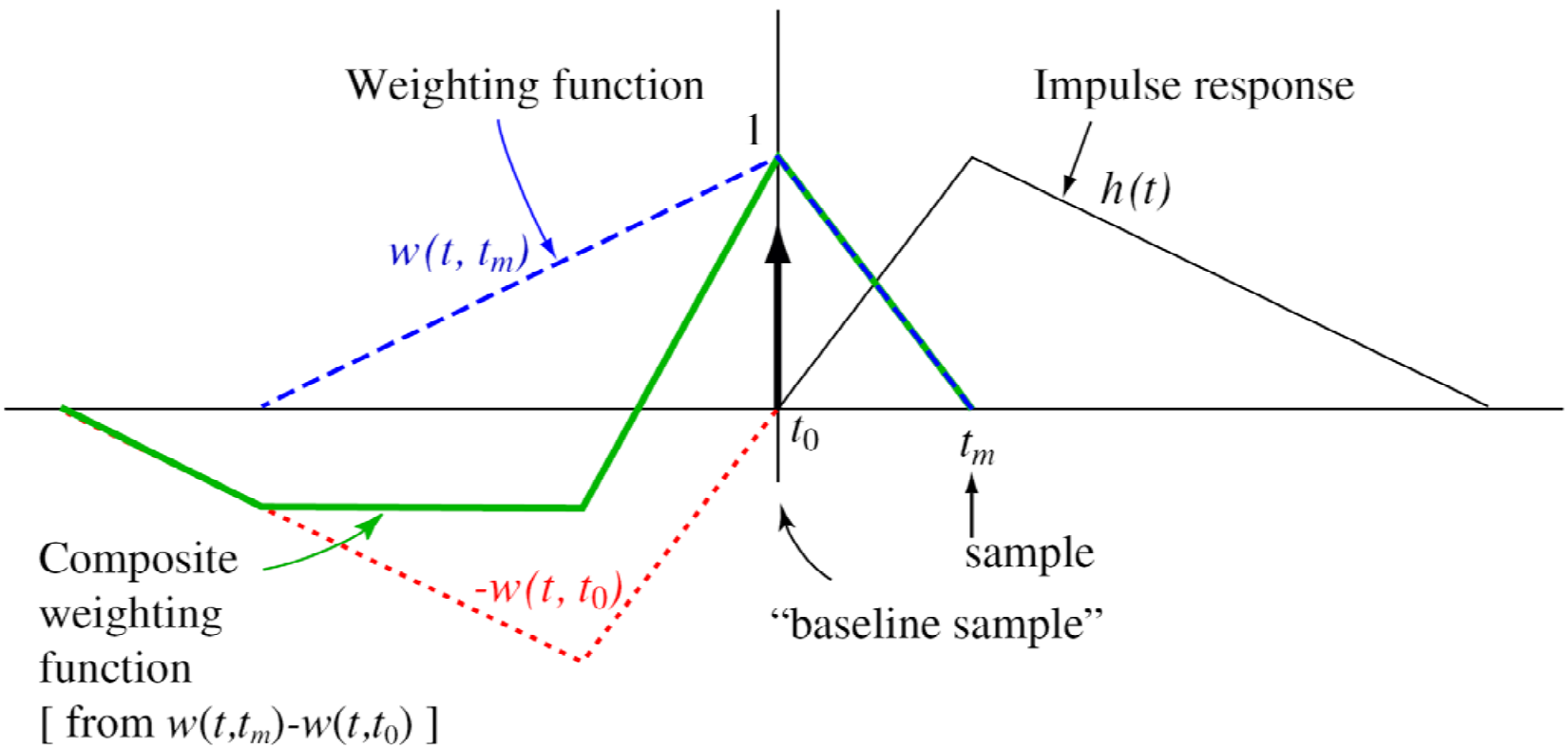
4. Signal processing, i.e., “filtering” or “pulse shaping”

Weighting Function



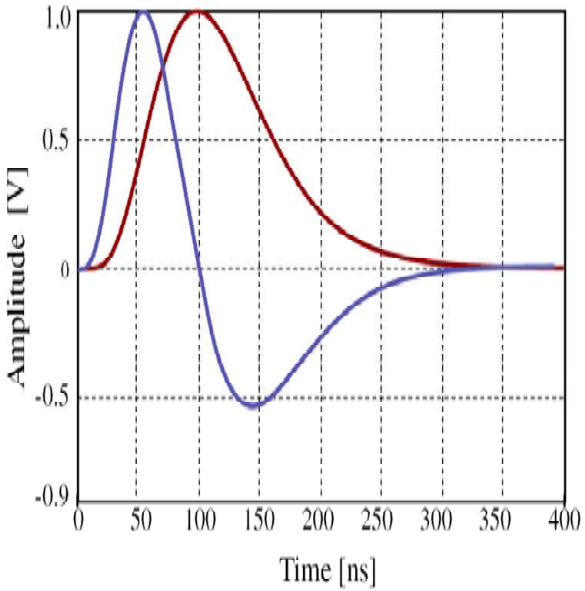
∴ Each sample carries a memory of the past events determined by the impulse response of the system preceding the sampler.

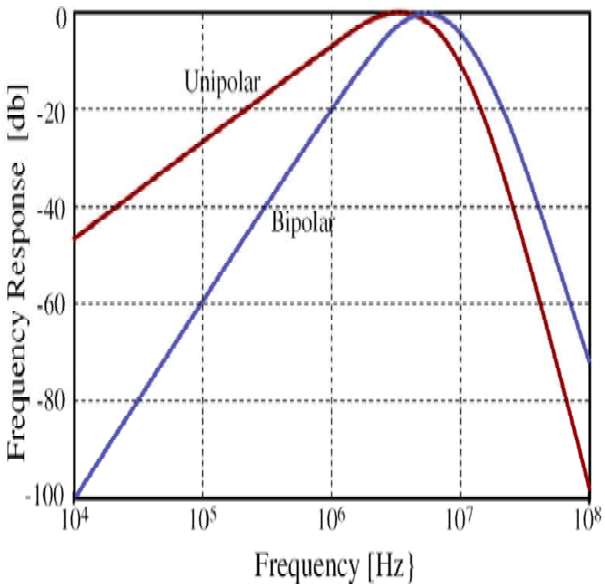
Composite Weighting Function for Correlated Double Sampling



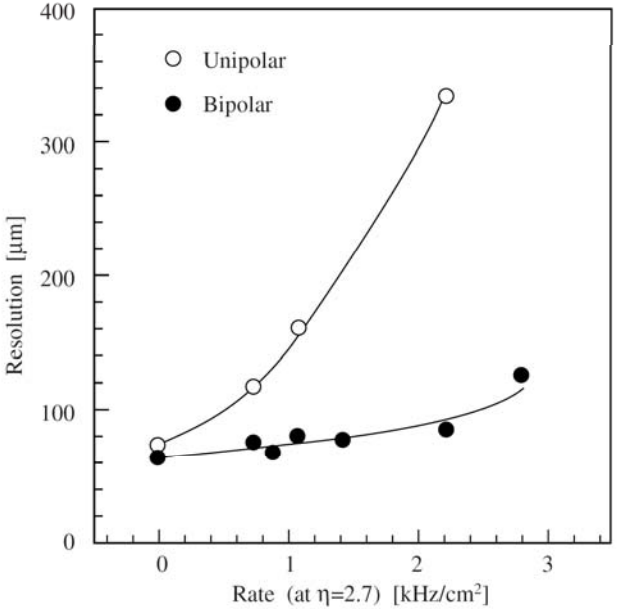
∴ Each sample carries a memory of the past events determined by the impulse response of the system preceding the sampler.

Weighting Functions ***w(t)*** and Transfer Functions $\left|H\left(j\omega t\right)\right|$





5th order semi-gaussian and its derivative



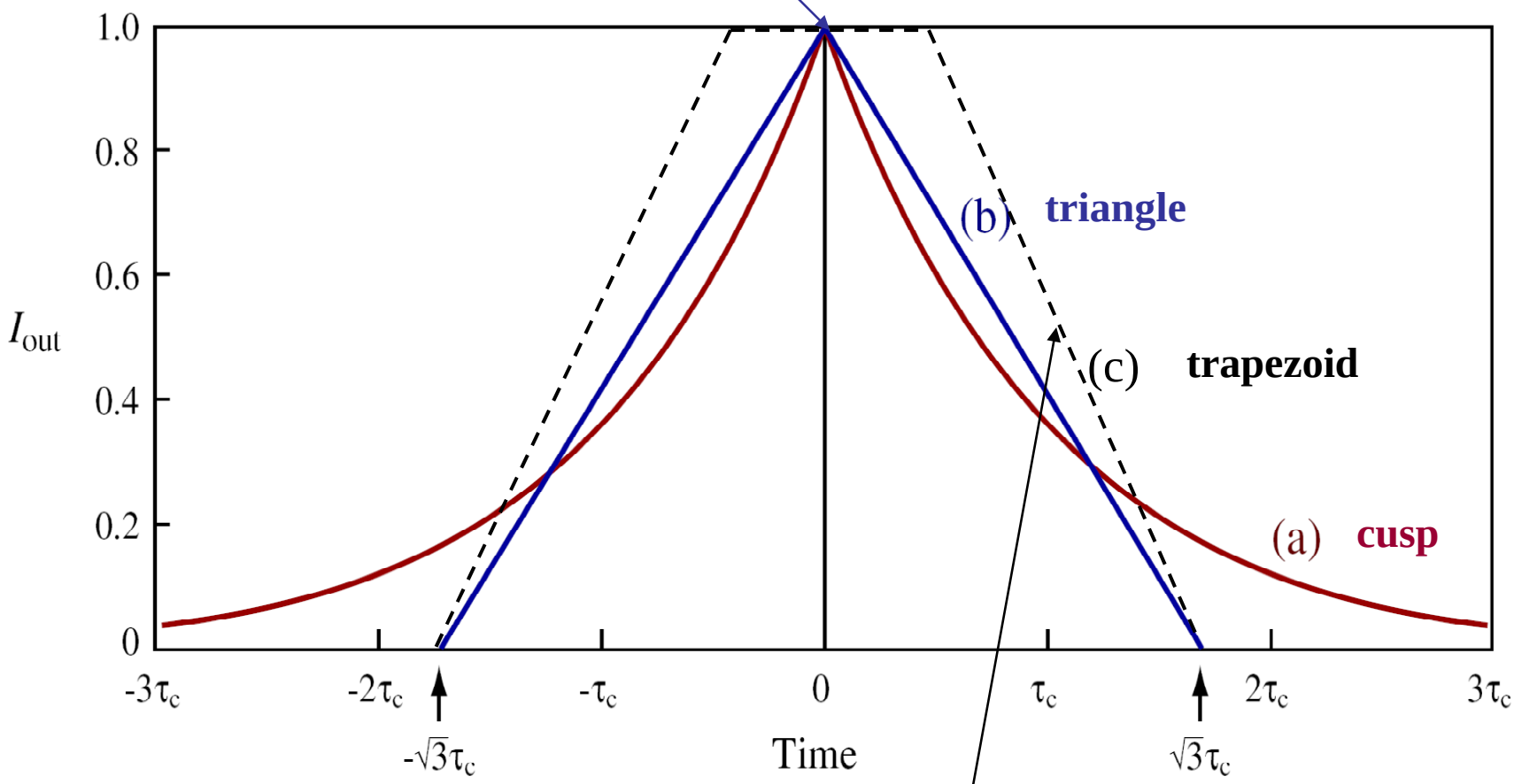
<u>Pileup Effects on centroid position resolution</u>:

Detector: 1.5 m long MWPC with interpolating cathode strip readout; Peaking time ~ 250 ns

<u>Bipolar "shaping"</u> results in lower pileup effects due to the *<u>area balance</u>* of the weighting function and in a higher series noise.

Optimum Filter for Amplitude Measurement

(delta function signal current)

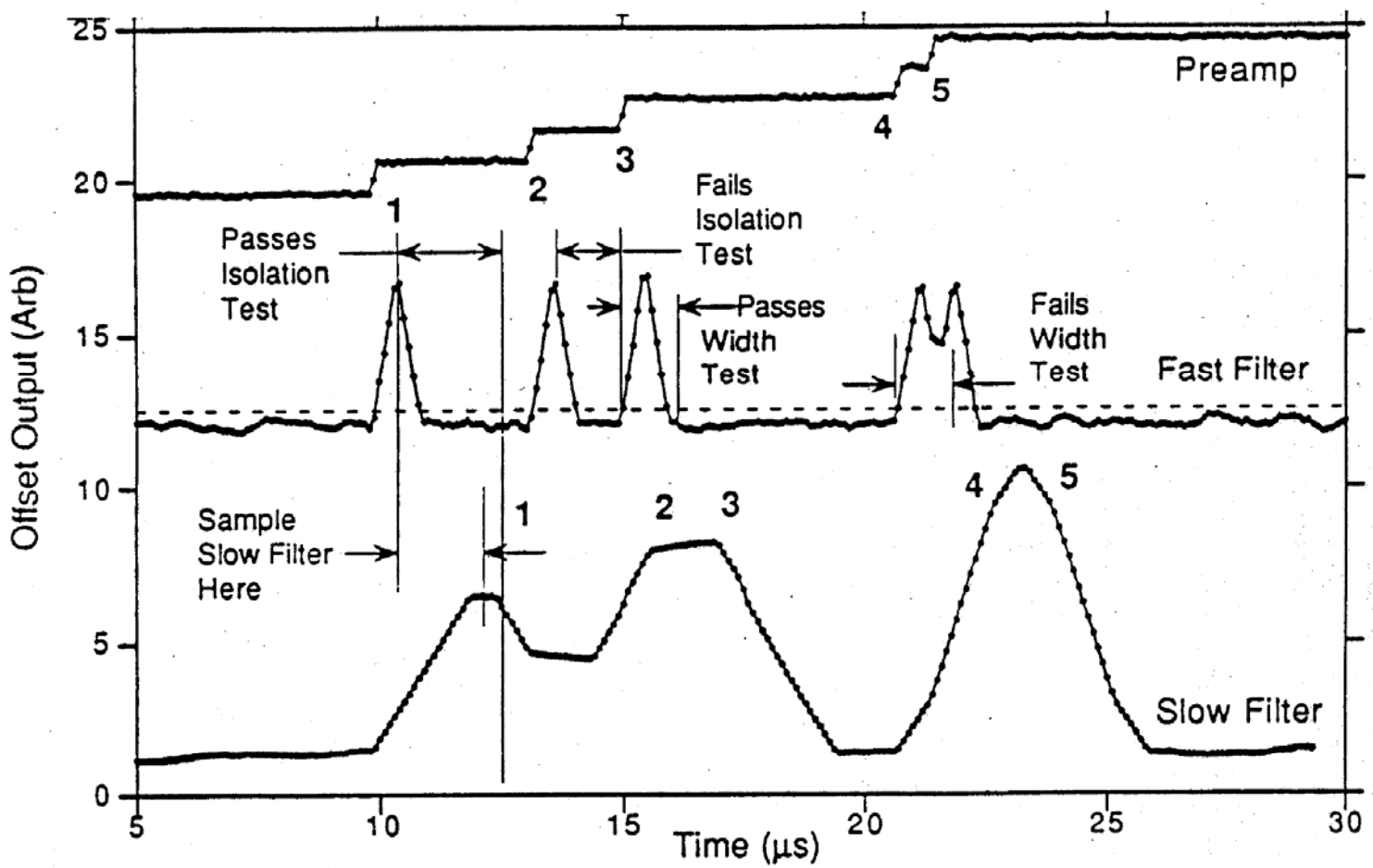


Trapezoid w(t) for reduced ballistic deficit with finite width signal current

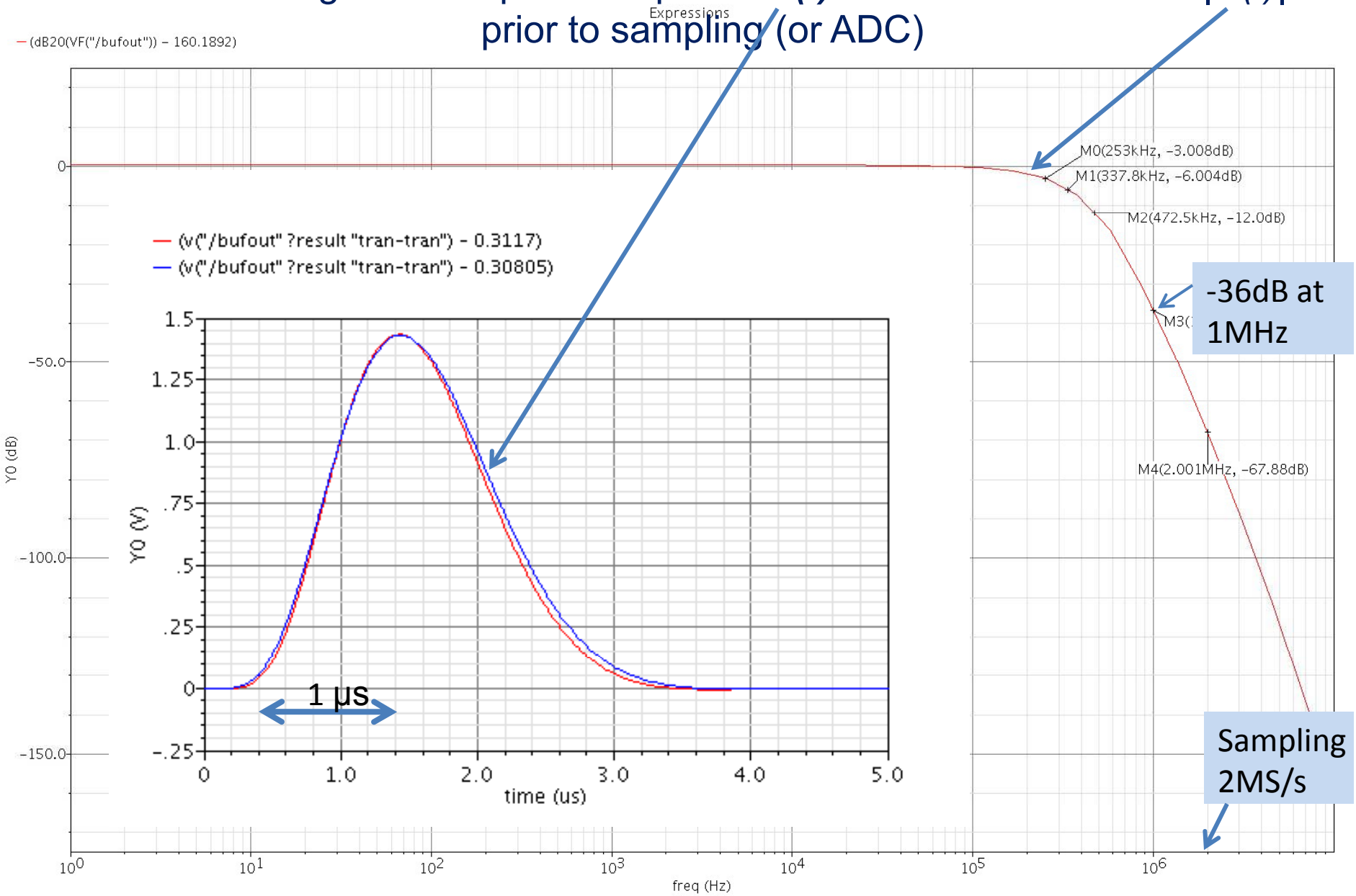
τ_c= noise corner time constant

Trapezoidal Weighting Functions by Digital (*Uncorrelated*) Signal Processing

From: X-ray Instrumentation Associates, App. Note 970323-1

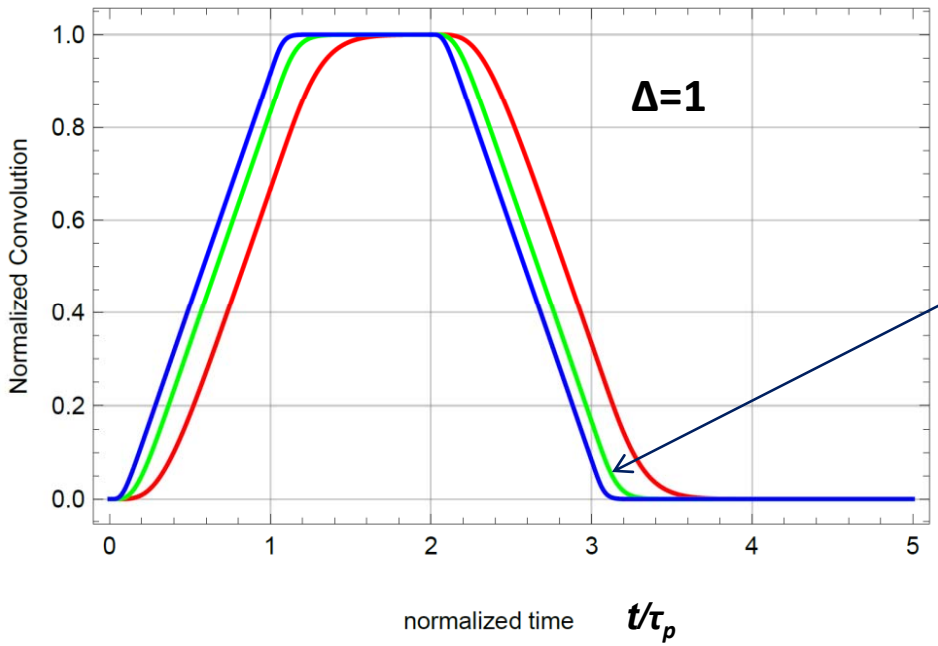


“Anti-aliasing filter”: Impulse response ***h(t)*** and transfer function |*H(f)*| prior to sampling (or ADC)

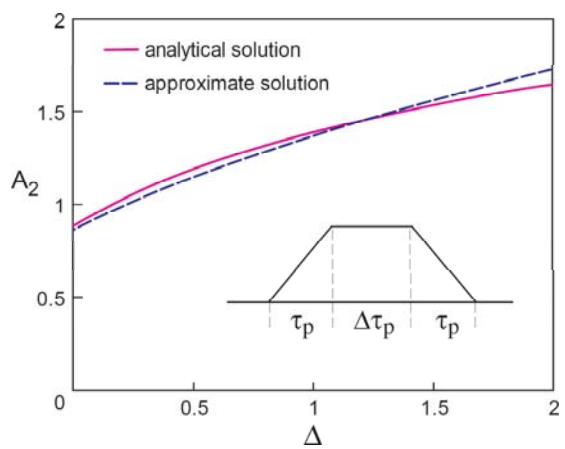


Trapezoidal weighting function in time and frequency domains

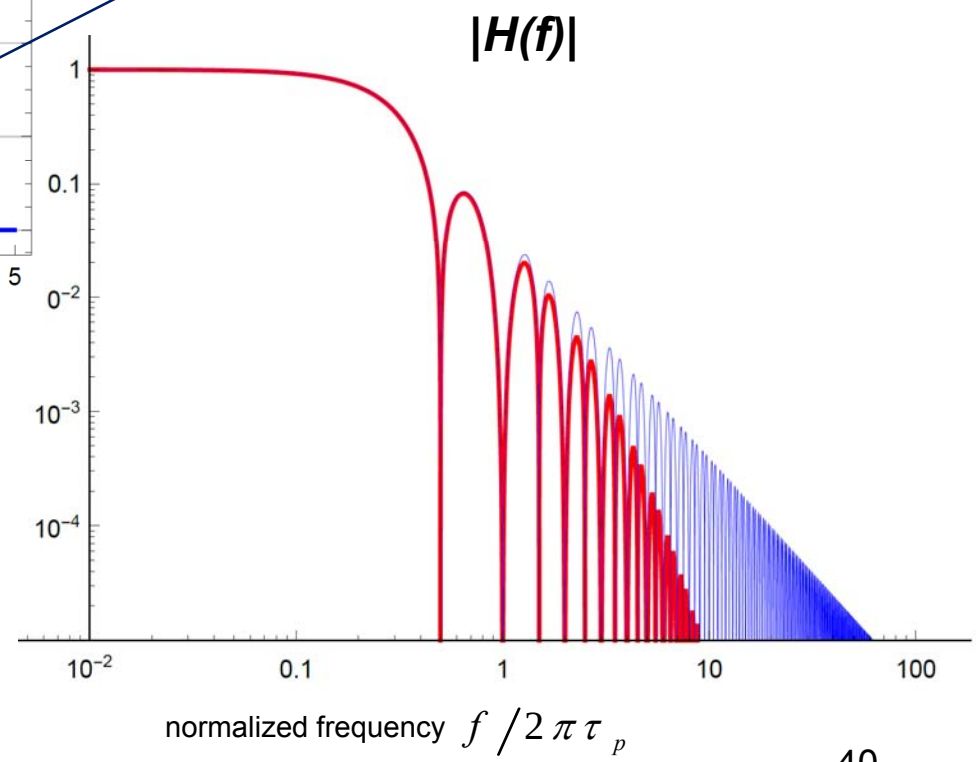
w(t)



Anti-aliasing filter (slide 39):
t_{pk}/τ_p= 1/20; 1/10; 1/5



(see slide 26)



5. Charge amplifier configuration and charge transfer from detector to amplifier

The first record of a Charge-Sensitive Amplifier Circuit

1948

Nr. 267431

Nr. 267431

Feb. 1948

SCHWEIZERISCHE EIDGENOSSENSCHAFT

EIDGENÖSSISCHES AMT FÜR GEISTIGES EIGENTUM

PATENTSCHRIFT

Veröffentlicht am 16. Juni 1950

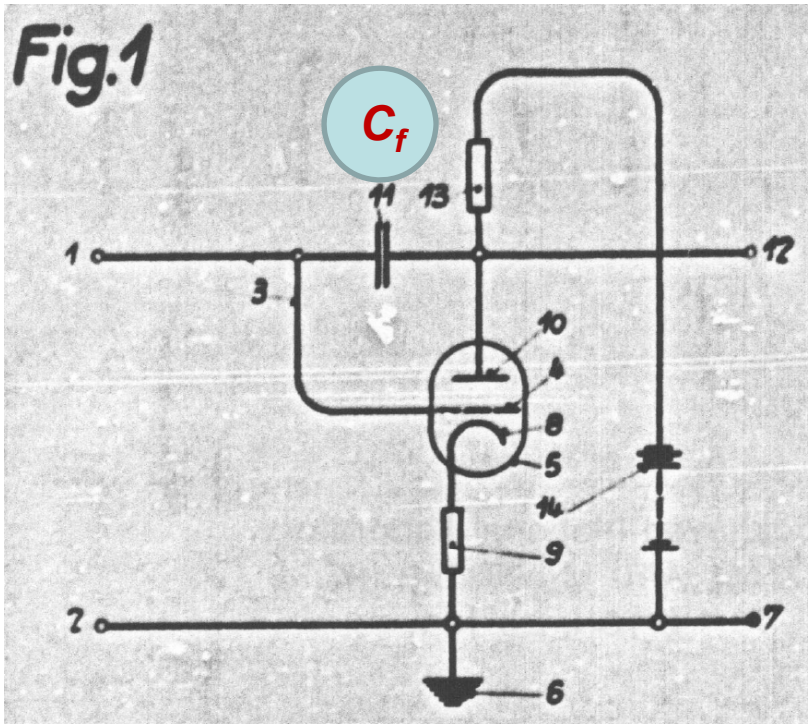
Klasse 66 a

Gesuch eingereicht: 12. Februar 1948, 18 Uhr. — Patent eingetragen: 31. März 1950.

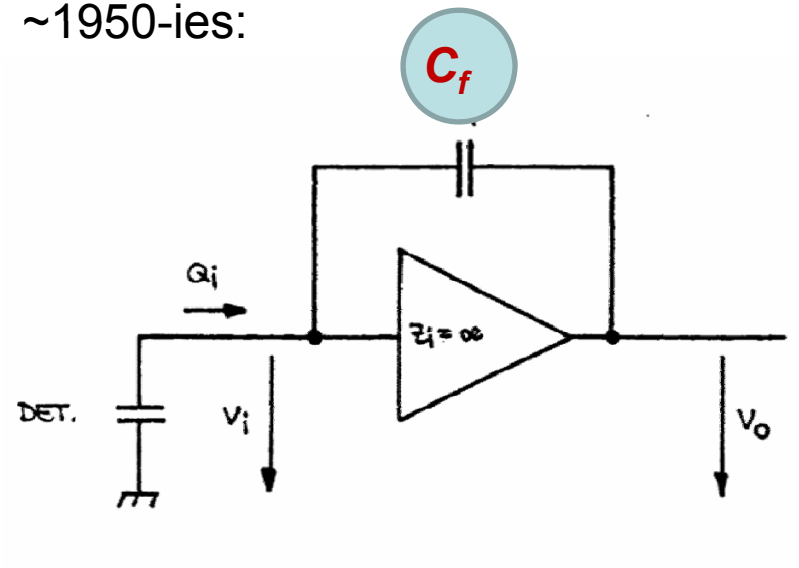
HAUPTPATENT

Schweizerische Lokomotiv- & Maschinenfabrik, Winterthur (Schweiz).

Meßverstärker zur Messung elektrischer Ladungen.



Classical "integrator" known from WWII (1941-5) appears as charge amplifier in ~1950-ies:

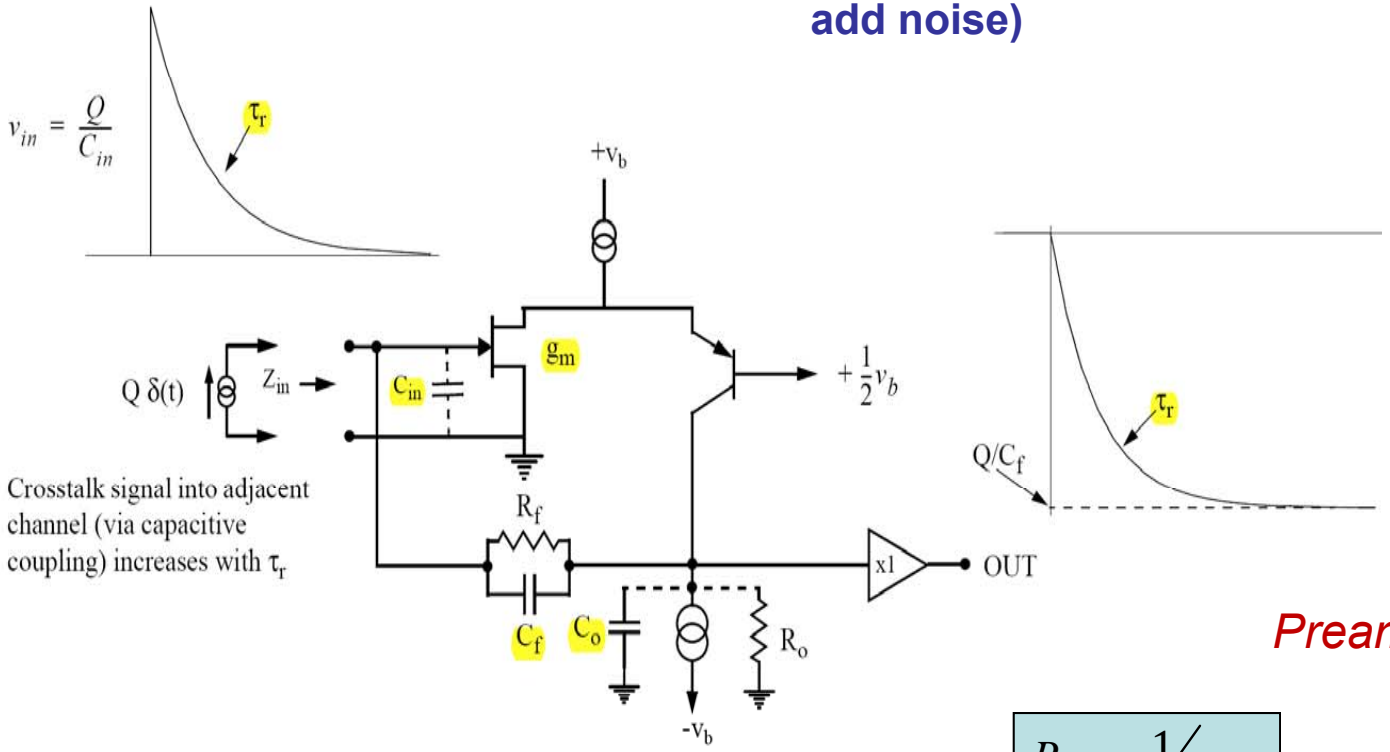


Input capacitance ~ open-loop gain x C_f

Vacuum tube at the input until ~1963 when the first *JFET* is used …

Basic Feedback Preamplifier Configuration

Note: feedback function *per se* does not affect ENC (feedback components may add noise)



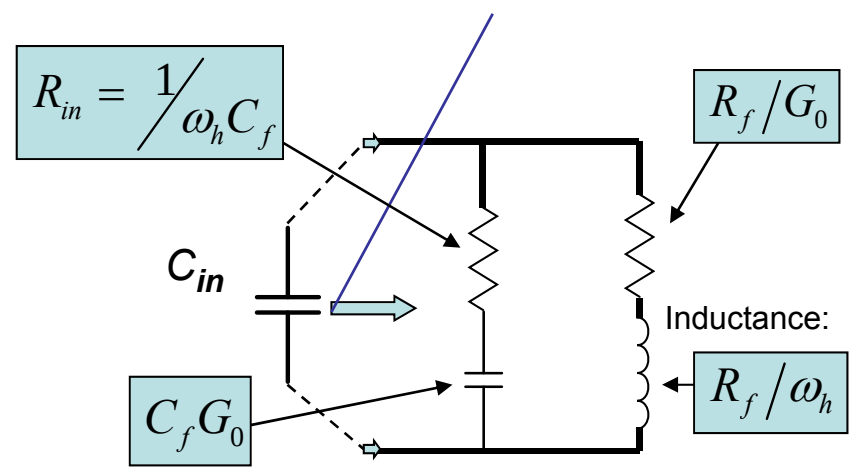
$$G_o = g_m R_o$$

$$\omega_h = g_m / C_o \qquad R_{in} = \frac{C_o}{g_m C_f}$$

$$\omega_L = \frac{1}{C_o R_o} \qquad \tau_r = C_{in} R_{in} = \frac{C_{in}}{C_f\,\omega_h} = \frac{1}{g_m} \cdot \frac{C_{in} C_0}{C_f}$$

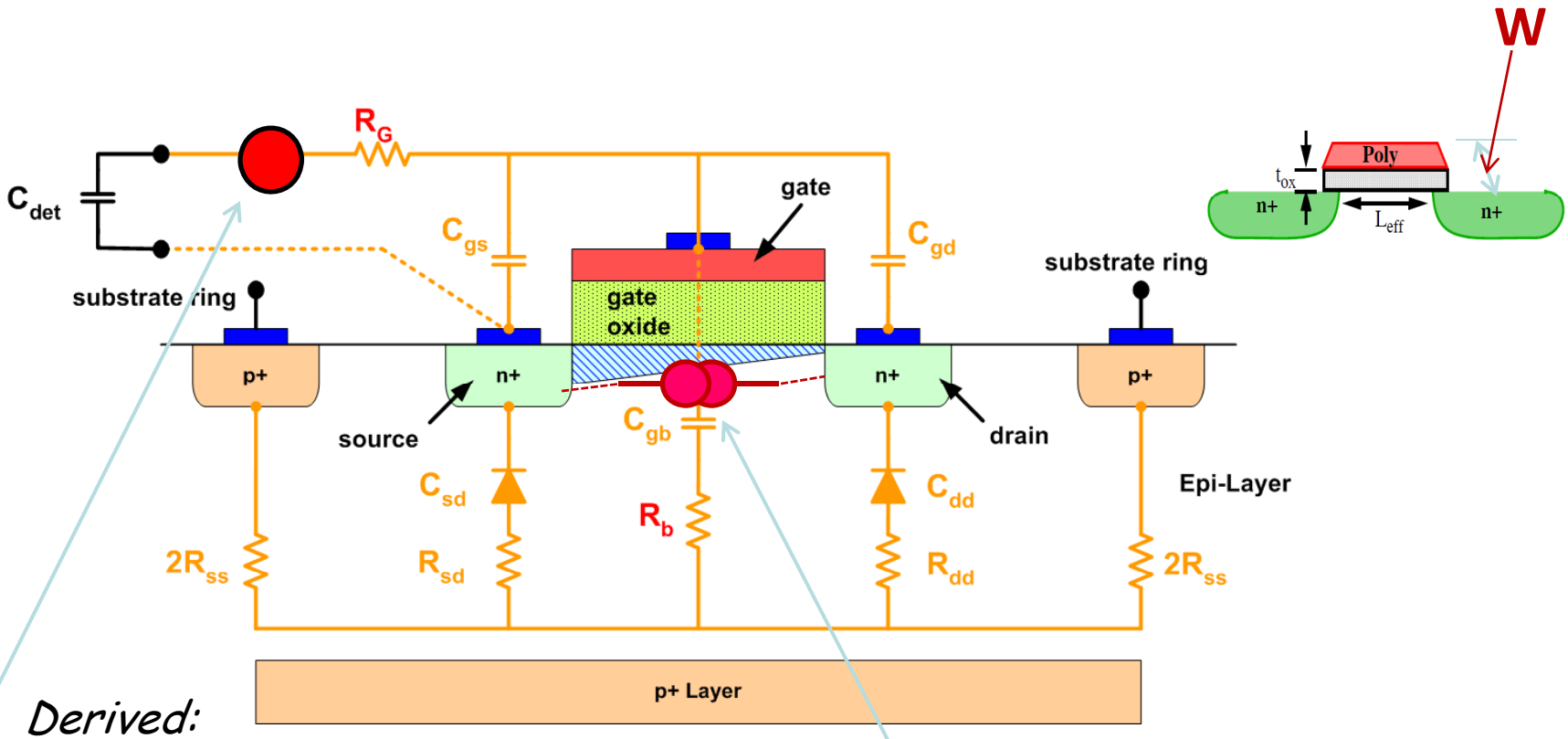
Rise time constant

Preamp input eq. circuit



Aperiodic response for $R_f \geq 2 \frac{1}{\omega_h C_f} \cdot \frac{C_{in}}{C_f}$

Noise Intrinsic to Gain Mechanism in (N)MOS Transistor



Derived:

$$e_n^2 = 4kT\frac{\gamma}{g_m} \quad \left[V^2/Hz\right]$$

= equivalent "series" noise voltage spectral density

Basic:

i_n^2 channel (drain-source) current fluctuations (thermal or shot noise)

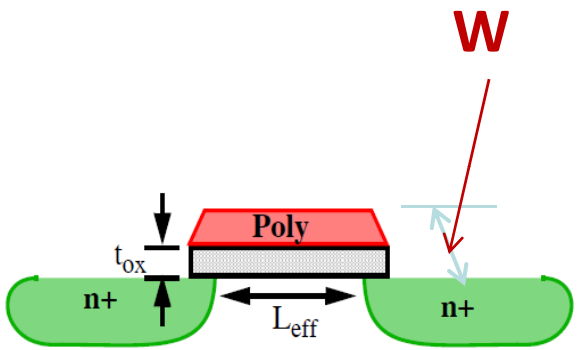
What do different transistors have in common ?
-- *Fluctuations associated with the gain mechanism*

Intrinsic (white) noise, although from a different mechanism for each device type, can be expressed by the transconductance in terms of the equivalent noise resistance,

$$R_{neq} = \gamma / g_m$$

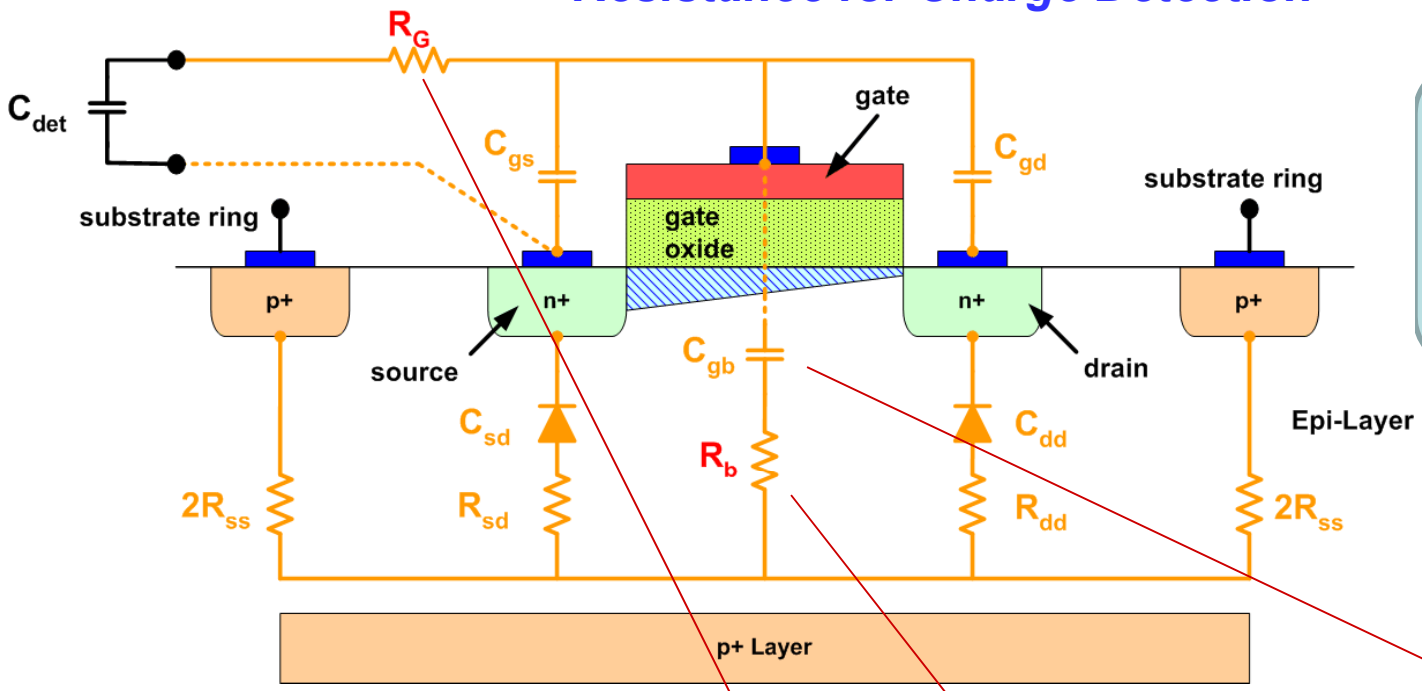
$\gamma - values:$

BJT	1/2
JFET	2/3
CMOS (strong inv..)	2/3
CMOS (weak inv.)	1/2
CMOS <~180nm	>2/3



Noise (voltage) spectral density: $e_n^2 = 4kT \dfrac{\gamma}{g_m} \quad \left[V^2 / Hz \right]$

Additional (white) noise sources in MOSFETs: and Equivalent Series Noise Resistance for Charge Detection



"Intrinsic" channel noise:

$$e_n^2 = 4kTR_n\,;\; R_n = \gamma / g_{ms}$$

$$\gamma \geq 2/3 \text{ for FETs}$$

$$\gamma = 1/2 \text{ for BJTs}$$

$$\frac{R_{eq}}{\gamma / g_{ms}} = 1 + \frac{\delta}{5\gamma}\left(\frac{C_{gs}}{C_{in}}\right)^2 + \frac{1}{\gamma}\left(R_g g_{ms}\right) + \left(R_b g_{mb}\right)\frac{g_{mb}}{g_{ms}} + \frac{1}{\gamma}\left(R_b g_{ms}\right)\left(\frac{C_{gb}}{C_{in}}\right)^2$$

Gate induced

«1

Intrinsic channel noise

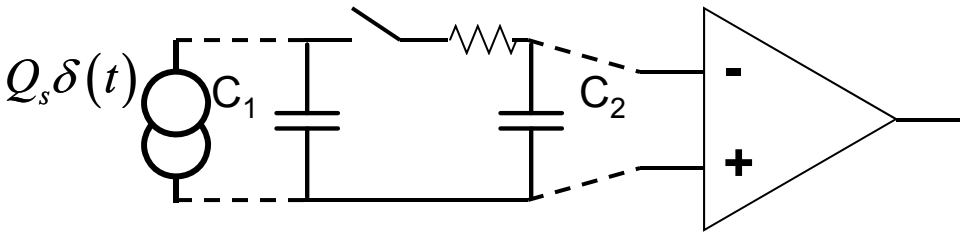
Gate resistance

Substrate resistance

Induced into gate (shielded by the inversion layer!?)

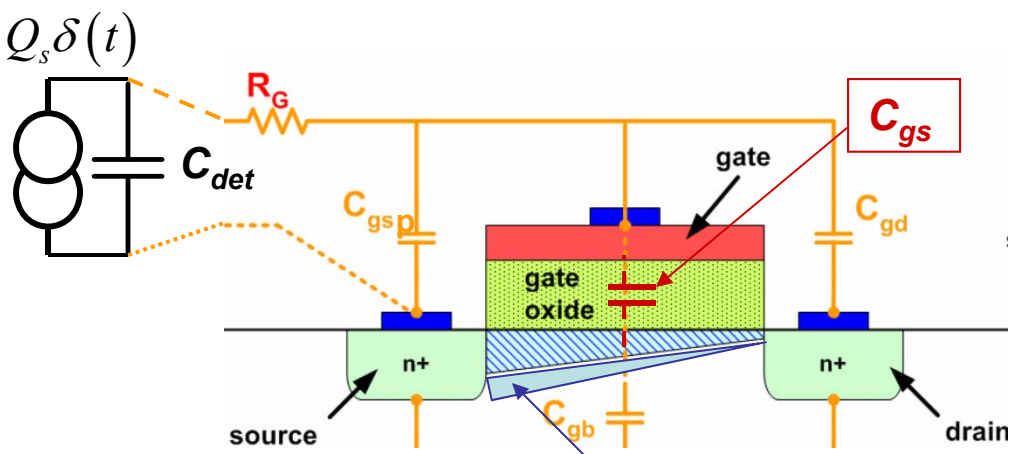
Charge Transfer from Detector to Amplifier

Transfer by *conduction*:



$$Switch\ closed: Q_1 = Q_s \frac{C_1}{C_1 + C_2}; Q_2 = Q_s \frac{C_2}{C_1 + C_2}$$

Q_s *is distributed as the ratio of capacitances*



$$C_{gs}\ vs\ C_{\det}\ matching\ needed!$$

"useful" charge: $\Delta Q_c = Q_s \Big/ \left[1 + \left(C_{\det} + C_{gsp} + C_{ds}\right)/C_{gs}\right]$

Matching of the Input Transistor to the Detector – series white noise

$$ENC = \frac{e_n\left(C_d + C_{gs}\right)}{\tau_p^{1/2}}$$

$$e_n^2 = 4kT\frac{\gamma}{g_m} \quad \left[V^2/Hz\right]$$

$$\Delta Q_c / \Delta I_d = \tau_e$$

$$\Delta Q_c = \Delta V_{gs} C_{gs}$$

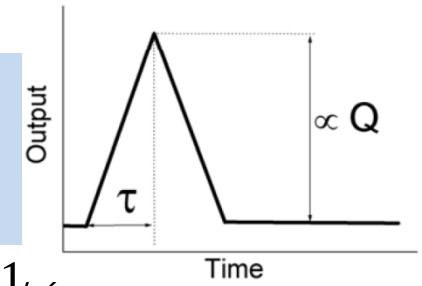
$$\Delta I_d / \Delta V_{gs} = g_m$$

$$f_T \approx 1/2\pi\tau_e = \left(1/2\pi\right) g_m / C_{gs}$$

$$\frac{g_m}{C_{gs}} = \tau_e \propto L_{eff}$$

$$ENC^2 = 4kT\gamma\frac{\tau_e}{\tau_p}\frac{\left(C_d + C_{gs}\right)^2}{C_{gs}}$$

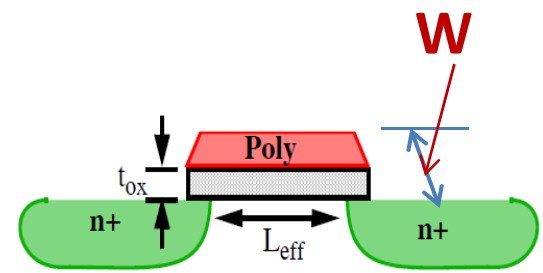
$$ENC \rightarrow \min \; for\; C_d = C_{gs}; \gamma = 1/2$$



The lowest noise for a transistor amplifier that could be achieved under ideal circumstances and no power limitation:

$$ENC_{s\,opt} \cong 2\sqrt{2}\sqrt{k_B T C_{gs}}\sqrt{\tau_e / \tau_p}$$

With *power constraint*, input MOS transistor is optimized by increasing *W* and decreasing current density (toward weak inversion), while the capacitances are not matched: $C_{gs\,opt} \leq (1/3) C_d$



6. Fluctuations on a Capacitance and Charge Measurement Sensitivity (and some less known noise properties)

$$\sigma_q^2 = k_B T C$$

$$\sigma_v^2 = {k_B T}/{C}$$

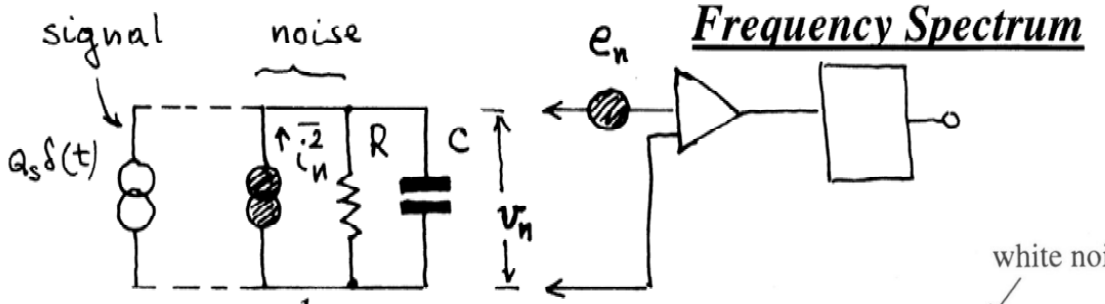
Boltzmann Constant: $k_B \cong 1.38 \times 10^{-23}\, JK^{-1}$

T= temperature

C= capacitance

Veljko Radeka
radeka@bnl.gov

Thermal Noise, Total Fluctuation without band-limiting: *kTC noise*

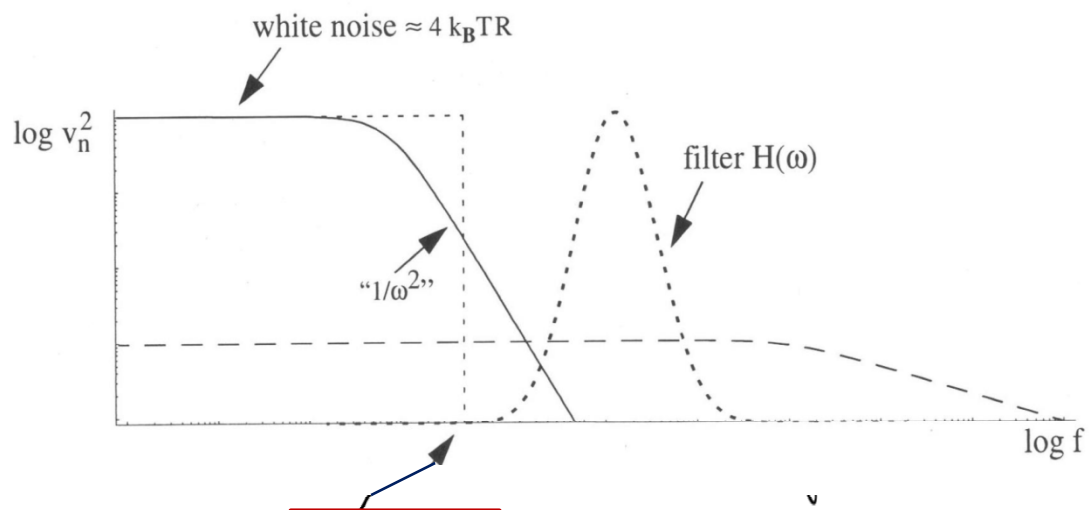


Frequency Spectrum

$$Y = \frac{1}{R} + j\omega C$$

$$\overline{i_n^2} = 4k_BT/R$$

$$\overline{v_n^2} = \overline{i_n^2}\left|Y^{-1}(\omega)\right|^2 = 4k_BTR\frac{1}{1+(\omega CR)^2}$$



Eq. bandwidth $f_h = \frac{1}{4RC}$

R determines the frequency spectrum, while its integral is determined only by C

Total fluctuation:

$$\sigma_v^2 = \int_o^\infty \overline{v_n^2}\,df = \frac{k_BT}{C}$$

$$\sigma_q^2 = k_BTC$$

"independent of R"

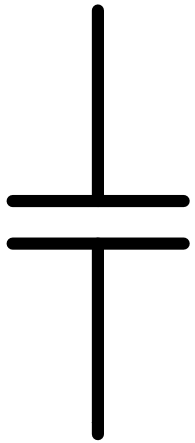
Equipartition:

$$(1/2)k_BT = (1/2)\sigma_q^2/C = (1/2)C\sigma_v^2$$

1. C=1pF, R=1GΩ — RC = 1ms, f_h = 250 Hz
2. C=100fF, R=10kΩ — RC=1ns, f_h = 250 MHz

Charge and Voltage *Total Fluctuations* on Capacitance

Capacitance: $C\ [F]$	***Charge fluctuation:*** $(kTC)^{1/2}/q_e\ [rms\ e]$	***Voltage fluctuation:*** $(kT/C)^{1/2}\ [V]$
1a	**0.4**	**64m**
10a	1.26	20m
100a	4	6.4m
1f	**1.26x10**	**2.0m**
10f	4.0x10	0.64m
100f	1.26×10^2	0.20m
1p	**4.0×10^2**	**64μ**
10p	1.26×10^3	20μ
100p	4×10^3	6.4μ



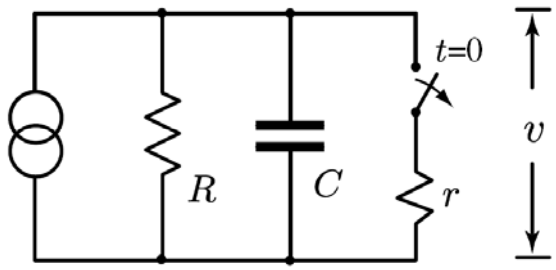
Dynamic range:

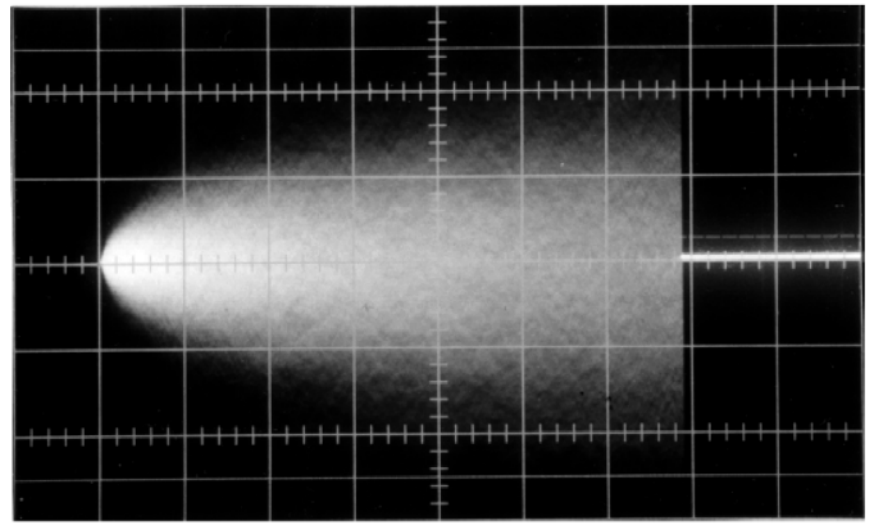
$$500mV/5\sigma \approx 500$$

ENC (if no filtering):
≈126 rms e

Transient Build-up of Noise: ***kTC noise vs time***

$$\overline{i_n^2} = 4k_BT/R$$



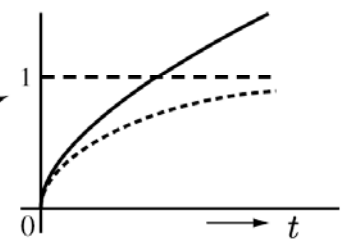


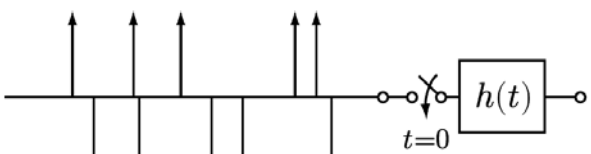
Campbell:

$$\sigma_v^2 = \frac{1}{2}\,\overline{i_n^2}\int_0^t h^2(u)du = \frac{k_BT}{C}(1-e^{-2t/\tau})$$

$$\underline{\sigma_v/(k_BT/C)^{1/2}} = \underline{(1-e^{-2t/\tau})^{1/2}}$$

$$\frac{\sigma\,(t)}{(k_BT/C)^{1/2}}$$





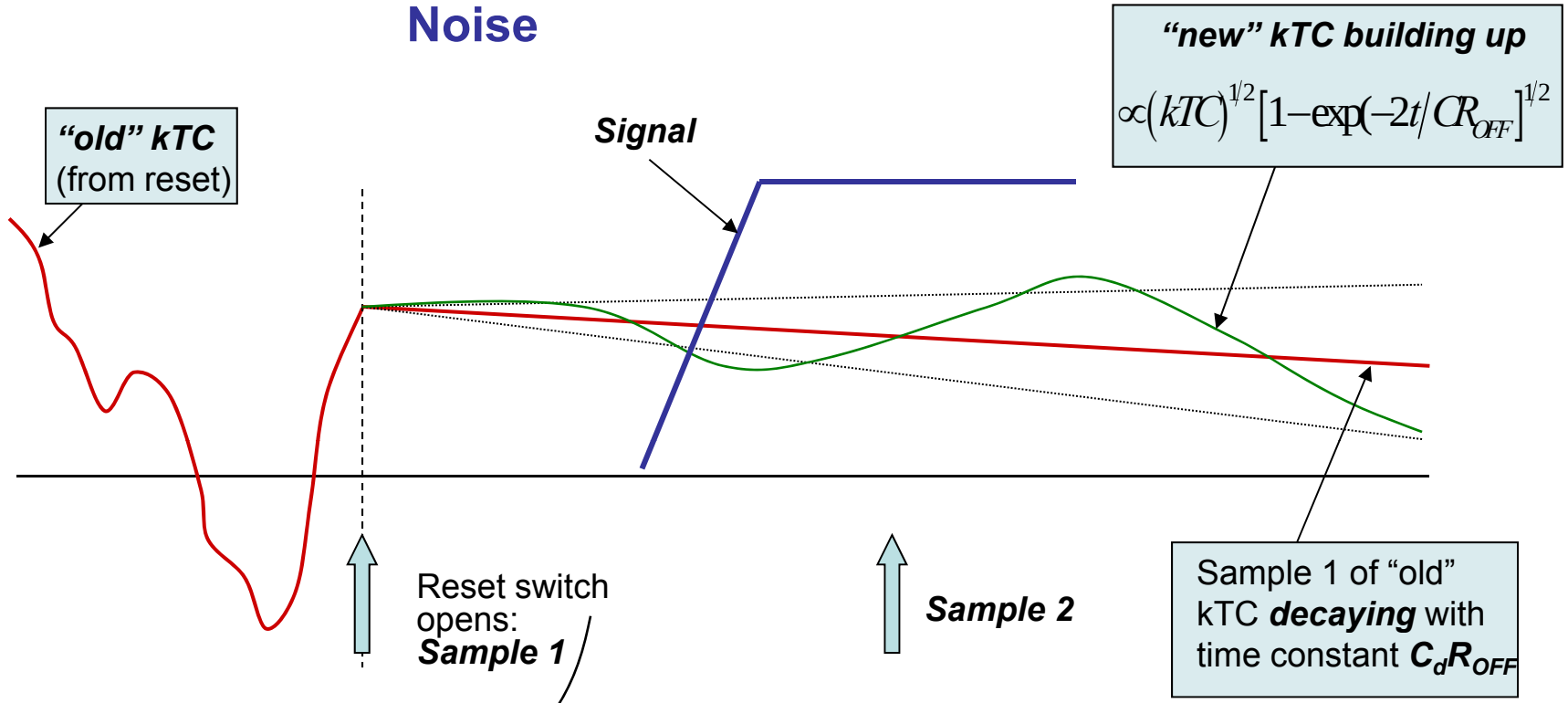
$$h(t) = \frac{1}{C}\,e^{-t/\tau}$$

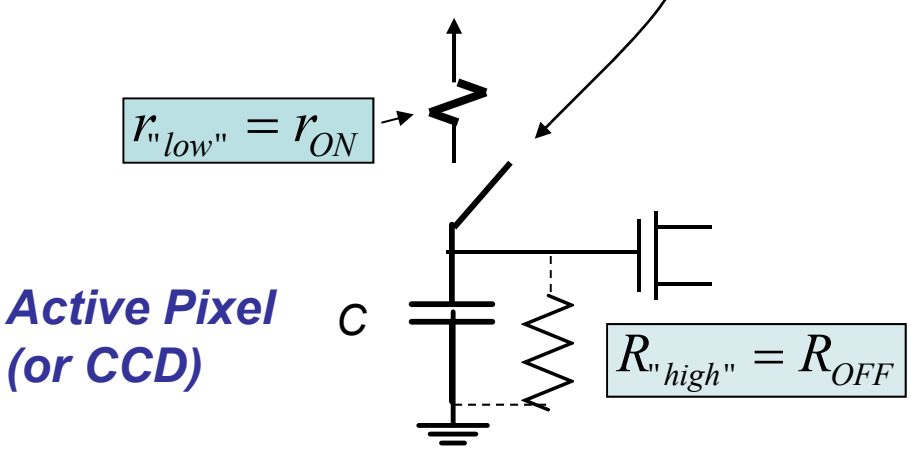
For $t/\tau \ll 1$: $\sigma_v^2 \propto t$ (random walk)

$$\sigma_v \approx (k_BT/C)^{1/2}\cdot(2\frac{t}{\tau})^{1/2}$$

For $\left.\begin{array}{l}\tau = RC = 1\text{s},\\ t \quad\quad\quad = 1\mu\text{s}\end{array}\right\}$ $\sigma_v/(k_BT/C)^{1/2} \approx$ 4.5%

Correlated Double Sampling (CDS) and *kTC* Noise





Active Pixel (or CCD)

$$R_{OFF} / r_{ON} \sim 10^6 - 10^{11}$$

Example:

$C \sim 20$ fF

$r_{ON} \sim 10^3$ ohms $\quad r_{ON}C \sim 20$ ps

$R_{OFF} \sim 10^{13}$ ohms $\quad R_{OFF}C = 0.2$ s

A note …

Noise in electronic and electromechanical systems is usually analyzed in the context of its frequency spectrum and of all sensor parameters. The so called ***"kTC" noise, i.e., the fluctuation of the charge stored on a capacitance C***, sometimes referred to as "reset noise", and/or, "reset transistor noise", refers to **the *total fluctuation as governed by the equipartition principle***. *In* some cases, it represents a limit to the measurement accuracy.

In some other cases, with most radiation detectors and CCDs, it only represents the worst case, and a much better noise performance can be achieved. While the total charge fluctuation on a capacitance is determined as *kTC by the equipartition* principle, ***the noise affecting the measurement can be reduced to a very small fraction of this value***, by minimizing the ***dissipative real part*** of the node impedance, and by ***restricting the bandwidth*** to the region of the frequency spectrum where the noise from the dissipative part is negligible. The total fluctuation limit is most difficult to avoid in the simplest detector readout schemes, where no filtering (band limiting) prior to sampling is applicable, such as with pixel matrix imagers.

A few points on *kTC* noise

1. *Fluctuation-dissipation theorem* with Nyquist's expression for thermal noise is essential for calculation of noise spectra and for detailed information on noise sources.

2. *Equipartition theorem* provides no detailed information, but provides a *check on the integrals* of noise spectra (the total fluctuation).

3. *Transient behavior* of noise in switched capacitor circuits and matrix readout pixel arrays is best understood by means of *Campbell's theorem*, which provides *noise variance vs time*.

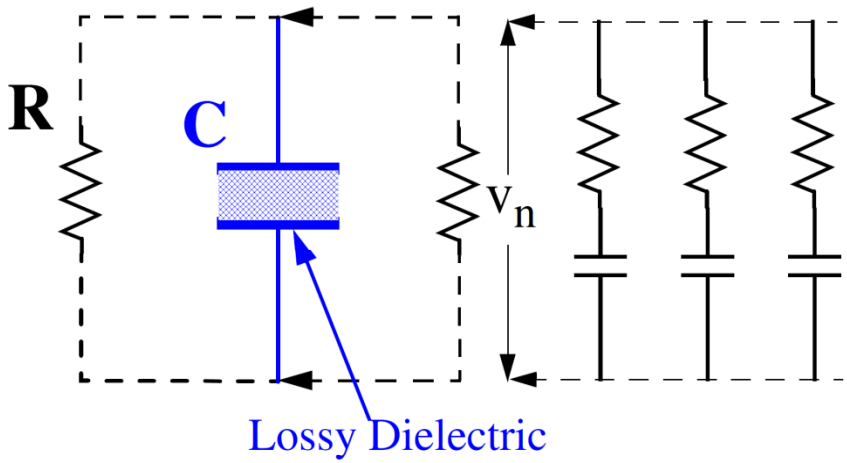
4. A complete charge reset and charge transfer by a switch result in $\sigma_q^2 = k_B TC$, independently of the switch ON resistance. This noise can be subtracted only if the *first sample* in the CDS is *before the signal*.

5. Transfer (i.e., direct transport) of charge without switching (as in a CCD) does not result in $k_B TC$ noise. *Reset* of the sense amplifier *does*.

6. In *resonant* sensors and vibration isolators, noise well *below the resonant frequency* is very important. It is inversely proportional to the quality factor Q.

7. Noise from Dielectrics

Thermal Noise from Dielectrics



(All) dielectrics are lossy:

- Circuit boards G10/FR4: **D~0.02**
- Fused silica, teflon, polystyrene: **~10^{-4}**
- Rogers RT/duroid ~ **4x 10^{-4}**

Permitivity: $\varepsilon = \varepsilon' + j\varepsilon'' = \varepsilon'\left(1 + j\frac{\varepsilon''}{\varepsilon'}\right)$

Dissipation factor (*tanδ*): $\frac{\varepsilon''}{\varepsilon'} = D = \frac{G(\omega)}{\omega C}$

Noise current: $i_n^2 = 4kTG(\omega) = 4kTCD\omega$

Eq. noise voltage (1/f): $v_n^2 = i_n^2 \frac{1}{(\omega C)^2} = 4kTD\frac{1}{\omega C}$

Eq. noise charge due to dielectric loss: $ENC^2{}_D \approx kTC_D(2.4D)$

An Example:

For C = 1 pF at T = 293 K

$\sigma_q = (k_B\ T\ C)^{1/2} = 400$ e rms

$ENC_a < 5$ e (with an optimized amplifier)

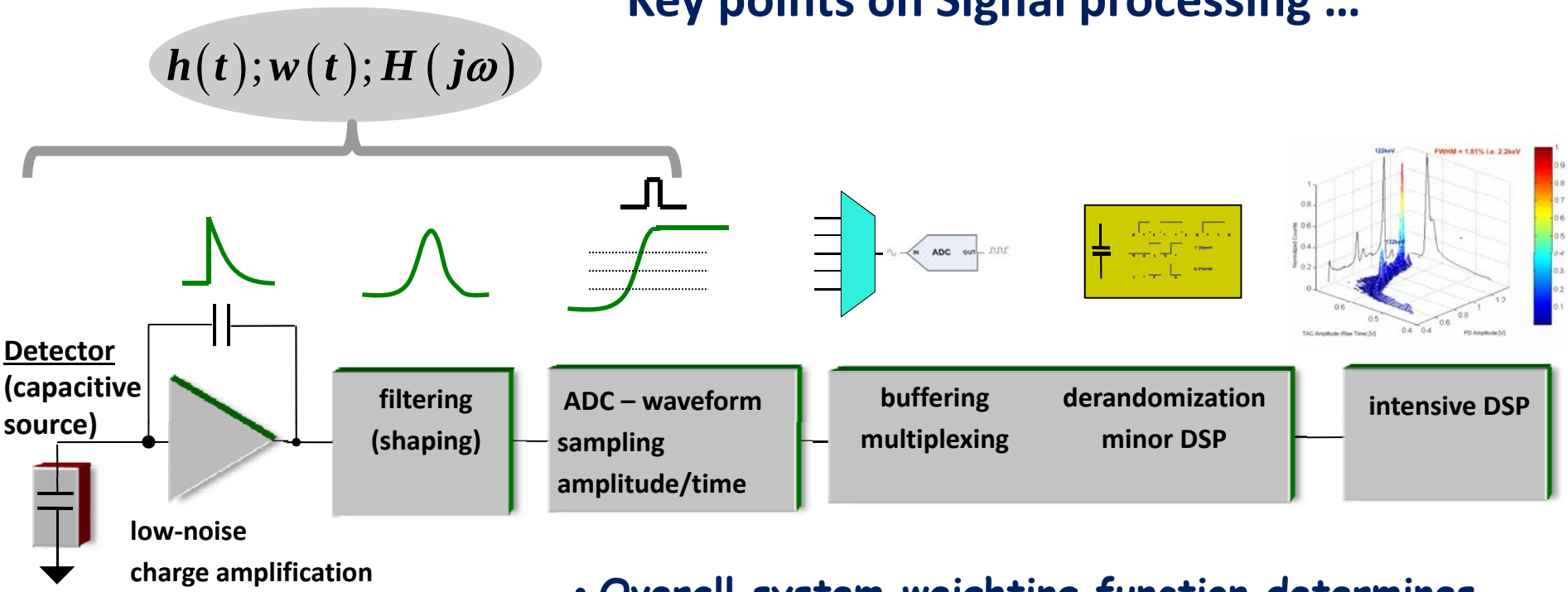
Dielectric Noise Contribution:

$D \approx 5\times10^{-5}$, $ENC_D \approx 4$ e rms

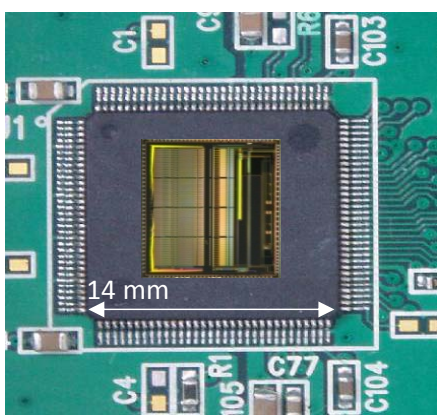
$D \approx 2\times10^{-2}$, $ENC_D \approx 86$ e rms (G10 circuit board)

8.Concluding Remarks

Key points on Signal processing …



- **Overall system weighting function determines equivalent noise charge (ENC).**



- **Input transistor series noise should be dominant** – this is a test of how good are the system design and implementation.

- The use of feedback at the input and the choice of circuit configuration should not affect ENC.

9. Literature

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Appendix

A. 1
Noise Calculation: Time Domain and Frequency Domain

- For <u>time invariant</u> systems impulse response <u>h(t)</u> and weighting function <u>w(t)</u> are interchangeable for noise calculations.

From Parseval's theorem, noise variance can be expressed as:

$$\sigma^2 = \bar{n}\, q^2 \int_{-\infty}^{\infty} h^2(t)dt = 2\,\bar{n}\, q^2 \int_{o}^{\infty} |H(\omega)|^2\, df$$

Campbell's theorem

Also: $\sigma^2 = W_o \int_{o}^{\infty} |H(\omega)|^2\, df$

Thus noise spectral density: $W_o = 2\,\bar{n}\, q^2 = 2q_e I_o$ for shot noise
(similarly $W_o = 4kT/R$ for thermal noise)

<u>Parallel noise integral</u>:

I_2 $$\overline{ENC_p^{\,2}} = \tfrac{1}{2} W_{op} \int_{-\infty}^{\infty} h^2(t)dt = W_{op} \int_{o}^{\infty} |H(\omega)|^2 df$$

parallel noise (current) spectral density = W_{op}

<u>Series noise integral</u>:

I_1 $$\overline{ENC_s^{\,2}} = \tfrac{1}{2} W_{os}\, C_{in}^{\,2} \int_{-\infty}^{\infty} h'^2(t)dt = W_{os} C_{in}^{\,2} \int_{o}^{\infty} \omega^2 |H(\omega)|^2\, df$$

series noise (voltage) spectral density, $W_{os} = \overline{e_n^{\,2}} = 4kTR_s$

(since $\int_{-\infty}^{\infty} h'^2(t)dt = 2\int_{o}^{\infty} \omega^2 |H(\omega)|^2\, df$)

- For <u>time variant</u> systems, noise is calculated using <u>weighting function</u> and time domain relations.

A.2 Parallel Noise due to ***Dark Current*** in Devices with ***Avalanche Gain***

Parallel noise (from Campbell's theorem):

$$ENC_p^2 = nq^2 \int_{-\infty}^{\infty} w^2(t)dt = nq^2 t_G$$

$$nq^2 = q(nq) = qI_o$$

n = rate of charge impulses

t_G = equivalent integration time

- Devices ***without avalanche gain***: $q = e$ = electron charge
- Devices ***with avalanche gain*** M : $q = Me$ = charge in each impulse in Poisson sequence

Parallel noise due to dark current in avalanche photo-diodes:

$$ENC_p^2 = n(Me)^2 t_G$$

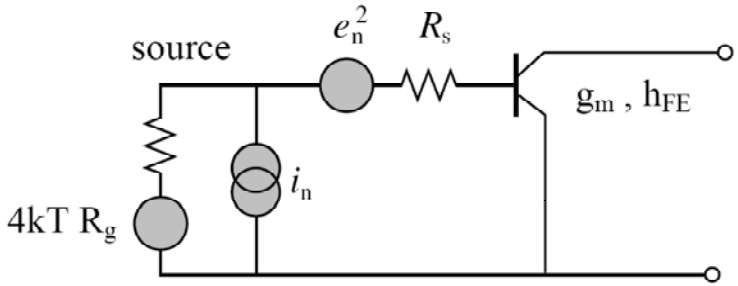
$$ENC_p^2 = I_o M \cdot e\, t_G$$

Avalanche gain magnifies the noise (ENC_p) by $M^{1/2}$ compared to the shot noise from a current I_o ,

i.e., the noise due to ***avalanche dark current*** I_o equals the noise due to single electron current MI_o .

(Surface leakage current noise is not subject to avalanche gain.)

A3. Noise Figure vs Noise Voltage, Noise Current and Noise Temperature



$R_s = 1/2g_m + r_{bb'}$
$i_n^2 = 2\ eI_b = 2e\ \ I_c/h_{FE}$

$NF = 10 \log_{10} [(\text{source} + \text{ampl.})/\text{source}]$

$NF = 10 \log_{10} [1+(e_n^2 + i_n^2 R_g^2)/4kTR_g]$

For $i_n^2 R_g^2 << e_n^2$, i.e., $R_g = 50$:

$\underline{NF = 10 \log_{10} [1 + R_s/R_g]}$ $= 10 \log_{10} [1 + T_n/T]$ [db]

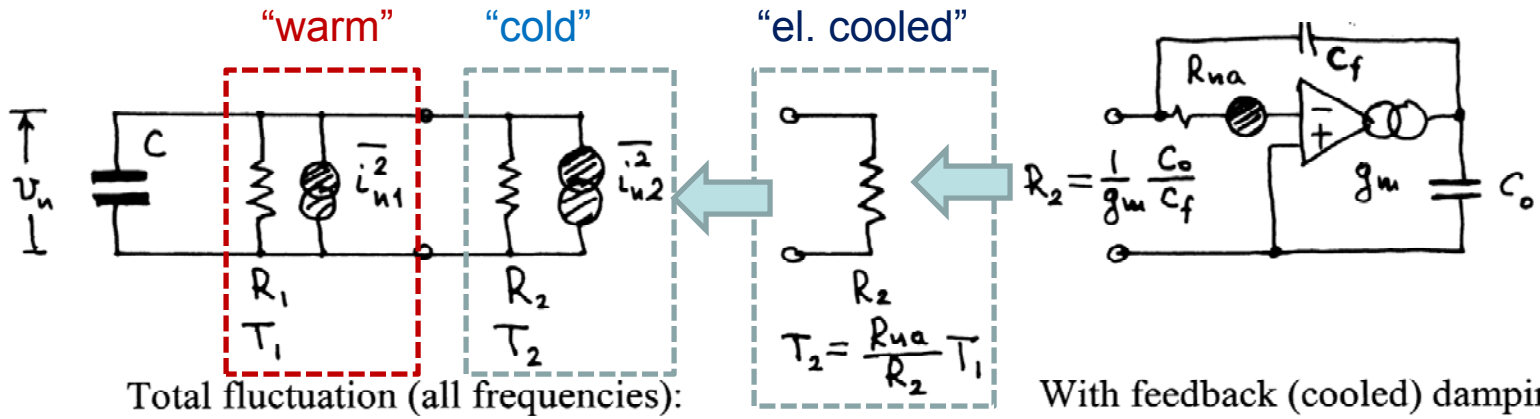
T_n = ampl. noise temperature

$R_s T = R_g T_n \rightarrow T_n/T = R_s/R_g$

NF [db]	R_s [ ]	e_n[nV/Hz$^{1/2}$]	T_n[K]
3	50	0.91	293
2	29	0.71	170
1	13	0.47	76
0.5	6	0.32	35

<u>ENC</u> from <u>e_n</u> , <u>i_n</u> (with $C_D + C_A$ and t_m)

A4. Noise in Resistors at Different Temperatures and *"Electronic Cooling"* by Feedback



Total fluctuation (all frequencies):

$$\sigma_v^2 = \frac{k_B}{C} \cdot R_1 \| R_2 \left(\frac{T_1}{R_1} + \frac{T_2}{R_2} \right)$$

1. for $T_1 = T_2 \rightarrow \sigma_v^2 = \frac{k_B T_1}{C}$

2. if $T_2 = 0 \rightarrow \sigma_v^2 = \frac{k_B T_1}{C} \cdot \frac{1}{1 + R_1 / R_2}$

With feedback (cooled) damping:

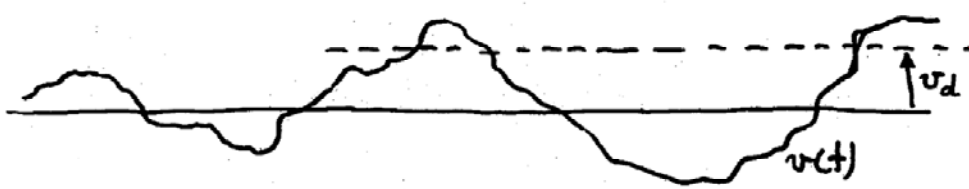
$$\sigma_v^2 = \frac{k_B T_1}{C} \cdot \frac{1}{1 + R_1 / R_2} \left(1 + \frac{R_{na} R_1}{R_2^2} \right)$$

σ_v min for $R_2 = (R_1 R_{na})^{1/2}$

$$\boxed{\rightarrow \sigma_v^2 = \frac{kT_1}{C} \cdot \frac{2}{1 + (R_1 / R_{na})^{1/2}}}$$

$R_1 = 10^6 \Omega$, $R_{na} = 100 \Omega$ $\Big\}$ $R_2 = 10^4 \Omega$, $\sigma_v^2 \cong \frac{k_B T_1}{C} \cdot \frac{1}{50}$

A5. Zero-Crossing Statistics of Noise



Discriminator threshold

$W(\omega) =$ spectral density

$K(\tau) =$ autocorrelation function

$\sigma = [K(0)]^{1/2} =$ rms noise

Rate of ***positive*** zero crossings:

$$n_{zc+} = \frac{1}{2\pi}\left[-\frac{K''(0)}{K(0)}\right]^{\frac{1}{2}} = \frac{1}{2\pi}\left[\frac{\int_0^\infty \omega^2 W(\omega)d\omega}{\int_0^\infty W(\omega)d\omega}\right]^{\frac{1}{2}}$$

Rate of positive level crossings:

$$n(v_d)_+ = n_{zc+} \cdot \exp\left[-v_d^2 / 2K(0)\right]$$

Example: 2nd order high frequency cutoff (2 RC integrations)

Solution:

$$n_{zc+} = \frac{1}{2\pi(\tau_1\tau_2)^{1/2}}$$

For: $\tau_1 = \tau_2 = 50ns; 1\mu s$

$n_{zc+} = 3MHz; 150kHz$

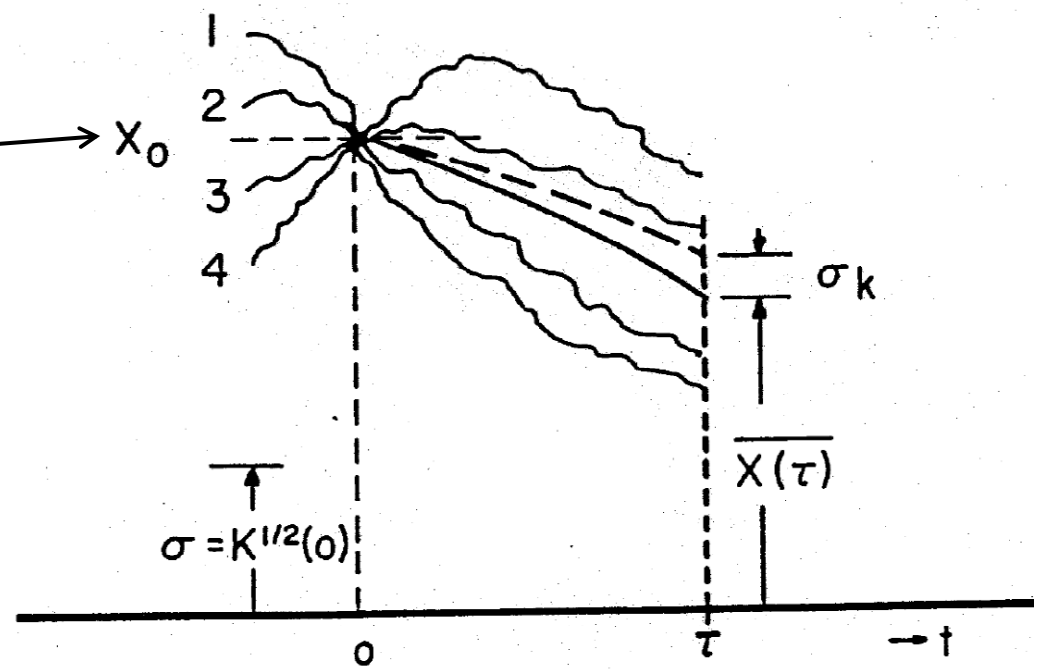
Threshold crossing rate:

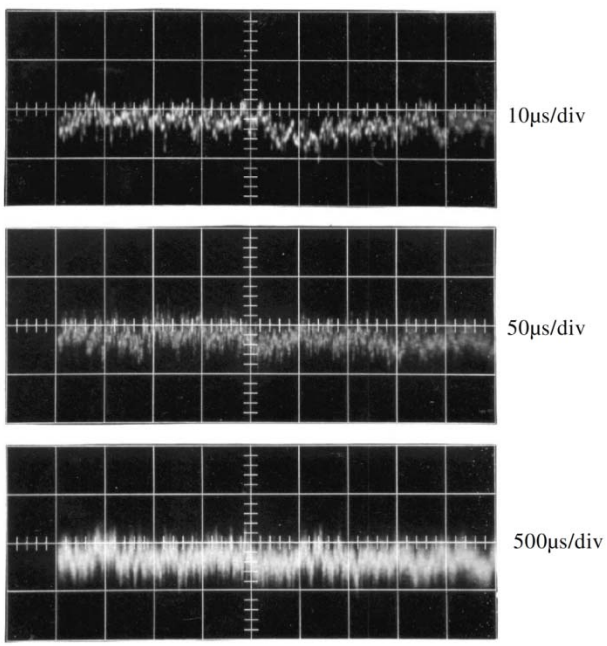
$v_d / \sigma \Rightarrow$	$n(v_d)_+ / n_{zc+}$
2	1.4×10^{-1}
3	1.1×10^{-2}
4	3.3×10^{-4}
5	4×10^{-6}

J.S. Bendat, Principles and Applications of Random Noise Theory, J. Wiley&Sons, 1958,p. 125

A6. Autocorrelation Function: Scope measurement

Scope trigger at 4-5 σ





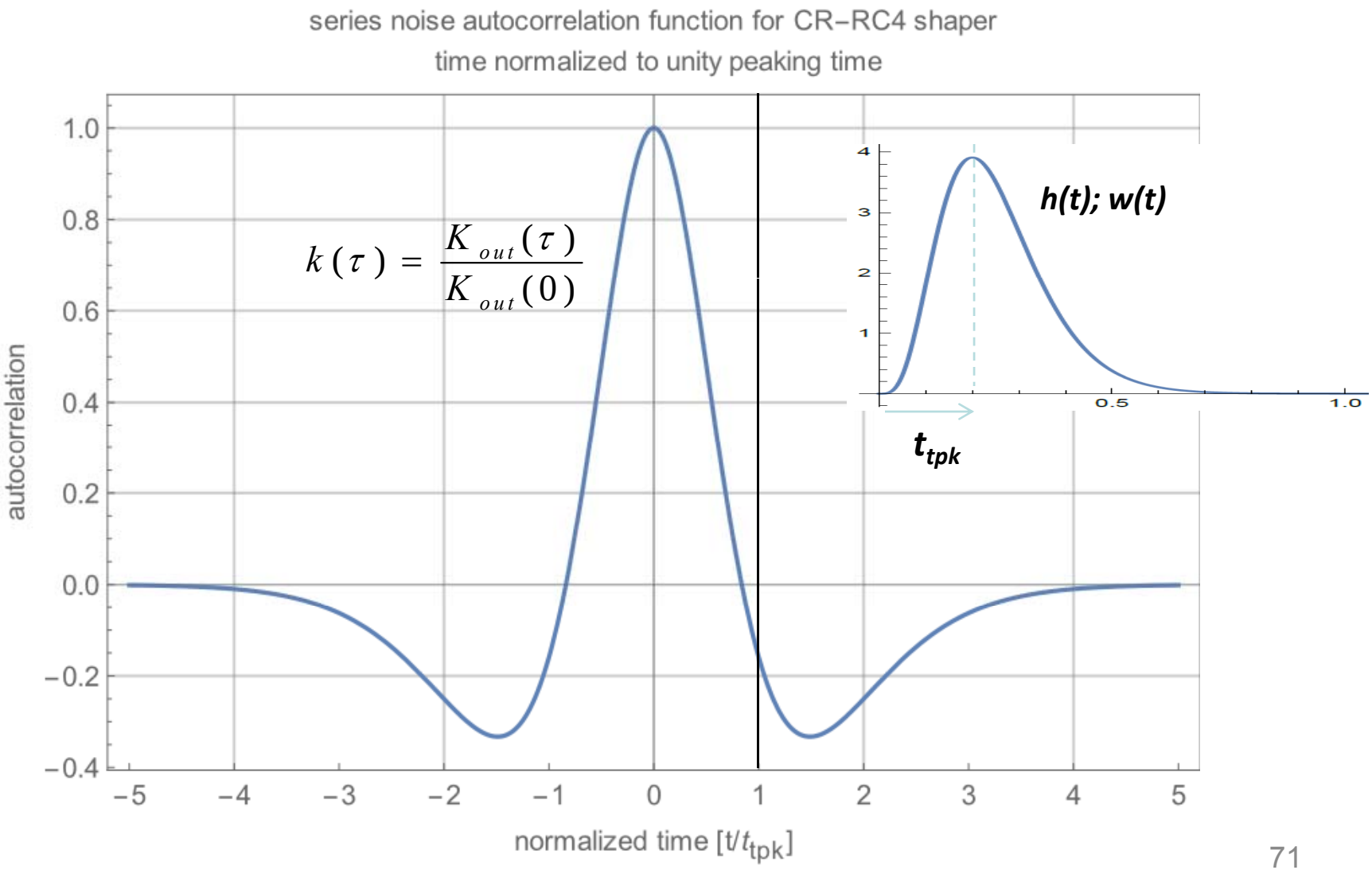
$1/|f|$ noise — different time scales

$$\frac{\overline{X(\tau)}}{X_0} = \frac{K(\tau)}{K(0)} = k(\tau)$$

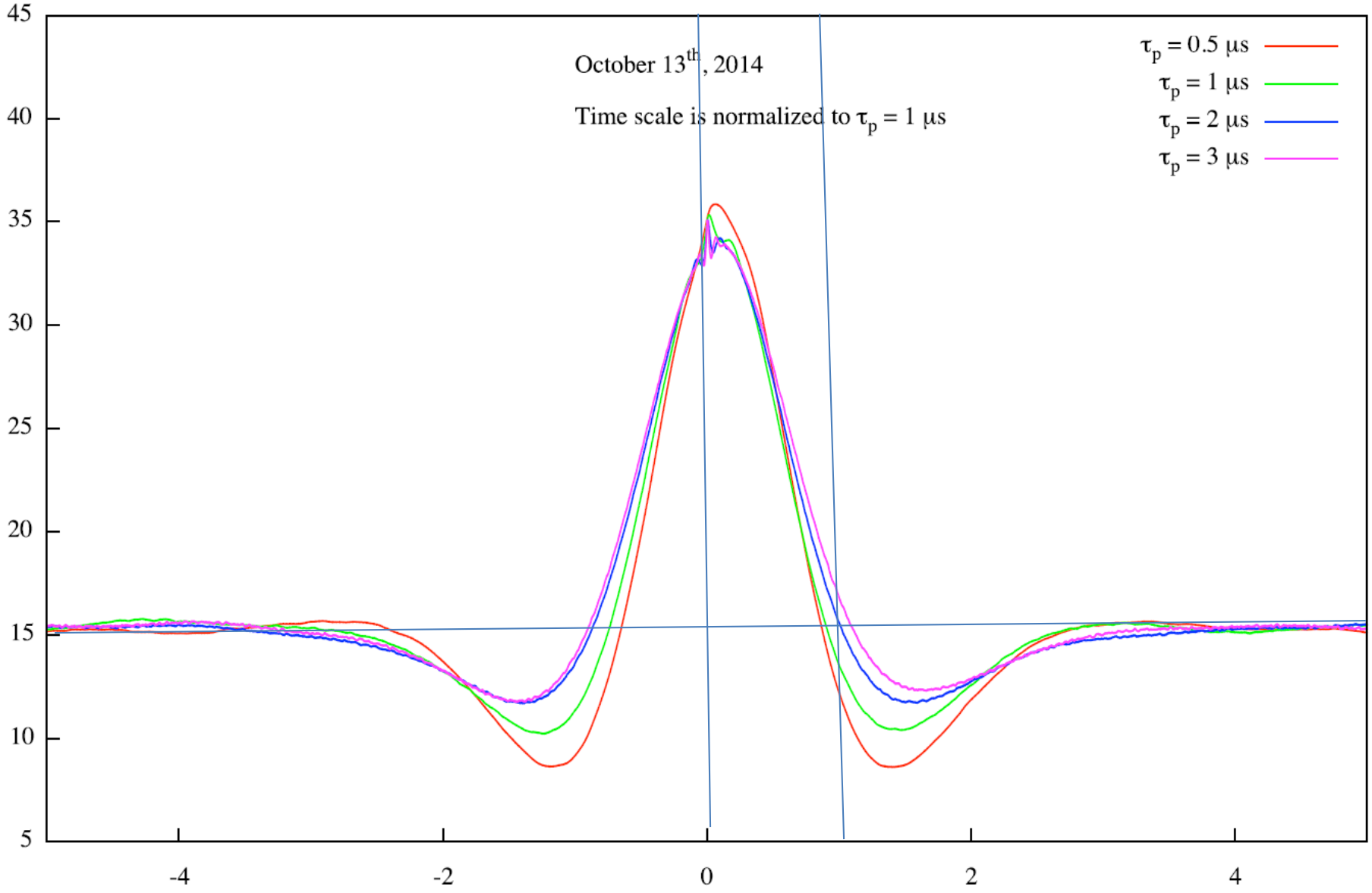
$$\sigma_k^2 = K(0) - \frac{K^2(\tau)}{K(0)} = \sigma^2\left[1 - k^2(\tau)\right]$$

Autocorrelation function at the output of the anti-aliasing filter (prior to ADC)

for $i_{neq}^2 = v_n^2 \omega^2 C^2_{in}$ (1st transistor white series noise), calculated



An Example of Noise Autocorrelation Measurements by Digital Oscilloscope



Detector Signal Processing IEEE NSS 2014

Veljko Radeka, BNL

Slide Captions and Notes (Figure numbers refer to slide numbers):

1. Signal Formation and Ramo's Theorem

Figs. 4. And 5. These figures illustrate Ramo's theorem for induced signals, current and charge. $\boldsymbol{E_w}$ is the weighting field in units of 1/cm, and it is a measure of electrostatic coupling between the moving charge and the sensing electrode. The procedure to calculate the induced current as a function of time is as follows. First, the weighting field is determined by solving Poisson's equation analytically or numerically assuming unity potential on the sensing electrode of interest and zero potential on all other electrodes. Next, the velocity of the moving charge as a function of position is determined from the operating (applied) field on the detector. This gives the induced current as a function of the position of the moving charge. Third, the position of the moving charge as a function of time is determined by solving the equations of motion. This is necessary in the case of ballistic motion of charge, but it is simple in the case of transport by drift as the charge carriers follow the applied electric field.
If we are interested only in the total induced charge and not in the waveforms, the induced charge is simply given by the difference in the weighting potentials between any two positions of the moving charge. An example of the weighting-field (potential) profiles is illustrated by the plot of equipotential lines for planar geometry with a strip sensing electrode. The operating (applied field) in this case is uniform and perpendicular to the electrodes. The *weighting field map* is in general quite different from that of the *operating field*; the two field maps are identical only in some special cases.
The minus sign in Ramo's equation for the induced current results from the arbitrary assumption of induced current *into* the electrode being *positive*.

Fig. 6. This is a simple case where the real (operating) electric field and the weighting field have the same form ***=1/d***. The induced current waveforms shown are for a detector with different electron and hole (positive ion) mobilities. For extended ionization the waveforms result from superposition of the waveforms for localized ionization, and the currents decrease as the carriers arrive at the electrodes from different initial positions within the bulk of the detector. In some detector media the positive ion mobility is much lower than the electron mobility resulting in a long ion transit time and very low induced current. In such a case the charge induced in a short time is position dependent, ***q(x/d).***

Fig. 7. Weighting field (potential) for strip and pixel electrode configuration. The shielding effect is inversely proportional to the ratio of the distance between the planar electrodes and the strip width (i.e., pixel radius). The shielding effect is more pronounced for pixels than for strips. The result of these configurations is that the signal charge

(integral of the induced current) becomes independent of the position of the origin of ionization for most of the volume of the detector except near the readout electrodes. This effect is used in detectors where only electrons are collected during the integration time, such as Cadmium Zinc Telluride (CZT), and some gas and noble liquid detectors. To illustrate this, histograms are shown for a strip and pixel illuminated by a beam of penetrating x-rays absorbed uniformly through the detector.

Fig. 8. Charge collection and signal formation in **GEM** (Gas Electron Multiplier), **Micromegas** (MICROMEsh GAseous Structure) and **MCP** (Micro-Channel Plate) based detectors. These three electron multipliers (sometimes referred to as "detectors", although they are only a part of the detector system, have in common that the signal can be induced on electrodes different and separate from the electrode where the electrons are actually collected. The two electrode layers are separated by a layer of dielectric and, as a consequence, the signal charge induced on the readout electrode is always smaller than the charge collected. Such an arrangement can be exploited in several ways, by making possible: a) placement of readout strips and electronics outside of the gas or vacuum enclosure; spreading of the induced charge footprint, and thereby position interpolation; limiting the energy of any discharge to protect the electrodes and readout microelectronics.

Fig. 9. Weighting field and induced charge on high resistivity electrode (shown in Fig. 8).

Fig. 10. Notes on Weighting Field - Potential and Induced Signals

2 .Noise Mechanisms

Fig. 12. The basis of a noise process can be represented as a sequence of randomly generated elementary impulses that has a Poisson distribution in time and mean rate of occurrence $<n>$. Upon acting on a physical system with impulse response much longer than $<\boldsymbol{n}>^{-1}$, the characteristic noise waveforms (e.g., such as those we observe on an oscilloscope) are produced as a superposition of responses to individual impulses. The noise variance at the output of the physical system (a simple RC filter or a complete readout system) is calculated by using Campbell's theorem, which states that the sum of mean square contributions of all preceding impulses equals the variance. The expressions for the variance are given after subtracting the mean value. The variance is determined by the rate of impulses $<\boldsymbol{n}>$, their area $\boldsymbol{q}$ (charge), and by the impulse response (i.e., the weighting function $\boldsymbol{w(t)}$ of the measurement system, the preamplifier and the subsequent readout chain).

For detailed description: V.R., Ann. Rev. Nucl. Part. Sci. **38** (1988) 217.

Almost any noise spectrum can be generated from a random sequence of impulses (i.e., white noise with "infinite bandwidth") by using an appropriate filter.
"Infinite bandwidth" implies a noise spectrum which is flat over the frequency range where our measurement system has a non-zero response. Simple integration of white

noise results in "random walk" with $1/f^2$ spectrum. An elementary impulse response for generation of this noise is the step function $U(t)$. Generation of $1/|f|$ noise is somewhat more elaborate. It requires fractional integration of *order one half*. The impulse response of the transforming filter is $U(t)/t^{1/2}$, as shown in the figure. The basic feature of any noise generating mechanism for low frequency divergent noises is an "infinitely long memory", i.e., very long memory, for individual independent elementary perturbations. For a discussion of the basics: [Ref. 10].

Fig. 13. Calculation Spectral Densitiy and Variance for Shot Noise and Thermal Noise

Fig. 14. A noise spectrum very close to $1/|f|$ can be generated by superposition of relaxation processes with uniform distribution of life times. The relaxation process is described by the probability $U(t)\ exp(-t/\tau)$, which represents a step change with exponential decay.

Trapping-detrapping in semiconductors is one such possible mechanism for generation of $1/|f|$ noise. A single trap in the gate oxide (or the interface between the gate oxide and the channel) of an MOS transistor results in a drain current waveform shown in the upper left of the figure. This phenomenon is referred to as the ***random telegraph noise*** [Refs.] and it is observed readily in the very small transistors in deep submicron technology. The spectral density of such a noise is Lorentzian as shown in the figure. Superposition of the spectra for a number of traps with a distribution of life times results in $1/|f|$ noise.

A hardware generator of $1/|f|$ noise can be made using the fact that white noise passed through a simple RC integrator has a Lorentzian spectral density. A circuit which transforms white noise into $1/|f|$ noise can be made requiring about one time constant (one RC circuit) per decade of frequency, as shown in [Ref. 10].

Fig. 15. $1/|f|$ noise is one of the fractal processes, and its waveform preserves the same features independently of the time scale. Another expression of this is independence of the measurement variance (i.e., the noise power) upon the time scale of the measurement as long as the ratio of the high frequency and the low frequency cutoffs remains constant. As the bandpass moves along the frequency spectrum the spectral density integral (i.e., the measurement variance) remains constant for $f_h/f_l=const.$ In detector pulse processing it is well known that the contribution of $1/|f|$ noise to the equivalent noise charge (ENC) remains independent of the shaping time.

3. Equivalent Noise Charge (ENC) Calculation

Fig. 17. Functional overview of a typical detector readout chain. The design of various blocks of the chain will vary in the transistor technology used, circuit configuration and many details. What determines the noise limitation to the precision of the amplitude and time (as well as of the signal waveform) measurements is the weighting function of the overall signal processing chain.

Fig. 18. This figure illustrates principal noise sources in charge amplifiers

Fig. 19. This figure illustrates principal noise sources in charge amplifiers and an equivalent diagram for calculation of the equivalent noise charge (ENC).

Two elementary noise generators are included in the equivalent circuit, a series noise voltage generator representing the noise in the amplifying device, and a parallel noise current generator representing various noise sources not inherent to amplification (detector leakage current noise, parallel resistor noise, etc.). Both types of noise are assumed to have a white spectrum. Two forms of presentation of these two noise sources in terms of a sequence of random pulses are shown, as ***charge (or voltage)*** at the input of the amplifier, and as a ***current*** injected into the input capacitance (comprised of the detector+amplifier+parasitic capacitances). *The presentation of the series noise in terms of a current into the detector input is the derivative of the charge (voltage) representation.* The sequence of voltage impulses representing the amplifier series noise thus corresponds to an equivalent sequence of ***current doublets*** (derivatives of delta function) injected at the detector. The parallel noise is by its origin a current source in parallel with the detector, and it is presented by a sequence of ***impulses*** (delta functions). *It is this difference in the location of the two white noise sources with respect to the detector capacitance that makes their apparent noise spectra and their effect on the measurement quite different.*

The series ***1/|f|*** noise contribution to ENC is independent of the peaking time and the time scale of the overall system response as long as the shape of the weighting function is preserved. This corresponds to a constant ratio of the high frequency and low frequency cutoffs, as indicated in Fig. 14. The ***1/|f|*** noise due to a dissipative dielectric depends on the dielectric loss factor ***D=tan(δ),*** as shown in Fig. 43. It can be significant with detector-amplifier connections on glass fiber circuit boards.

The expressions for the equivalent noise voltage ***spectral density*** at the input of a noiseless amplifier, and for the equivalent noise current spectral density as if originating in parallel with the detector capacitance are given in this figure. They are arrived at as follows:

1/f noise physical spectral density is defined as $A_f \big/ f \; in \; [V^2/Hz]$.

"Physical" (unilateral) equivalent ***noise voltage spectral density*** due to all three noise sources defined above and illustrated in Fig. 6.11, referred to the input of the preamplifier:

$$v_n^2 = e_n^2 + \frac{A_f}{f} + 2q_e I_0 \frac{1}{C_{in}\omega^2}$$

"Physical" (unilateral) equivalent ***noise current spectral density*** into the input capacitance C_{in} obtained by differentiation of v_n^2, i.e., multiplying by $\omega^2 C_{in}^2$ in the frequency domain,

$$i_{neq}^2 = v_n^2 \omega^2 C_{in}^2 = \omega^2 C_{in}^2 e_n^2 + C_{in}^2 \omega^2 \frac{A_f}{f} + 2qI_0 = \omega^2 C_{in}^2 e_n^2 + 2\pi C_{in}^2 A_f \omega + 2qI_0$$

Fig. 20. A qualitative illustration of the noise spectra for series white and 1/f noise from the sensor input node to the output of the analog portion of the readout chain prior to ADC Overall response, i.e. weighting function of this portion of the readout chain represents anti-aliasing filter in case of subsequent digital signal processing (slides

Fig. 21. The equivalent noise charge (ENC) is calculated by integrating the ***noise current spectral density multiplied by the square of the system response in either the time domain (weighting function) or the frequency domain (transfer function),***

$$ENC^2 = \frac{1}{2} e_n^2 C_{in}^2 I_1 + \pi C_{in}^2 A_f I_2 + qI_0 I_3$$

$$I_1 = \int_{-\infty}^{\infty} \left[w'(t) \right]^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} \left| H(j\omega) \right|^2 \omega^2 d\omega = \frac{A_1}{\tau}$$

$$I_2 = \int_{-\infty}^{\infty} \left[w^{(1/2)} \right]^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} \left| H(j\omega) \right|^2 \omega d\omega = A_2$$

$$I_3 = \int_{-\infty}^{\infty} \left[w(t) \right]^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} \left| H(j\omega) \right|^2 d\omega = A_3 \tau$$

where τ is the time width parameter of the weighting function, either the peaking time of the function, or some other characteristic time constant of the filter implemented in hardware.

I_1, I_2, I_3 are the noise integrals for the *series (voltage)* white noise and the series 1/f noise, and for the *parallel (current)* noise respectively. The integrals are derived in time domain from Campbell's theorem and expressed in frequency domain using Parseval's theorem [Appendix A1]. The coefficients A_1, A_2, A_3 are the ***form factors of the weighting function*** (and the equivalent transfer function). Their values for some frequently used functions are given in Fig. 18.

Fig. 21. Basic relations for noise calculation in time domain and frequency domain, used in slide 20 calculation.

Fig. 23. Some more detail on the calculation of integrals I_1, I_3 and their approximate evaluation by piece-wise linear approximation of the weighting function:

Calculation of equivalent noise charge (ENC) for a signal processing chain described by a weighting function ***w(t)***. A bipolar weighting function is assumed in this case. The noise calculation is performed in time domain by using Campbell's theorem which was introduced in Fig. 11. For parallel noise, the superposition of effects of all random impulses leads to the expression for ENC_p^2, where $\overline{i_n^2} = 2\overline{n}q^2$, $\overline{n}$ = mean rate of impulses, q = impulse charge. For a current contributing full shot noise (all charge carriers generated randomly) $\overline{i_n^2} = 2\, q_e I_o$, where q_e = electron charge and $I_o = \overline{n}\, q_e$ is the mean current. For a resistor in parallel with the detector $\overline{i_n^2} = 4\, kT/R_p$. $\overline{i_n^2}$ is the physical noise power spectral density. The weighting function is normalized to unity so that the definition of ***ENC is "the noise charge which produces an output of the same magnitude as an impulse signal of equal charge"***. For calculation of the series noise, we use the representation in terms of an equivalent current generator connected in parallel with the detector. A doublet $\boldsymbol{C_{in}\, \delta'(t)}$ acting upon the weighting function ***w(t)*** produces by convolution $\boldsymbol{C_{in} \cdot w'(t)}$. By integration of mean square contributions of all previous doublets, the expression for ENC_s^2 is obtained, where $\overline{e_n^2}$ is the noise spectral density for series noise in V^2/Hz. In terms of an equivalent series noise resistance $\overline{e_n^2}$ = 4 kTRs.

Noise contributions for both types of noise due to various segments (piece-wise linear approximation) of the weighting function are shown in the figure (expressions for integrals I_1 and I_3). In these calculations, either the impulse response of the system or the weighting function (its mirror image) can be used for time-invariant systems. ***For time-variant (gated or switched) systems, only a weighting function describes the performance correctly, while an apparent impulse response (waveform at the output) is not correct and can be misleading.*** Steepest parts of the weighting function contribute most to ENC_s, as they correspond to larger bandwidth. Flat parts do not contribute anything. In contrast, ENC_p is largely proportional to the width of the weighting function where it has any significant value.

Eqs. for ENC in Figs. 15-19 provide an insight into the general behavior of signal processing systems with respect to noise. The ENC due to series white amplifier noise is inversely proportional to the slope of the weighting function and therefore proportional to the bandwidth of the system. The ENC due to parallel white noise is proportional to the width of the weighting function and therefore to the overall integration time. If the weighting function form remains constant the ENC due to *1/f* noise is independent of the width of the weighting function, since the ratio of the high frequency cutoff and low frequency cutoff remains constant, Fig. 12. From Eqs. in Figs. 15-19 the optimum width parameter (known as the ***"noise corner time constant")*** of the weighting function is given by,

$$\tau_{opt} = \left(R_s R_p\right)^{1/2} C_{in} \left(A_1 / A_3 \right)^{1/2} ,$$

and it is not affected by *1/f* noise.

A bipolar weighting function, i.e., impulse response h(t), with equal lobes would result in square root of two higher ENC than for a unipolar function (single lobe). If the amplitude of the second lobe is less than one half, its rms noise contribution becomes small (<12%).

The half-order integral I_2 for *1/f* noise is not amenable to such a simple interpretation as for I_1 and I_3, and it will be discussed in Fig. 19.

Fig. 24. Following on the piecewise linear approximation of the weighting function in Fig. 16, a simple relation for the equivalent noise charge (ENC) due to series white noise is derived. It requires knowledge of three parameters: noise spectral density $\boldsymbol{e_n}$, total input capacitance (detector+amplifier) $\boldsymbol{C_{in}}$, and peaking time $\boldsymbol{t_m}$ of the triangle approximating the weighting function. Such an approximation is useful for noise estimation, since the series noise integral for a 5th order semi-gaussian weighting function with the same peaking time differs by only ~10%. In a preamplifier design, the expected $\boldsymbol{e_n}$ can be determined from the operating conditions (current and transconductance) of the first transistor.

Fig. 25. From Fig. 15 simple relations follow for ENC due to parallel shot noise and resistor (thermal) noise. The gated integrator case illustrates that the ENC for shot noise is simply the square root of the variance of a Poisson sequence of impulses counted for a time $\boldsymbol{t_G}$ (e.g., a gated integrator system). By Campbell's theorem the contribution of each impulse to the variance is determined by the weighting function, and for a given weighting function the parallel noise integral $\boldsymbol{I_2}$ has to be determined. For an approximation by a triangle with a peaking time $\boldsymbol{t_m}$, $I_2 = (2/3)t_m$. The parallel noise contribution for the triangular weighting function is the same as for gated integration one third as wide. The contribution by the parallel resistor thermal noise can be compared simply to the shot noise by the "***50 mv rule***": a dc current $\boldsymbol{I_0}$ causing a voltage difference of ~50 mV on a resistor $\boldsymbol{R_p}$ contributes equal amount of noise as the resistor at room temperature.

Fig. 26. Calculation and Estimation of ENC for 1/f Noise.

1/f noise becomes a limiting factor in many physical measurements. We can imagine reducing the series white noise in charge measurements to a very low level by continuing to increase the measurement (integration) time τ, provided the parallel (leakage or dark current) noise is very low. We would eventually reach the "noise floor" due to the *1/f* noise. Once the 1/f noise spectral density is determined experimentally and defined by the parameter A_f in [volts^2] as in Eqs. (5) and (6), ENC can be calculated by integral I_2, Eq. (8). In time domain this is an integral of a fractional-order (half-order) derivative squared of the weighting function (a mathematical operation which cannot be called "trivial" before one learns how to do it, and it can be considered "tedious" at best). In frequency domain the calculation is somewhat easier for time-invariant systems, but for time-variant systems defining the transfer function $H(j\omega)$ is more difficult and less intuitive than determining the weighting function.

We illustrate this here on the example of a commonly used weighting function of trapezoidal form . There are many different hardware implementations of this function in different applications. Time-invariant versions have used delay line clipping and higher order RC prefilters. Gated integrator and higher order prefilters have been used in several applications, starting with germanium gamma-ray detectors [Ref. 9]. This function is widely used with CCDs in astronomy, implemented by correlated double sampling and dual-ramp integration.
We define the trapezoidal weighting function by the width of the ramp τ_p and the flat top as a fraction of the ramp, $\Delta\tau_p$. The equivalent noise charge for *1/f* noise is then,

$$ENC_f^2 = \pi C_{in}^2 A_f A_2 , \quad \text{where}$$

$$A_2 = \int_{-\infty}^{\infty} \left[w^{(1/2)}(t) \right]^2 dt$$

The coefficient A_2 vs the flat top Δ of the trapezoidal weighting function, according to an exact calculation (not reproduced here), is plotted in this figure.
The effect of the series *1/f* noise is lowest for a triangular weighting function, $\Delta = 0$. As the flat top is made longer, A_2 increases, since such a trapezoidal function has a higher ratio of its cutoff frequencies, which results in integrating a wider band of the *1/f* noise spectrum.

Since exact calculations of ENC_f for any weighting function can be time consuming, we emphasize here a simple estimation method, which provides results sufficiently close to the exact calculations for most purposes. It has been pointed out by Gatti *et al.* [42] that the three integrals in Fig.15 have to satisfy Cauchy-Schwartz inequality, which can be expressed in terms of the three weighting function coefficients (i.e., form factors),

$$A_2 \le (A_1 A_3)^{(1/2)}$$

Thus there is an upper limit to A_2 in relation to A_1 and A_3 which are easily calculated from Figs 15 and 16, as illustrated by a simple case of a triangular function in Figs. 17 and 18. A study of the most commonly used weighting functions, reveals that $A_2 / \sqrt{A_1 A_3}$ falls between 0.64 and 0.87, a spread of less than ±8% in the calculation of rms noise, so that for estimation of ***1/f*** noise the following approximate relation can be used,

$$A_2 \approx 0.75 (A_1 A_3)^{1/2}$$

For the trapezoidal weighting function , $A_1 = 2$ and $A_3 = \left(\Delta + 2/3\right)$, and the approximation for this case is,

$$A_2 \approx 0.75 \left[2\left(\Delta + 2/3\right) \right]^{1/2}$$

This approximation is plotted in the figure and it is within a few percent of the exact analytical solution.

In any noise analysis of charge amplifiers one will have already calculated, or otherwise determined the values of A_1 and A_3 , so that ***the information about the filtering (pulse shaping) effect on the series and parallel white noise will also provide an estimate of the 1/f noise***,

$$ENC_f^2 = \pi C_{in}^2 A_f A_2 \approx \pi C_{in}^2 A_f \left(0.75\sqrt{A_1 A_3}\right)$$

It is interesting to note that calculated values are: for a gaussian weighting function A_2=1.00; for a triangular weighting function 0.88; for a 4th order semi-gaussian 1.02; for CR-RC 1.18.

A_f is a parameter resulting from a measured spectral density and it does not contain any specific information about the properties of the amplifying device unless other parameters are known.
For input transistor optimization a parameter which is to the first order independent of the device dimensions is more useful [15], $K_f = A_f C_{GS}$ [joule]. This constant ranges from 10^{-27}J for junction field-effect transistors (JFETs) to ~10^{-25}J for p-channel and ~10^{-24}J for n-channel MOS transistors.

The discussion here was intended to provide some insight: ***ENC_f depends (rather weakly) only on the shape of the weighting function, but not on the time scale***.

Fig. 27. A summary of noise coefficients for some frequently used weighting functions.

Both calculated and approximate values for A_2 are given for comparison. ***ENC*** calculation is straightforward requiring the knowledge of the amplifier series noise spectral density e_n , total input capacitance C_{in} , shot noise contributing (leakage or dark) current I_0, and ***1/f*** noise spectral density parameter A_f .

Figs. 28-31.. ENC vs peaking time for white series, white parallel and 1/f noise.

Figs. 32. Noise corner frequency for ***1/f*** noise and white series noise for an NMOS transistor with a fairly high ***1/f*** noise. Transistor ***1/f*** noise is characterized by the constant K_F, which is independent of the device width and it is dependent on device technology [Refs. 15, 17]. This constant ranges from ~ 10^{-27} for the best JFETs to ~ 10^{-24} for some NMOS devices. The value for A_f is determined from the ***1/f*** spectral density (where the white noise is negligible) multiplied by the measurement frequency.

4. Signal processing, i.e.,"filtering" or "pulse shaping"

Fig. 34. The concept of weighting function is very useful for time domain noise analysis of time variant, sampled and switched systems. The role of "pulse shaping," "signal filtering," or "signal processing" is to minimize the measurement error with respect to the noise, various baseline offsets and fluctuations, and at high counting rates to minimize the effects of pulse overlap or pileup. The term "pulse shaping" implies that the amplifier-filter system is time invariant. In such a system the system parameters do not vary during the measurement, and a single measurement of amplitude or time is performed. Such a system is described completely by its impulse response.
In signal filtering, we also use time-variant methods, such as capacitor switching and correlated multiple sampling of the signal. The filtering properties of a time-variant system are described by its weighting function ***w(t)***. ***The weighting function describes the contribution that a noise impulse, occurring at time t_i, makes at the measurement t_m,*** as illustrated in the figure. It is essentially a measure of the memory of noise impulses (or any other signals) occurring before the observation time t_m. As shown, ***the weighting function for time-invariant systems is simply a mirror image in time of the impulse response, with its origin displaced to t_m.*** For a time-variant system, the impulse response (output waveform) is generally quite different from its weighting function. Time-invariant and time-variant processing could be devised to produce the same result, i.e., both methods will be described by the same weighting function, while their implementation will be quite different. The noise-filtering properties of any weighting function for detector signal processing can be most easily determined by the time domain analysis technique shown in Fig. 16. Such a time domain analysis method was first introduced by Wilson [Ref. 3.], and subsequently elaborated on in [Refs. 5,6,17].

Fig. 35. In general, the ***composite weighting function*** for multiple correlated sampling is obtained by superposition of weighting functions for individual samples. This is illustrated for ***correlated double sampling (CDS)***, a technique commonly used for readout of CCD's and large pixel arrays. Single sample processing is described by a symmetrical triangular impulse response approximating single RC differentiation and one or two RC integrations. The single sample weighting function with respect to the sampling time at t_m is shown (dashed), and it is a mirror image of the impulse response. It is assumed that a (delta function) signal of interest will arrive at time t_{0+}, and produce a response described by the impulse response. In double correlated sampling another sample is taken at t_0, just before the arrival of the signal. This sample, sometimes called "baseline sample", is subtracted from the "signal or measurement sample". The weighting function for the baseline sample is shown inverted and earlier in time by t_m-t_0. The composite weighting function (thicker solid line) is bipolar and it has area balance. This is another way of saying that CDS has zero dc response and that it attenuates (*but does not eliminate*) baseline fluctuations at low frequencies. The ENC can be easily calculated from such a composite weighting function by using the technique for time domain noise analysis shown in Fig. 16. (An analysis of such a case in frequency domain and without the use of composite weighting function is mathematically considerably more time involved).

Fig. 36. An example of some commonly used functions for unipolar and bipolar pulse shaping (left) and their frequency response (right). The unipolar response is achieved with 5 RC integrations and 1 RC differentiation, with RC = 20 ns. The bipolar response is due to 4 RC integrations and 2 RC differentiations (equivalent to a mathematical differentiation of the unipolar response). The noise integrals from figures 13 and 14, $I_1 = A_1/\tau_F$ and $I_3 = A_3\tau_F$, form factors A_1 and A_3, and τ_F = FWHM (approximately equal to zero-to-peak time) are:

	τ_F	I_1 [s^{-1}]	I_3 [ns]	A_1	A_3
unipolar	105	2.2 x 10^7	80	2.3	0.76
bipolar	52	6.2 x 10^7	58	3.2	1.1

Vertical scale for frequency response is in decibels (20 db = factor of 10 in amplitude). The series noise ENC_s^2 is higher for bipolar function of the same width as the unipolar one. As this function has area balance the response at low frequencies is significantly lower, and so is the sensitivity to low frequency baseline fluctuations, pileup and noise. Experimental results show a significant reduction in pileup effects with bipolar (area balanced) weighting functions.

Fig. 37. Impulse response *h(t)* of (a) the optimum filter for amplifier (series) white noise and (parallel) white noise current at the detector electrode. The filter requires a long time to respond. (b) Triangular impulse response optimized in width with respect to the noise corner time constant, given by $\tau_c = C_{in}\left(R_s R_p\right)^{1/2}$. The noise is higher by only 8% compared with the ideal filter. The width of both responses is determined by the noise corner time constant τ_c. The time of the amplitude measurement (peak of the response) is at the origin. (c) Trapezoidal weighting function provides uniform weighting at the flat top to reduce ballistic deficit for signals of finite width. Implemented with a gated integrator [Ref. 9.].

Fig 38. An example of reconstituted waveforms illustrating formation of trapezoidal functions, which can be adapted in their width to the counting rate. The top trace is the digitized preamplifier output with numbered x-ray steps. The middle and bottom traces are the corresponding fast and slow filter outputs. X-ray 1 is adequately isolated, so the slow filter output (with better S/N) is not affected by the subsequent event 2. Pulses 2 and 3 are resolved by the fast filter but pileup in the slow filter. Pulses 4 and 5 pileup in the fast filter, and are rejected on the basis of the fast filter pulse width. The sampling period in asynchronous (uncorrelated) sampling has to be much shorter than the peaking time of the required weighting function. For example, in high resolution gamma-ray spectrometry, 50 ns sampling period may have be used for peaking times in the microsecond range.

An anti-aliasing filter is an essential part of any sampling system. Its function is to limit the bandwidth prior to sampling so as to satisfy the Nyquist sampling criterion: the bandwidth at the output of this filter must be no more than one half of the sampling frequency. If this is not satisfied, the loss in S/N due to aliasing cannot be recovered by any subsequent processing. The role of digital filtering in x-ray and gamma-ray spectrometry is to create optimized weighting functions. In spite of the power of digital processing it is most efficient to cancel any long tails in the detector-preamplifier response by analog means. If the tail cancellation is performed digitally, much larger numbers of samples have to be processed (deconvolved) for each event. For asynchronous (uncorrelated) sampling for semiconductor detectors see [Ref. 19]. For signal processing with multiple synchronous (correlated) samples for liquid argon calorimeters see [Ref. 22].

Fig. 39. A typical anti-aliasing filter (5th 0rder with complex poles) prior to ADC in systems where the final weighting function is formed by digital signal processing. As an example, with a peking time of 1µs, 3db frequeccy is 253kHz. Nyquist criterion would require a sampling frequency of ~500kS/s. A factor of 4 oversampling is provide in this case by a sampling frequency of 2MS/s.

Fig. 40. Autocorrelation function at the output of the anti-aliasing filter (prior to ADC) for $i_{neq}^2 = v_n^2 \omega^2 C^2_{in}$ (1st transistor white series noise), calculated.

5. Charge Amplifier Configuration

Fig. 42. History of the charge amplifier feedback configuration. It was applied ("invented independently") to radiation detectors in the 1950-ies, while the (apparently) first charge feedback amplifier originated in an unrelated application in mechanical engineering in 1948.

Fig. 43. In the most basic charge amplifier feedback configuration only two transistors are essential to realize a complementary cascode. The current sources in positive and negative supplies can be realized by resistors or by low noise transistor current sources. There is only one significant pole (C_oR_o) in this circuit. Higher order poles are given by the unity gain frequency of the transistors used. The cascode alone is an "operational transconductance amplifier" (very high output impedance). With the follower amplifier x1 it becomes an operational amplifier.

<u>Gain and input impedance relations for the feedback charge amplifier configuration .</u> The frequency dependence of the open loop gain is inherent to a high gain single pole amplifier. It is described by two parameters, unity gain frequency $\omega_h = g_m/C_o$, and the gain "roll off" frequency (3 db point) $\omega_l = 1/R_oC_o$. The dc gain is then $|G_o| = \omega_h/\omega_l = g_m \cdot R_o$. g_m is the transconductance of the input transistor, C_o is the dominant pole capacitance and R_o is the dominant pole resistance. Input impedance with capacitive feedback has

two terms, a resistance $R_{in} = 1/\omega_h C_f$ in series with a capacitance $C_f G_o$. The resistance term R_{in}, in conjunction with the total input capacitance, determines the rise time of the detector-amplifier. The rise time constant of the output voltage (i.e., the transfer of charge from the detector capacitance to the feedback capacitance) is $\tau_r = R_{in} \cdot C_{in} = (1/\omega_h)\ (C_{in}/C_f) = (C_o/g_m)\ (C_{in}/C_f)$, where $C_{in} = C_{Det} + C_{ampl}$. The resistive input impedance has a noise corresponding to the amplifier series noise resistance R_{seq}, and it appears as a resistance with a noise temperature, $T_{eff} = T \cdot R_{seq}/R_{in}$. For values of R_{in} higher than R_{seq}, the amplifier can be used as a termination for delay lines with a noise lower than that of a termination with a physical resistor Z_o at temperature T. The noise temperature of the resistance Z_o realized by the capacitance in feedback is $T \cdot R_{seq}/Z_o$, and this is why it can be called "***electronically cooled termination***" or ***"electronically cooled damping",*** [Ref. 11]. The resistance in parallel with the feedback capacitance adds two more terms to the input impedance of the preamplifier: inductance R_f/ω_h in series with a resistance R_f/G_0. It is important to note the condition to achieve an aperiodic ("damped") response of the feedback amplifier.

The feedback configuration allows the ultimate in noise performance because the parallel noise sources can be made negligible by using a transistor with a very low gate leakage current and a very high feedback resistance (megaohms to gigaohms). The feedback resistor can be avoided altogether by the use of optoelectronic feedback or a transistor switch to maintain amplifier voltages in the operating range. Signal integration is performed on the feedback capacitance C_f. The long tail can be cancelled in subsequent pulse shaping by a simple pole-zero cancellation circuit (not shown in the figure). Pulse shaping at the preamplifier by reducing R_L or R_f would result in increased noise from the thermal noise of these resistors. The object of the design is to avoid dissipative components at the detector-amplifier input and thus to make R_f as large as possible.

Fig. 44. Overview of white noise sources in an NMOS transistor normalized to the intrinsic channel series noise resistance γ/g_{ms}. The gate induced noise contribution with capacitive sources, such as is the case for most radiation detectors, is usually negligible. In particular, at operating conditions to minimize the power in the input transistor, the optimum ratio C_{gs}/C_{in} is small. The contributions by the gate resistance and substrate resistance can be made small by the device design.

Fig. 45. All type of amplifying devices have fluctuations in their channel current associated with their gain mechanism. *Intrinsic (white) noise*, although from a different mechanism for each device type, can be expressed by the transconductance in terms of the equivalent noise resistance.

Fig. 46. In addition to the noise (fluctuations in the drain current) associated with the gain mechanism, there may be additional noise sources indicated in the figure.

Fig. 47. Transfer of charge from detector to amplifier.

In all cases where the amplifier is connected directly to the detector via a resistive conductor the charge produced by ionization is distributed among the detector capacitance, amplifier capacitance and any stray capacitance according to the ratio of capacitances. Due to this, only a fraction of the charge of interest (the signal) arrives where it matters – that is to the conduction channel of the input transistor where it controls the drain (collector) current. (An exception to this is if the two capacitors are connected by an inductor in which case the charge is transferred periodically between the two capacitors.) In case of a CCD the ionization charge is moved peristaltically in a potential well formed and driven by appropriate clock voltages applied to the gate electrodes. The charge shifted a few hundred (or thousand) times arrives at the collection electrode ("floating diode") which is connected to a source follower. In the CCD the charge arriving at the collection electrode is the original charge packet produced by ionization except for a few electrons lost to trapping. The charge transport in a conductor is by a small displacement of a large number of free electrons. CCD principle allows multiple measurements on the same charge packet .
Optimization of the signal to noise ratio requires appropriate matching of the transistor active capacitance (which controls the current) to all other capacitances connected to the input – a subject addressed in the section on ASIC design.

As mentioned above charge coupled devices (CCDs) make possible by their principle an additional degree of freedom in the processing of their signals. There is a fundamental difference in the treatment of charge produced by ionization (or photo emission) between the devices based on ***charge transfer*** and all the detectors based on ***collection of charge***. Collection of charge allows only "one look" at the charge, no matter for how long (weighting function width to optimize the noise). Charge transfer allows a charge packet to be moved back and forth in the proximity of the sense electrode, making possible "multiple looks" at the induced charge, i.e., a repetitive measurement. If we impose the same total measurement time on both types of measurements (single long time vs repetitive short times) the result for ENC due to the series white noise will be the same. However, the ENC for ***1/f*** noise will be reduced in the repetitive measurement. We know that due to the scaling invariance of ***1/f*** noise, a single measurement is independent of the shaping (integration) time, as the filter passband moves up or down the ***1/f*** spectrum, while ***the ratio of the upper and lower cutoff frequency remains constant***. In contrast, in the repetitive measurement, averaging of samples taken at a frequency f_0 performs ***narrowing of the bandpass*** around the repetition frequency. The higher the repetition frequency, the lower is the ***1/f*** spectral density for each sample. This method made possible the lowest read noise achieved in a CCD readout of less than ***1 e rms***, [Ref.35].

Fig. 48. Matching of the Input Transistor to the Detector – series white noise.

7. Fluctuations on a Capacitance and Charge Measurement Sensitivity – kTC Noise

Fig. 50. Integration of the power spectrum (spectral density) arising on a capacitance from the thermal noise of a resistor results in the total fluctuation of charge (and voltage), which is independent of the value of the resistance ***R***. The resistance (with the capacitance ***C***) determines the bandwidth of the noise. The ***kTC*** charge noise is quite high even on small capacitances. Most of this noise does not affect the measurement in systems where filtering and a very high parallel (feedback) resistance can be used. Such a system "looks" at the portion of the spectrum where the spectral density is very low. An example: high resolution x-ray spectrometry with silicon detectors. When the measurement is performed directly on the detector capacitance and the filtering is not possible, the full ***kTC*** noise is included in the measurement, and it can be reduced only by correlated double sampling - if applicable, as discussed in *Fig. 44*.

The equipartion theorem of statistical mechanics, assigns a fluctuation energy of $(1/2)k_BT$ to each degree of freedom of a system in thermodynamic equilibrium, equal to $(1/2)(\ \ \xi/\ \ )$ on a capacitance, giving the same result as the RC circuit calculation (integration of the entire noise spectrum). The equipartition theorem does not imply that there is a resistance in the circuit.

Fig. 51. Charge and Voltage Total Fluctuations on Capacitance at 300K

Fig. 52. Transient behavior of noise, after circuit parameters have been changed by switching, can best be studied by applying Campbell's theorem, as shown in the figure. The oscillogram shows build up of noise (multiple traces) after switching a white noise source onto an RC circuit. Such a build up occurs after a reset switch across a capacitor is opened.
This is illustrated some more in *Figs. 43 and 44*.

Fig. 53. This illustrates more completely what happens with ***kTC*** noise in active pixel sensors and CCDs. While the reset switch is closed the ***kTC*** noise extends to very high frequencies corresponding to the very short time constant $r_{ON}C$. When the switch is "opened" the time constant increases by many orders of magnitude. A value of the "old" ***kTC*** noise is stored on the capacitance, and it decays very slowly with this very long time constant. At the same time the "new" ***kTC*** noise builds up also very slowly, but faster than the stored value decays. From this, one can see the conditions under which correlated double sampling may reduce significantly the ***kTC*** noise: ***Sample 1 may be taken any time between opening of the reset switch and the arrival of the signal. Sample 2 may be taken any time after the arrival of the signal but before the "new" kTC noise has built up.*** The noise in this case is often referred to erroronously as the "reset noise", even though its origin is not in the reset action.

Fig. 54. A note on kTC noise.

Fig. 55. Some general remarks on ***kTC*** noise:

1. *Fluctuation-dissipation theorem* with Nyquist's expression for thermal noise is essential for calculation of noise spectra and for detailed information on noise sources.
2. *Equipartition theorem* provides no detailed information, but provides a *check on the integrals* of noise spectra (the total fluctuation).
3. *Transient behavior* of noise in switched capacitor circuits and matrix readout pixel arrays is best understood by means of *Campbell's theorem*, which provides *noise variance vs time*, as shown in *Figs. 40*.
4. A complete charge reset and charge transfer by a switch result in $\sigma_q^2 = k_B TC$, independently of the switch ON resistance. This noise can be subtracted only ***if the first sample in the CDS is taken before the signal.***
5. Transfer (i.e., direct transport) of charge without switching (as in a CCD) does not result in $k_B TC$ noise. ***Reset of the sense amplifier does.***

8. Noise from Dielectrics

Fig. 57. Thermal fluctuations in dielectrics generate electric noise the magnitude of which is related to the loss conductance of the dielectric by the dissipation-fluctuation theorem. This noise was first measured in charge amplifiers and analyzed in [Refs. 7 and 8]. For a dielectric with low losses, the dissipation factor is a constant over the frequencies of interest,

$$D = G(\omega)/\omega C_D ,$$

where $\boldsymbol{G(\omega)}$ and $\mathbf{C_d}$ are the loss conductance and the capacitance of the dielectric as measured on an impedance bridge at an angular frequency $\boldsymbol{\omega}$. The conductance $\boldsymbol{G(\omega)}$ generates a noise current at the frequency $\boldsymbol{\omega}$, according to Nyquist's formula,

$$\overline{i^2(\omega)} = 4kT\, G(\omega) df = 4kT\, (D\, C_D)\omega$$

This current is converted into a noise voltage on the input capacitance,

$$\overline{v^2(\omega)} = (4kT\, D\, C_D/\omega)\, (1/C_{in}^2)$$

The lossy dielectric generates an $|f|$ noise current spectrum in parallel with the input, which integrated on the input capacitance becomes $1/|f|$ noise. The equivalent noise charge due to this noise can be calculated by integrating the noise voltage at the output of the filter with respect to frequency and comparing it to the signal output. One obtains for the equivalent noise charge,

$$(ENC)^2 \approx 2.4\, kT\, (D\, C_D) .$$

An interesting characteristic of the dielectric noise is that its contribution is independent of both the input capacitance (except for the capacitance of the dielectric) and the filter time constant. It is also weakly dependent on the type of the filter (weighting function, see Fig. 26). In cases where the dielectric and/or its capacitance are not known, it is more convenient to use the loss conductance as measured on an impedance bridge at an arbitrary frequency $\boldsymbol{f_o}$ in the range of interest. Then,

$$DC_D = G(f_o)/2\pi f_o \quad .$$

Such noise arises in conventional transistor and IC plastic packages with relatively high losses. The noise contributions of these packages at 295°K have been found to range from about 25 rms electron charges for the very best to more than 100 rms e for the worst. A reduction by a factor of 2 to 3 in the rms equivalent noise charge was observed at 125°K. Glass fiber (G10, Fr4) circuit boards have relatively high dielectric losses (D~2%).

A stray capacitance of ***1pF*** of a trace on such a board at ***293 K*** contributes $\boldsymbol{ENC_D \sim 80\text{-}90}$ ***rms e!***

Clearly, detector-amplifier connections should be on low loss dielectrics (e.g., Teflon board; or Rogers RT/duroid), and the stray capacitance should be minimized.
Insulating materials even in the vicinity of the input lead should be kept to a minimum, as their noise is coupled capacitively to the input.

Calculation of the total fluctuation for complex networks (electrical and mechanical) shows that it (the integral of the noise spetrum) is given by the equipartition theorem, i.e., ENC^2=kTC

Fig. 59. Cocluding remarks

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Appendix

Fig. 65. ***A .1. Noise Calculation : Time Domain and Frequency Domain,***

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Fig. 66. ***A.2. Parallel Noise due to Dark Current in Devices with Avalanche Gain***

. *Important to note*: If we measure a dark current $\boldsymbol{I_0}$ from an avalanche photo diode, then the shot noise spectral density is not $\overline{i^2} = 2eI_0$ **,** but rather, $\overline{i^2} = 2eI_0 \cdot M$. Consequently, the $\boldsymbol{ENC^2}$ is magnified by the avalanche gain M .

Fig. 67. ***A.3. Noise Figure vs Noise Voltage, Noise Current and Noise Temperature***

Characterization of amplifier noise in terms of the noise figure applies to resistive signal sources and not to capacitive ones.

Fig. 68. ***A.4. Noise in Resistors at Different Temperatures and "Electronic Cooling" by Feedback***

The total fluctuation (by equipartition theorem) is a function of the temperature of dissipative components, and the effective temperature for a combination of resistors at different temperatures is easily determined. We have seen in *Fig.36* that a resistance can be realized by capacitive feedback around a transconductance amplifier (the basic charge amplifier configuration), $R_2 = R_{in} = (1/g_m)(C_0/C_f)$. The noise associated with this apparent resistance arises from the amplifier equivalent series noise resistance. It can be shown that the effective noise temperature $\boldsymbol{T_2}$ of $\boldsymbol{R_2}$ is given by [*Ref. 11*],

$$T_2 = (R_{na}/R_2)T_1 \ ,$$

where $\boldsymbol{R_{na}}$ is the amplifier equivalent series noise resistance at temperature $\boldsymbol{T_1}$.
The total fluctuation is then reduced by a factor determined by the value of the resistance to be achieved by feedback in relation to the amplifier series noise resistance.
Such a resistance can be used as "electronically cooled" damping or delay line termination with a lower noise than with a physical resistor. Since the "cooling" is achieved by using an active device, such a system is not considered to be in thermal equilibrium.

Fig. 69. ***A.5. Zero-Crossing Statistics of Noise***

. Knowledge of noise zero-crossing rate is needed in self-triggered systems when the detection threshold has to lowered to increase the detection sensitivity until the noise counts exceed a desired limit. As shown, the zero-crossing rate is defined by the second moment of the noise frequency spectrum. Due to this the zero crossing rate is affected by the shape of the spectrum as it approaches its high frequency cutoff. For an $(RC)^2$ low pass filter applied to white noise, the zero crossing rate equals the 3db cutoff frequency. For a uniform spectrum up until an abrupt (or high order) cutoff at $\boldsymbol{f_h}$, the zero crossing rate is $n_{zc+} = f_h/\sqrt{3}$. A discriminator level crossing rate ("noise counts") is determined from the gaussian distribution, as shown in the figure. At ~5 times the rms noise, the level crossing rate is reduced by more than 5 orders of magnitude from the zero-crossing rate.

Figs. 70-71. ***A.6 Noise Autocorrelation Function as a Diagnostic Tool***

Calculation of correlation functions for more sophisticated filters than the CR-RC filter becomes tedious and the expressions are rather involved. In such cases, as well as in cases where the noise spectrum is not exactly known, measurement of correlation functions might be simpler or necessary. A method is described here which requires no additional equipment except an oscilloscope.

It is known from random noise theory that the ensemble average value $\overline{X}(r)$ of a large number of samples, each of them taken at time $\boldsymbol{\tau}$ after the noise waveform has crossed some fixed level $\boldsymbol{X_o}$, is given by the correlation function,

$$\overline{X}(r)/X_o = k(\tau) = K(\tau)/K(0) \quad .$$

The correlation function can, in turn, be interpreted as the mean of the conditional probability density function that the noise will have value $\boldsymbol{X = X_o k(\tau)}$ *at time* $\boldsymbol{t = \tau}$, if it had value $\boldsymbol{X_o}$ at time $\boldsymbol{t = 0}$.

It follows from the above that if a trigger signal is derived for the time base of an oscilloscope, each time the noise crosses some predetermined level X_o - both with positive and negative slope - the mean value of the recorded oscillogram would represent the correlation function of noise. The variance of that mean value is given by

$$\sigma_k^2 = K(0) - K^2(\tau)/K(0) = \sigma^2[1-k^2(r)] \quad .$$

As the correlation function $K(\tau)$ approaches zero the variance of the mean approaches the variance of the noise. Therefore, to make the amplitude of the observed correlation function high compared to σ_k, trigger level X_o should be set high. However, the number of crossings of that level decreases as a Gaussian function of $X_o/\sqrt{2}\sigma$, where σ is the rms value of noise, see *A.4* and *Fig. 64*. It was found that for $X_o/\sigma \sim 4$ *the number of* X_o crossings is large enough for observation and recording of noise in a short time.

Fig. 72. ***An Example of Noise Autocorrelation Measurement by Digital Oscilloscope***

While with an analogue oscilloscope the mean value of the (auto) correlation function has to be estimated by eye, as in [*Ref. 41, which also gives further references*], modern digital oscilloscopes perform averaging of noise waveforms, and a function with negligible fluctuations is obtained. This figure shows an example of autocorrelation functions as a function of the peaking time for systemresponse as in Fig. 39. At 0.5µs white series noise after a semigaussian filter is dominant. At longer peaking times, the contribution to ENC by series 1/f noise and parallel white noise becomes more pronounced.

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SEMICONDUCTOR TECHNOLOGY AND ELEMENTARY CIRCUIT CONFIGURATIONS

Christophe de la Taille

Front-End electronics

IEEE NSS-MIC short course

Christophe de LA TAILLE

OMEGA microelectronics group
Ecole Polytechnique & CNRS IN2P3
http://omega.in2p3.fr

Organization for Micro-Electronics desiGn and Applications

Outline

1. Basics on front-end electronics : charge preamps
2. High speed designs : sipm readout
3. More insights on design and technology : pixel readout

Lectures for physicists, not electronics engineers => will concentrate on front-end and performance of detector, not on detailed engineering

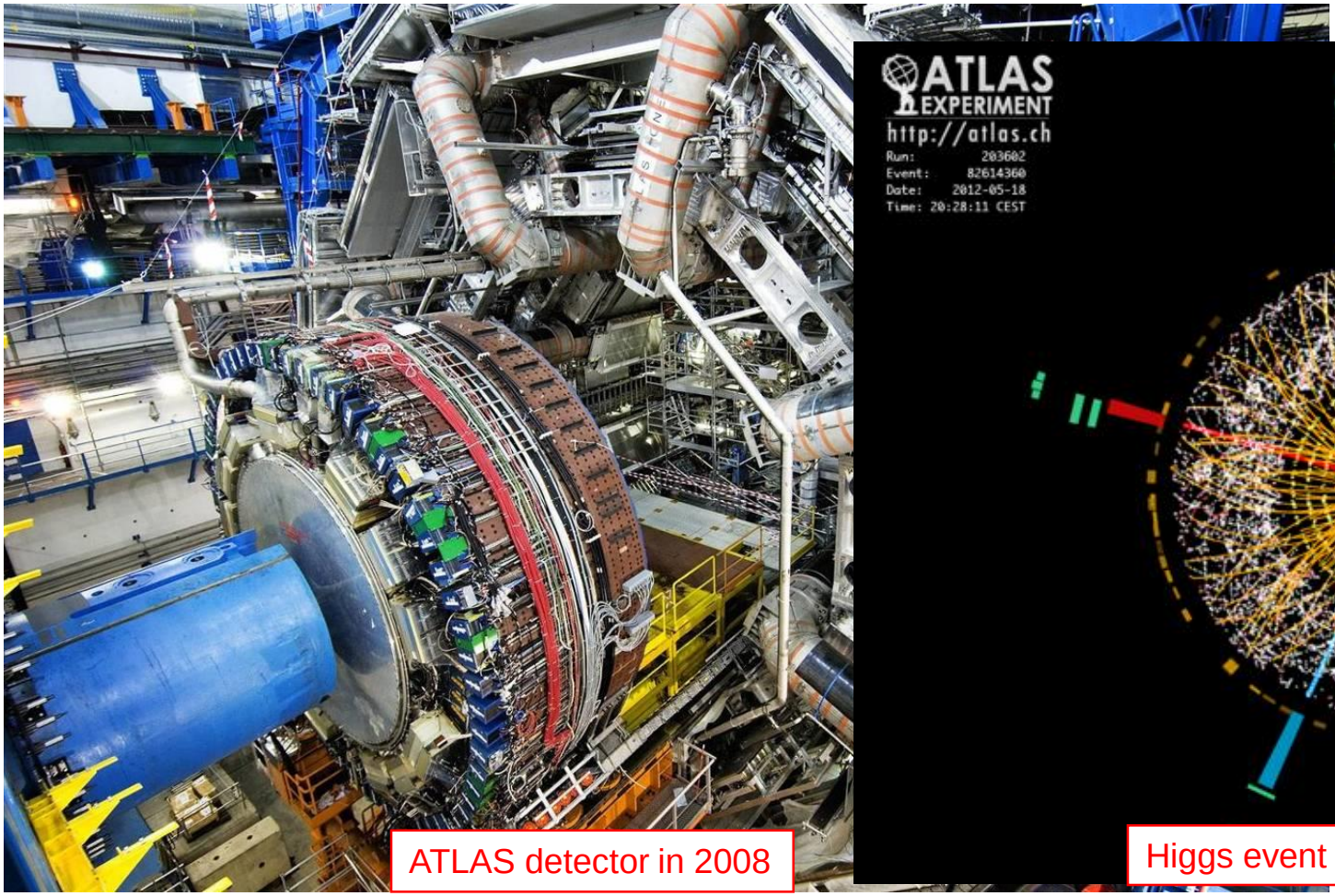
Many more slides than allocated time : don’t be afraid !

I will skip many details : they are for further reference

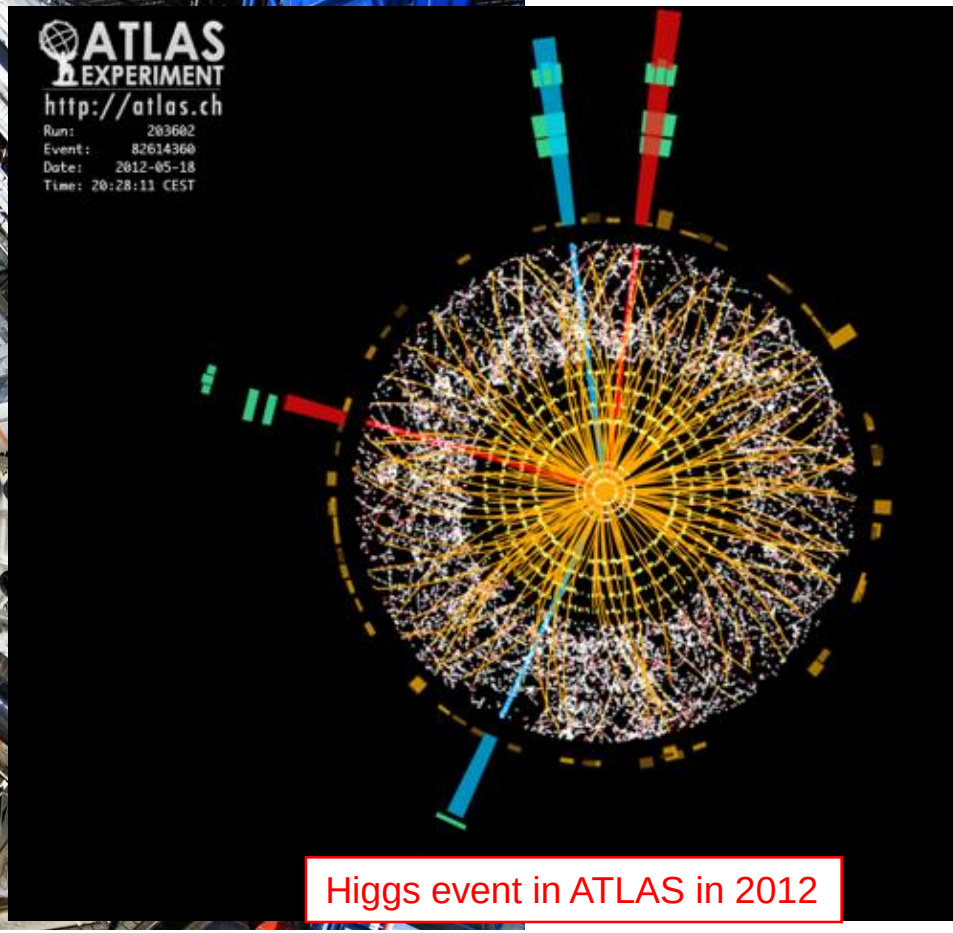
No prerequisites needed (apart from R=U/I)

Electronics in experiments

- A lot of electronics in the experiments…
  - The performance of electronics often impacts on the detectors
  - Analog electronics (V,A,A…) / Digital electronics (bits)



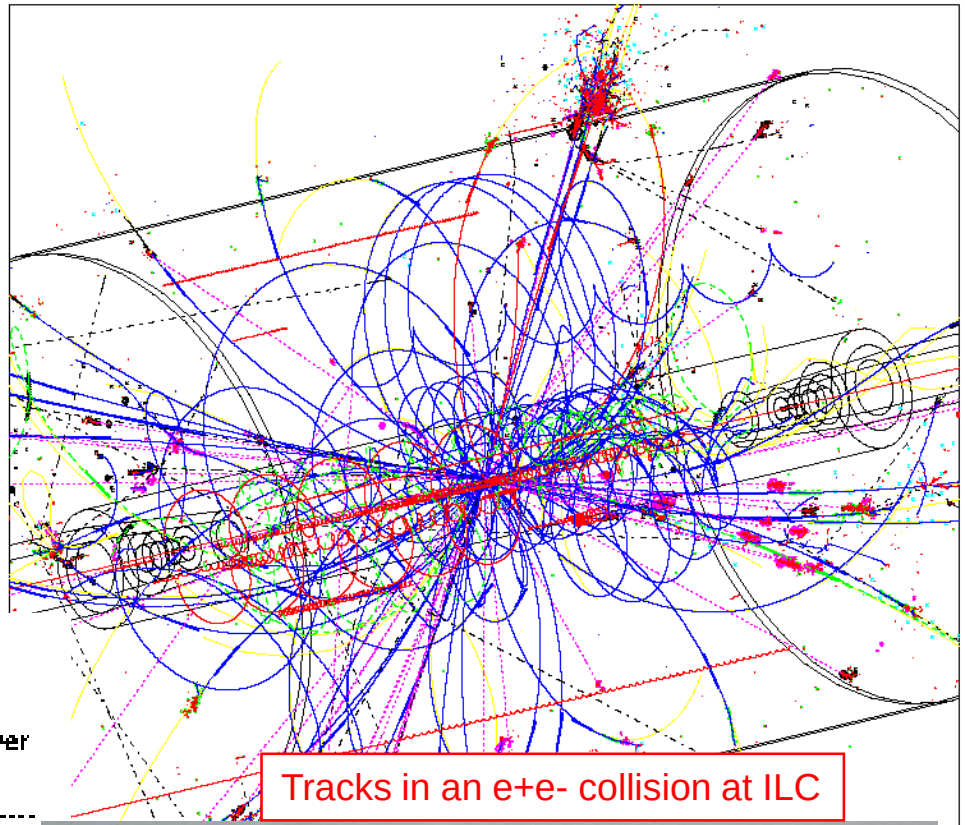
ATLAS detector in 2008



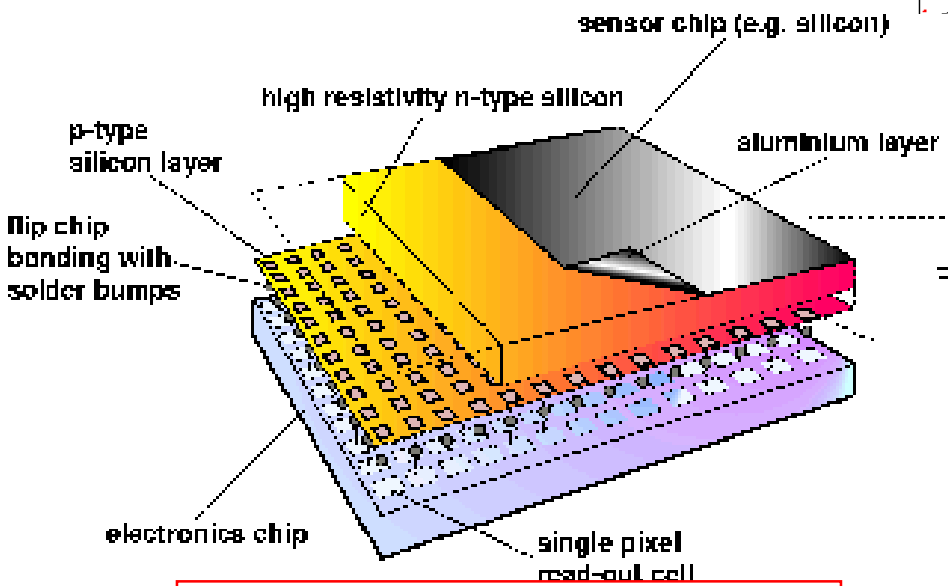
Higgs event in ATLAS in 2012

Electronics enabling new detectors : trackers

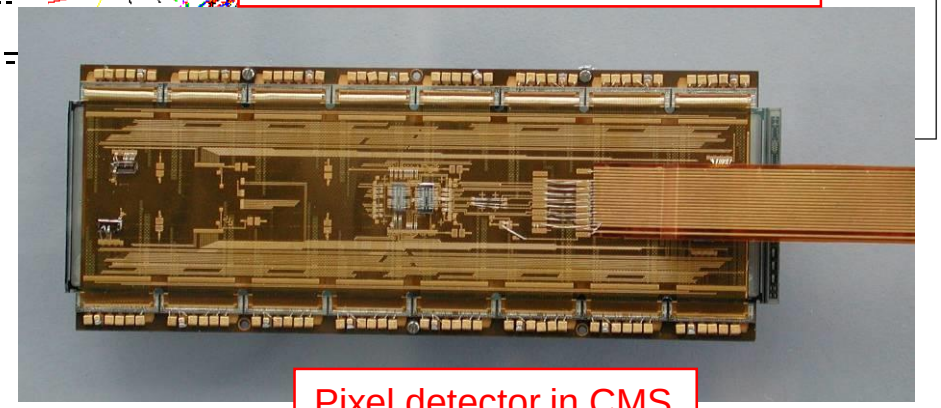
- Measurement of (charged) particle tracks
  - millions of pixels (~100 µm)
  - binary readout at 40 MHz
  - High radiation levels
  - Made possible by ASICs



Tracks in an e+e- collision at ILC



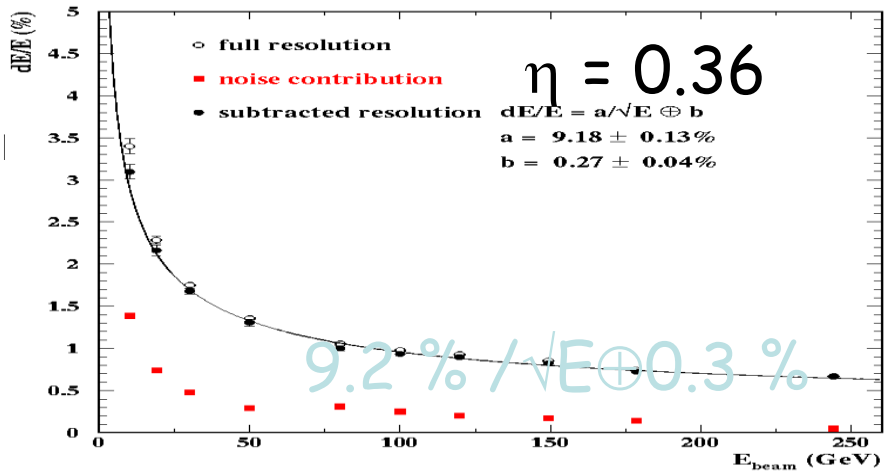
Pixel detector and readout electronics



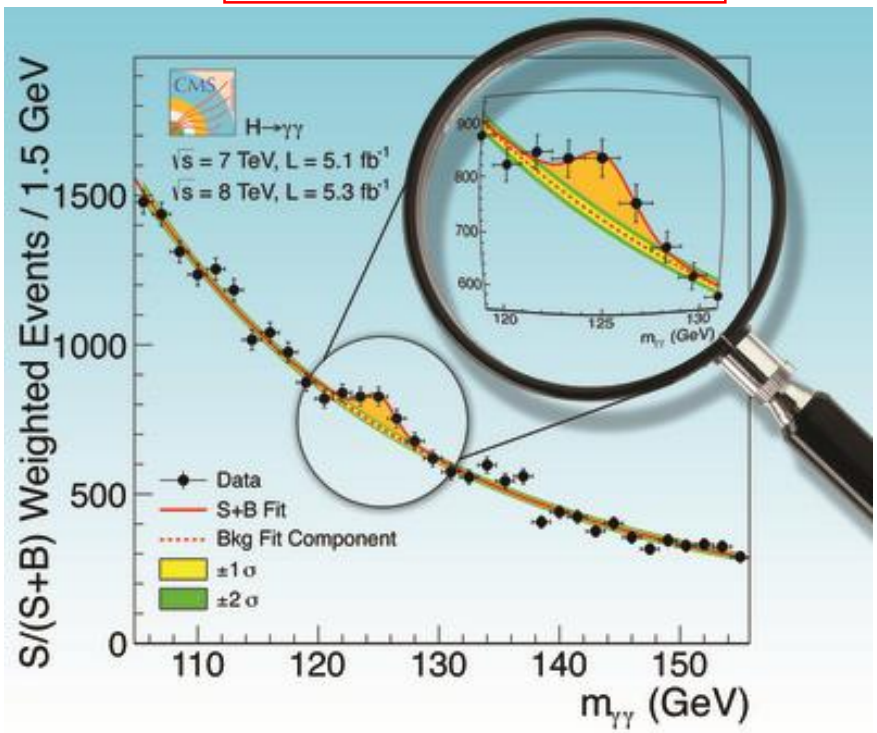
Pixel detector in CMS

Importance of electronics : calorimeters

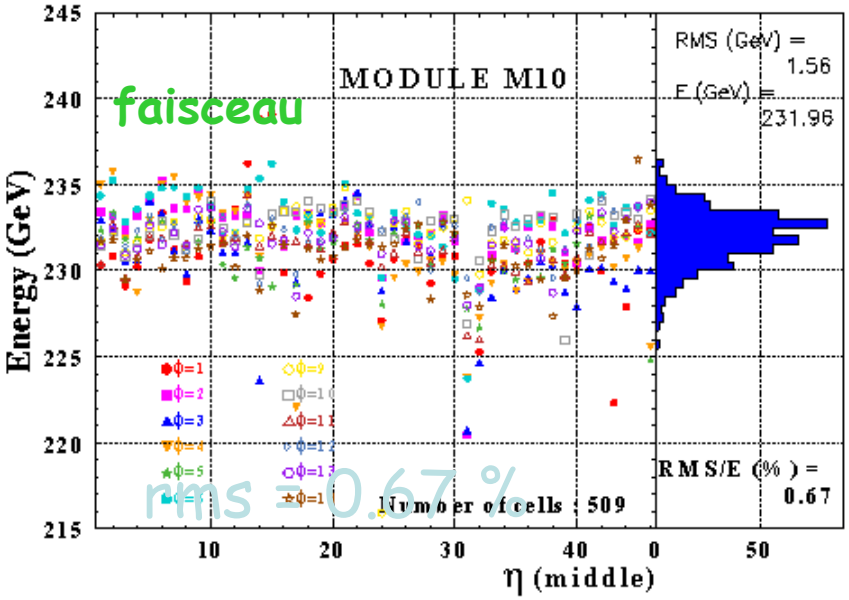
- Large dynamic range (10^4-10^5)
- High Precision ~1%
  - Importance of low noise, uniformity, li
  - Importance of calibration



H -> γ γ in CMS calorimeter

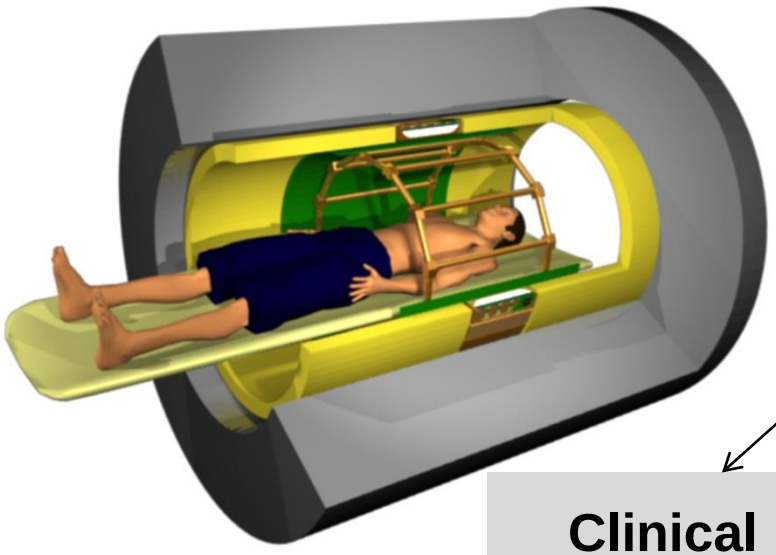


Energy resolution and uniformity in ATLAS



Societal applications : PET

© P. Fischer, Heidelberg University



PET Ring / Scanner

Clinical PET
(Whole Body PET)

Preclinical PET
(Animal PET)

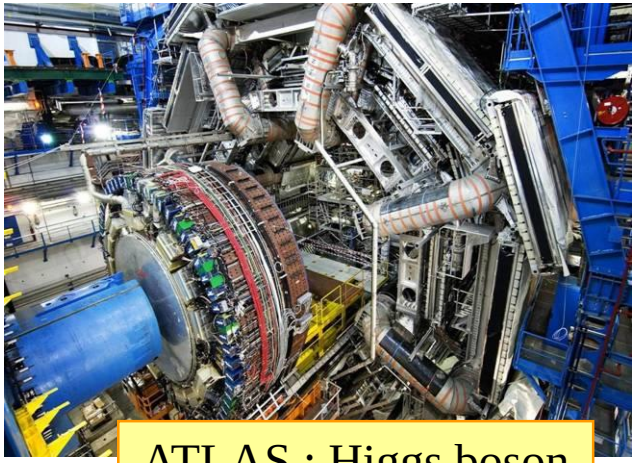
- For humans

- large diameter FOV (>60 cm)
- spatial resolution: **few mm**
- time resolution CRT< **400 ps** for ToF
- high sensitivity (low dose) ➔ large area
- high total data rate

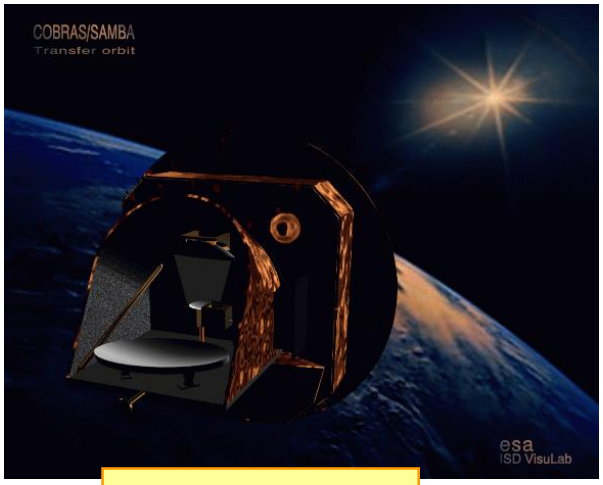
- For mice, rats, rabbits (& human brain)

- Small diameter FOV (4-15 cm)
- spatial resolution: **< 1 mm**
- time resolution only for coinc. (few ns)
- medium sensitivity
- Depth - of - Interaction desirable to fight parallax effect

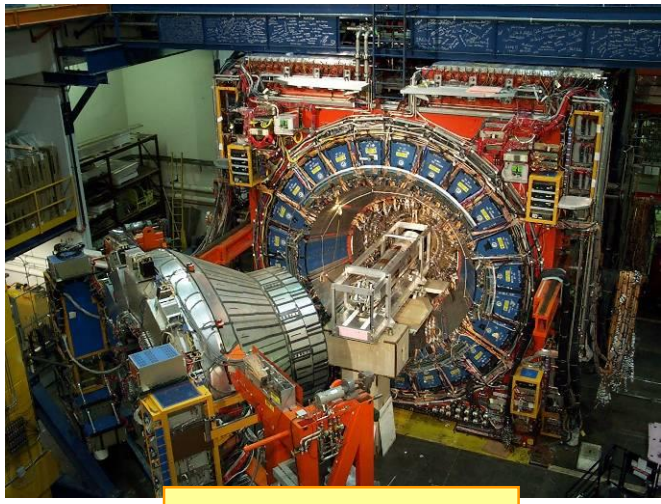
A large variety of detectors…



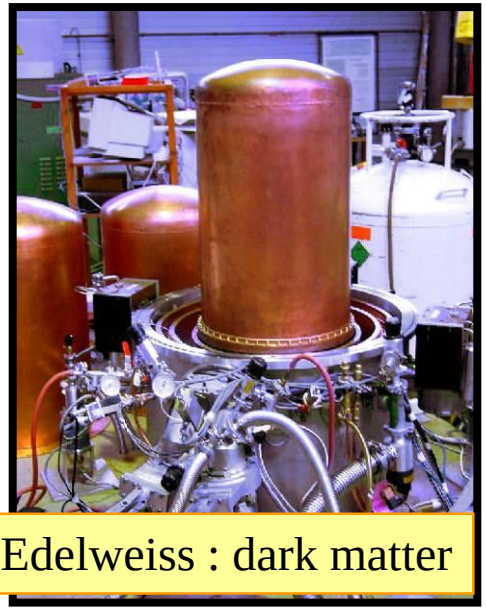
ATLAS : Higgs boson



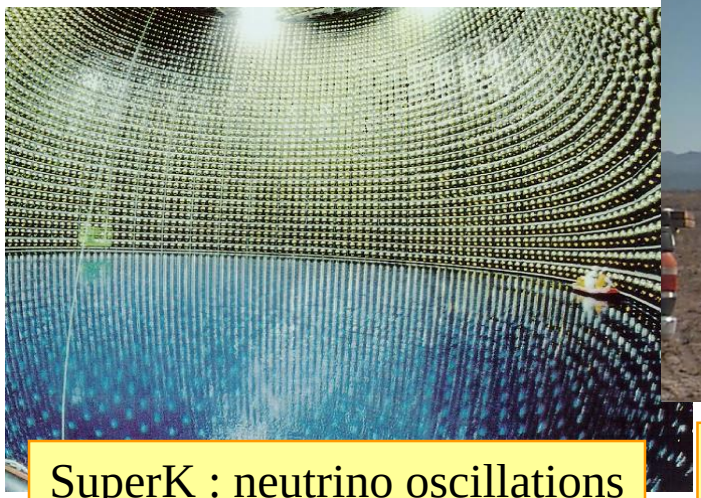
Planck : CMB



CDF : top quark



Edelweiss : dark matter

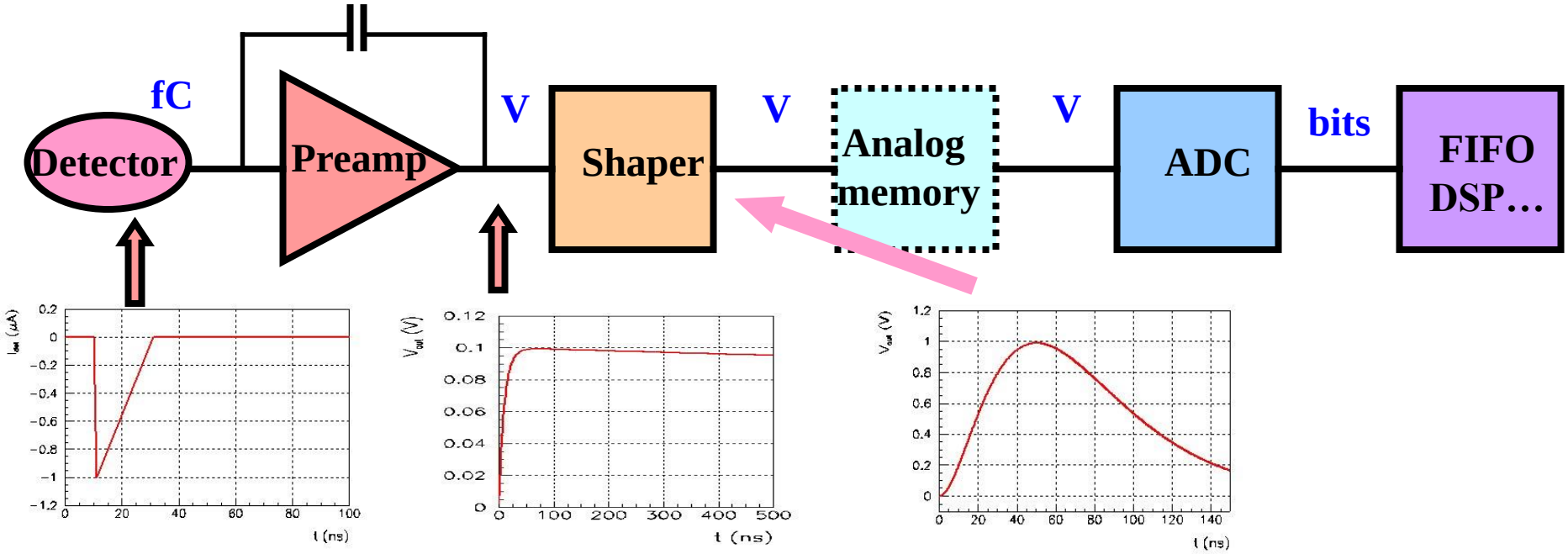


SuperK : neutrino oscillations

AUGER : cosmic rays 10^{20}eV

Overview of readout electronics

- Most front-ends follow a similar architecture



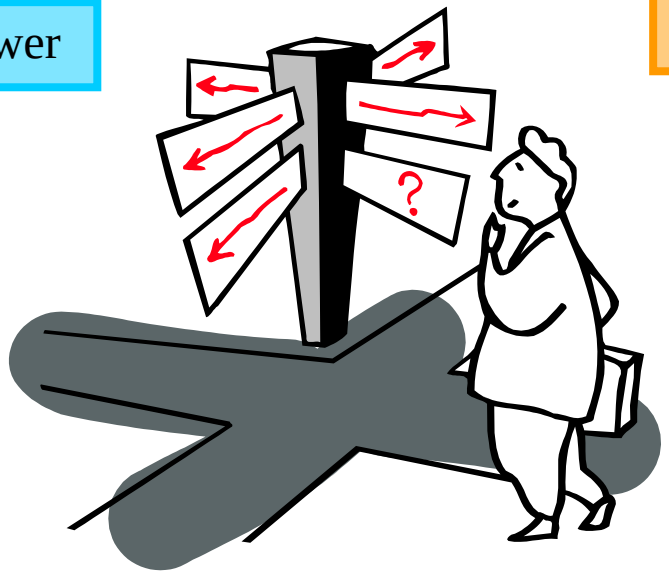
- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels
- Trends : high speed, low power

Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

Radiation hardness

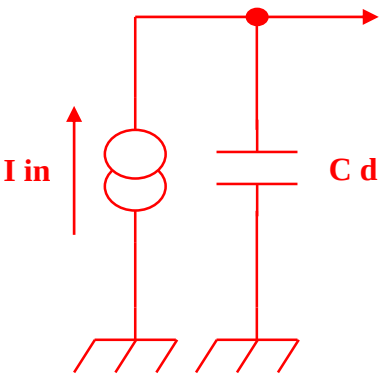
Low cost !

(and even less)

Low material

Detector modelization

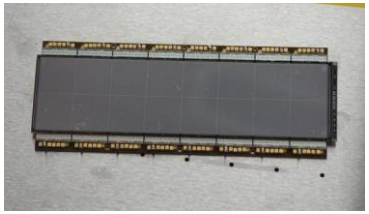
- Detector = capacitance Cd
  - Pixels/strips : 0.1-10 pF
  - PMs/SiPMs : 3-300 pF
  - Ionization chambers 10-1000 pF
  - Sometimes effect of transmission line



Detector modeilization

- Signal : current source
  - Pixels : ~100e-/µm
  - PMs : 1 photoelectron -> 10^5-10^7 e-
  - Modelized as an impulse (Dirac) : $i(t)=Q_0\delta(t)$

- Missing :
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration…



CMS pixel module

ATLAS LAr calorimeter

Signal & Source modelization (cf part 2)

Vacuum Photomultipliers

$G = 10^5 – 10^7$

Cd ~ 10 pF

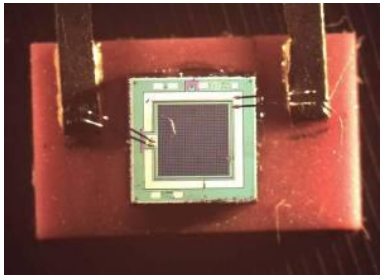
L ~ 10 nH

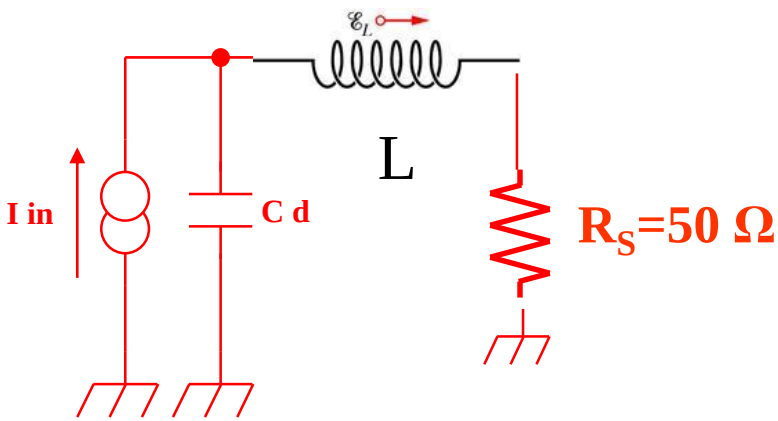
Silicon Photomultipliers

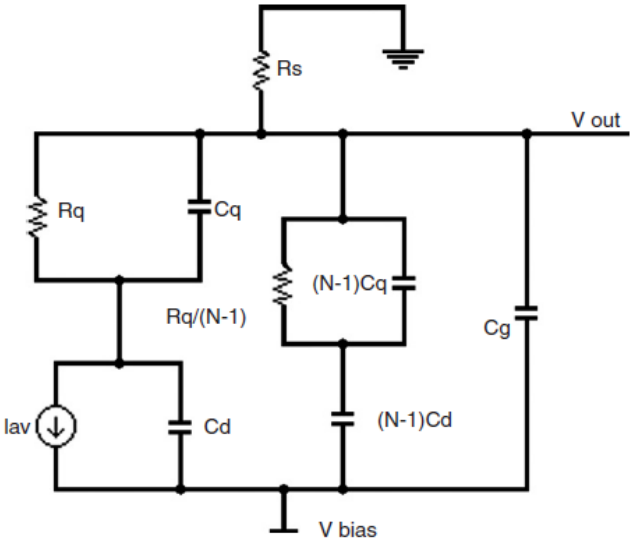
$G = 10^5 – 10^7$

C = 10 - 400 pF

L = 1 – 10 nH







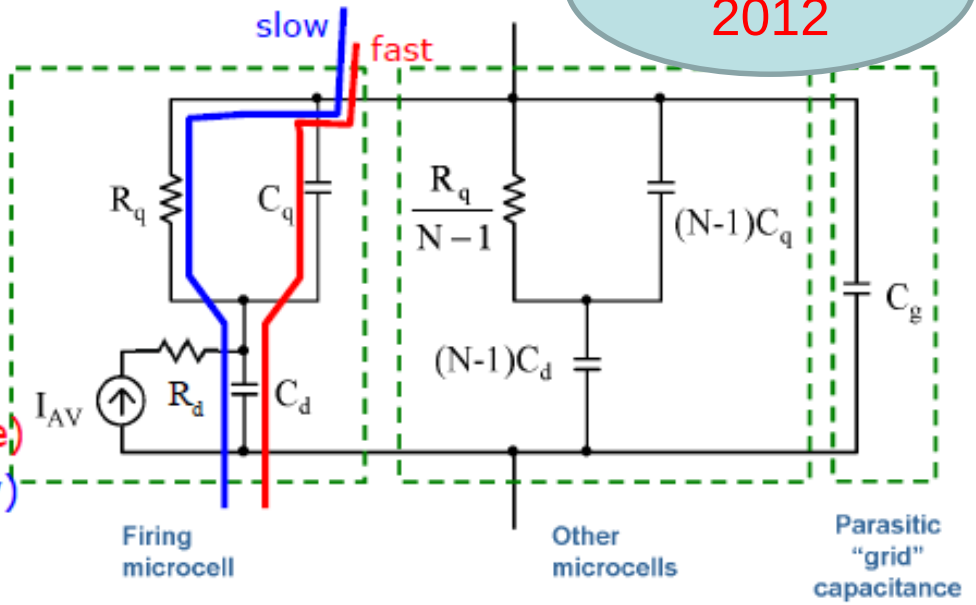
Optimizing signal shape for timing

Collazuol 2012

Single cell model → $(R_d||C_d)+(R_q||C_q)$
SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

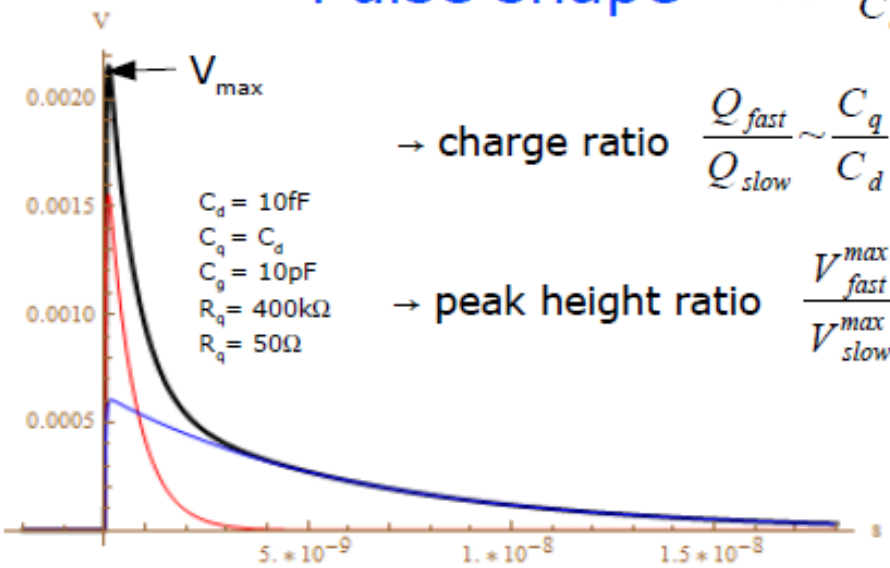
Signal = slow pulse ($\tau_{d\ (rise)}, \tau_{q\text{-}slow\ (fall)}$) +
+ fast pulse ($\tau_{d\ (rise)}, \tau_{q\text{-}fast\ (fall)}$)

- $\tau_{d\ (rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-}fast\ (fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-}slow\ (fall)} = R_q\ (C_q+C_d)$ (slow; cell recovery)



Pulse shape

$$V(t) \simeq \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right)$$



→ charge ratio $\frac{Q_{fast}}{Q_{slow}} \sim \frac{C_q}{C_d}$

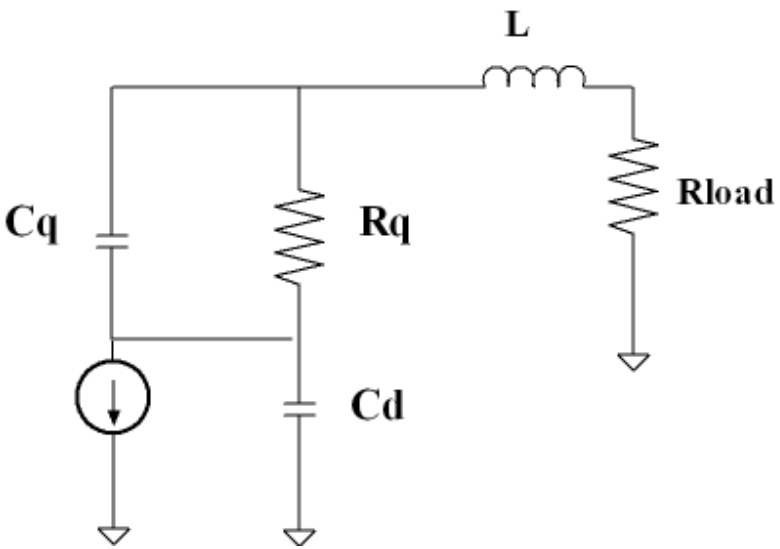
→ peak height ratio $\frac{V^{max}_{fast}}{V^{max}_{slow}} \sim \frac{C_q^2 R_q}{C_d C_{tot} R_{load}}$

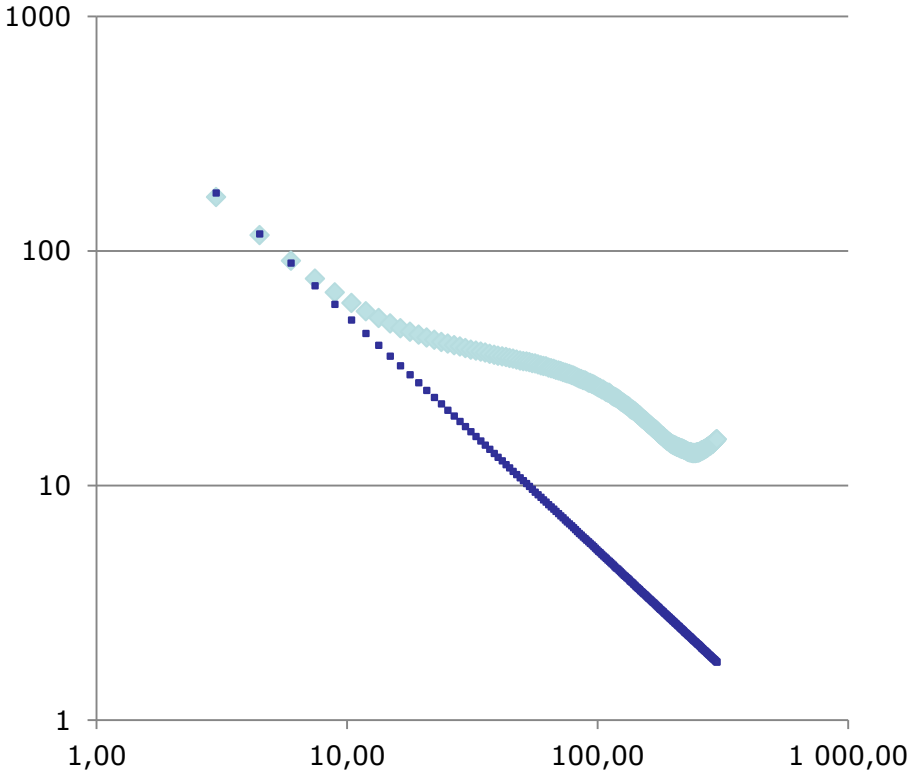
increasing with Rq and $1/R_{load}$ (and Cq of course)

Increasing C_q/C_d or/and R_q/R_{load}
→ spike enhancement
→ better timing

SiPM impedance and model

- RLC too simple, inaccurate at high frequency
- CdRqCqLR OK
  - May better explain HF noise behaviour

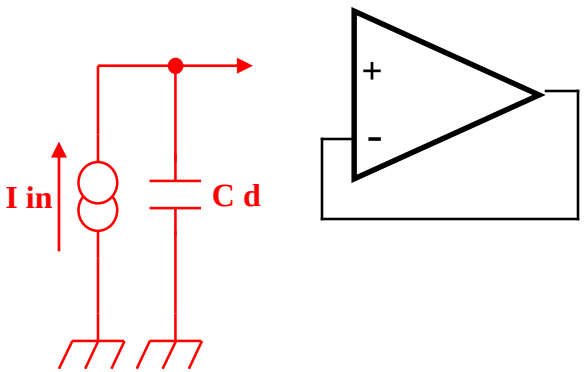




Measured impedance
MPPC HPK 3x3 mm
Line : C = 320 pF

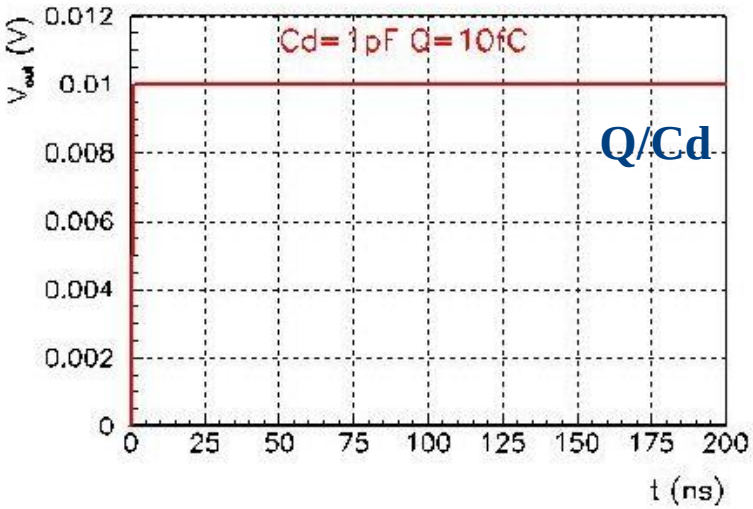
Reading the signal

- Signal
  - Signal = current source
  - Detector = capacitance C_d
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC



- Integrating on Cd
  - Simple : $V = Q/C_d$
  - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
  - Need a follower to buffer the voltage… => parasitic capacitance
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty Cd…

Voltage readout

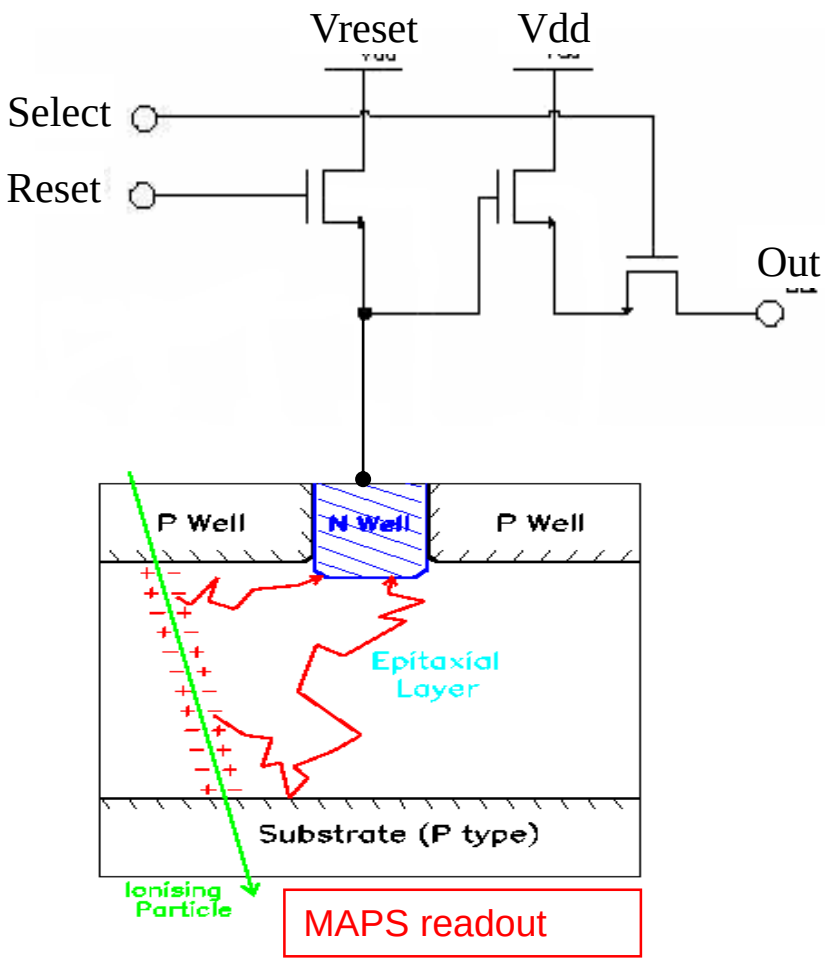


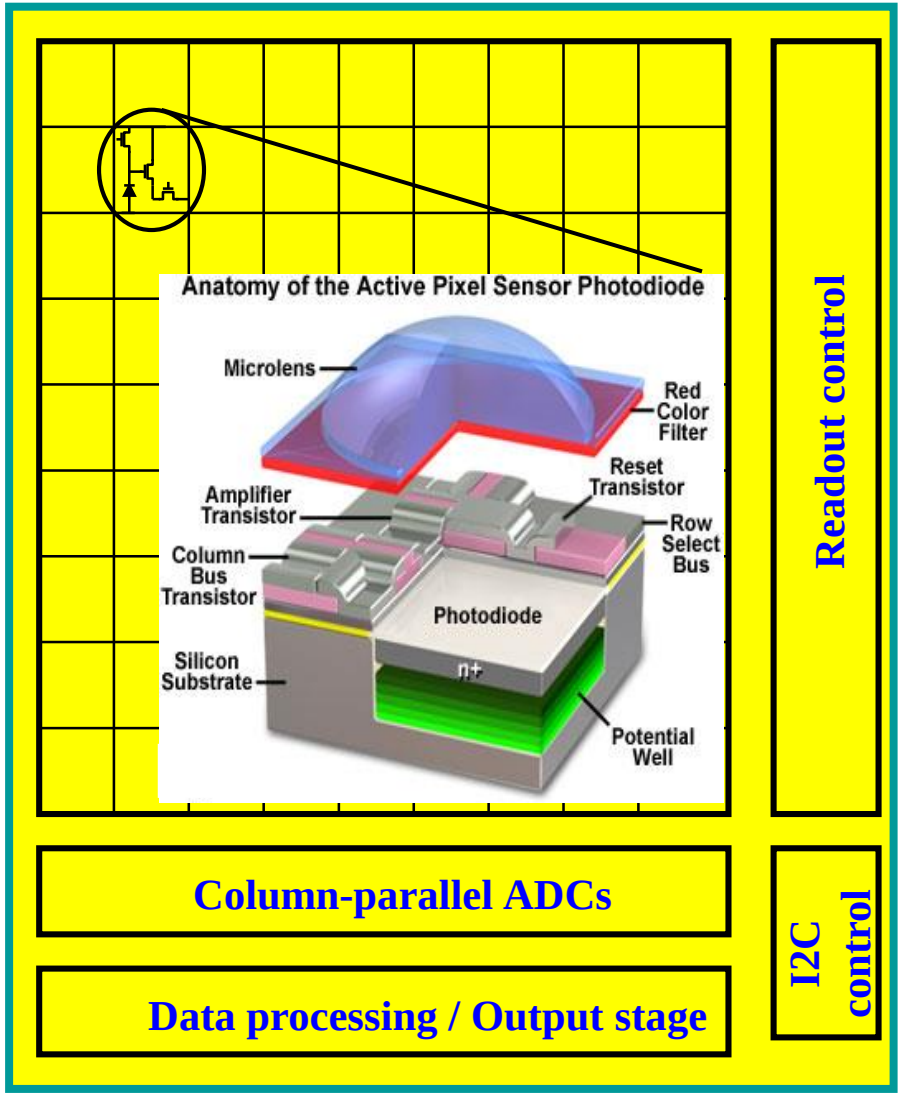
Impulse response

Example : Monolithic active pixels

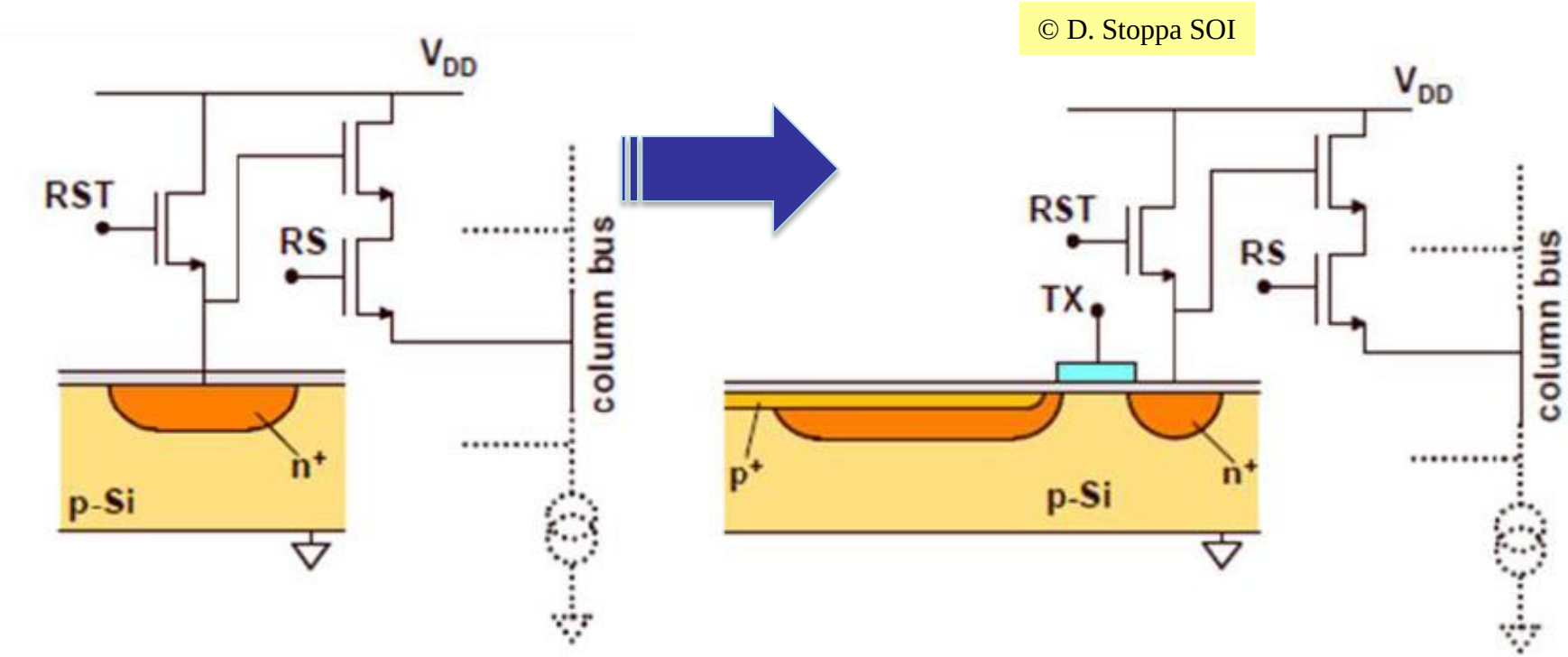
© R Turchetta RAL

- Epitaxial layer forms sensitive volume (2-20μm)
- Charge collection by diffusion
- Read ~100 e- on Cd~10fF = few mV





CMOS Image sensor technology

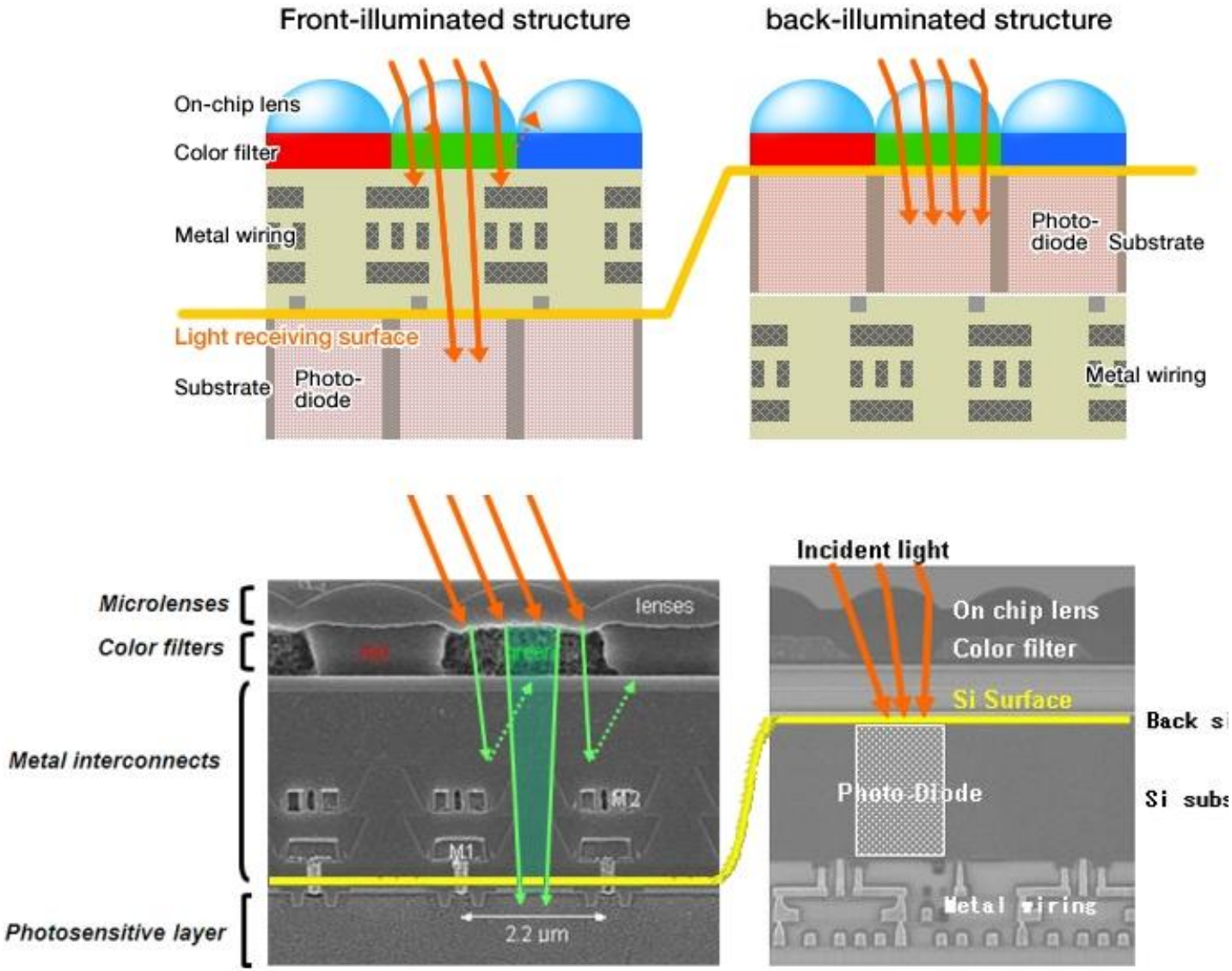


http://indico.cern.ch/conferenceTimeTable.py?confId=170595#20120917

Pinned photodiode:

- 1/10 dark current
- Integration capacitance is small (floating diffusion)
- Correlated-Double-Sampling -> no more kT/C
- Sharing of in-pixel electronics

CMOS sensor technology



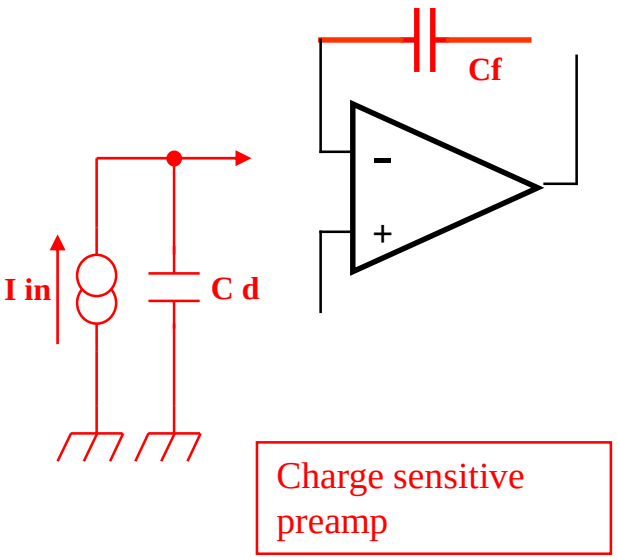
- 65nm CMOS-CIS, Pinned photodiode:
- Pixel pitch <**1.1um**
- Global shutter, **DR>80dB**
- Extra pixel-level circuitry (8um pitch)
- Rolling shutter, **DR>140dB**
- In-pixel Buried SF, High-Gain Column Amplifier and CMS:
- **PN<0.7e**
- Special Column-level ADCs:UHDTV,
- 3**3Mpixel@120fps**

Ideal charge preamplifier

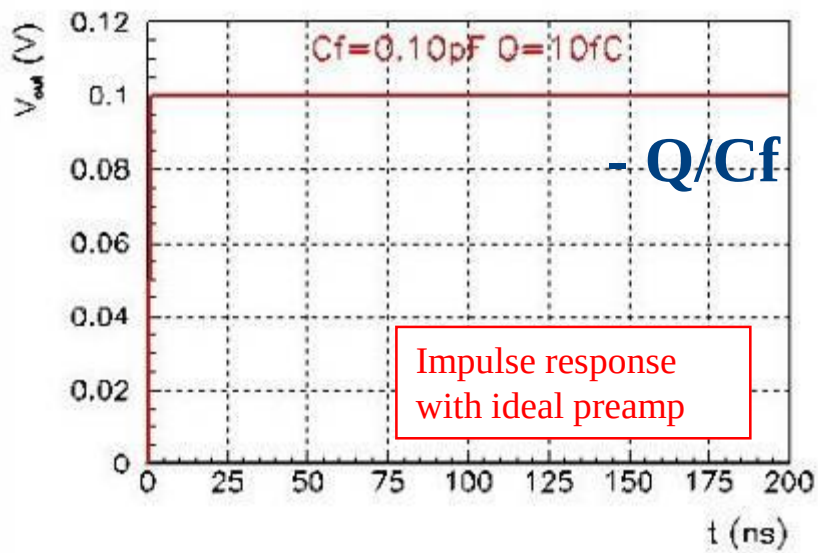
- ideal opamp in transimpedance
  - Shunt-shunt feedback
  - transimpedance : v_{out}/i_{in}
  - Vin-=0 =>$V_{out}(\omega)/i_{in}(\omega) = - Z_f = - 1/j\omega C_f$
  - Integrator : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

$$\boxed{v_{out}(t) = - Q/C_f}$$

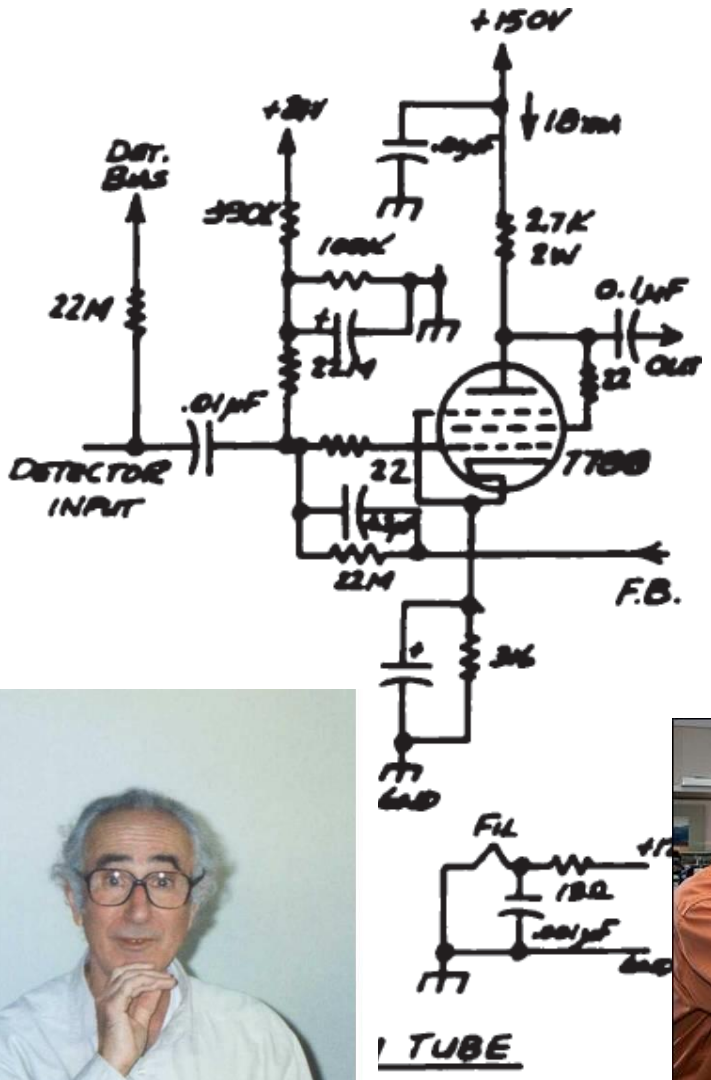
  - « Gain » : $1/C_f$: 0.1 pF -> 10 mV/fC
  - C_f determined by maximum signal

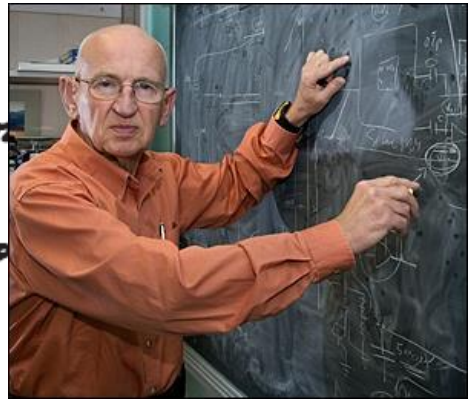


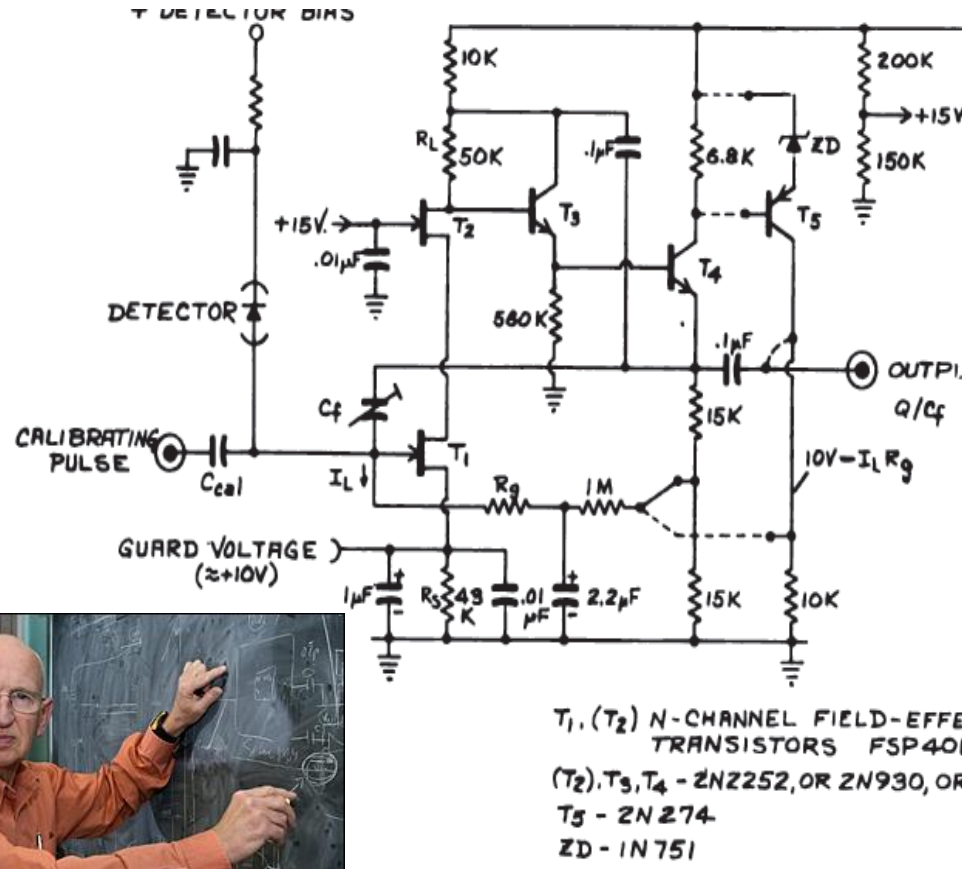
- Integration on Cf
  - Simple : $V = - Q/C_f$
  - Unsensitive to preamp capacitance C_{PA}
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics
  - But always built with custom circuits…



New developments in charge preamps (1963)



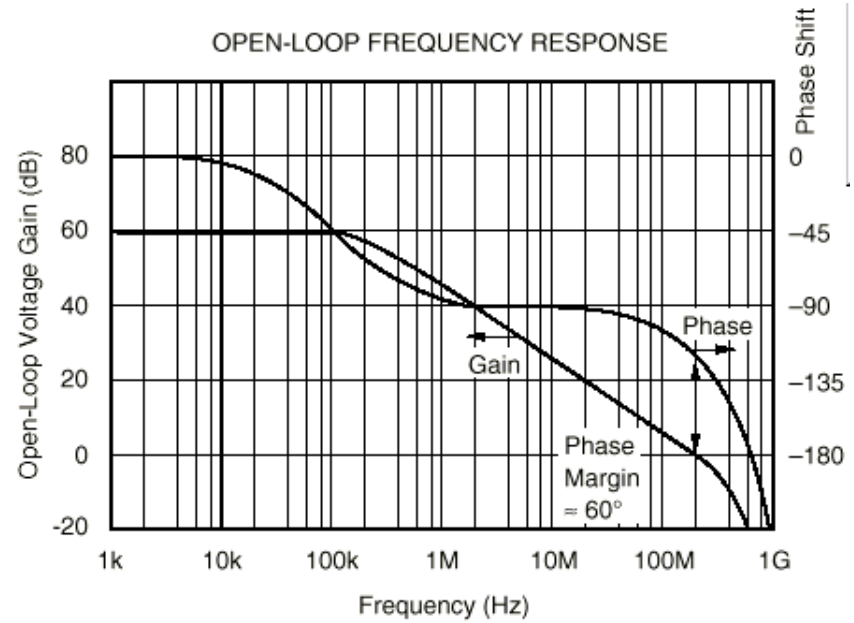


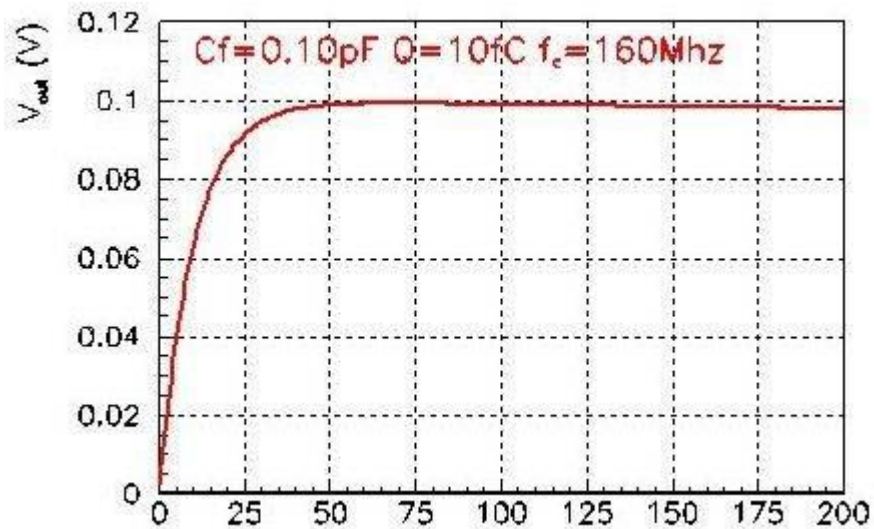


Radeka's preamp (Monterrey 63)

Preamp speed

- Finite opamp gain
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + C_d / G_0 C_f)$
  - Small signal loss in $C_d/G_0C_f << 1$ (ballistic deficit)
- Finite opamp bandwidth
  - First order open-loop gain
  - $G(\omega) = G_0/(1 + j\ \omega/\omega_0)$
    - G_0 : low frequency gain
    - $G_0\omega_0$: gain bandwidth product
- Preamp risetime
  - Due to gain variation with ω
  - Time constant : τ *(tau)*
  - $\tau = C_d/G_0\omega_0C_f$
  - Rise-time : $t_{10\text{-}90\%} = 2.2\ \tau$
  - Rise-time optimised with $w_{C\ or}\ C_f$





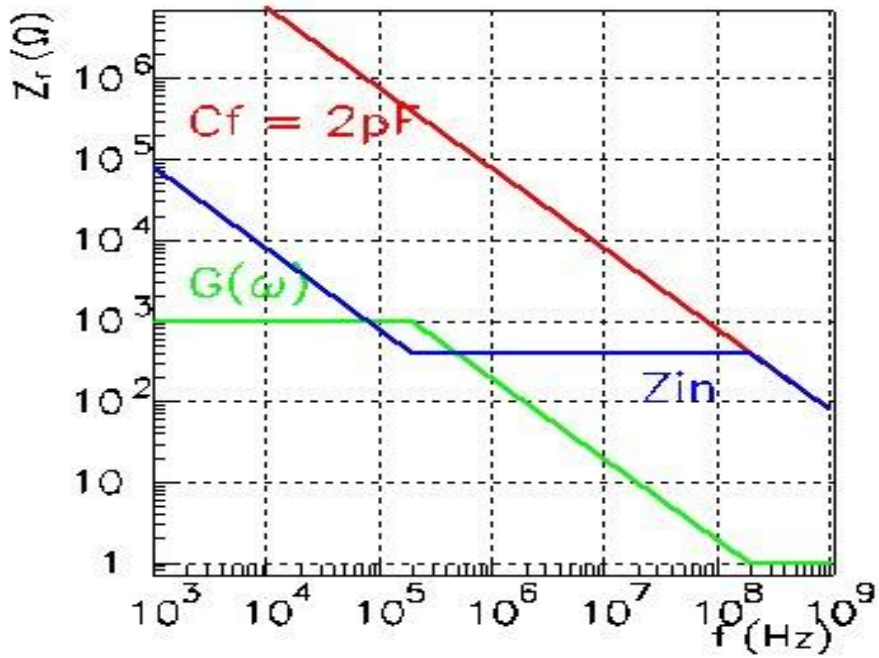
Impulse response with non-ideal preamp

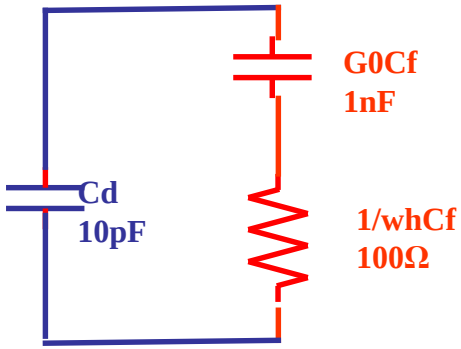
Charge preamp seen from the input

- Input impedance with ideal opamp
  - Zin = Zf / G+1
  - Zin->0 for ideal opmap
  - « Virtual ground » : Vin = 0
  - Minimizes sensitivity to detector impedance
  - Minimizes crostalk

- Input impedance with real opamp
  - Zin = $1/j\omega\, G_0 C_f + 1/\, G_0 \omega_0\, C_f$
  - Resistive term : Rin = $1/\, G_0 \omega_0\, C_f$
    - Exemple : $w_C = 10^{10}$ rad/s C_f= 1 pF => Rin – 100 Ω
  - Determines the input time constant : $t = R_{eq} C_d$
  - Good stability= (…!)
  - Equivalent circuit :

Input impedance or charge preamp





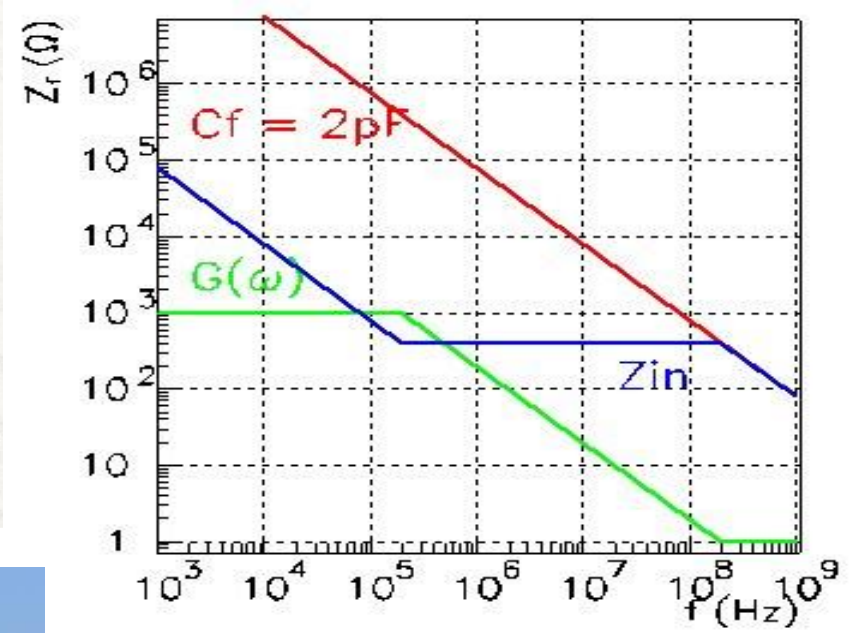
Electronically cooled resistors [TNS 73]

SIGNAL, NOISE AND RESOLUTION IN POSITION-SENSITIVE DETECTORS*

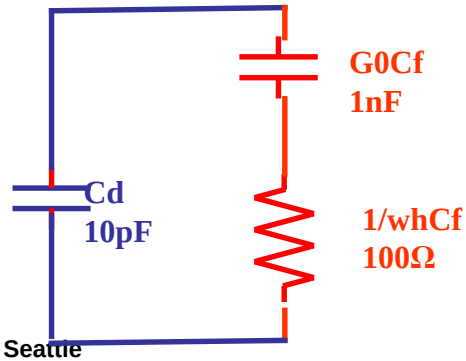
V. Radeka
Brookhaven National Laboratory
Upton, N. Y. 11973

ABSTRACT

An analysis is presented of signal, noise and position resolution relations for some of the most interesting position-sensing methods. "Electronic cooling" of delay line terminations is introduced in order to reduce noise in the position-sensing with delay lines. A new method for terminating transmission lines and for "noiseless" damping which employs a capacitance in feedback is presented. It is shown that the position resolution for the charge division method with resistive electrodes is determined only by the electrode capacitance and not by the electrode resistance, if optimum filtering is used.



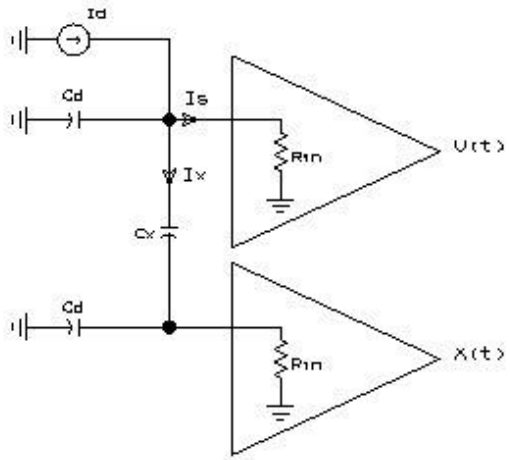
$$Zin = 1/j\omega\, G_0 C_F + 1/\, G_0 \omega_0\, C_F$$



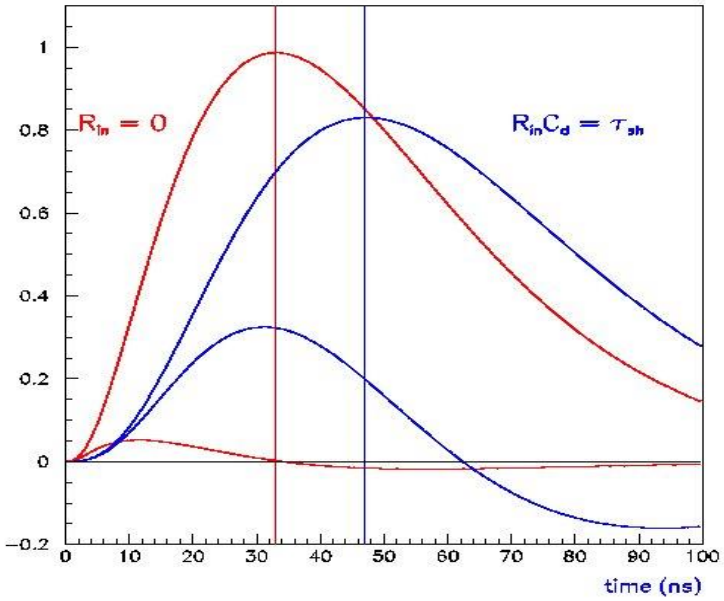
Crosstalk

- Capacitive coupling between neighbours
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to Cx/Cd and preamp input impedance
  - Slowed derivative if RinCd ~ tp => non-zero at peak

- Long distance crosstalk
  - Inductive/resistive common ground return
  - References impedance
  - Connectors : mutual inductance



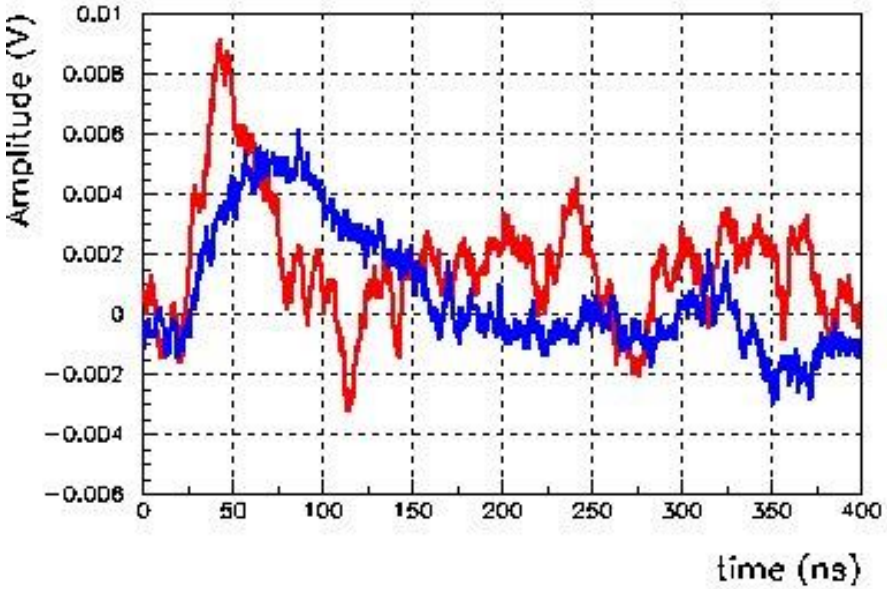
Crosstalk electrical modelization



Electronics noise

- Definition of Noise
  - Random fluctuation superposed to interesting signal
  - Statistical treatment

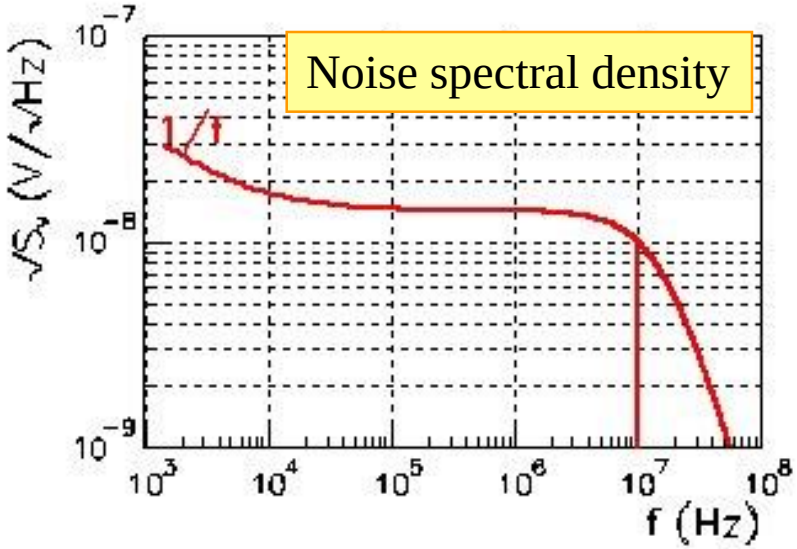
- Three types of noise
  - Fundamental noise (Thermal noise, shot noise)
  - Excess noise (1/f …)
  - Parasitics -> EMC/EMI (pickup noise, ground loops…)

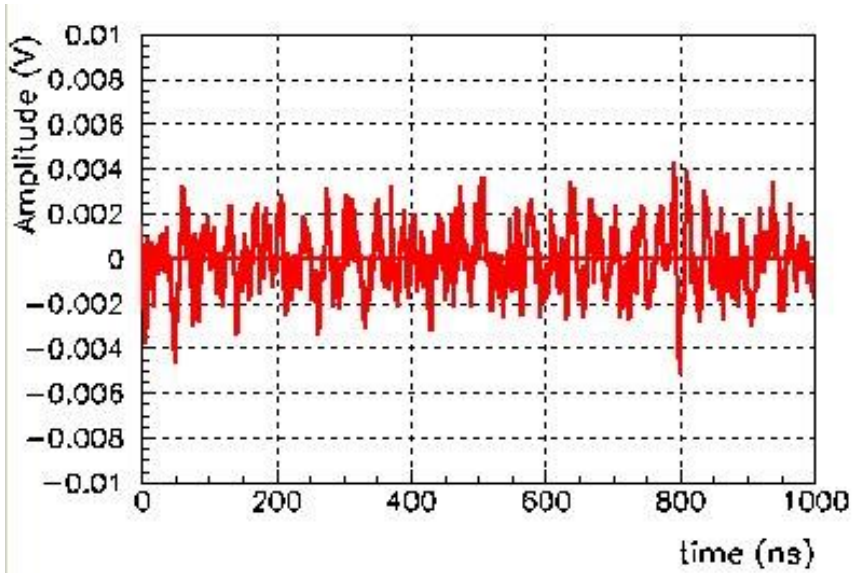


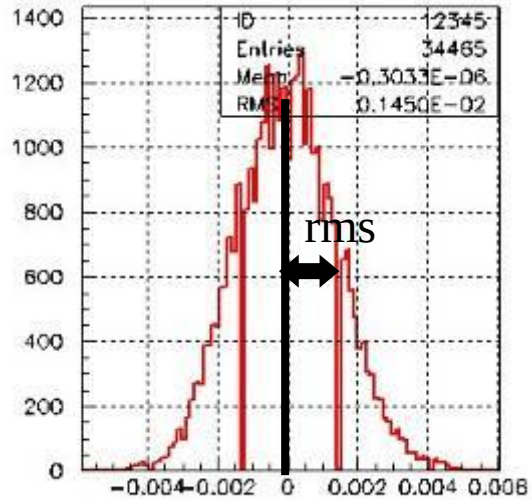
Electronics noise

- Modelization
  - Noise generators : e_n, i_n,
  - Noise spectral density of e_n & i_n : $S_v(f$
  - $Sv(f) = |\mathcal{F}(e_n)|^2$ (V^2/Hz)

- *Rms* noise Vn
  - $V_n^2 = \int e_n^2(t)\,dt = \int Sv(f)\,df$
  - White noise (e_n) : $v_n = e_n \sqrt{\frac{1}{2}\pi f_{-3dB}}$



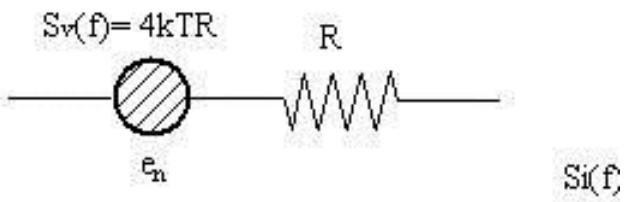




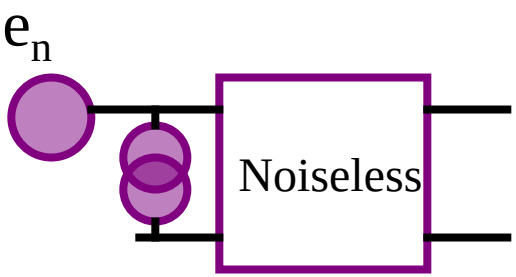
Rms noise vn

Calculating electronics noise

- Fundamental noise
  - Thermal noise (resistors) : Sv(f) = 4kTR
  - Shot noise (junctions) : Si(f) = 2qI



- Noise referred to the input
  - All noise generators can be referred to the input as 2 noise generators :
  - A voltage one e_n in series : series noise
  - A current one i_n in parallel : parallel noise
  - Two generators : no more, no less…



- **To take into account the Source impedance**

- **Golden rule :**
  - **Always calculate the signal before the noise**
    what counts is the signal to noise ratio

Noise generators referred to the input

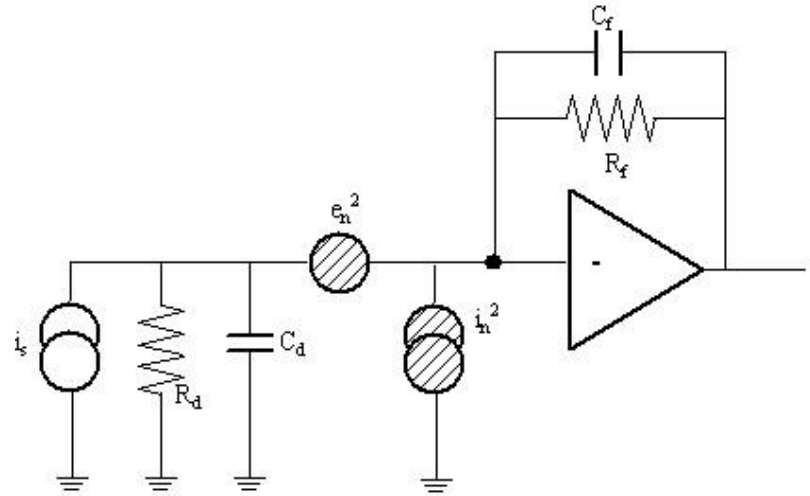
Noise in transimpedance amplifiers

- 2 noise generators at the input
  - Parallel noise : (i_n^2) (leakage)
  - Series nosie : (e_n^2) (preamp)

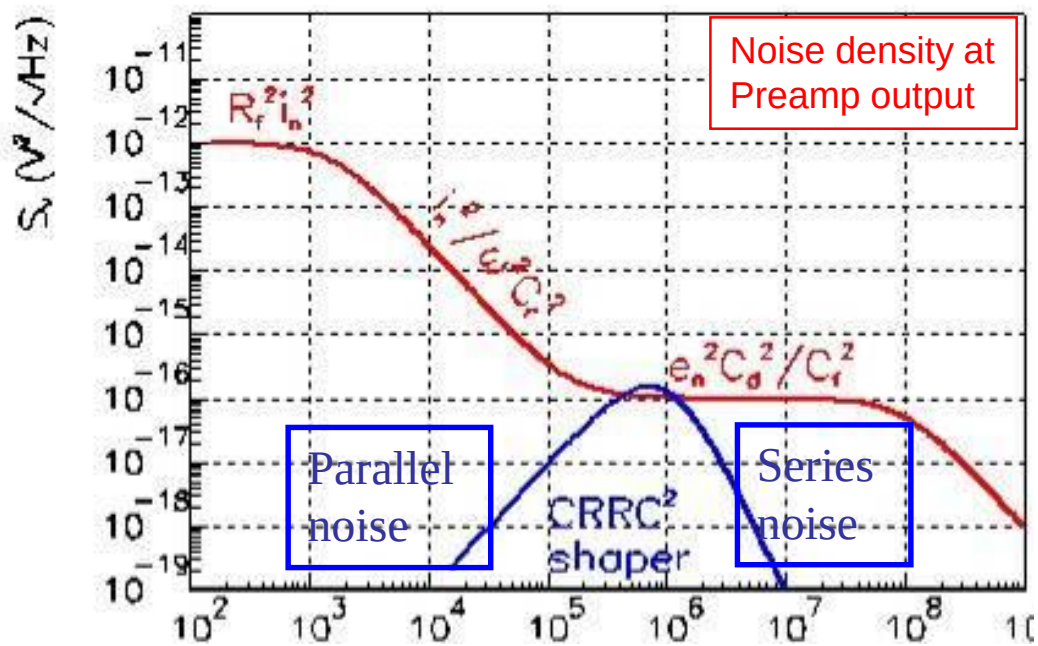
- Output noise spectral density :
  - $Sv(\omega) = (i_n^2 + e_n^2/|Z_d|^2) * |Z_f|^2$

- For charge preamps
  - $Sv(\omega) = i_n^2 /\omega^2 C_f^2 + e_n^2 C_d^2/C_f^2$
  - Parallel noise in $1/\omega^2$
  - Series noise is flat, with a « noise gain » of C_d/C_f

- *rms* noise V_n
  - $V_n^2 = \int Sv(\omega)\, d\omega/2\pi \rightarrow \infty$
  - Benefit of shaping…



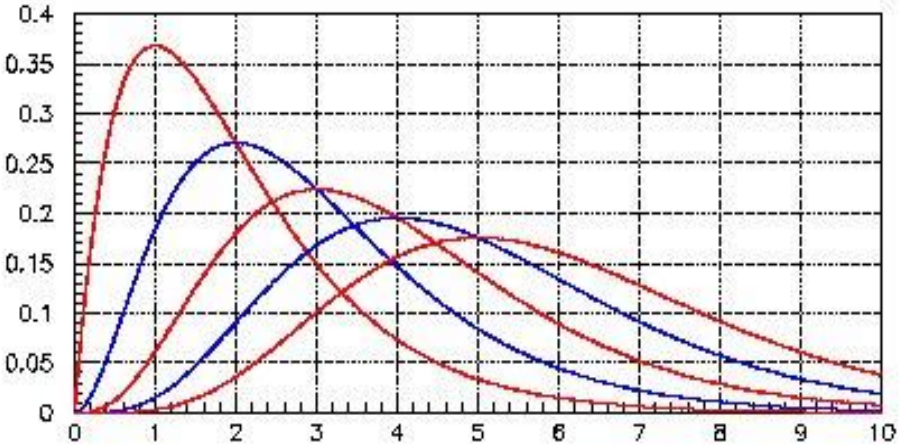
Noise generators in charge preamp

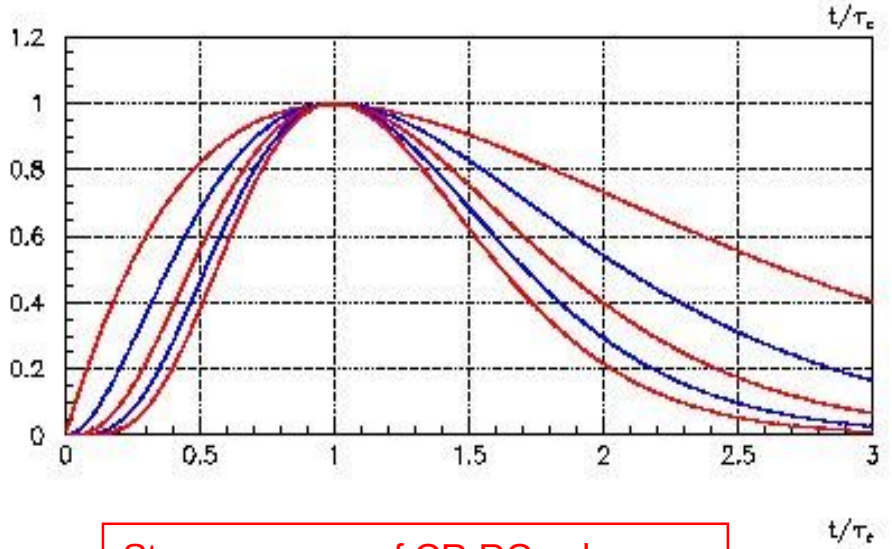


Equivalent Noise Charge (ENC) after CRRC^n

- Noise reduction by optimising useful bandwidth
  - Low-pass filters (**RC^n**) to cut-off high frequency noise
  - High-pass filter (**CR**) to cut-off parallel noise
  - -> pass-band filter CRRC^n

- Equivalent Noise Charge : ENC
  - Noise referred to the input in electrons
  - ENC = Ia(n) $e_n C_t/\sqrt{\tau}$
    $\oplus$ Ib(n) $i_n * \sqrt{\tau}$
  - Series noise in $1/\sqrt{\tau}$
  - Paralle noise in $\sqrt{\tau}$
  - 1/f noise independant of τ
  - Optimum shaping time $\tau_{opt} = \tau_c/\sqrt{2n-1}$



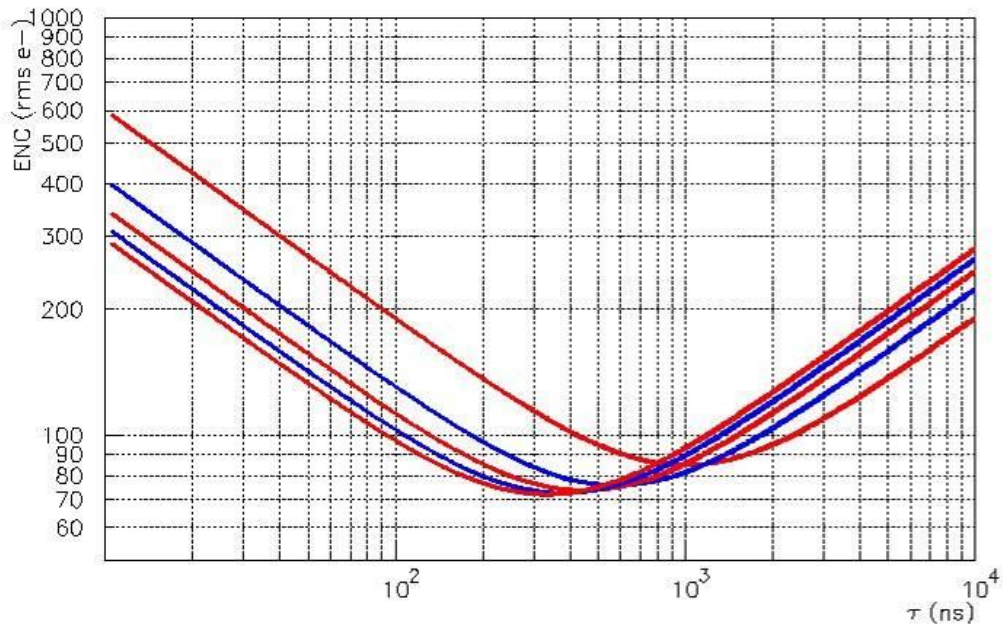


Step response of CR RCn shapers

Equivalent Noise Charge (ENC) after CRRC^n

- Peaking time tp (5-100%)
  - ENC(**tp**) independent of n
  - Also includes preamp risetime

- Complex shapers are obsolete :
  - Power of digital filtering
  - Analog filter = CRRC ou CRRC^2
  - antialiasing



ENC vs tau for CR RCn shapers

Equivalent Noise Charge (ENC) after CRRC^n

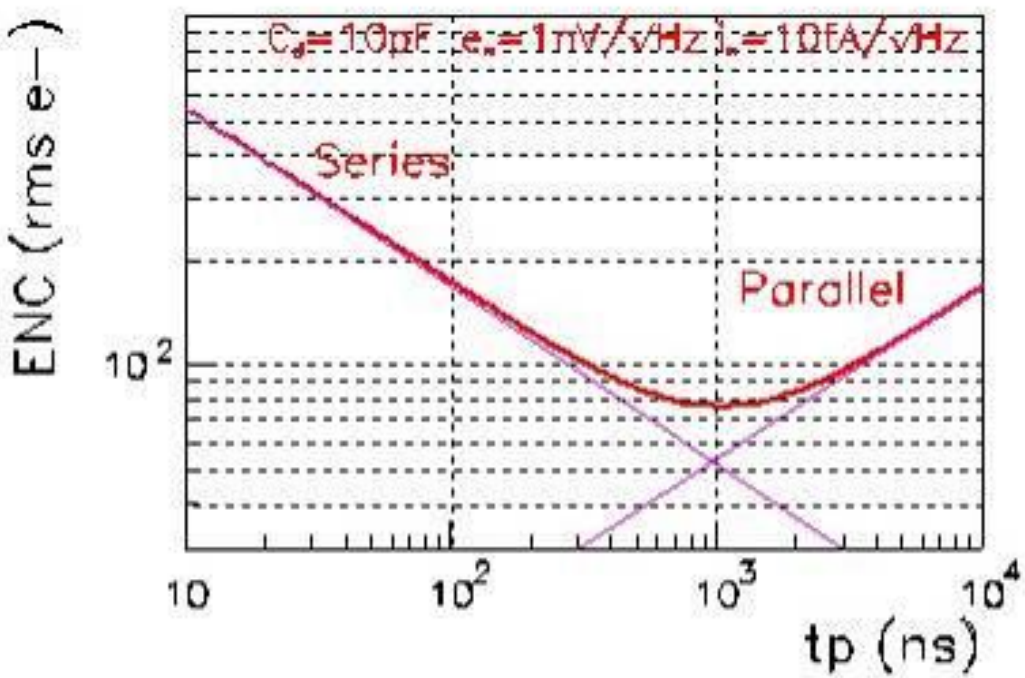
- A useful formula : **ENC (e- rms) after a CRRC^2 shaper :**

$$\boxed{ENC = 174\ e_n C_{tot}/\sqrt{t_p}\ (\delta) \oplus 166\ i_n \sqrt{t_p}\ (\delta)}$$

  - e_n in nV/ √Hz, i_n in pA/ √Hz are the preamp noise spectral densities
  - C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
  - t_p (in ns) is the shaper peaking time (5-100%)

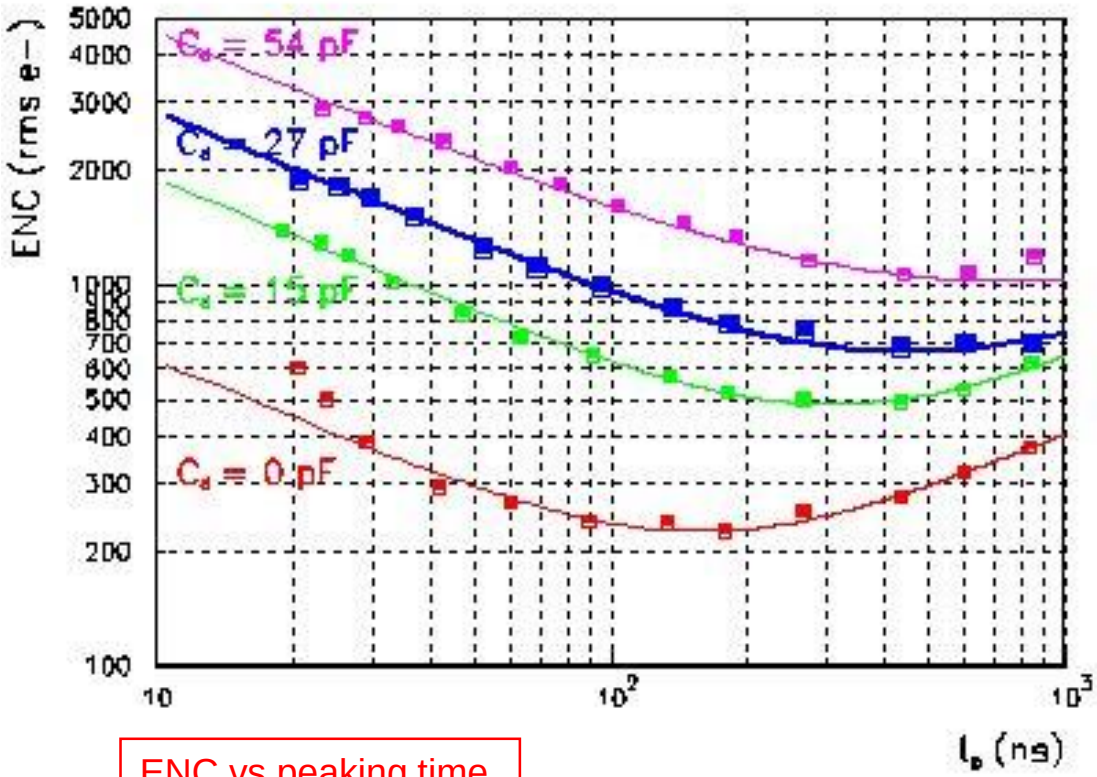
- **Noise minimization**
  - Minimize source capacitance
  - Operate at optimum shaping time
  - Preamp series noise (en) best with high trans-conductance (g_m) in input transistor

    => large current, optimal size

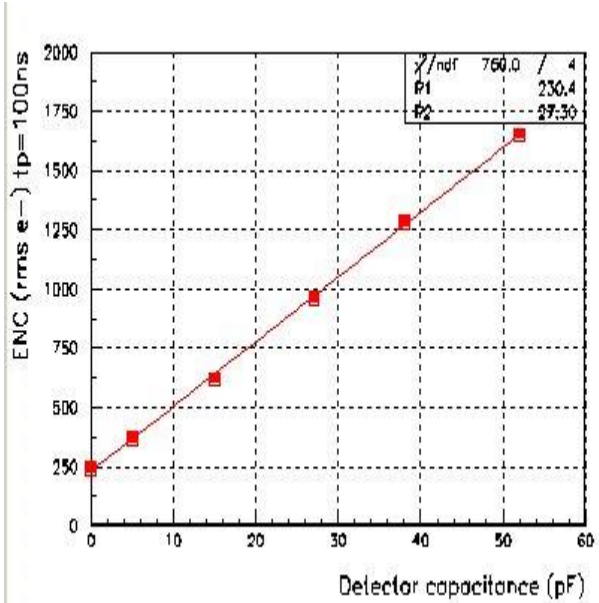


Example of ENC measurement

- 2000/0.35 PMOS 0.35µm SiGe Id=500 µA
  - Series : en = 1.4 nV/√Hz, C_{PA} = 7 pF
  - 1/f noise : 12 e-/pF
  - Parallel : in = 40 fA/√Hz

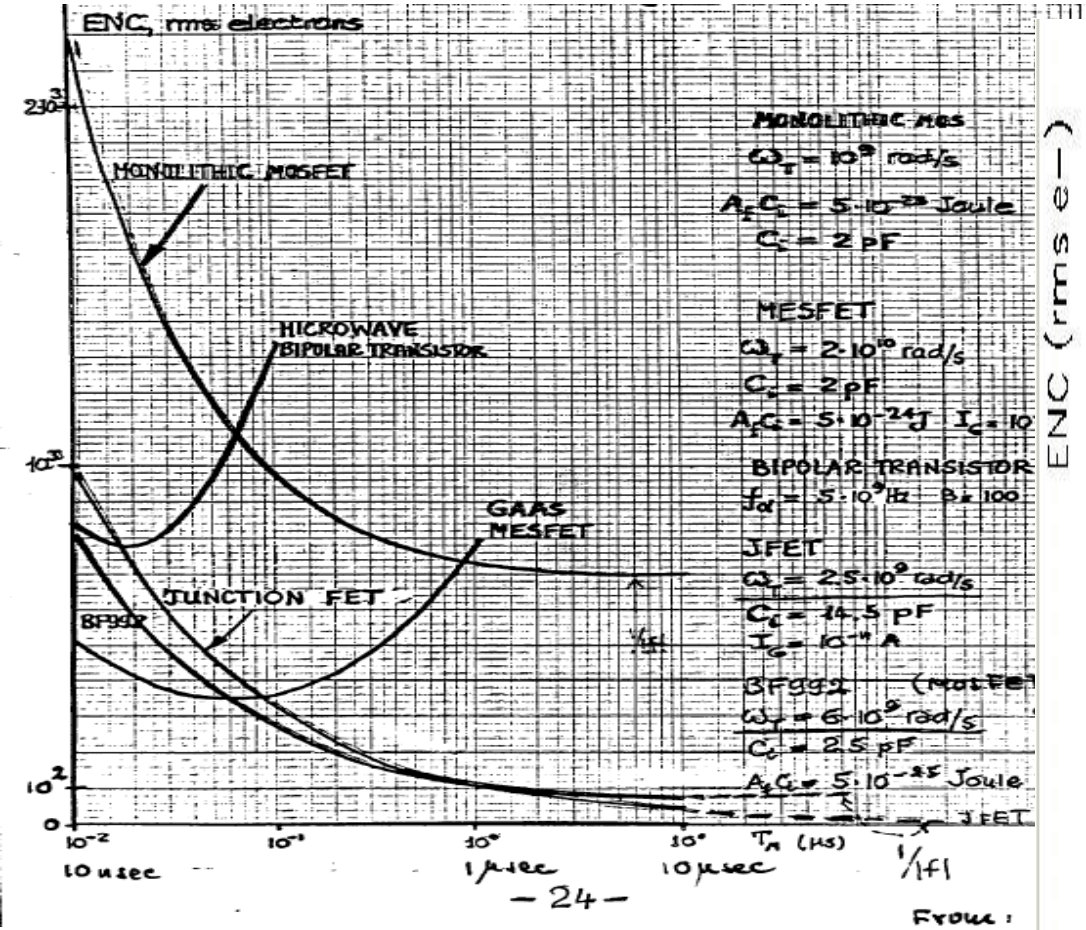


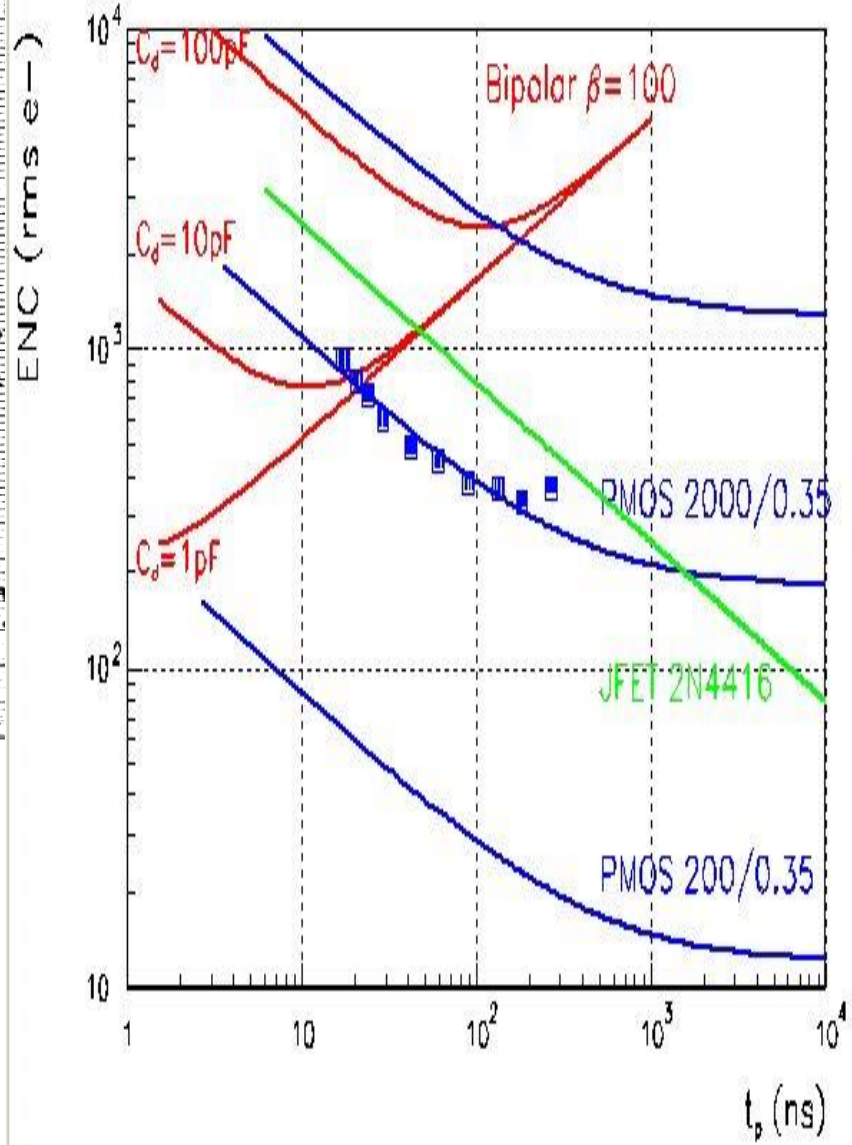
ENC vs peaking time



ENC vs Capacitance tp=100ns

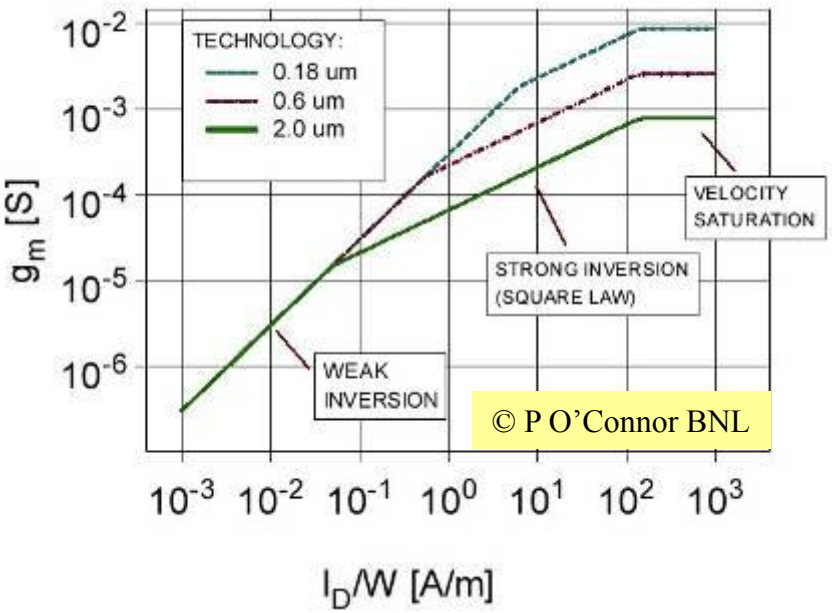
ENC for various technologies





MOS input transistor sizing

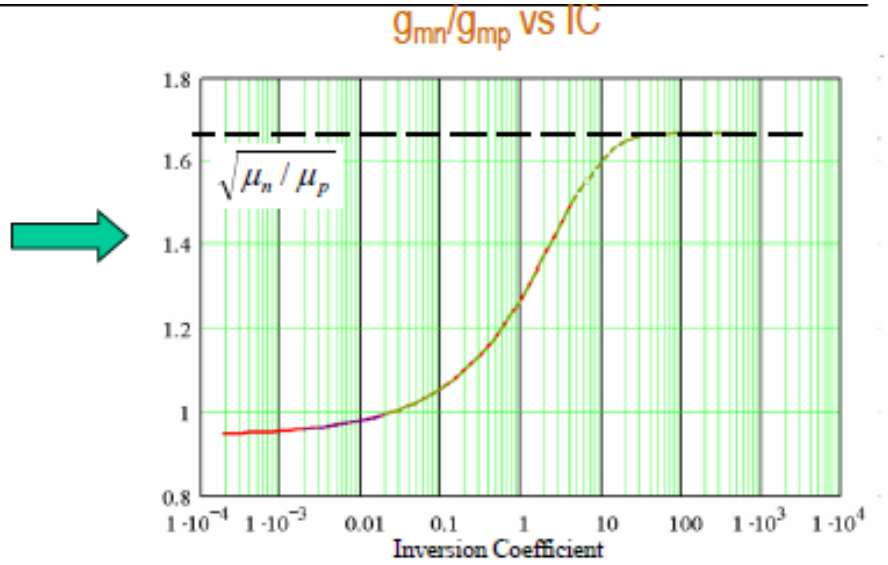
- Capacitive matching : strong inversion
  - g_m proportionnal to W/L $\sqrt{I_D}$
  - C_{GS} proportionnal to W*L
  - ENC propotionnal to (Cdet+C_{GS})/ $\sqrt{gm}$
  - Optimum W/L : C_{GS} = 1/3 Cdet
  - Large transistors are easily in moderate or weak inversion at small current

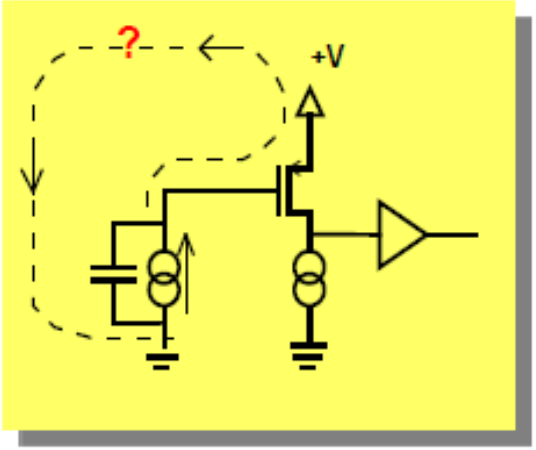


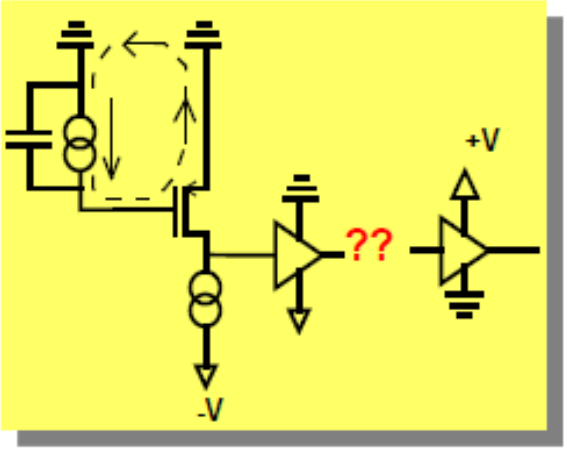
- Optimum size in weak inversion
  - g_m proportionnal to I_D (indep of W,L)
  - ENC minimal for C_{GS} minimal, provided the transistor remains in weak inversion

PMOS vs NMOS [Paul O'Connor BNL]

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse V_{BS} to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin t_{ox}*
- *Single-supply operation of PMOS-input preamp awkward:*



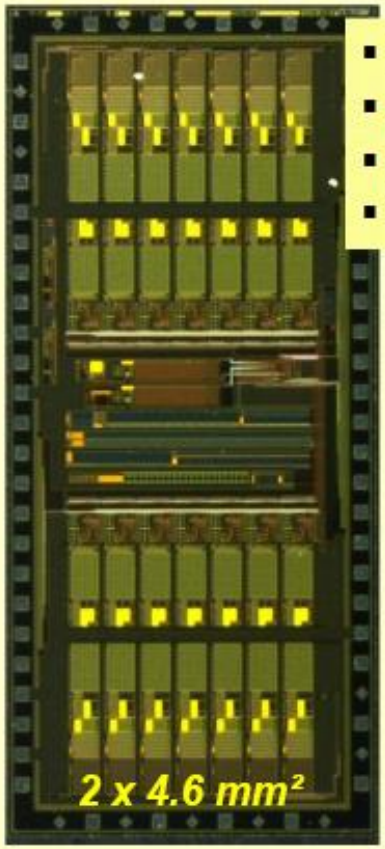




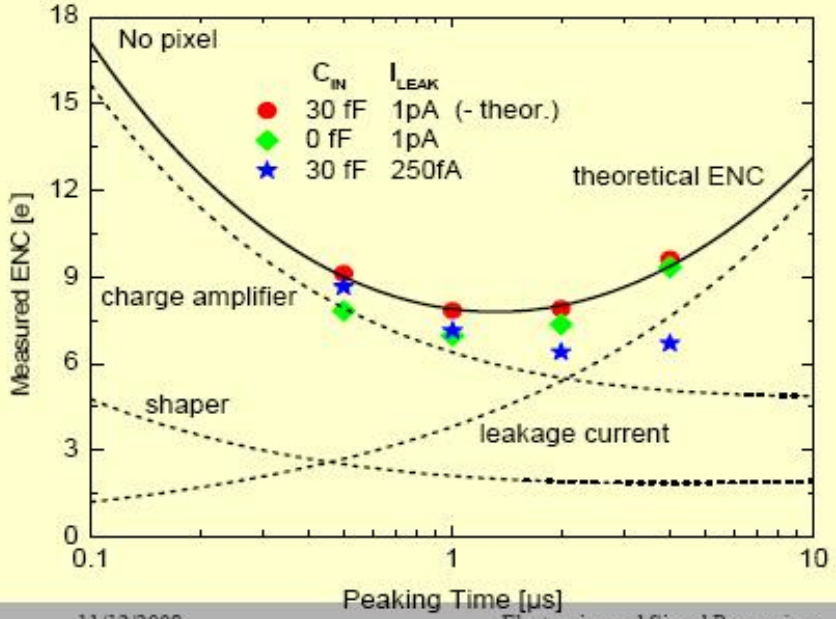
Ultra-Low Noise ASIC High Resolution X-Ray Spectroscopy

Collaboration with NASA at Moon Elemental Mapping

16 mm² Semiconductor Drift Pixels, 500 cm²



- 14 channels, 1.2 mW/channel
- sub-10 electrons resolution
- peak detection and sparse readout
- 30,000 transistors, dev. time: 15 months

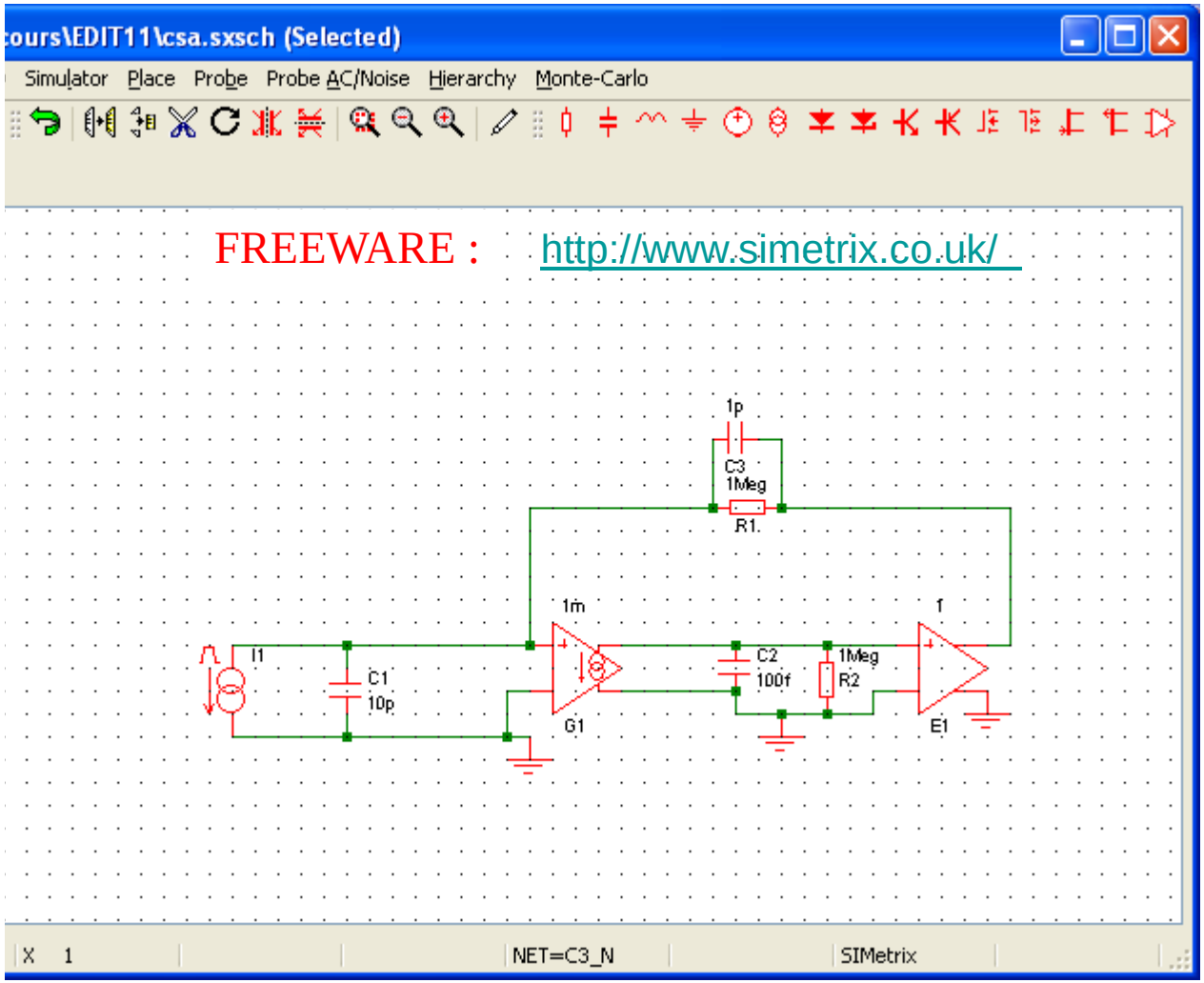


G. De Geronimo et al., NSS (2007)

Simple simulations : Simetrix freeware

Example : bandwidth and EMC of simple charge preamp

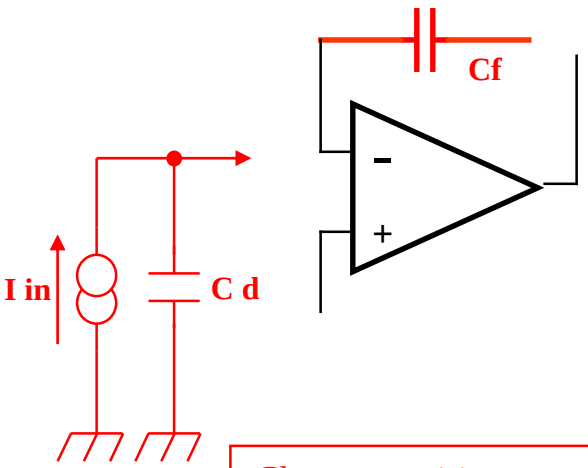
- Simulate impulse response
- Frequency response
- Input impedance
- Ballistic deficit
- Effect of amplifier gain
- Effect of resistive feedback
- Test pulse injection
- Effect of input capacitance
- Parasitic inductance
- Capacitive crosstalk
- Resistive/Inductive ground return



Summary of lecture 1

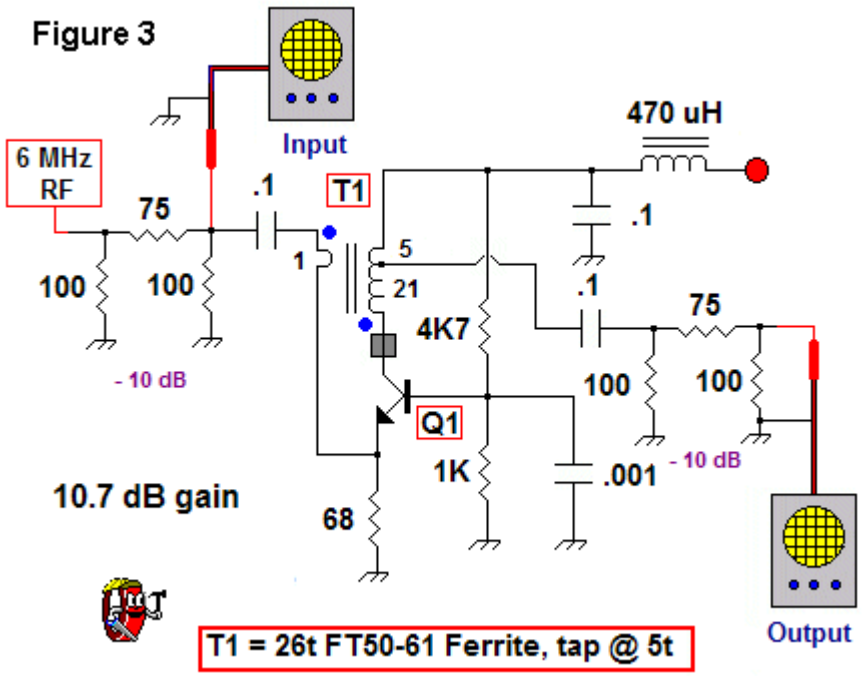
- Importance of front-end on electronics on physics performance

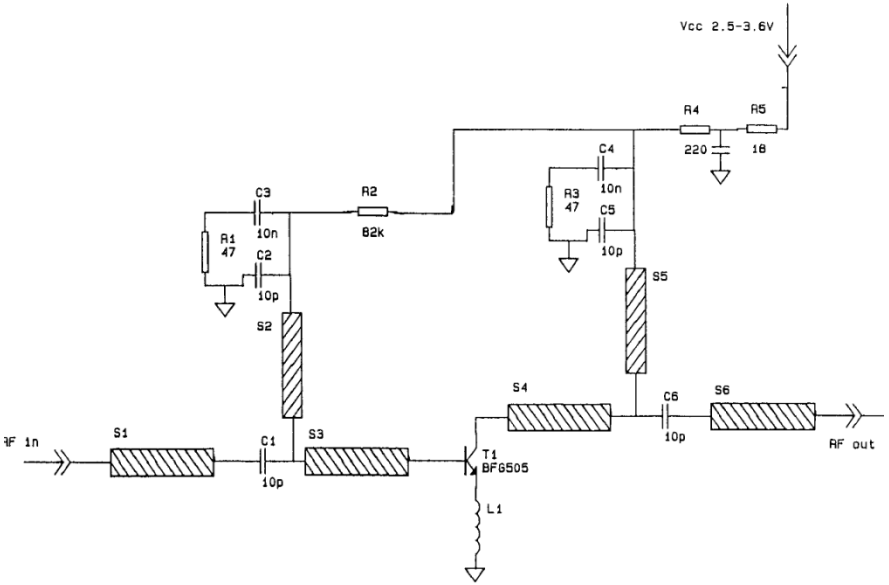
- Benefits of charge preamplifiers : low noise, low crosstalk
  - The front-end of 90% of particle physics detectors…
  - But always built with custom circuits…



Charge sensitive preamp :
Vout = -Q/Cf

High speed preamps…

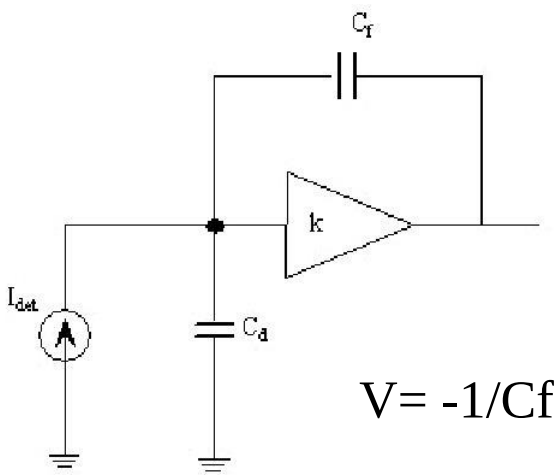




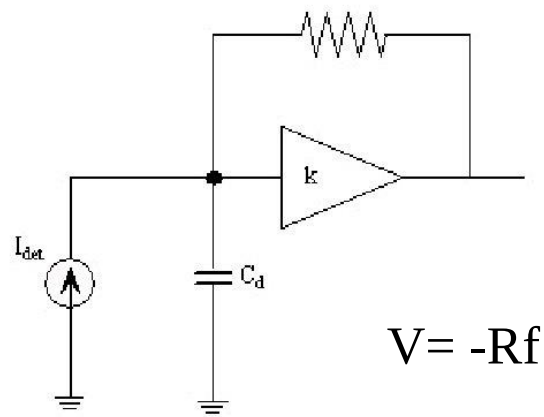
Charge and Current preamps

- Charge preamp
- Capacitive feedback Cf
- Vout/Iin = - 1/jωCf
- Perfect integrator : vout=-Q/Cf∫
- Difficult to accomodate large SiPM signals (200 pC)
- Lowest noise configuration
- Need Rf to empty Cf

- Current preamp
- Resistive feedback Rf
- Vout/Iin = - Rf
- Keeps signal shape
- Need Cf for stability



$$V = -1/Cf \int i(t)dt$$



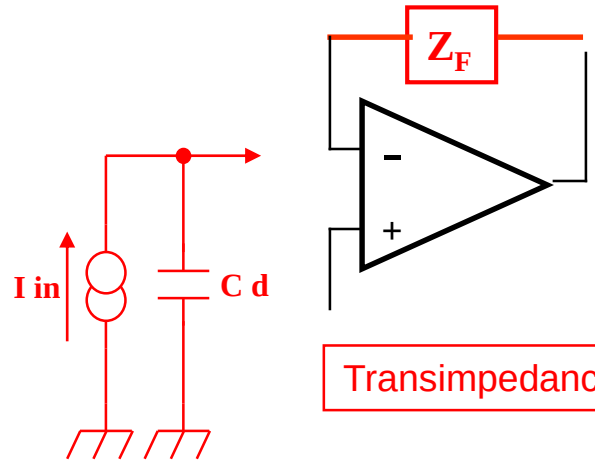
$$V = -Rf \; i(t)$$

Transimpedance configuration

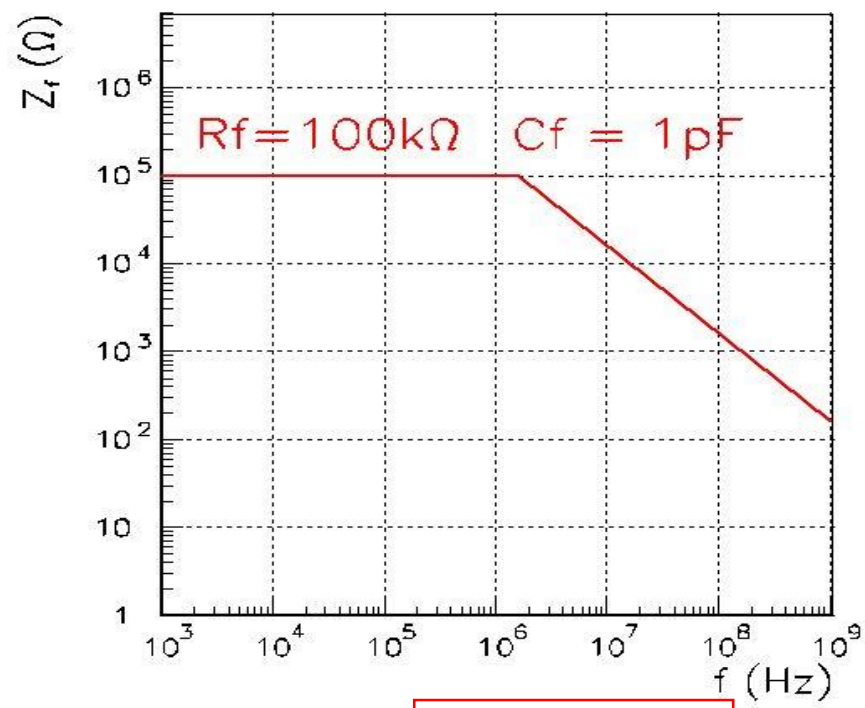
- Transfer function
  - Using a VFOA with gain G
    - $V_{out} - v_{in} = - Z_f\, i_f$
    - $V_{in} = Z_d\,(i_{in} - i_f) = - v_{out}/G$
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + Z_f /GZ_d)$

- $Zf = Rf / (1 + j\omega\, RfCf)$
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - R_f$
    current preamp
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f$
    charge preamp

- Ballistic defict with charge preamp
  - Effect of finite gain : G_0
  - Output voltage «only» Q C_d/G_0C_f



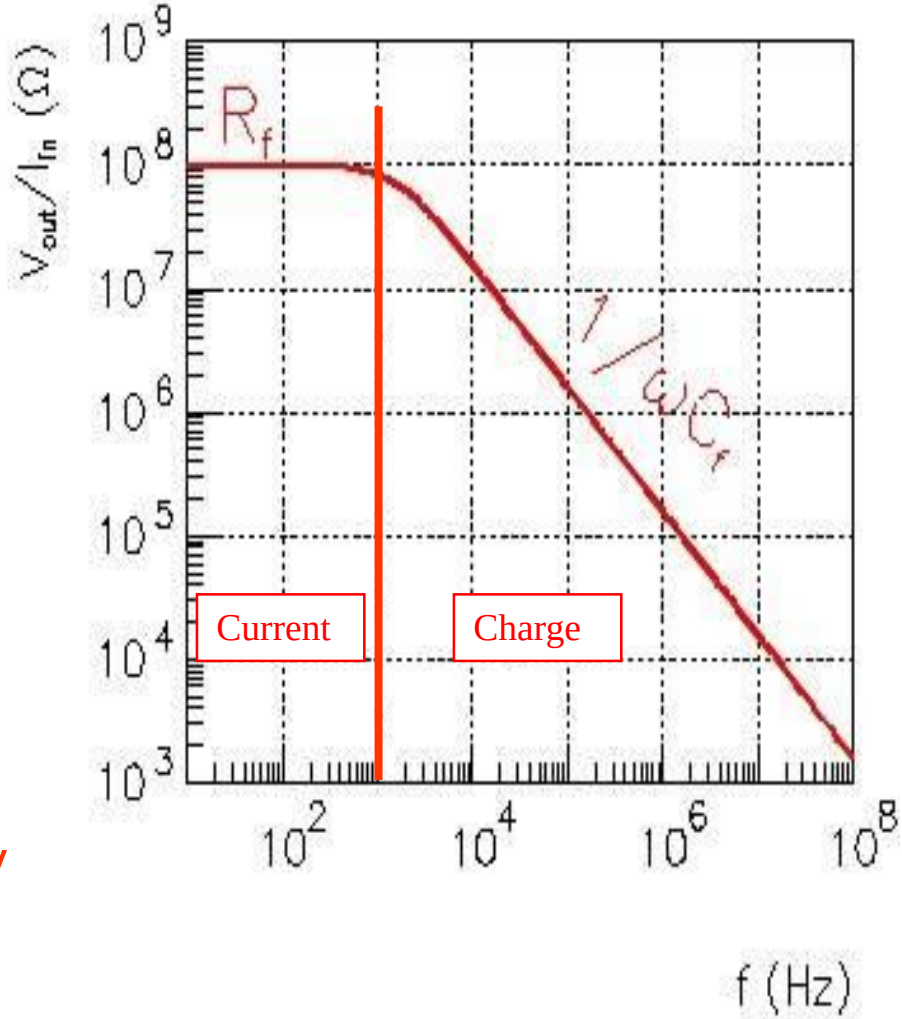
Transimpedance amplifier



Transfer function

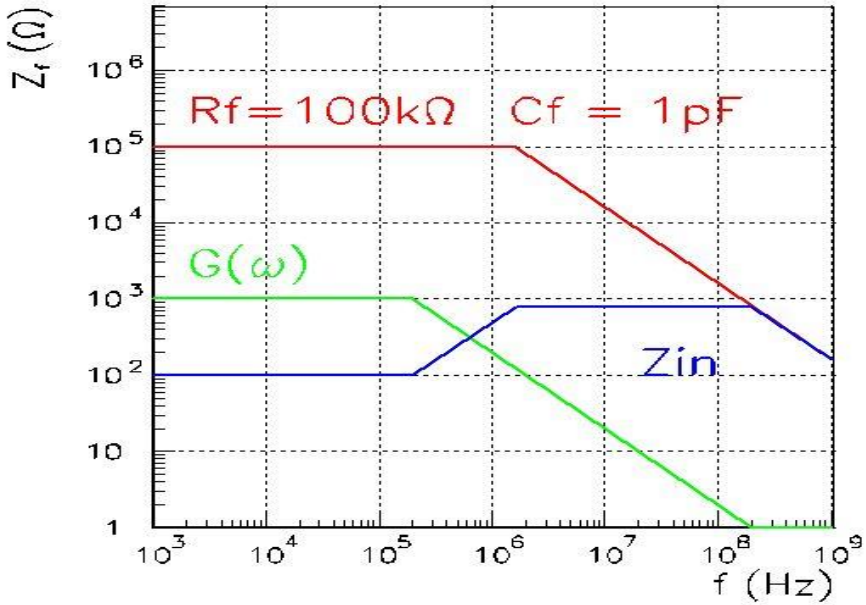
Charge vs Current preamps

- Charge preamps
  - Best noise performance
  - Best with short signals
  - Best with small capacitance
- Current preamps
  - Best for long signals
  - Best for high counting rate
  - Significant parallel noise
- Charge preamps are <u>not slow</u>, they are <u>long</u>
- Current preamps are <u>not faster</u>, they are <u>shorter</u> (but easily unstable)

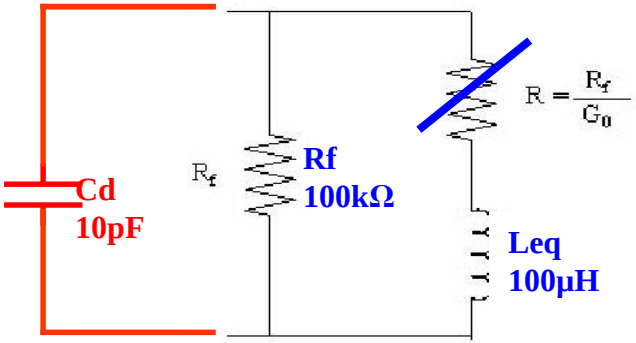


Input impedance

- Input impedance
  - Zin = Zf / G+1
  - Zin->0 virtual ground
  - Minimizes sensitivity to detector impedance
  - Minimizes crosstalk
- Equivalent model
  - $G(\omega) = G_0/(1 + j\,\omega/\omega_0)$
- Terms due to Cf
  - $Zin = 1/j\omega\, G_0 C_f + 1/\, G_0\omega_0\, C_f$
  - Virtual resistance : $Req = 1/\, G_0\omega_0\, C_f$
- Terms due to Rf
  - $Zin = R_f/\, G_0 + j\,\omega\, R_f/\, G_0\omega_0$
  - Virtual inductance : $Leq = R_f/\, G_0\omega_0$
- Possible oscillatory behaviour with capacitive source



Input impedance or TZA



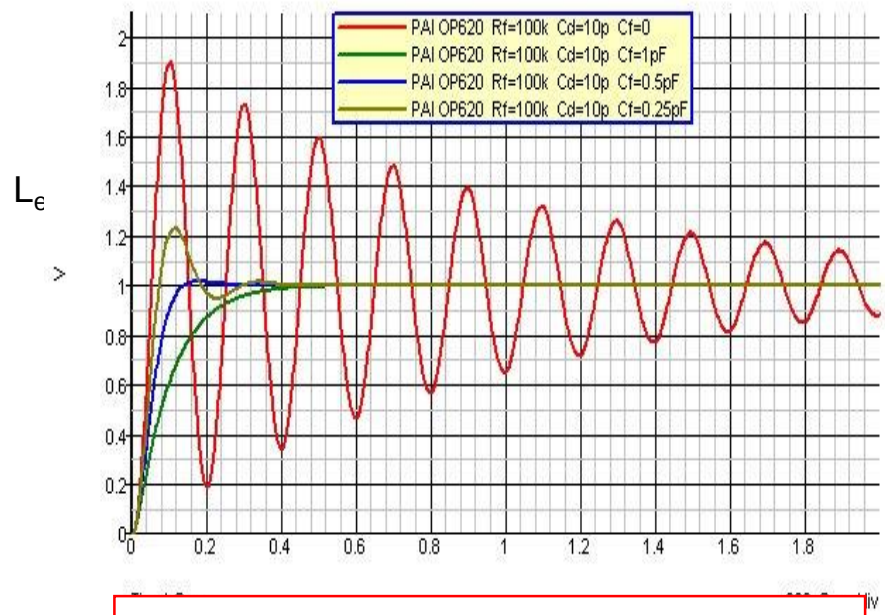
Equivalent circuit at the input

Current preamplifiers :

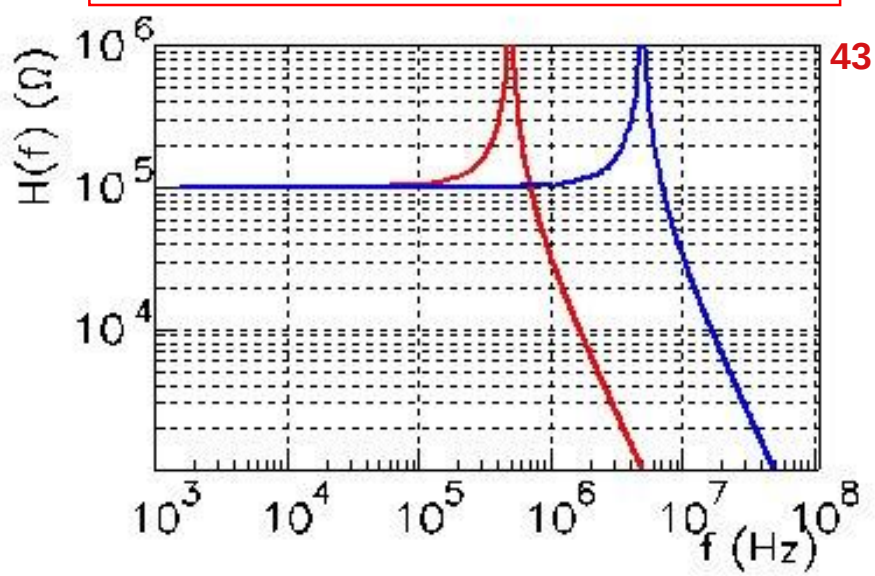
- Easily oscillatory
  - Unstable with capacitive detector
  - Inductive input impedance :
    $= R_f / \omega_C$
  - Resonance at : $f_{res} = 1/2\pi \sqrt{L_{eq}C_d}$
  - Quality factor : $Q = R / \sqrt{L_{eq}/C_d}$
    - $Q > 1/2$ -> ringing
  - Damping with capacitance C_f
    - $C_f = 2 \sqrt{(C_d/R_f\, G_0\omega_0)}$
    - Easier with fast amplifiers

- In frequency domain
  - $H(j\omega) = -Rf / (1 + j\omega\, RfC_d/))$
  - $G(\omega) = G_0 /(1+j\omega/\omega_0)$

  $H = - Rf / (1 + j\omega\, R_fC_d/G_0 - \omega^2\, R_fC_d /G_0\omega_0)$

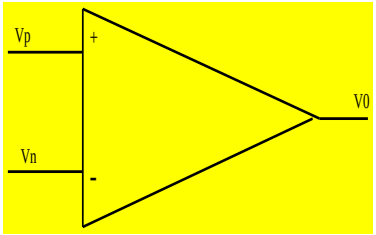


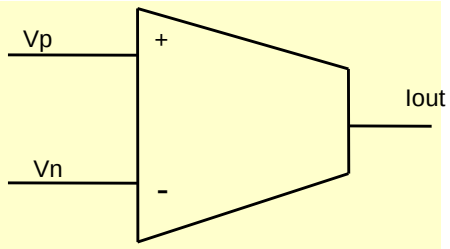
Step response of current sensitive preamp



Amplifiers : a large zoo

- Voltage feedback operationnal amplifier (VFOA)
- Voltage amplifiers, RF amplifiers (VA,LNA)
- Current feedback operationnal amplifiers (CFOA)
- Current conveyors (CCI, CCII +/-)
- Current (pre)amplifiers (ISA,PAI)
- Charge (pre)amplifiers (CPA,CSA,PAC)
- Transconductance amplifiers (OTA)
- Transimpedance amplifiers (TZA,OTZ)

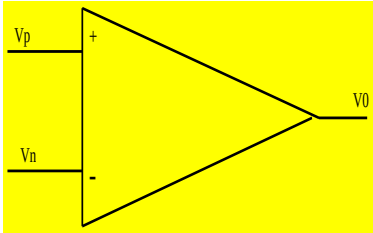




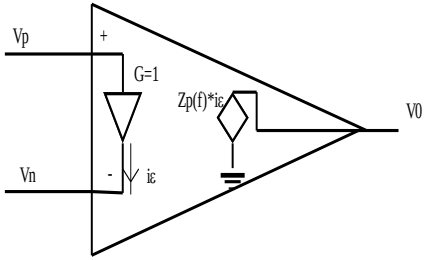
- Mixing up open loop (OL) and closed loop (CL) configurations !

Only 4 open-loop configurations

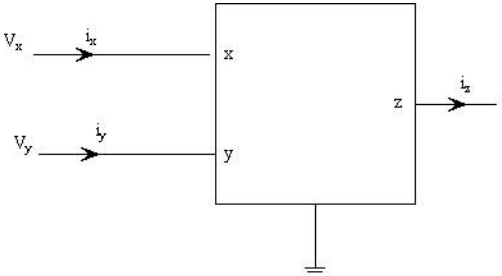
- Voltage operationnal amplifiers (OA, VFOA)
  - Vout = G(ω) Vin diff
  - Zin+ = Zin- = ∞ Zout = 0



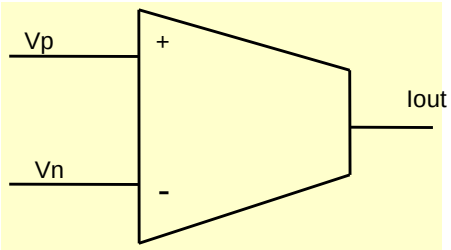
- Transimpedance operationnal amplifier (CFOA !)
  - Vout = Z(ω) iin
  - Zin- = 0 Zout = 0



- Current conveyor (CCI,CCII)
  - Iout = G(ω) Iin
  - Zin = 0 Zout = ∞

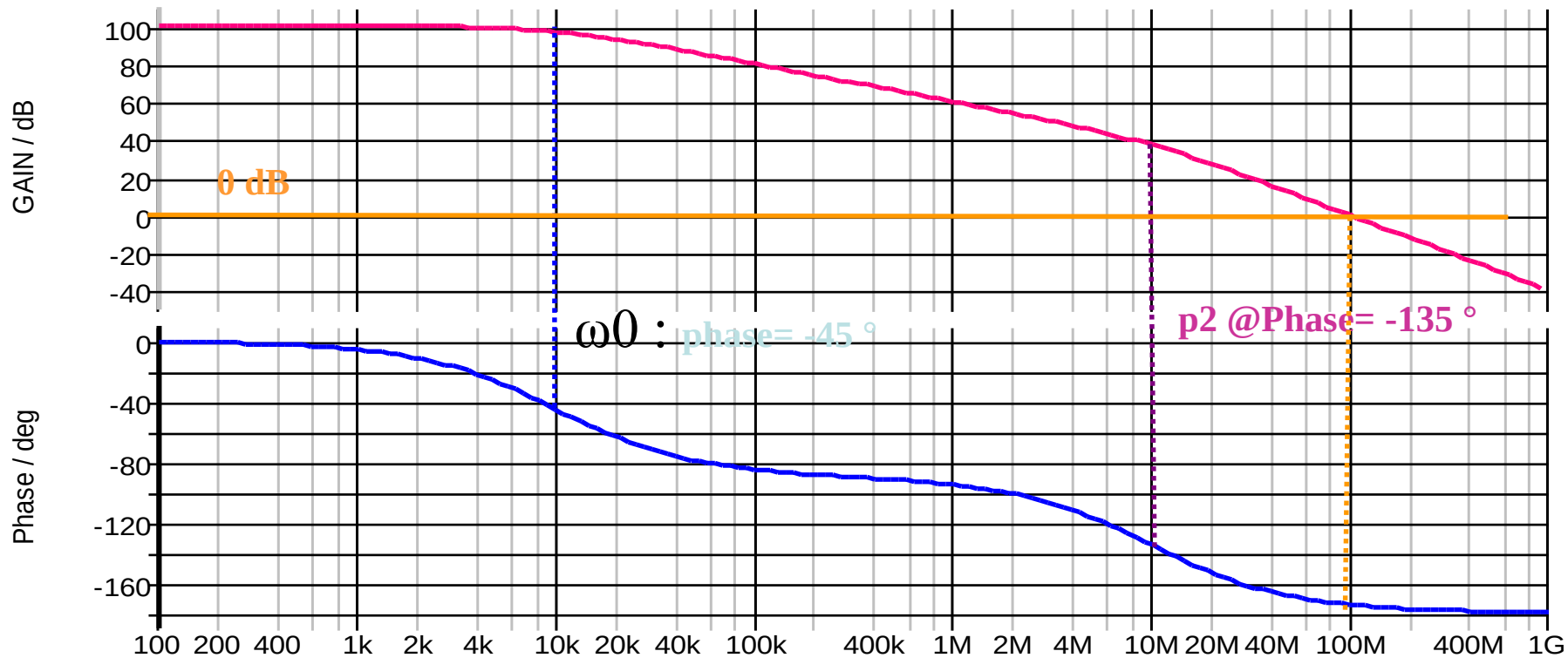


- Transconductance amplifier (OTA)
  - Iout = Gm(ω) Vin diff
  - Zin+ = Zin- = ∞ Zout = ∞



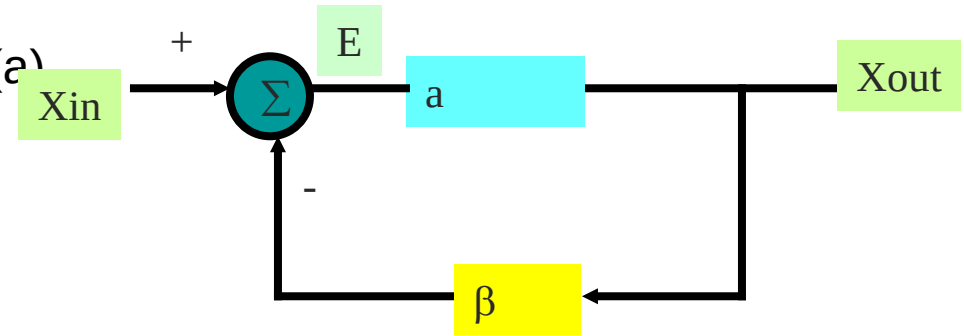
Open loop gain variation with frequency

- Define exactly what is « gain » vout/vin, vout/iin…
- « Gain » varies with frequency : $G(j\omega) = G_0/(1 + j\,\omega/\omega_0)$
  - $\mathbf{G_0}$ low frequency gain
  - $\boldsymbol{\omega_0}$ dominant pole
  - $\boldsymbol{\omega_C = G_0\,\omega_0}$ Gain-Bandwidth product (sometimes referred to as unity gain frequency)



Feedback : an essential tool

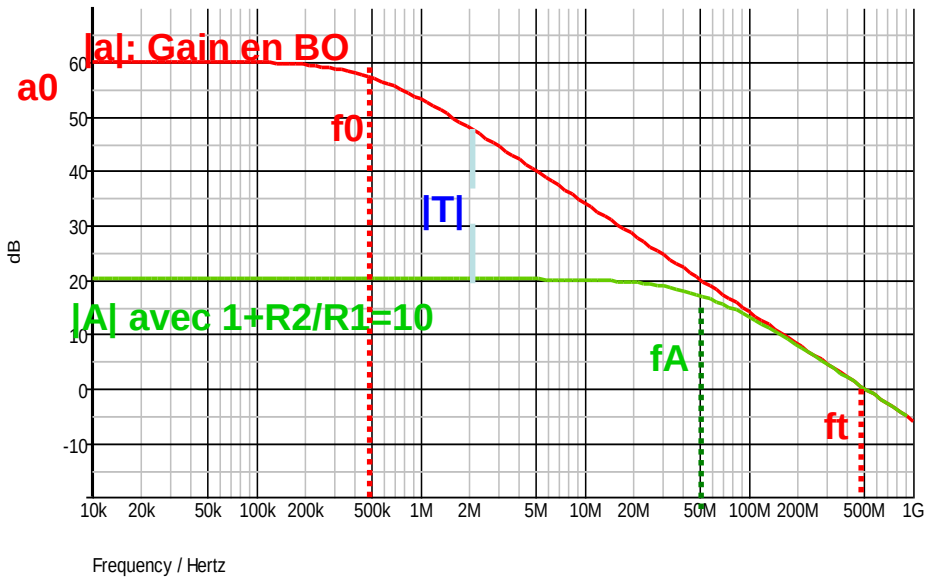
- Improves gain performance
  - Less sensitivity to open loop gain (a)
  - Better linearity



- Essential in low power design
- Potentially unstable

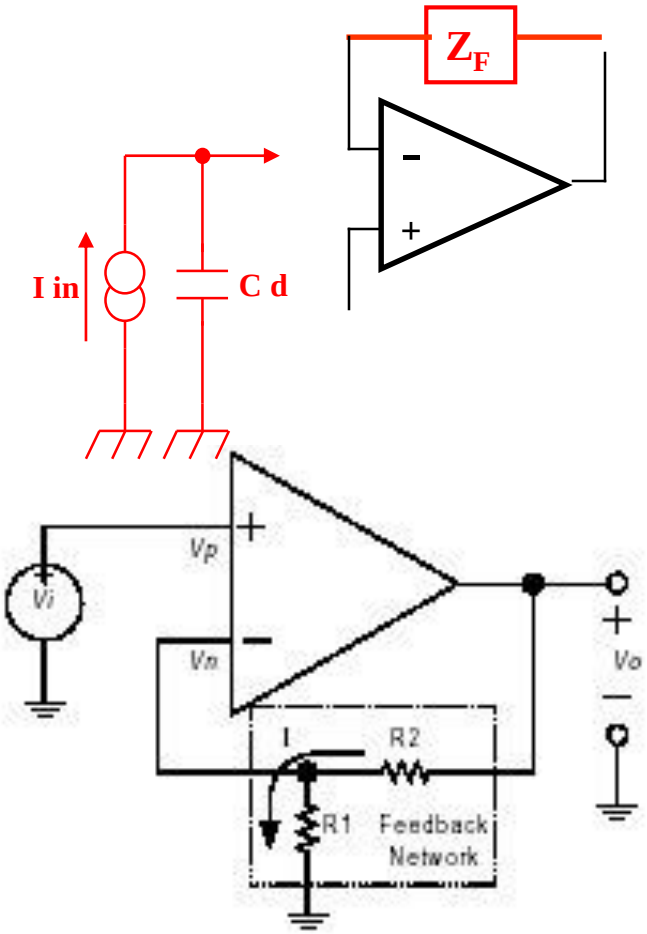
$$\frac{Xout}{Xin} = \frac{a}{1 + a\beta} = \frac{1/\beta}{1 + 1/a\beta}$$

- Feedback constant : β = E/Xout
- Open loop gain : a = Xout/E
- Closed loop gain : Xout/Xin -> 1/β
- Loop gain : T = 1/aβ



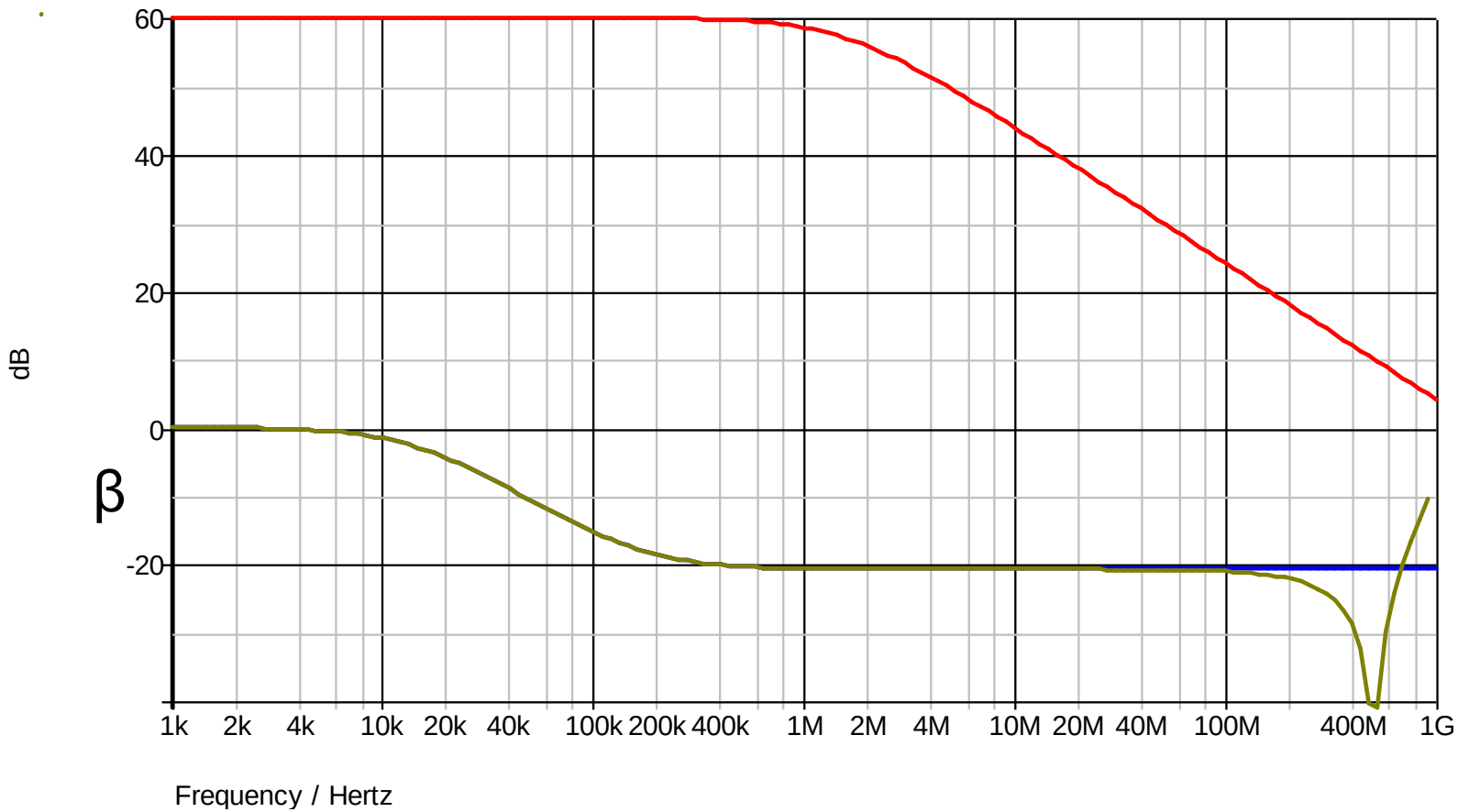
Only 4 feedback configurations

- Shunt-shunt = transimpedance
  - Small Zin (= Zin(OL)/T) -> current input
  - small Zout (= Zout(OL)/T) -> voltage output
  - De-sensitizes transimpedance = 1/β = Zf
- Series-shunt
  - Large Zin (= Zin(OL)*T) -> voltage input
  - Small Zout (= Zout(OL)/T) -> voltage output
  - Optimizes voltage gain (= 1/β)
- Shunt series
  - Small Zin (= Zin(OL)/T) -> current input
  - Large Zout (= Zout(OL)*T) -> current output
  - Current conveyor
- Series-series
  - Large Zin (= Zin(OL)*T) -> voltage input
  - Large Zout (= Zout(OL)*T) -> current output
  - Transconductance
  - Ex : common emitter with emitter degeneration



Preamp stability

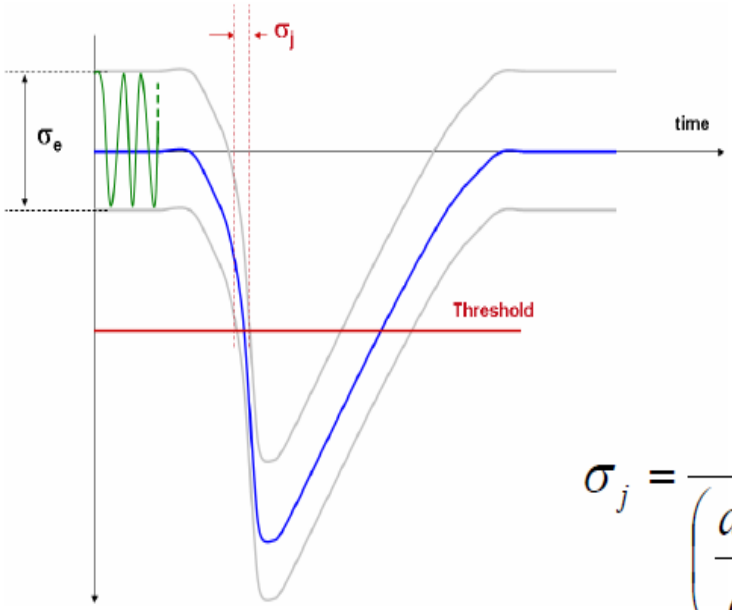
- Calculating β = E/Xout = Zd/(Zd+Zf)



Noise and jitter

- Electronics noise dominated by series noise en
  - Large detector capacitance
  - For voltage preamp and load resistor RL,
  - Output rms noise $Vn^2=(en^2+4kTRs)\ G^2\ \pi/2*BW_{-3dB}$
  - Typical values : Rs=50 Ω, en=1 nV/√Hz Vn=1 mV for G=10, BW=1GHz
  - For current sensitive preamps, possible noise peaking due to Cd

- Jitter
  - Part due to electronics noise :
  - σt = σv / (dV/dt)
  - Minimized by increasing BW

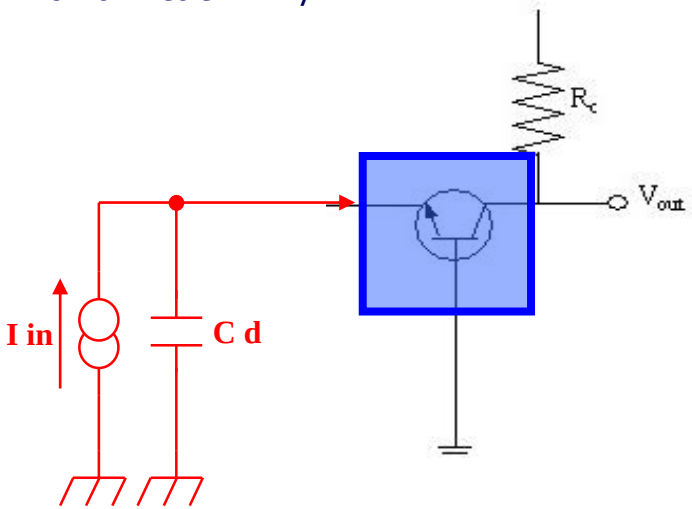


$$\sigma_j = \frac{\sigma_e}{\left(\frac{dV}{dt}\right)_{threshold}}$$

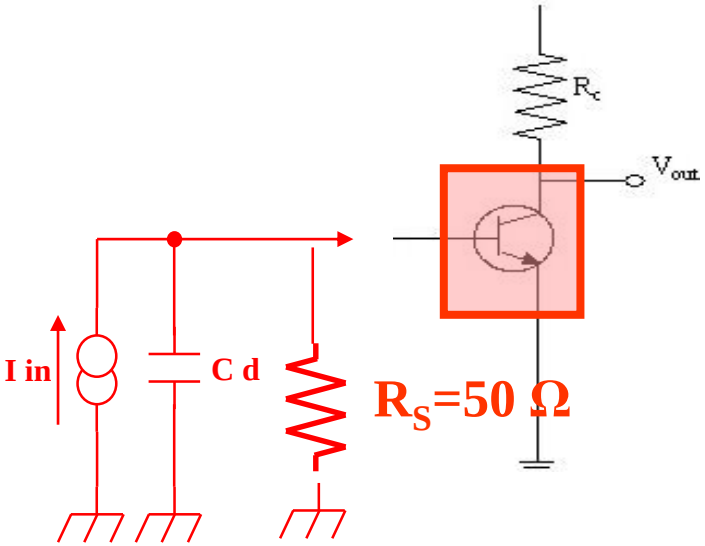
High speed configurations

- Open loop configurations : current conveyors, RF amplifiers
- Usually designed at transistor level MOS or SiGe

- **Current conveyors**
- Small Zin : current sensitive input
- Large Zout : current driven output
- Unity gain current conveyor
- E.g. : (super) common-base configuration
- Low input impedance : Rin=1/gm
- Transimpedance : Rc
- Bandwitdth : 1/2πRcCu > 1 GHz

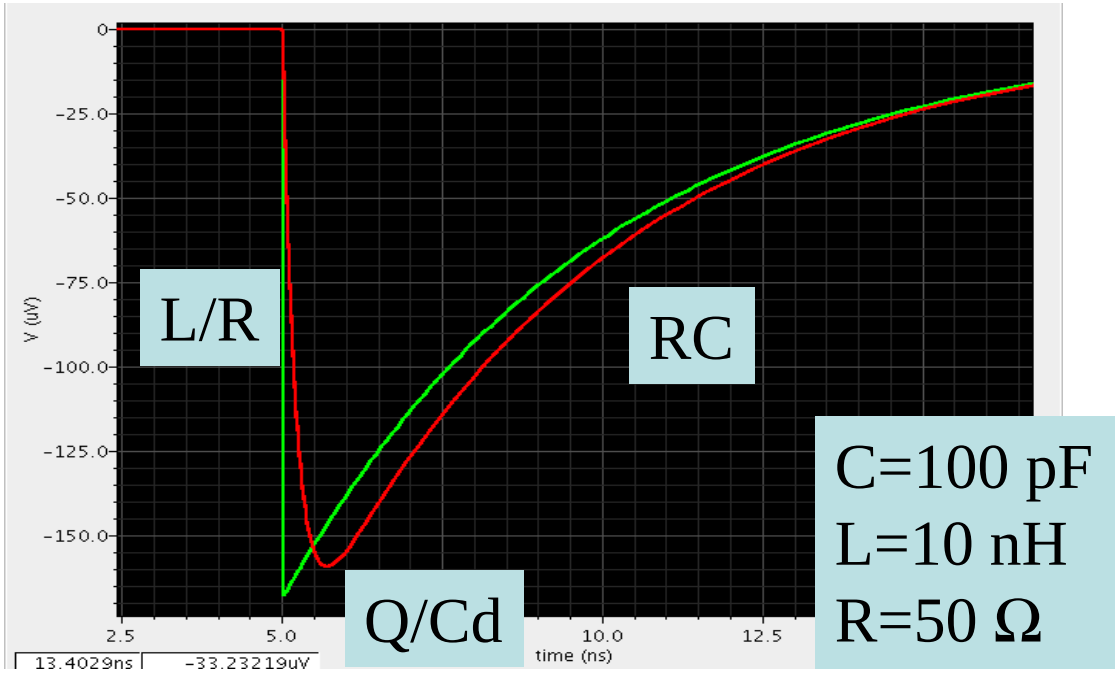


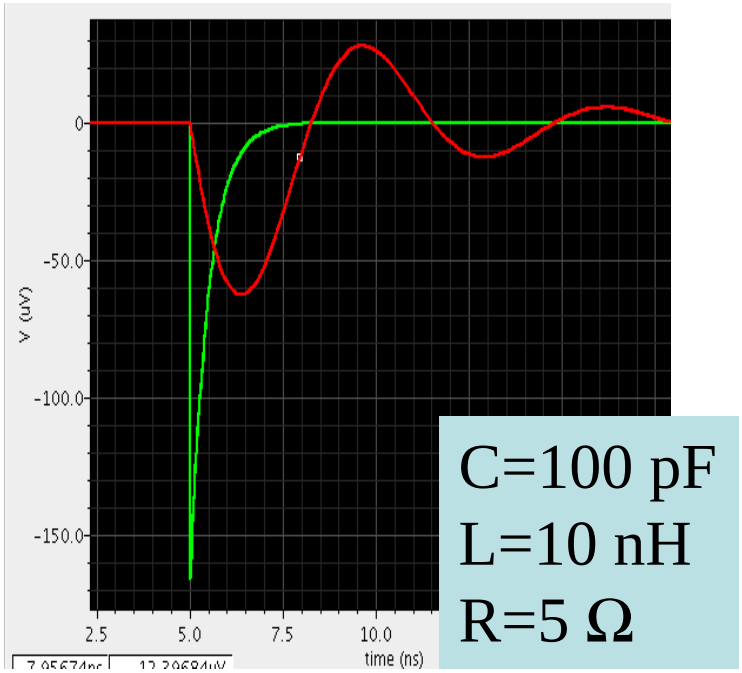
- **RF amplifiers**
- Large Zin : voltage sensitive input
- Large Zout : current driven output
- Current conversion with resistor R_S
- E.g. common-emitter configuration
- Transimpedance : -gmRcRs
- Bandwitdth : 1/2πRsCt



Examples of pulse shapes

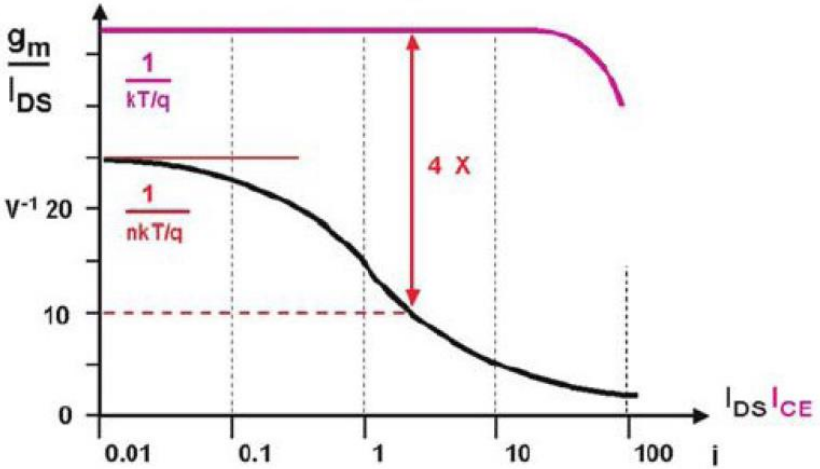
- Short pulse : Q=16 fC, Cd=100 pF, L=0-10 nH, RL=5-50 Ω
- Smaller signals with SiPM (large Cd) ~ mV/p.e.
- Sensitivity to parasitic inductance
- Choice of RL : decay time, stability
- Convolve with current shape… (here delta impulse)

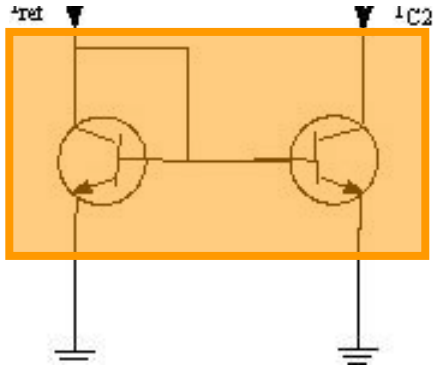


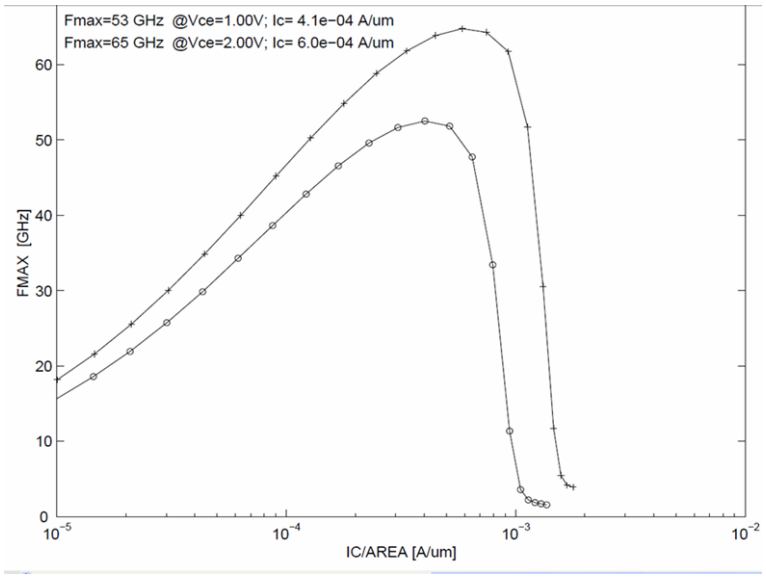


Power and speed with SiGe

- BJT : best g_m /I ratio (1/U_T)
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance (A~mV*µm)
- $V_{BE} = V_T \mathrm{Ln}(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T







Comparison CE/CB

- Experimental measurements on SiGe test structures

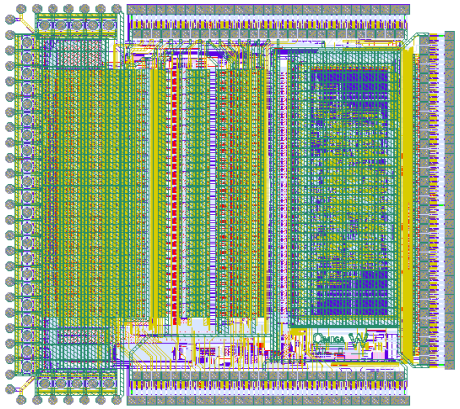
Testboard #3	RF (Common Emitter)	Common Base	Super Common Base
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

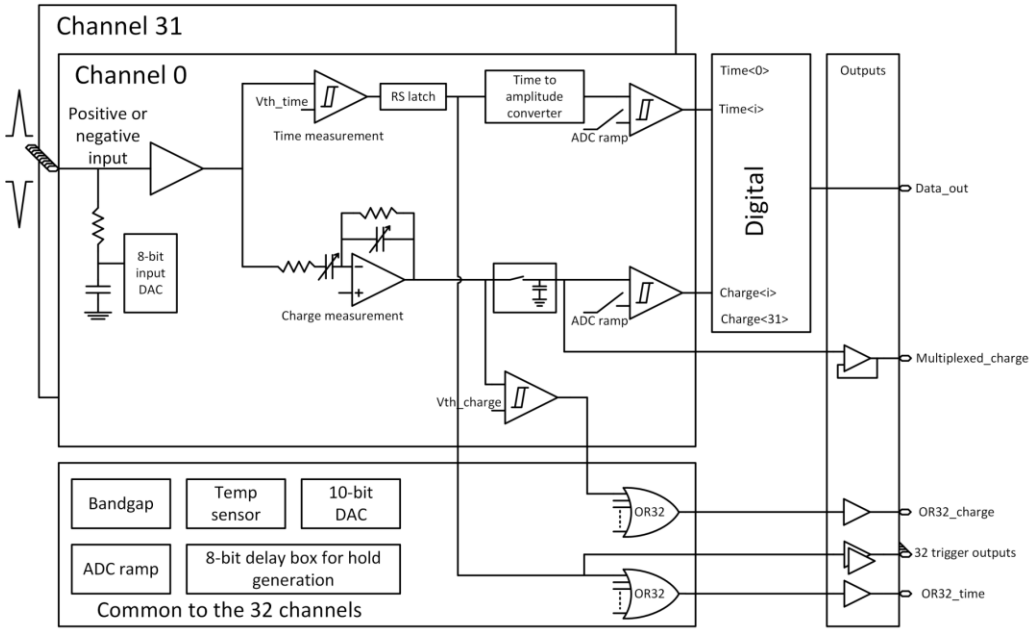
With 1pe-=160 fC

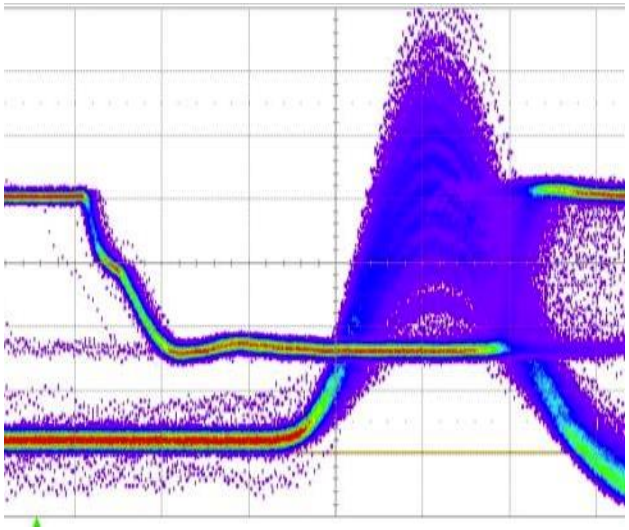
PETIROC2 [http://omega.in2p3.fr]

- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
  - RF, common emitter SiGe fast amplifier, DC coupled to detector, GBWP 10GHz@1mW
  - Fast SiGe discriminator, BW 1GHz @ 1.5mW
- 32 trigger outputs and multiplexed data output
- Embedded 10 bit ADC and 50 ps TDC
- Dual threshold : first photons and energy

weeroc

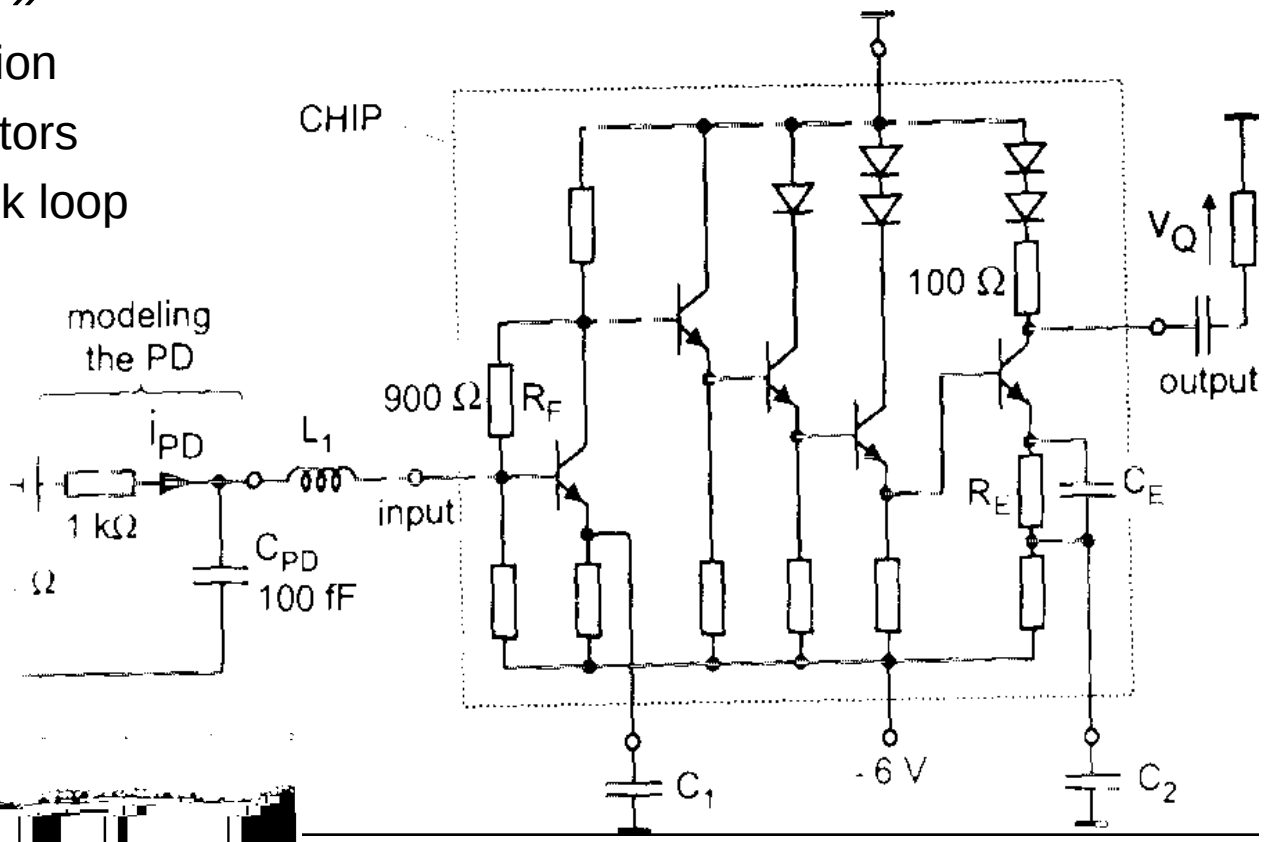


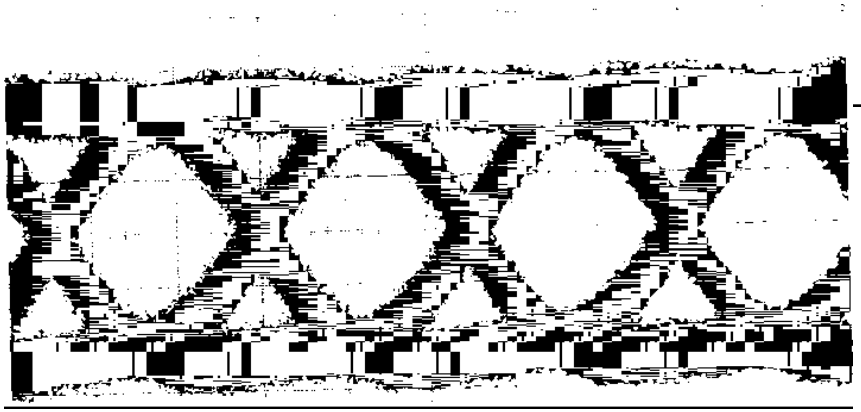




40 Gb/s transimpedance amplifier

- « Simple architecture »
  - CE + CC configuration
  - SiGe bipolar transistors
  - CC outside feedback loop
  - « pole splitting »





A few (personal) comments

- Strong push for high speed front-end > GHz
  - Essential for timing measurements
  - Several configurations to get GBW > 10 GHz
  - Optimum use of SiGe bipolar transiistors

- Voltage sensitive front-end
  - Easiest : 50Ω termination, many commercial amplifiers (mini circuit…)
  - Beware of power dissipation
  - Easy multi-gain (time and charge)

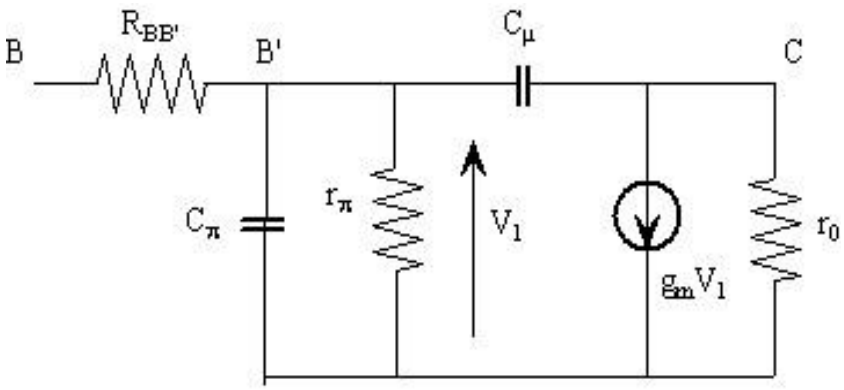
- Current sensitive front-end
  - Potentially lower noise, lower input impdance
  - Largest GBW product

- In all cases, importance of reducing stray inductance

Summary of transistor level design

- Performant design is at transistor level

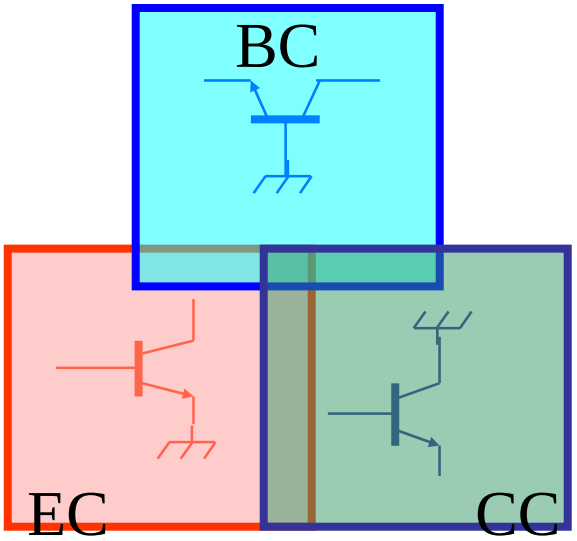
- Simple models
  - hybrid π model
  - Similar for bipolar and MOS
  - Essential for design



High frequency hybrid model of bipolar

- **Three basic configurations**
  - Common emitter (CE) = V to I (transconductance)
  - Common collector (CC) = V to V (voltage buffer)
  - Common base (BC) = I to I (current conveyor)
- **See backup slides**

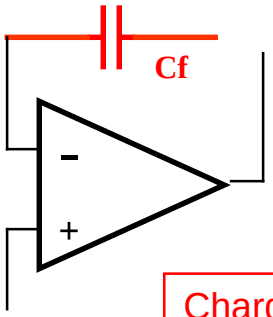
- Numerous « composites »
  - Darlington, Paraphase, Cascode, Mirrors…



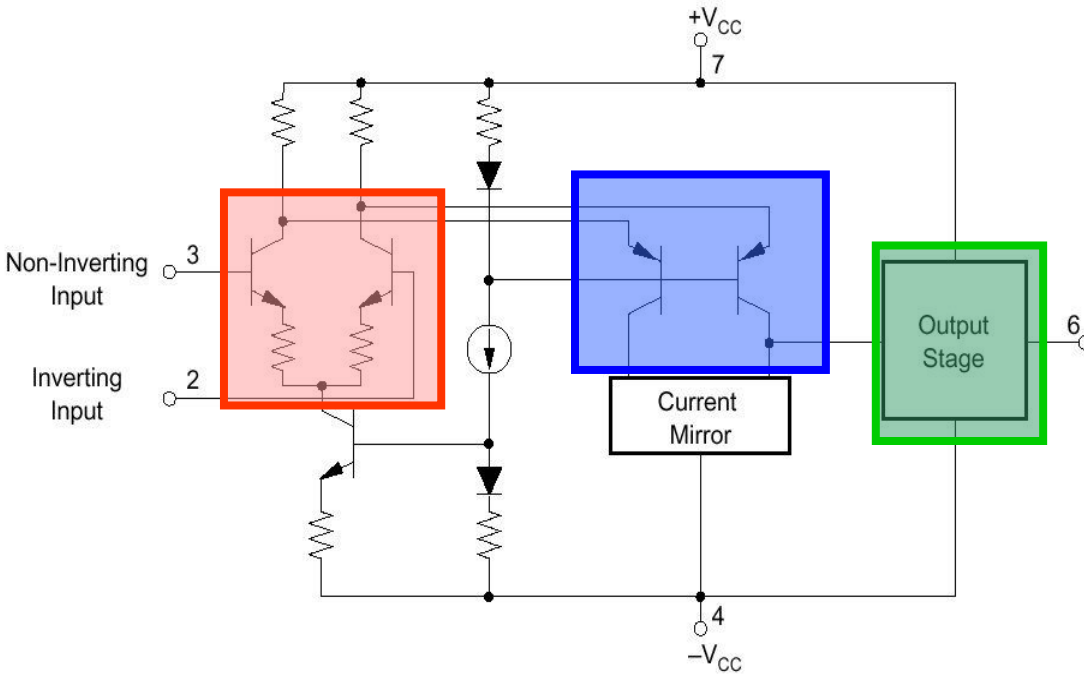
The *Art* of electronics design

Designing a charge preamp…

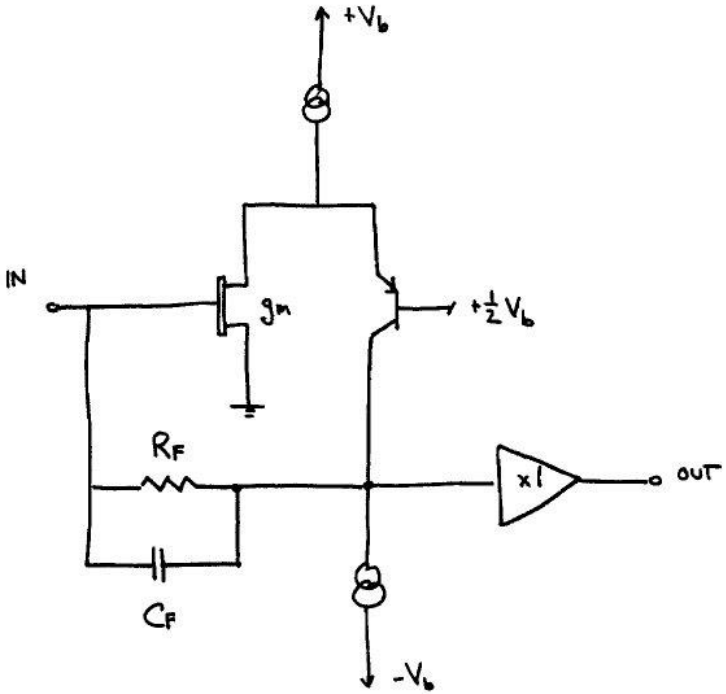
- From the schematic of principle
  - Using of a fast opamp (OP620)
  - Removing unnecessary components…
  - Similar to the traditionnal schematic «Radeka 68 »
  - Optimising transistors and currents



Charge preamp



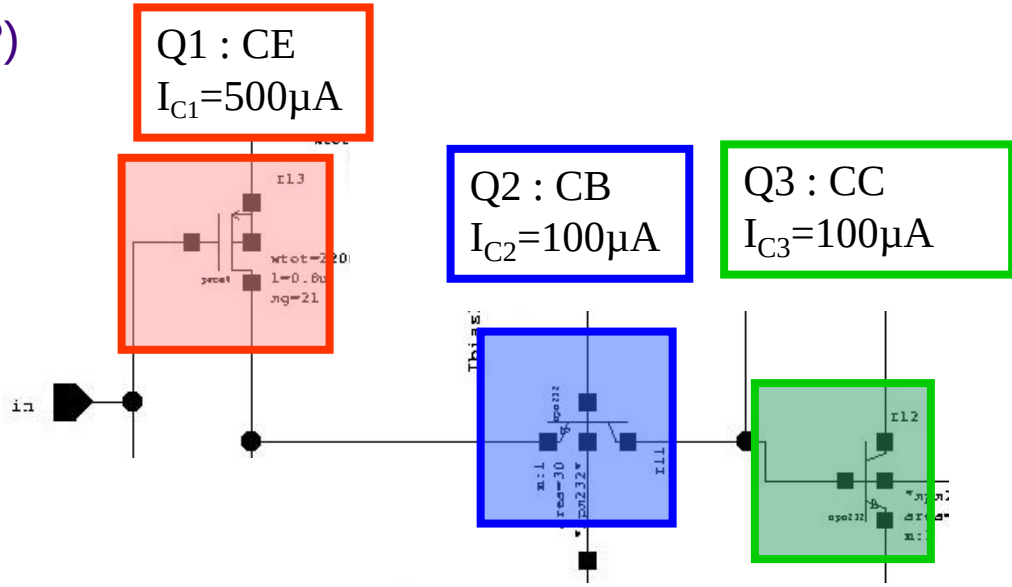
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

Example : designing a charge preamp (2)

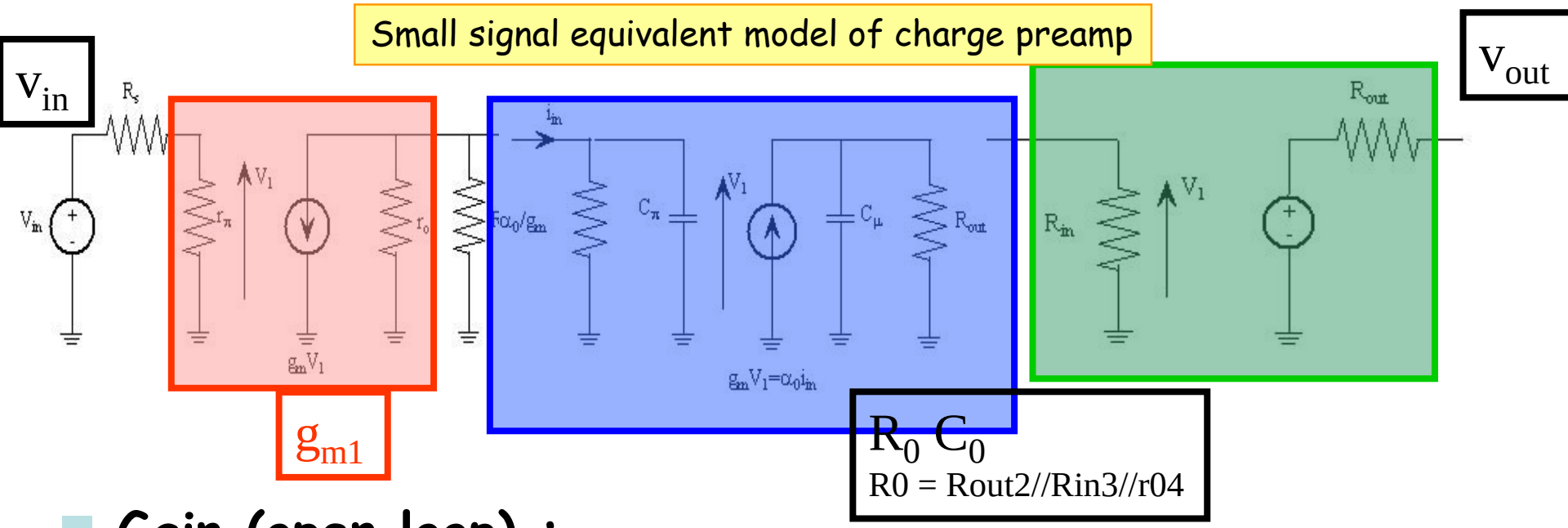
- Simplified schematic
- Optimising components
  - What transistors (PMOS, NPN ?)
  - What bias current ?
  - What transistor size ?
  - What is the noise contribution of each component ?
  - how to minimize it ?
  - What parameters determine the stability ?
  - Waht is the saturation behaviour
  - How vary signal and noise with input capacitance ?
  - How to maximise the output voltage swing ?
  - What is the sensitivity to power supplies, temperature…



Simplified schematic of Charge preamp

Example : designing a charge preamp (3)

- Small signal equivalent model
  - Transistors are replaced by hybrid π model
  - Allows to calculate open loop gain



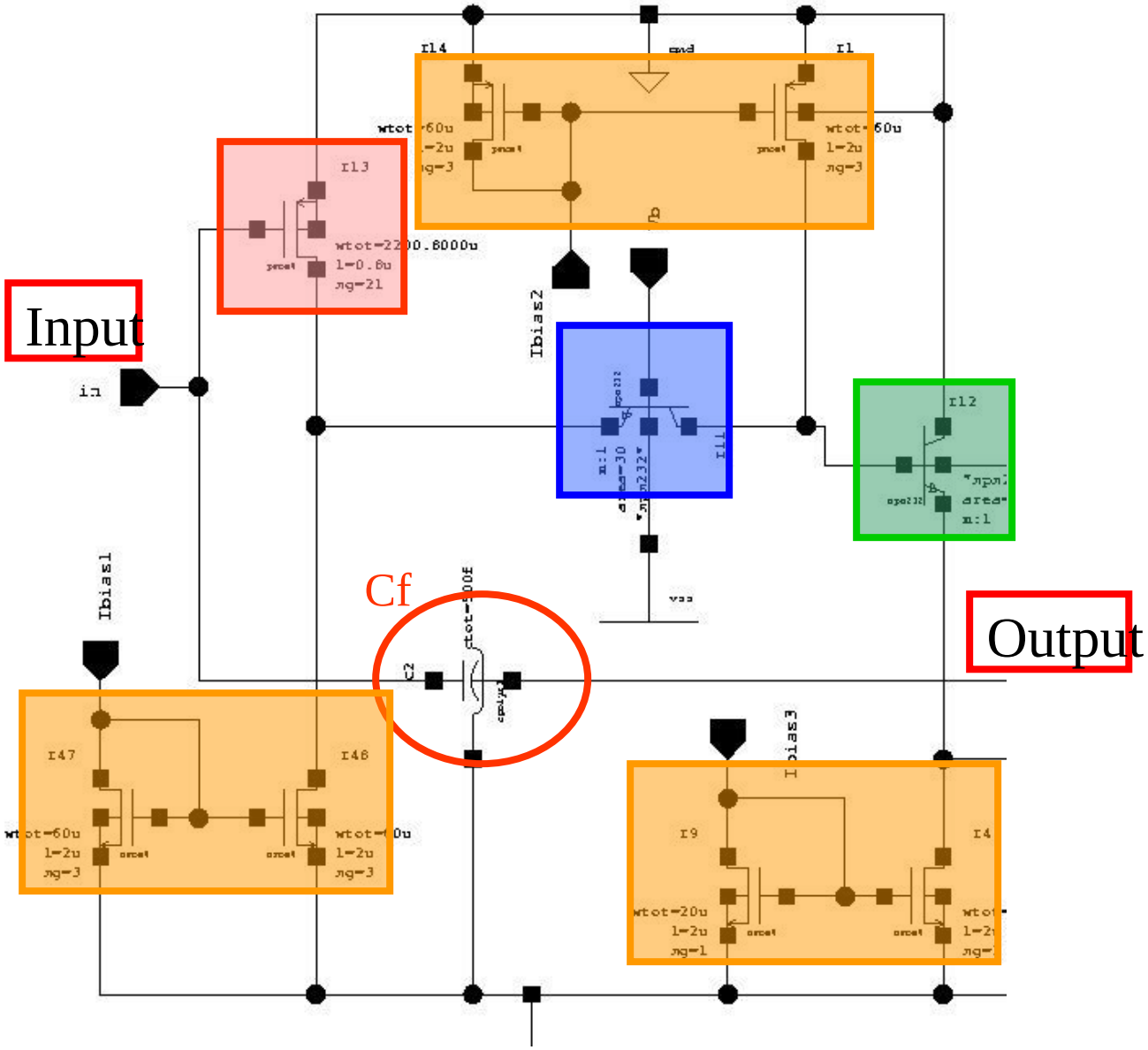
Gain (open loop) :

$$v_{out}/v_{in} = - g_{m1} R_0 /(1 + j\omega \ R_0 C_0)$$

- *Ex : g_{m1}=20mA/V , R_0=500kΩ, C_0=1pF => $G_0=10^4$ $\omega_0=210^6$ $G_0\omega_0=2\ 10^{10}$ = 3 GHz !*

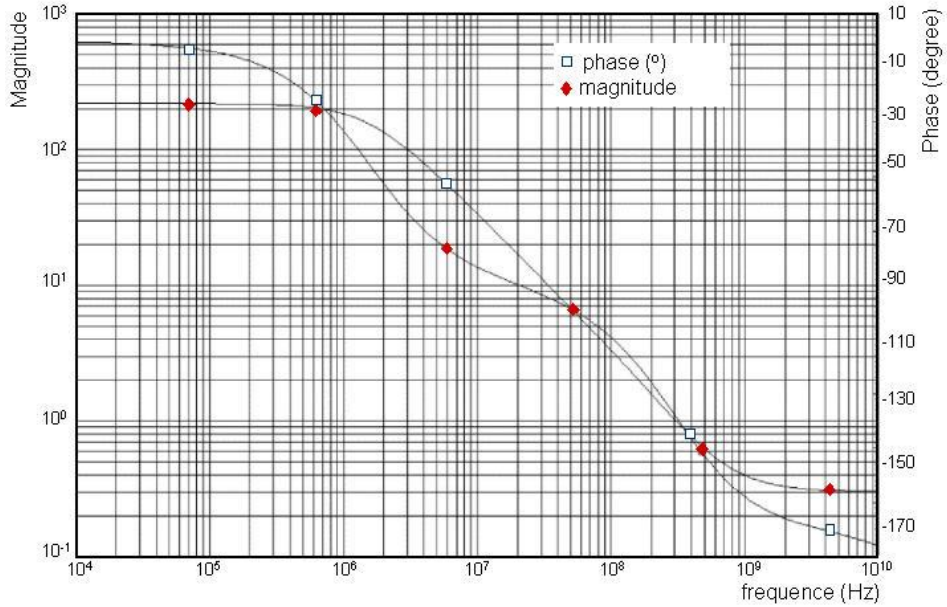
Example : designing a charge preamp (4)

- Complete schematic
  - Adding bias elements

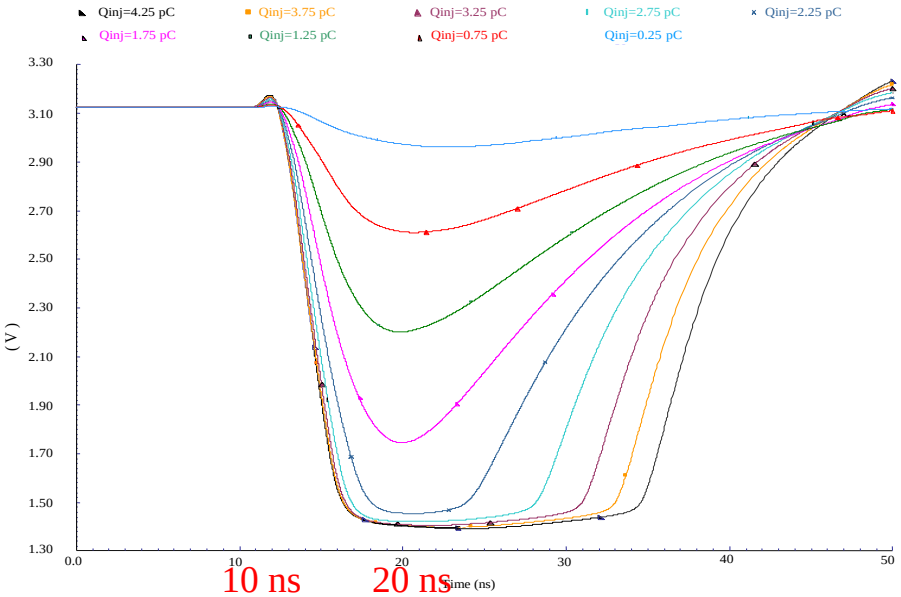


Example : designing a charge preamp (5)

- Complete simulation
  - Checking hand calculations against 2nd order effects
  - Testing extreme process parameters (« corner simulations »)
  - Testing robustness (to power supplies, temperature…)



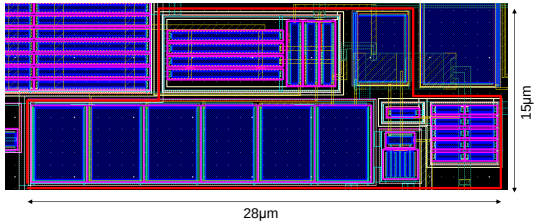
Simulated open loop gain



Saturation behaviour

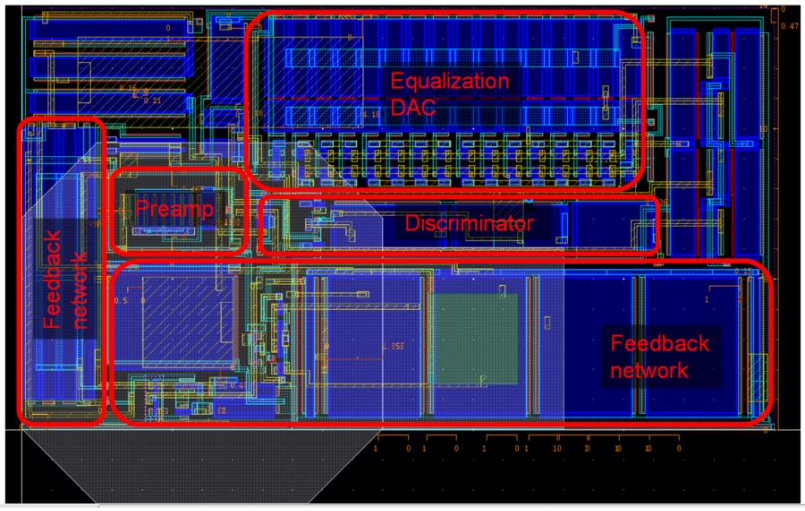
Example : designing a charge preamp (6)

- Layout
  - Each component is drawn
  - They are interconnected by metal layers



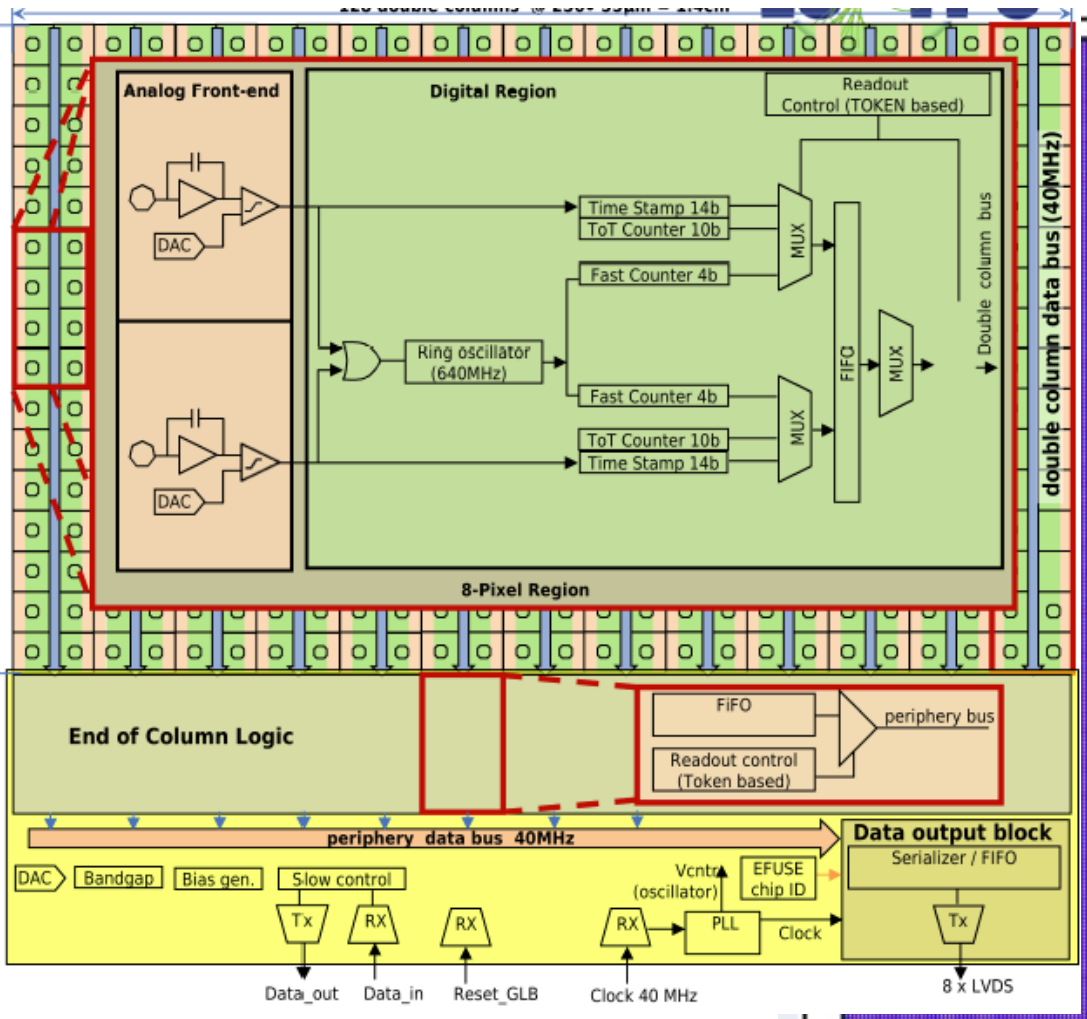
Charge preamp in 65nm
Clicpix P. Valerio (CERN 2013)

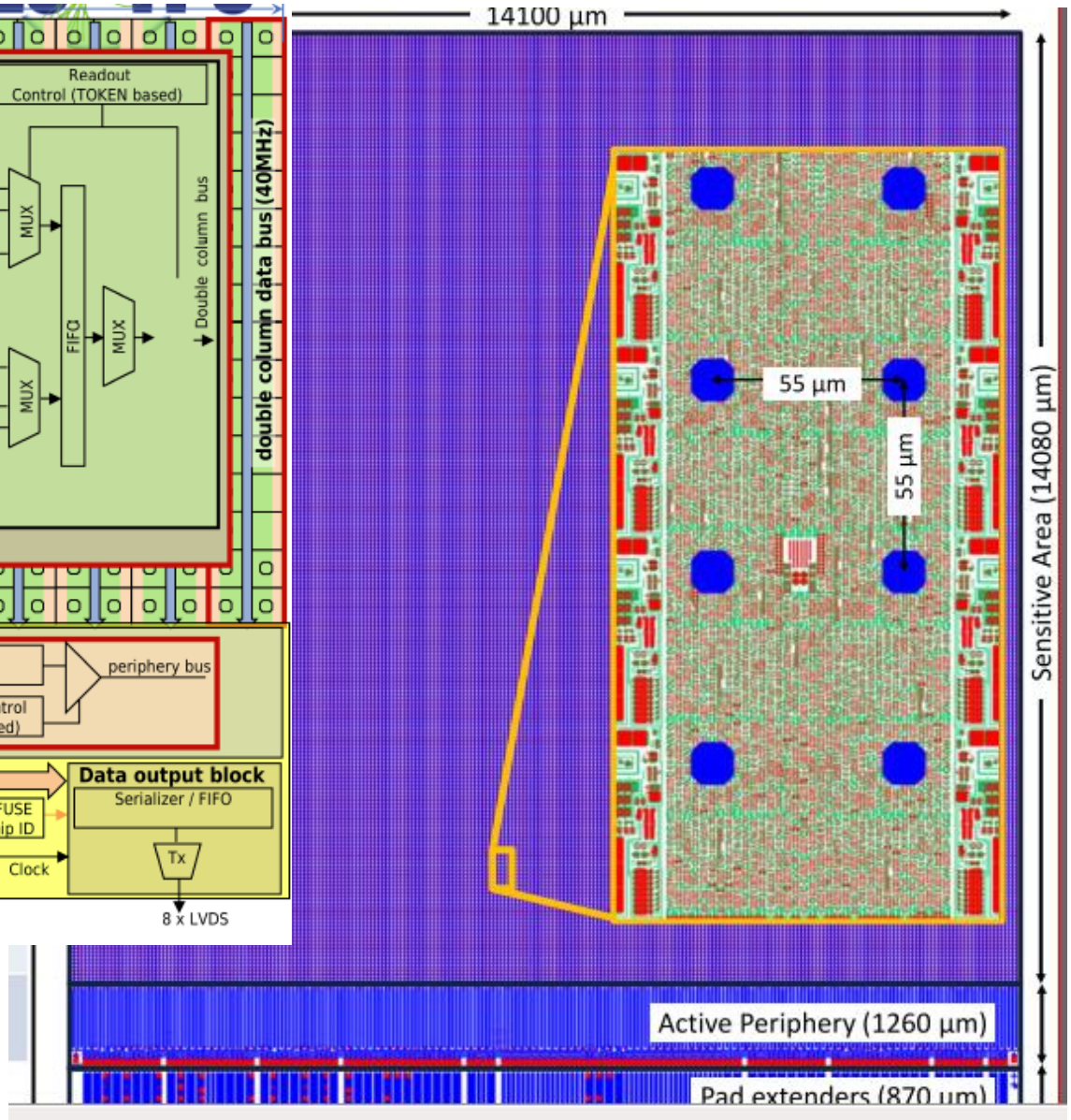
- Checks
  - DRC : checking drawing rules (isolation, minimal dimensions…)
  - ERC : extracting the corresponding electrical schematic
  - LVS (layout vs schematic) : comparing extracted schematic and original design
  - Simulating extracted schematic with parasitic elements



- Generating GDS2 file
  - Fabrication masks : « reticule »

From preamp to chip : Timepix 3…

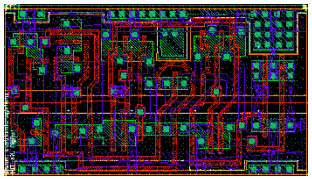


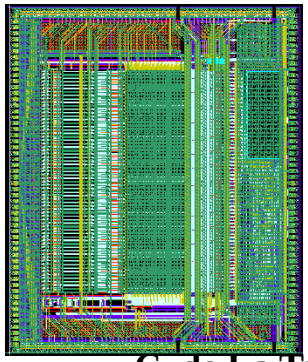


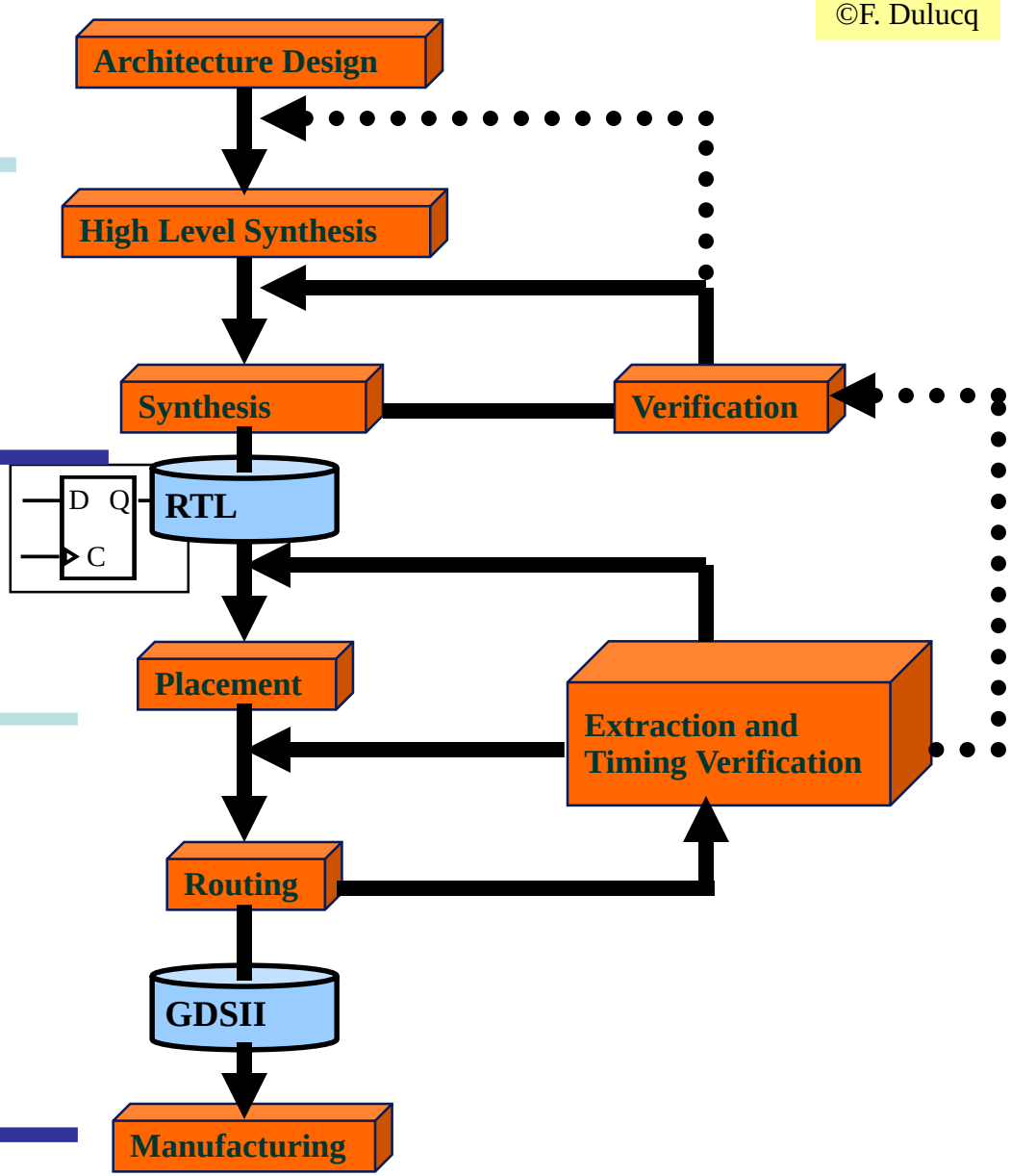
Digital implementation global Flow

©F. Dulucq

```
process(Rstb, Clk)
begin
  if Rstb ='0' then
    Q <= '0';
  elsif rising_edge Clk then
    Q <= D;
  end if;
end process;
```





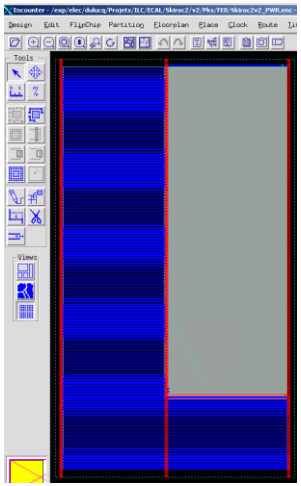


ASIC specific flow for digital routing

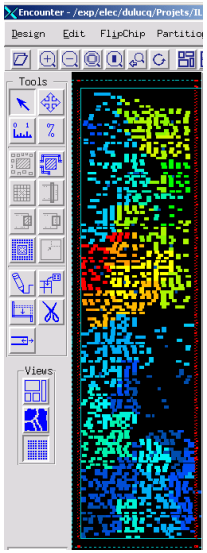
Omega

©F. Dulucq

Skiroc2 power planning



Skiroc2
clock tree



IO Pad Placement

Power planning
(Stripes & rings)

Global Placement

DFT (scan chains)

Clock Tree Synthesis

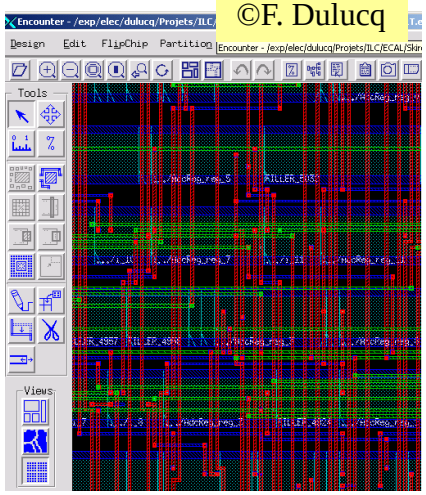
Global Routing

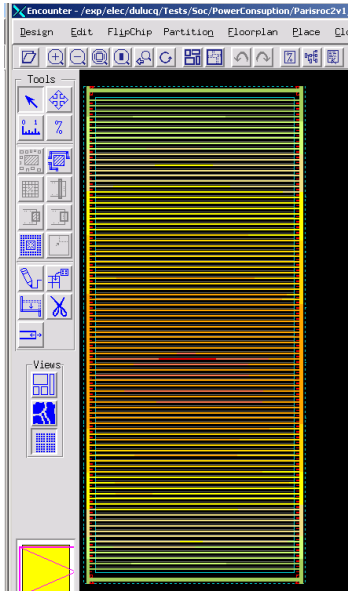
LVS / DRC
Specific Analysis (IR, Antennas)

GDS2

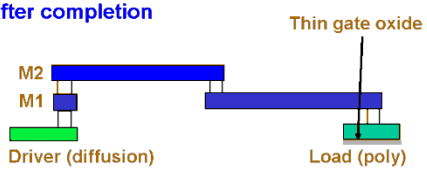
Extraction and
Delay Calc. Timing
Verification

(M1, M2, M3) =
(blue, red, green)



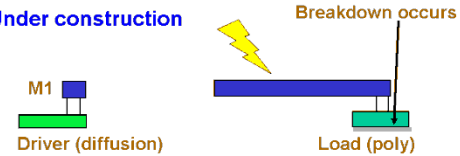


(a) After completion



Antennas fixing

(b) Under construction



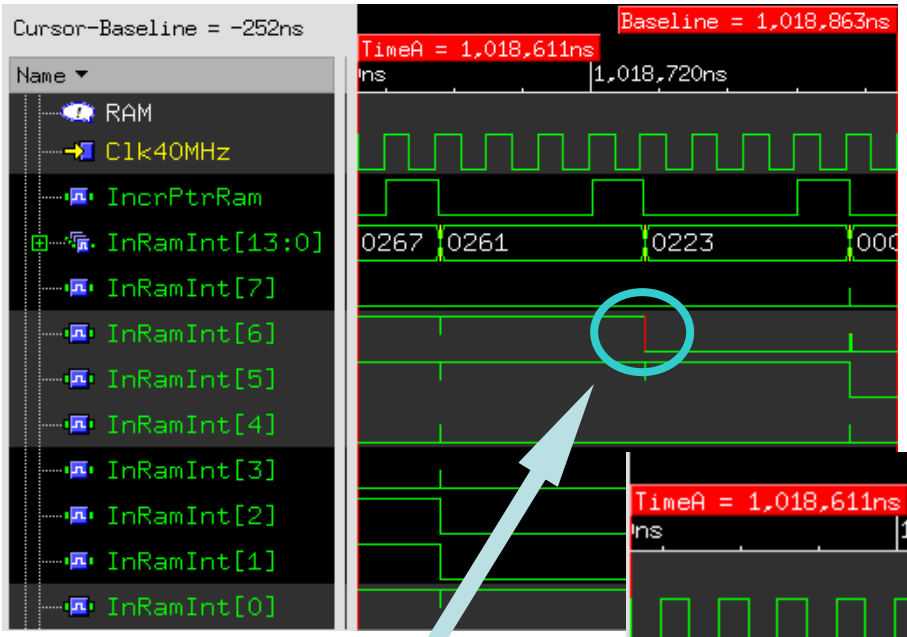
Pentium4

Parisroc2 IR drop Analysis
(red = drop > 5mV)

Post layout simulation (extracted RC)

©F. Dulucq

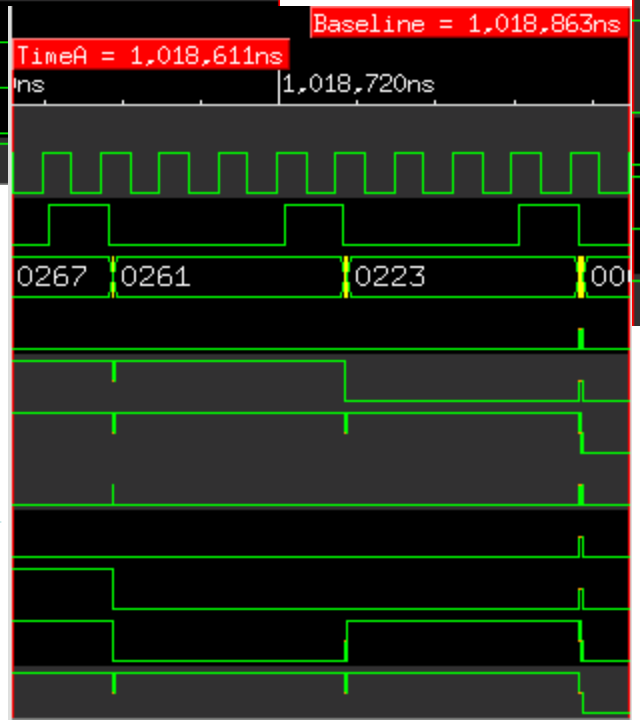
MIN PVT (1.6 ; 3.6V ; -50°C)



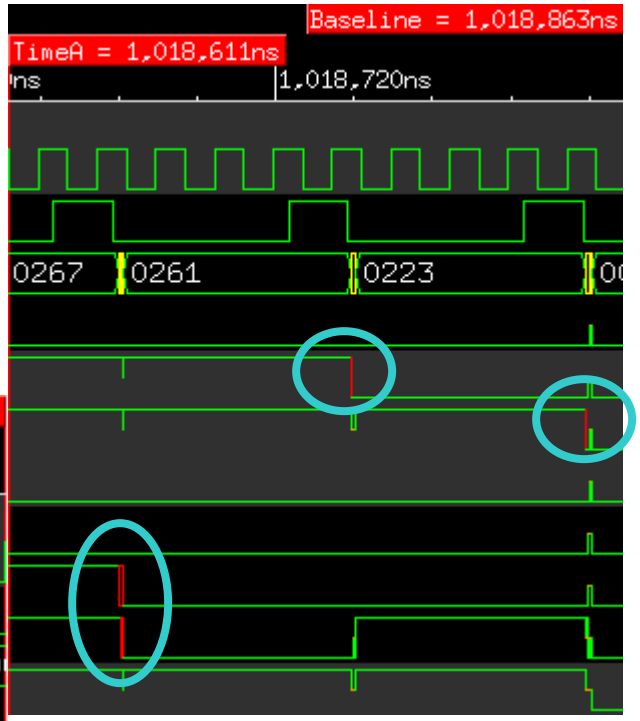
1 violations

TYP PVT (1 ; 3.3V ; 25°C)

0 violations



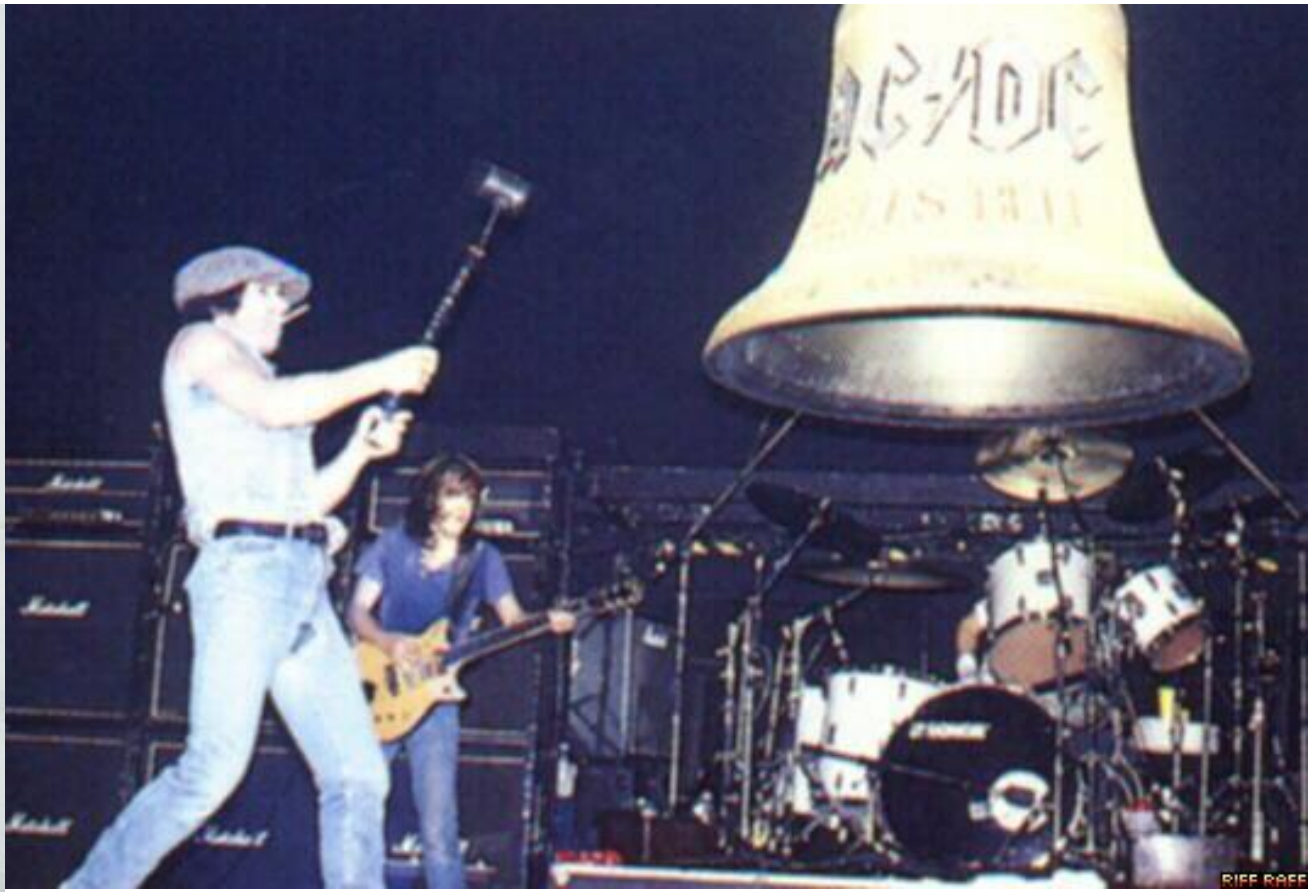
MAX PVT (1.4 ; 3V ; 125°C)



4 violations

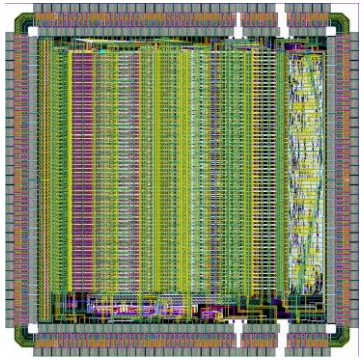
Electromagnetic compatibility (EMC-EMI)

- Coexistence analog-digital
  - Capacitive, inductive and common-impedance couplings
  - A full lecture !
  - A good summary : there is no such thing as « ground », pay attention to current return



(R)evolution of analog electronics (2)

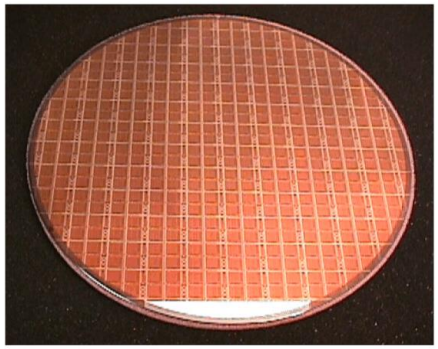
- ASICs : Application Specific Integrated Circuits
  - Access to foundries through multiproject runs (MPW)
  - Reduced development costs : 600-1000 €/mm^2 compared to dedicated runs (50-200 k€)
  - Full custom layout, at transistor level
  - mostly CMOS & BiCMOS



MAROC : 64ch
MaPMT readout chip

- Very widespread in high Energy Physics
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better performance : reduction of parasitics
  - Better reliability (less connections)
  - But longer developpement time

- Trends :
  - Evolution of technologies (see next slides)
  - Low power design

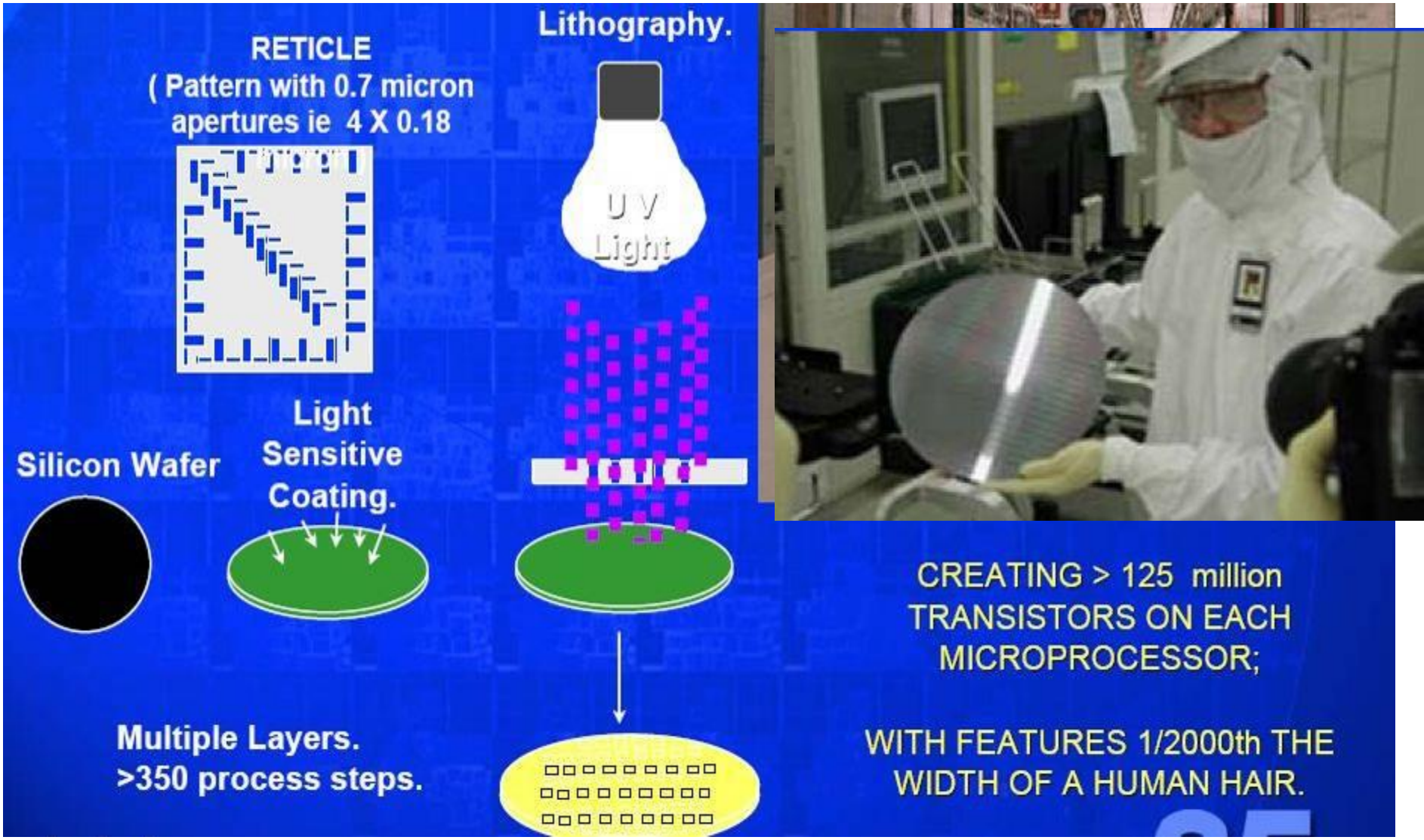


300 mm wafer

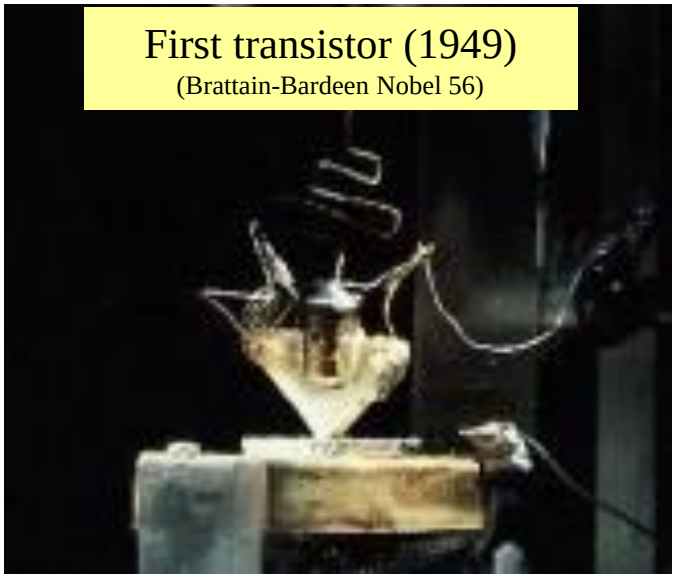
Processing of ASICs

© Intel

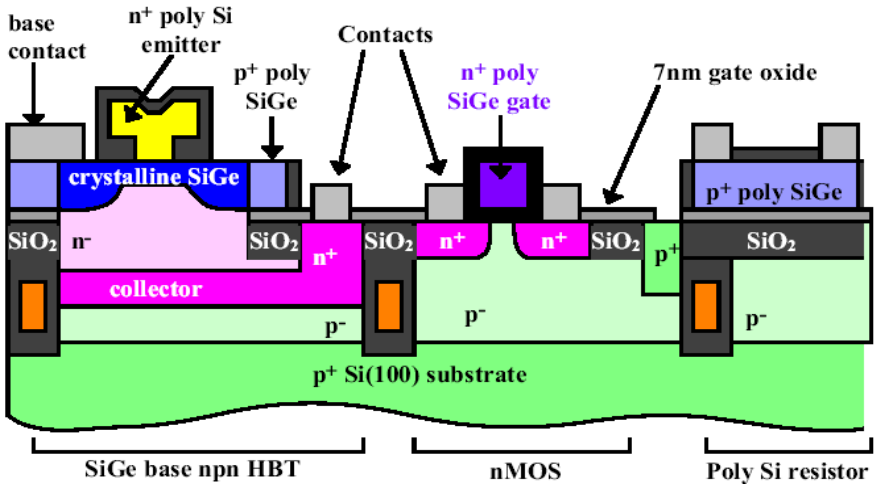
- From Sand to ICs…



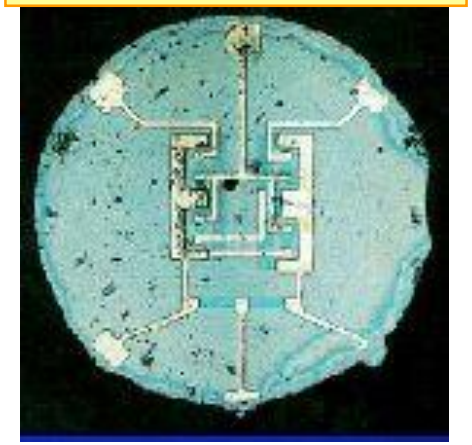
Evolution of technologies



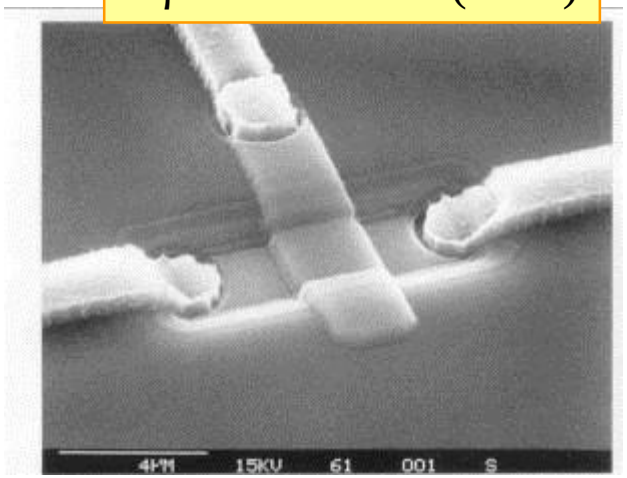
SiGe Bipolar in 0.35µm monolithic process



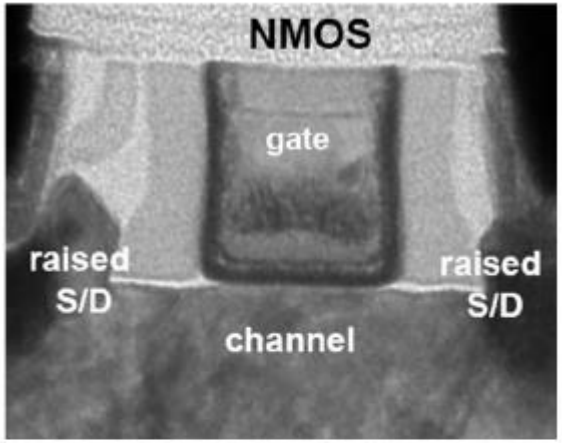
First planar IC (1961)



5 µm MOSFET (1985)

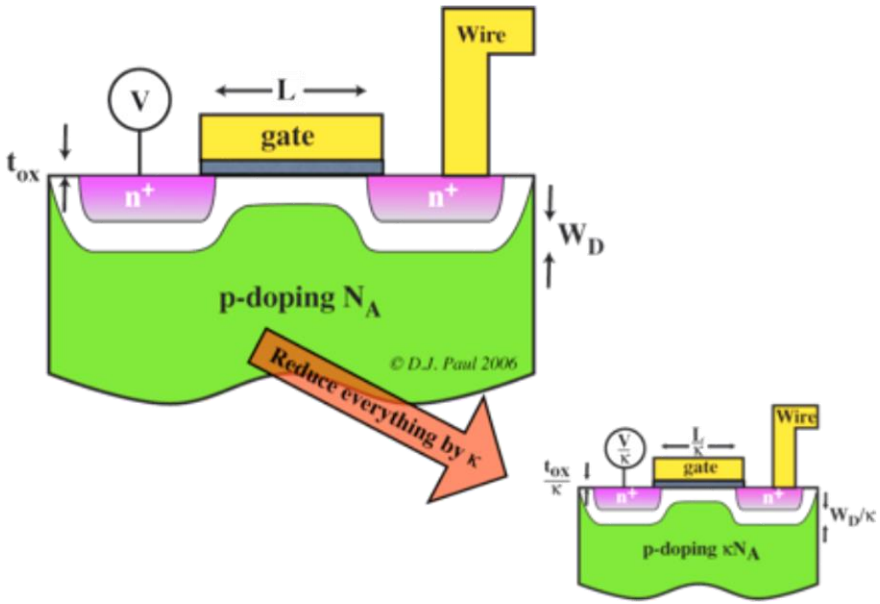


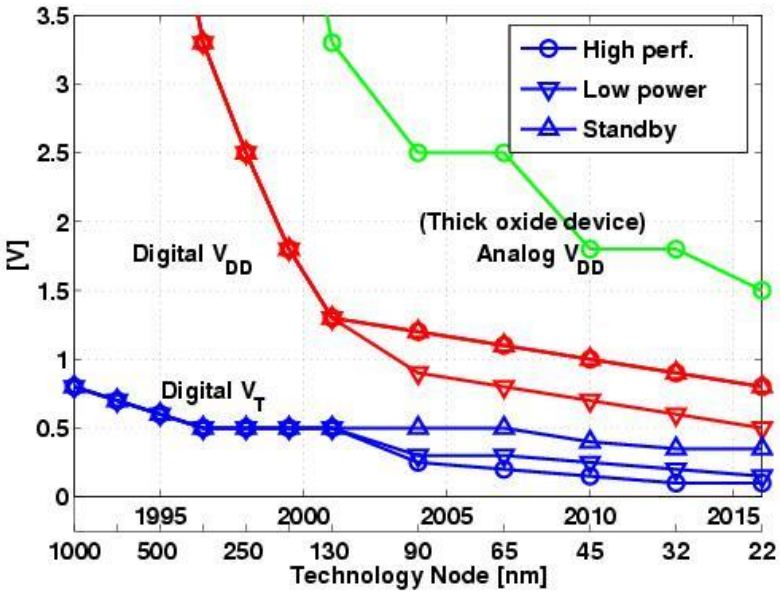
32 nm MOSFET (2010)



CMOS scaling

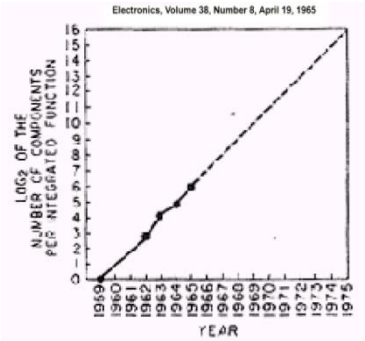
- Reduction of dimensions
  - « Quasi-constant voltage scaling »
  - Decrease of W,L,tox
  - (partial) decrease of V_{DD} et V_{Th}
- Improvement of speed as $1/L^2$
  - Improvement of transconductance as W/L and reduction of capacitance as WL
- Power increases as k and power density even worse
  - VDD does not scale as L

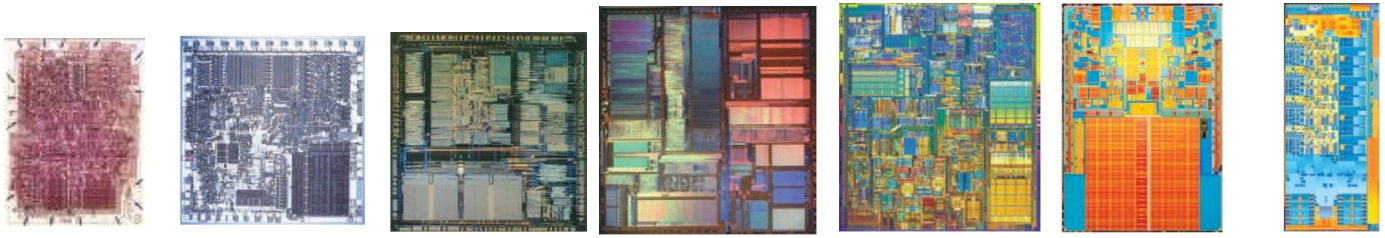




Evolution of CMOS technologies

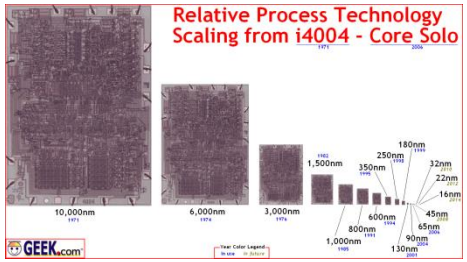
- Moore's law : number of transistors doubling every ~2 years
- Technology nodes (gate length) *0.7 every 2 years



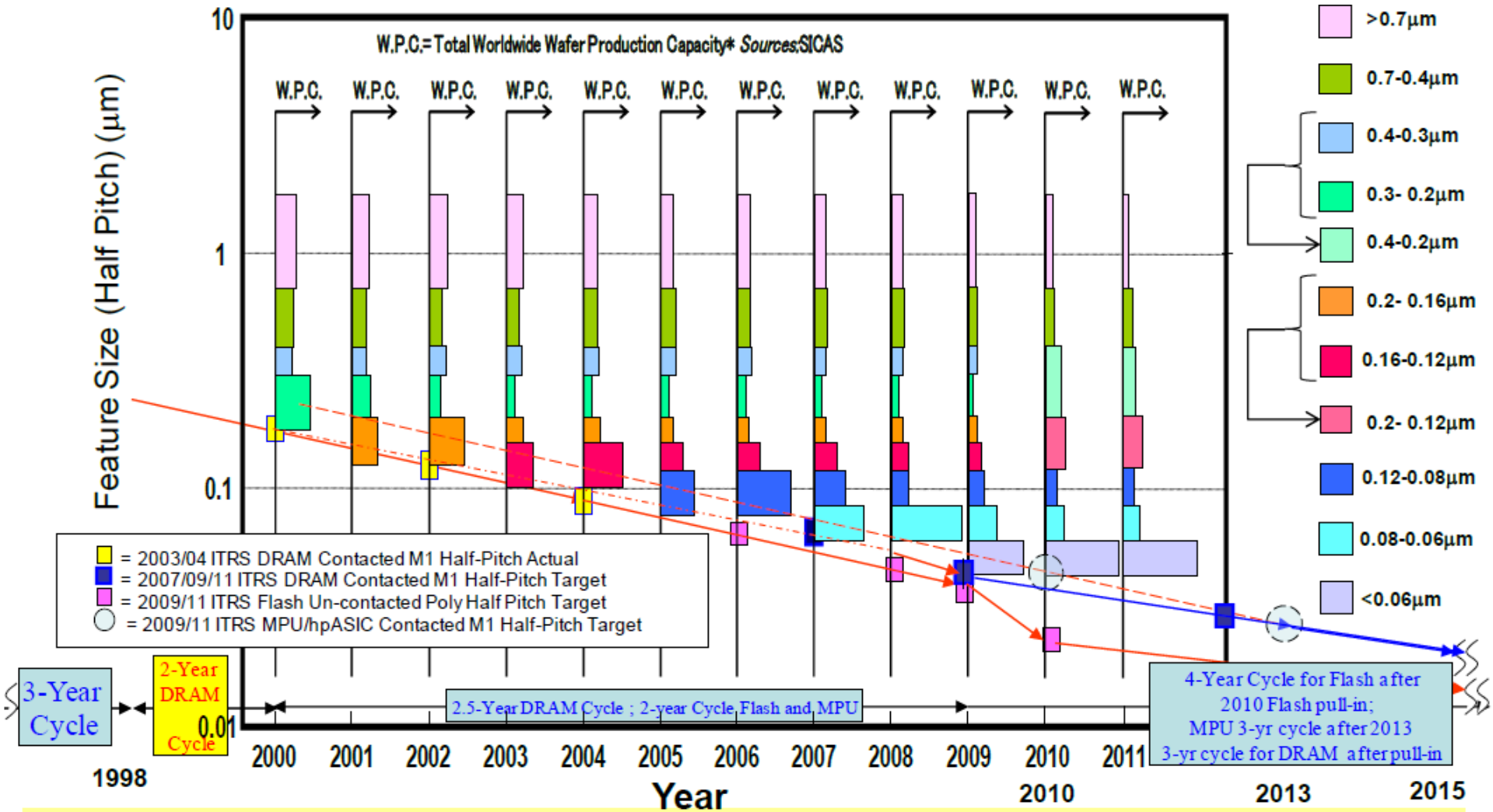


Processor	4004	8086	i386	Pentium	Pentium 4	Core2	3G Core7
Year	1971	1978	1985	1993	2000	2007	2012
Clock	108 kHz	10 MHz	16 MHz	66 MHz	1.5 GHz	2.4 GHz	2.9 GHz
Technology	10 µm	3 µm	1.5 µm	0.8 µm	0.18 µm	65 nm	22 nm
Nb transistors	2300	29000	275000	3.1M	42M	291M	1.4G

http://www.intel.com/content/www/us/en/history



ITRS 2011 roadmap



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 1Q data for 2011. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf

© K. Troki (CMP)

Example of prices, prototyping

CNRS – INPG – UJF

CMOS	.35 µ	AMS	650 €/mm²
CMOS opto	.35 µ	AMS	810 €/mm²
CMOS HV	.35 µ	AMS	1000 €/mm²
CMOS	130nm	ST	2200 €/mm²
CMOS	65 nm	ST	7500 €/mm²
CMOS	40 nm	ST	15000 €/mm²
SiGe BiCMOS	.35 µ	AMS	890 €/mm²
SiGe:C BiCMOS	130nm	ST	3500 €/mm²
SOI	130nm	ST	4000 €/mm²
SOI	65nm	ST	9500 €/mm²
Poly-SOI-Metal	MUMPS	MEMSCAP	3700 €/cm²

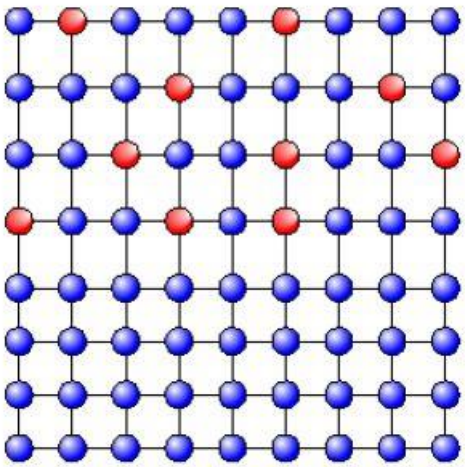
CMP annual users meeting, January 20th 2011, PARIS

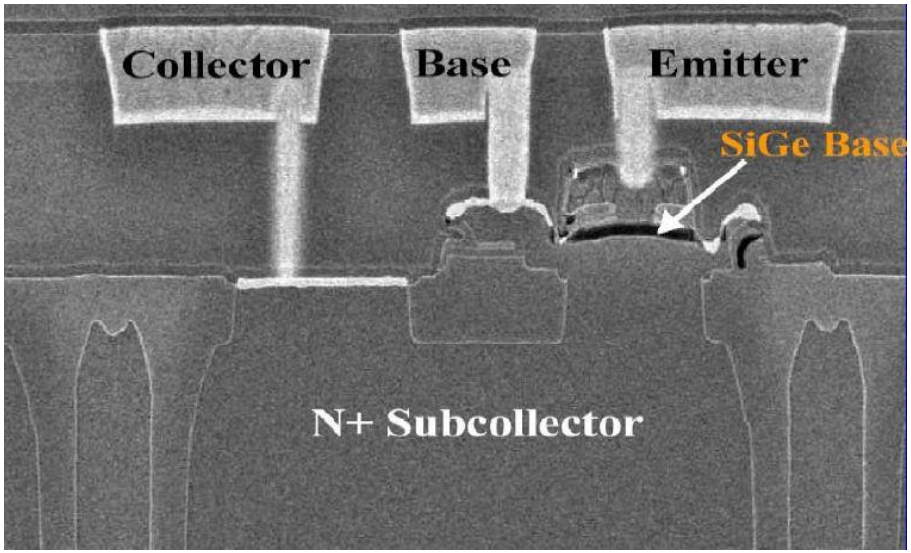
http://cmp.imag.fr/aboutus/slides/Slides2011/02_Runs_2011.pdf

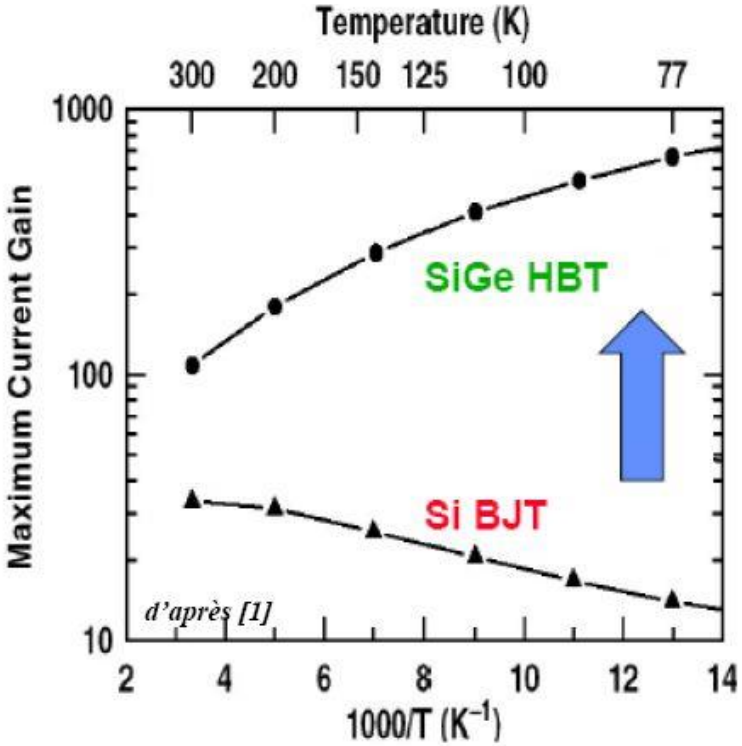
SiGe technology

© R. Hermel

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixe

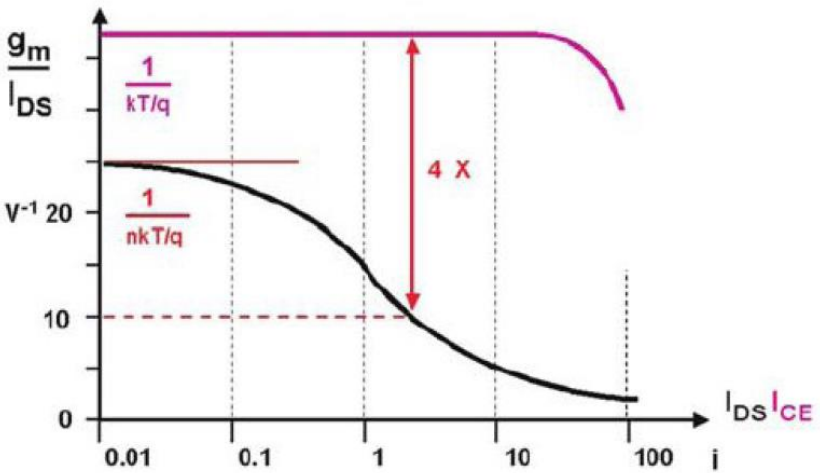


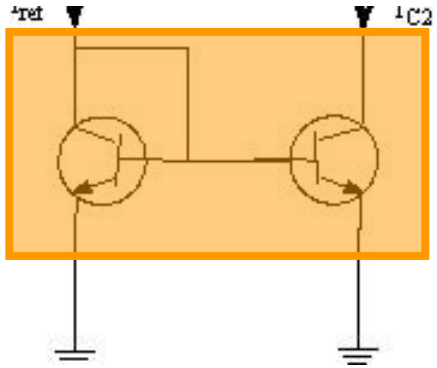


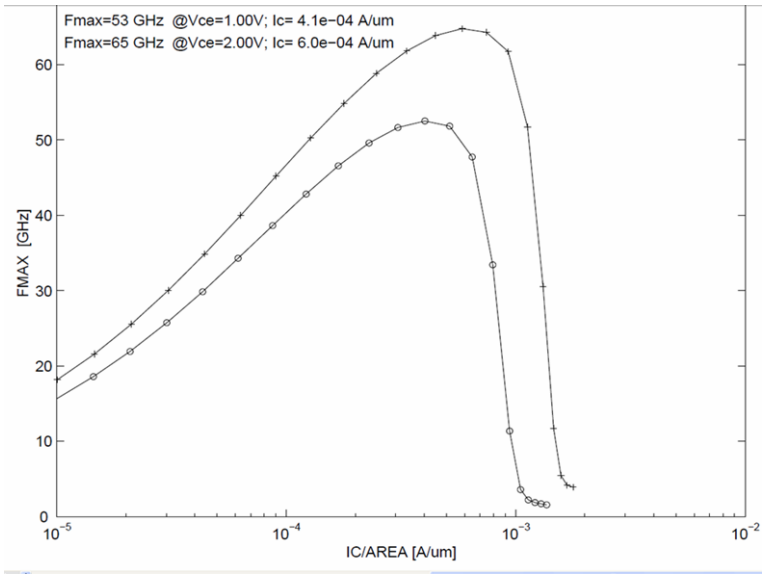


Power and speed with SiGe

- BJT : best g_m /I ratio (1/U_T)
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance (A~mV*µm)
- $V_{BE} = V_T \mathrm{Ln}(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T

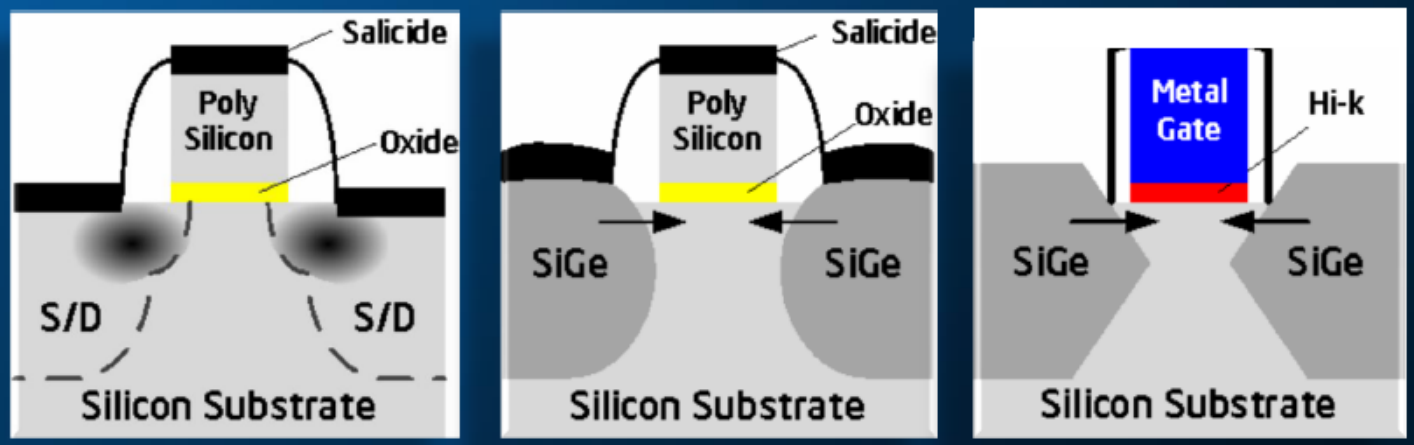






Intel CMOS Transistor Architecture Evolution in the Last Decade

.13 um and before	90nm/65 nm	45 nm/32 nm
Traditional	Strained Silicon	High k/Metal Gate + Strained Silicon



CMOS scaling has evolved from classical dimensional scaling to modern scaling with innovations in structures and materials

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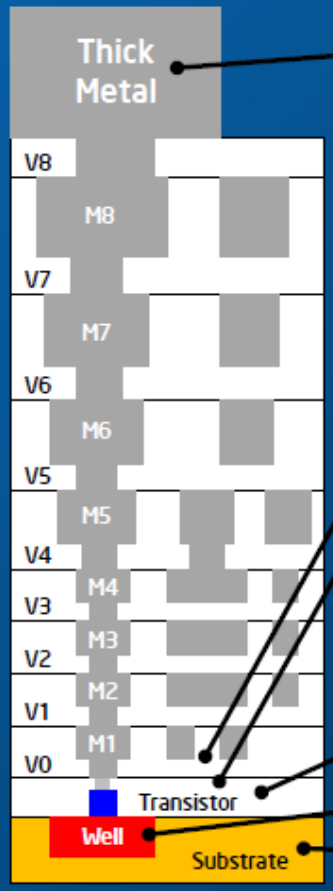
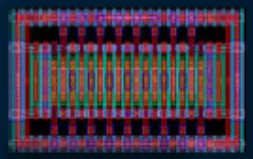
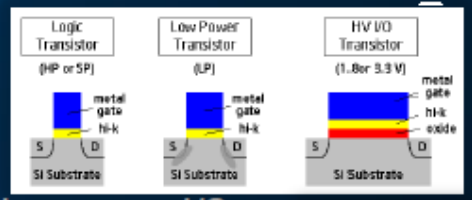
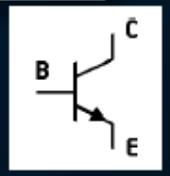
32 nm RF CMOS Technology

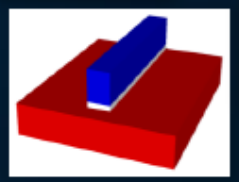


- TM1 Inductor: high Q and density
- Passives:
  - Precision Resistor
  - High Q Inductor
  - High Density Decap
- HV PA Transistor
- RF Transistor: Templates/Modeling
- Transistor:
  - Logic, low power, I/O
  - JFET, BJT
- Well: Triple Well/Deep Nwell
- Substrate: High Resistivity

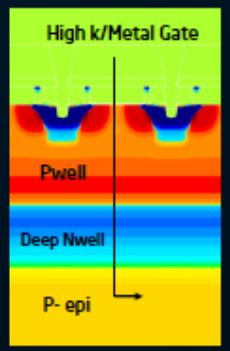








RF Models



Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements

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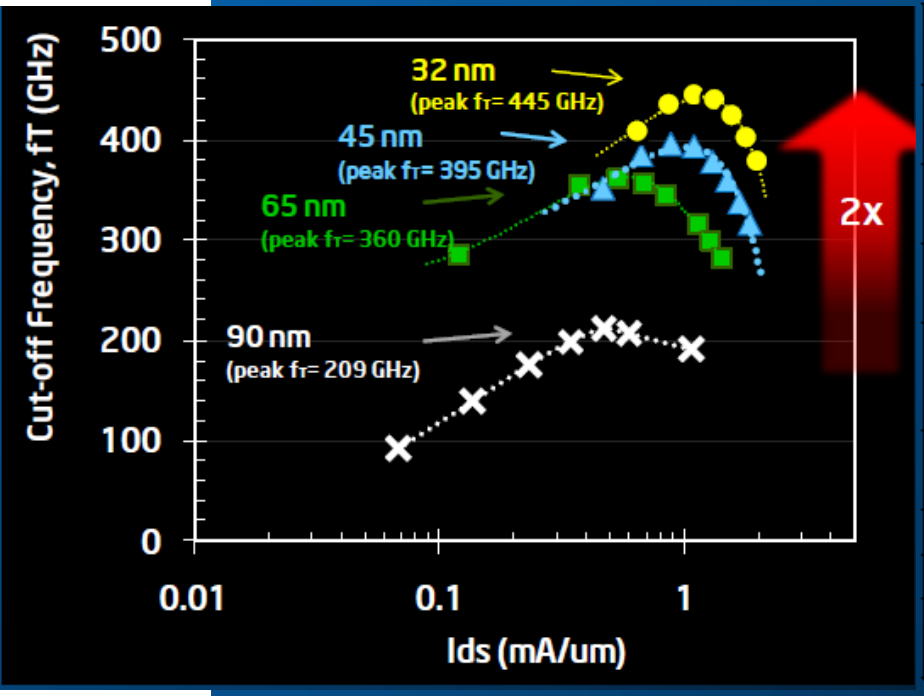
RF CMOS Technology Performance Metrics



RF Devices	RF Circuits	Key Device Characteristics
Logic Transistor	MAC/BB, ADC, DAC	Idsat, Idlin, Vt, Ioff
Analog Transistor	ADC, DAC, MAC/BB	Gm, Rout, Matching, Linearity, Noise, NF_{min}
RF Transistor	PA, Mixer, T/R Switch	f_T, f_{max}, 1/f Noise, NF_{min}
PA Transistors	PA	Ron, Linearity, f_T, f_{MAX}, Efficiency, Breakdwn V,
Precision Resistors	ADC, DAC, BB Filter, others	R, σR/R, Matching
Linear Capacitors	PLL, VCO	C, Q, Matching
Varactors	PLL, VCO	Tuning Ratio, Q, Kv_{CO},
Inductor/ Transformer/Balun	PA, LNA, Mixer	L, Q

What are the impacts of CMOS scaling on these metrics ?

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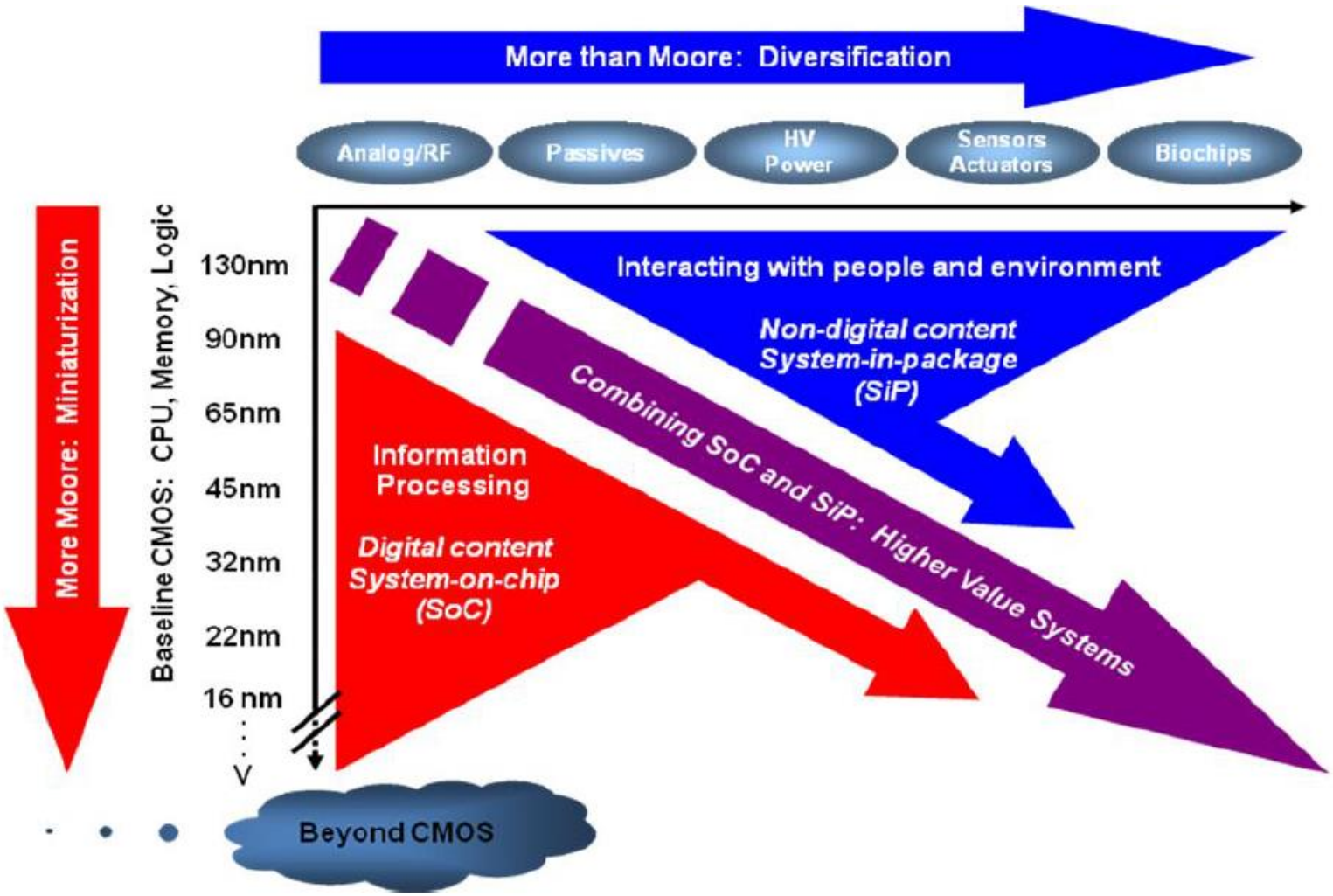
« Moore » and « More than Moore »



Generic MOSFET scaling trends

Novel materials and architectures

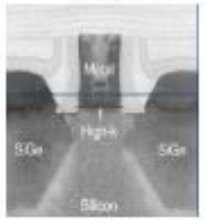
http://www.sematech.org/meetings/archives/symposia/9027/pres/Session%202/Jammy_Raj.pdf

New Mat'l/Structure

High-K
MG

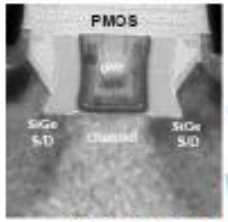
planar

45nm
2007



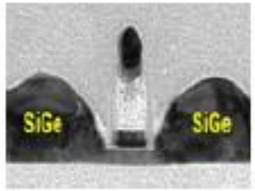
(Production)
Intel IEDM 2007

32nm
2009



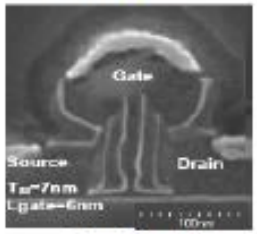
(Production)
Intel IEDM 2009

22nm
2011+



IBM, IEDM 2009

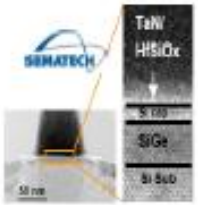
16nm (?)
2013+



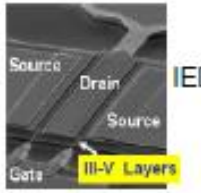
6nm Length
B. Doris IEDM 2002

12 nm + (2015+)

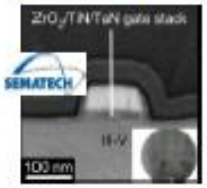
Si-Ge Device



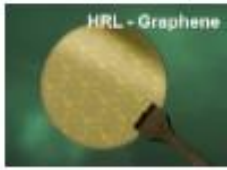
III-V Device



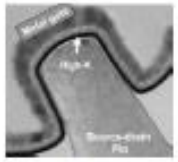
Intel,
IEDM 2007,9



T-FET

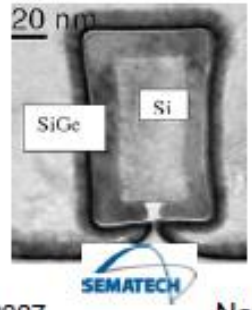


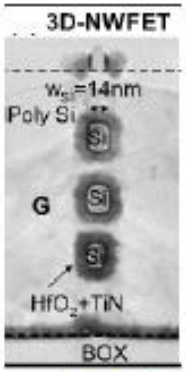
Non-planar



Intel Tri-Gate,
VLSI 2006

NXP FINFET, VLSI 2007

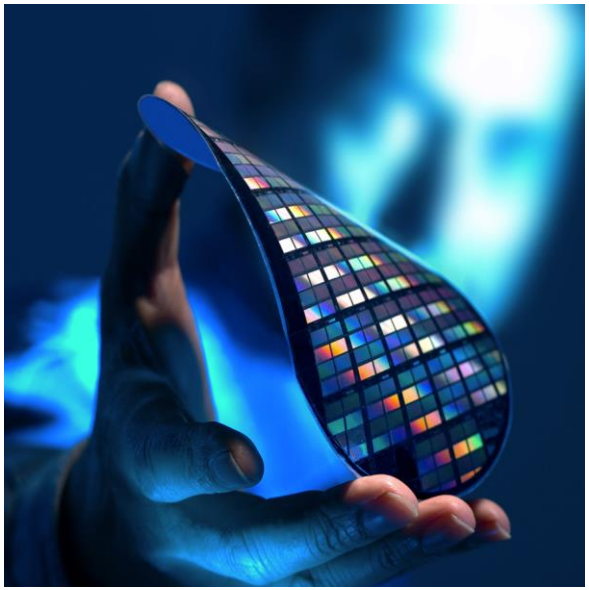


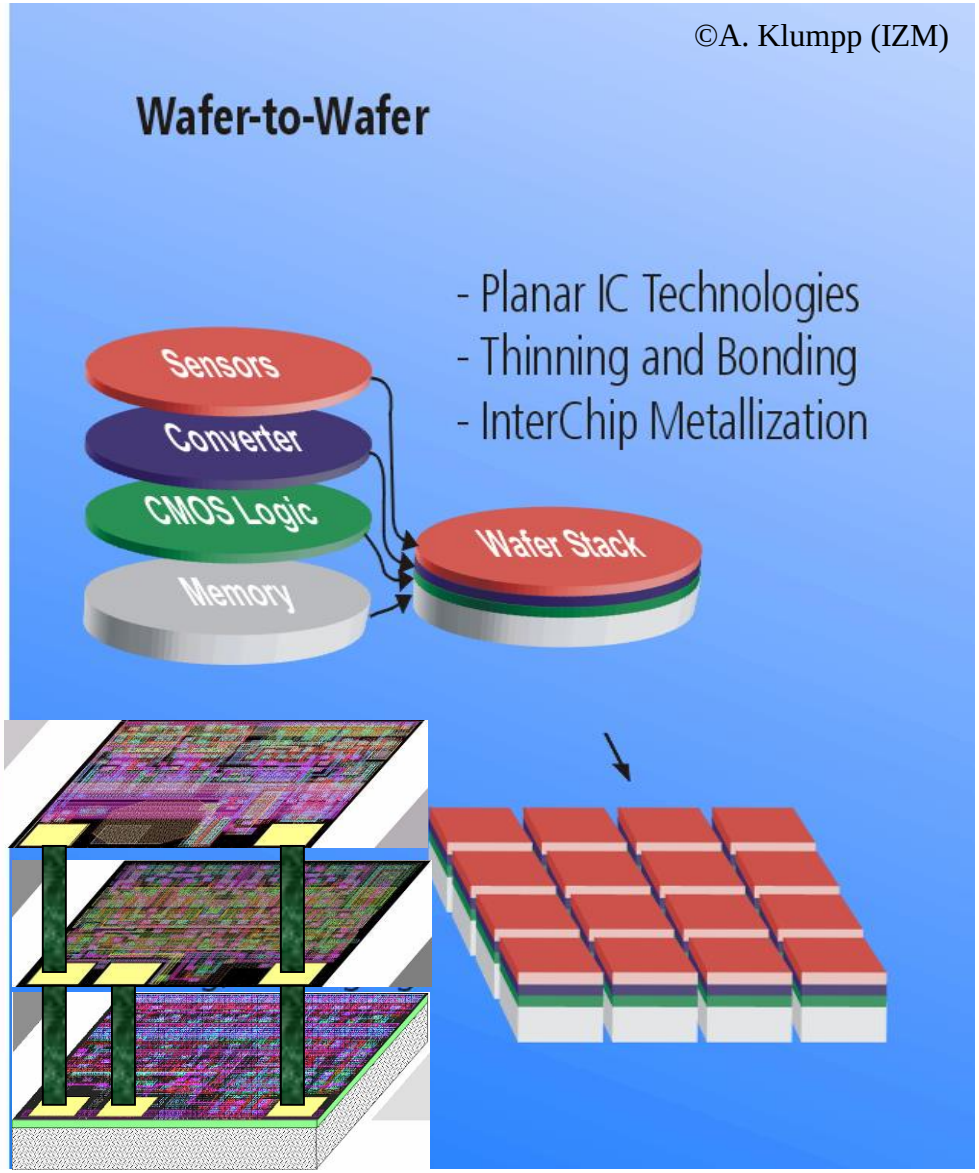


Nano-wire (LETI IEDM'08)

3D technology

- Increasing integration density, mixing technologies
- Wafer thinning to <50 µm
- Minimization of interconnects
- Large industrial market
  - Processors, image sensors…

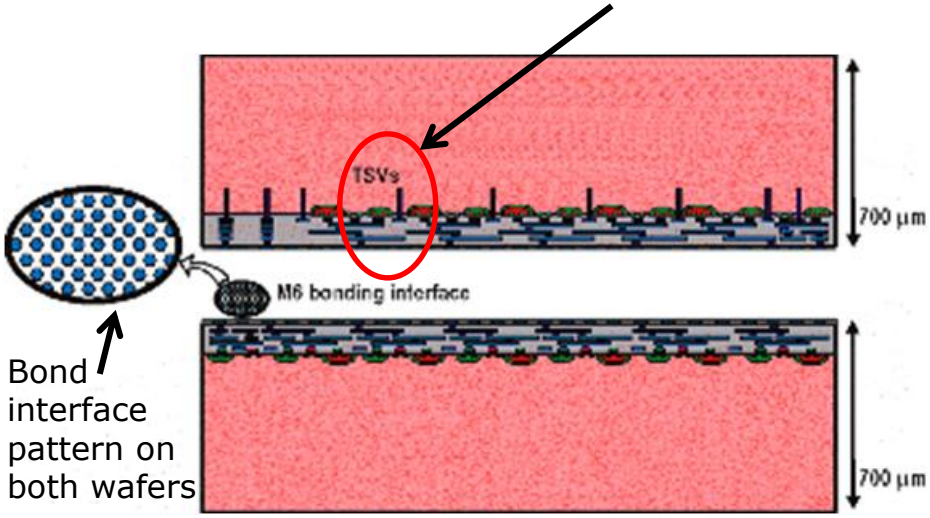




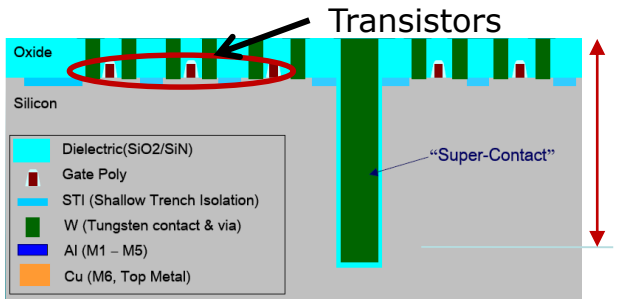
3D technology in HEP

© R. Yarema (FNAL)

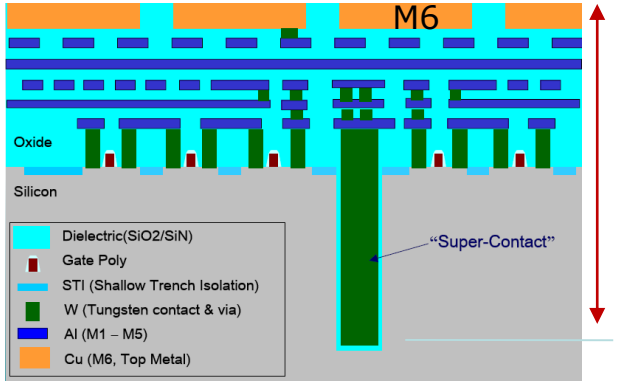
- Access to 3D via Tezzaron
  - 130 nm Global foundry wafers
  - 1µm vias (Via middle process)
  - Cu-Cu bonding face to face

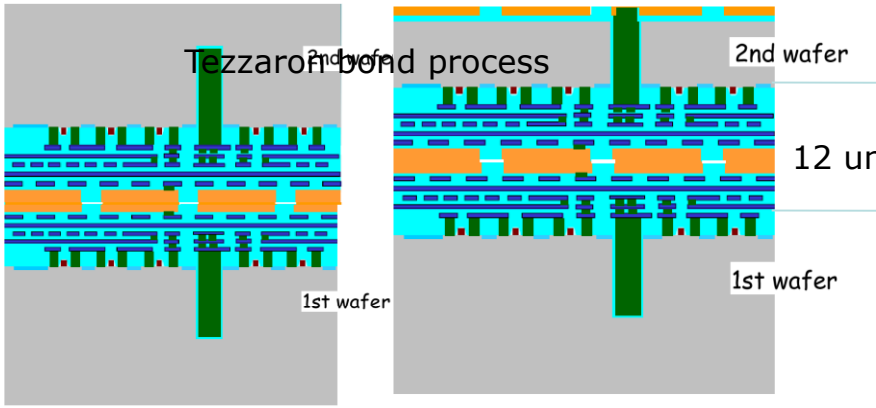


After FEOL fabricate 6 um super contact (via)

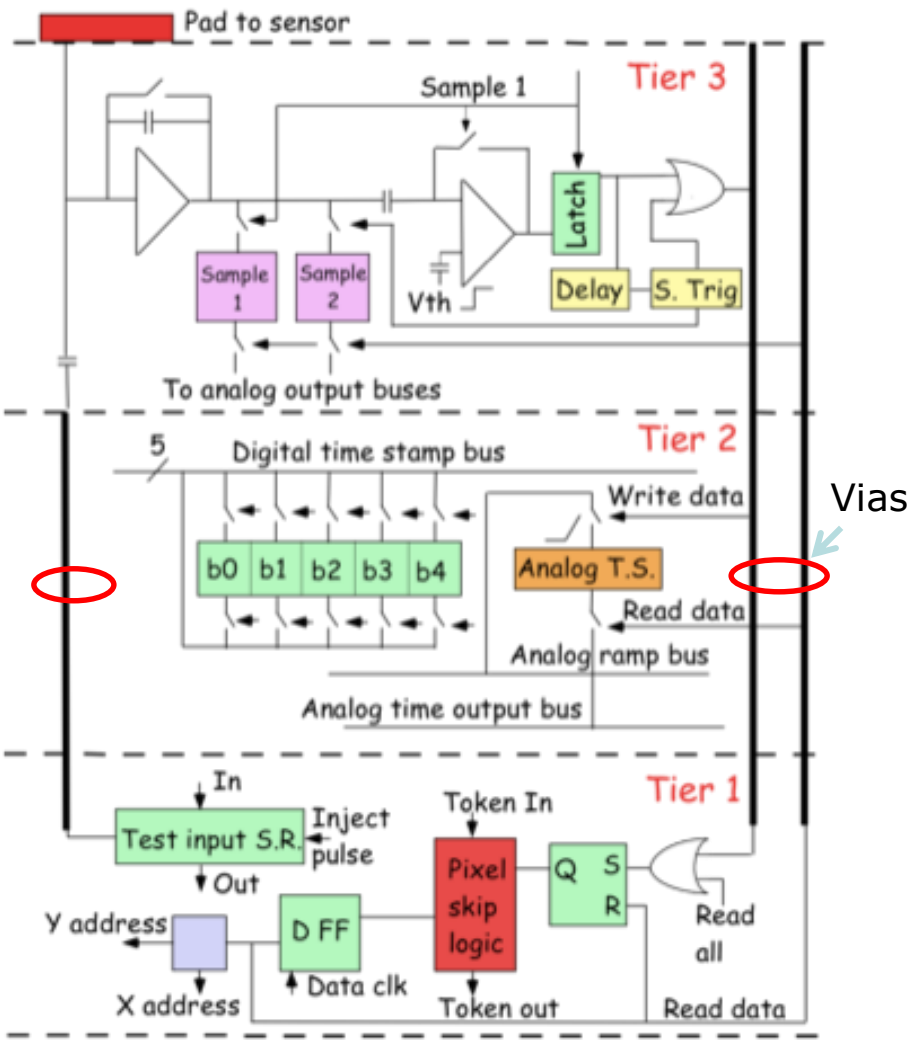


Complete BEOL processing

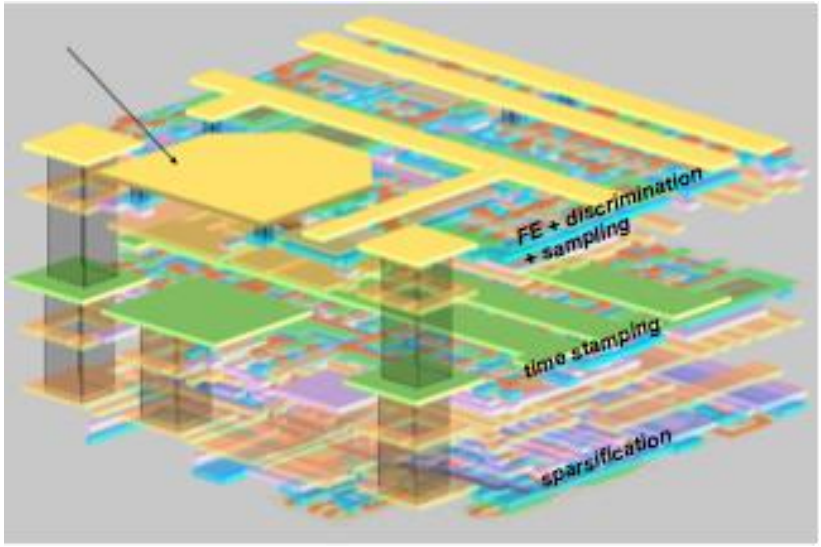




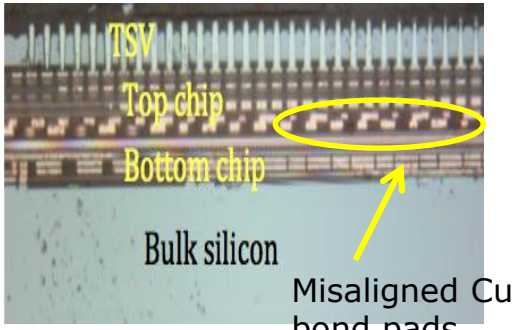
Exampe of realization at FNAL



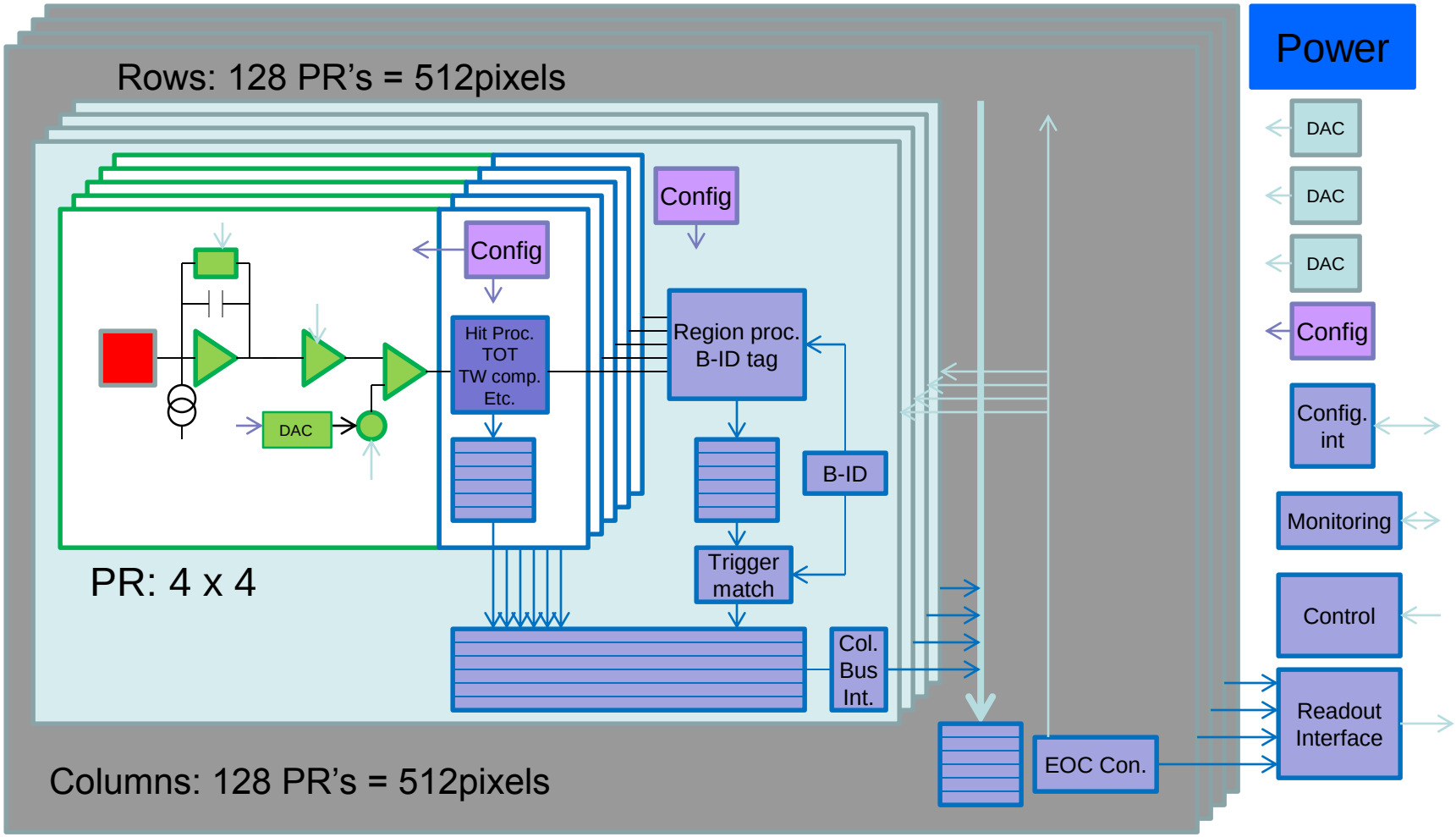
© R. Yarema (FNAL)



V1P1 3D chip by FNAL



General pixel chip architecture



- Pixels: 4 x 4 x ~128 x ~128 = ~256k (262144)
- Chip size = ~50um x 4 x 128 = ~2.6cm x ~3cm (Yield maximization required)
- Obviously resembles LHCb/ALICE, FEI4, LHCb Velopix and other high rate pixels
  - And any other data driven (HEP) chip/system: System on a chip

Medipix related hybrid pixel readout chips

Medipix1 (1998)	*1μm SACMOS, 64x64 pixels, 170x170μm²* *PC / Frame based readout*
Medipix2 (2001)	*0.25μm CMOS, 256x256 pixels, 55x55μm²* *PC / Frame based readout*
Timepix (2006)	*0.25μm CMOS, 256x256 pixels, 55x55μm²* *PC, ToT, ToA / Frame based readout*
Medipix3 (2009)	*0.13μm CMOS, 256x256 pixels, 55x55μm²* *PC / Frame based readout* *Event by event charge reconstruction and allocation*
Dosepix (2011)	*0.13μm CMOS, 16x16 pixels, 220x220μm²* *ToT, PC / Rolling shutter (programmable column readout)* *Event by event binning of energy spectra (16 digital thrs)*
Timepix3 (2013)	*0.13μm CMOS, 256x256 pixels, 55x55μm²* *PC; ToT, ToA (simultaneous)/ Data driven readout*
Velopix	*0.13μm CMOS, 256x256 pixels, 55x55μm²,* *ToA, Binary/ToT (TBD), Data driven readout*
Smallpix	*0.13μm CMOS, 512x512 pixels, 40x40μm² (TBD), TSV compatible* *PC, iToT; ToA, ToT1 (simultaneous)/ Frame based (ZC)*
Clicpix prototype (2013)	*65nm CMOS, 64x64 pixels, 25x25μm²* *ToA, ToT1 (simultaneous)/ Frame based (ZC)*

Summary of lecture 2

- Performant design is at transistor level
- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex

10 ans d'évolution des spécifications techniques pour la réalisation d' ASIC

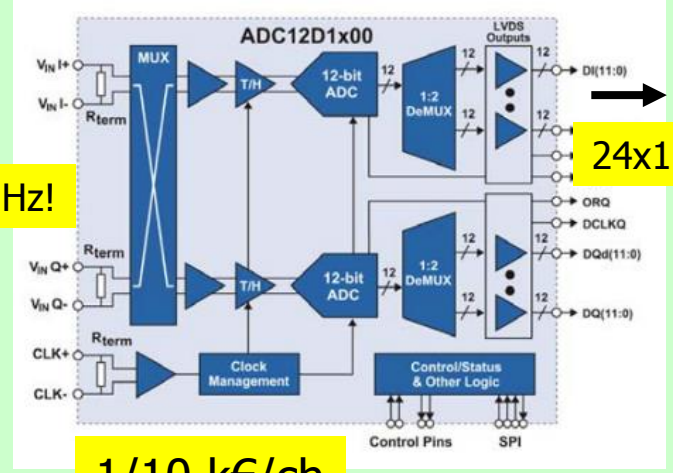
G. Deptuch, Fermilab

Waveform digitizers [S. Ritt PSI]

Ωmega

FADCs

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s

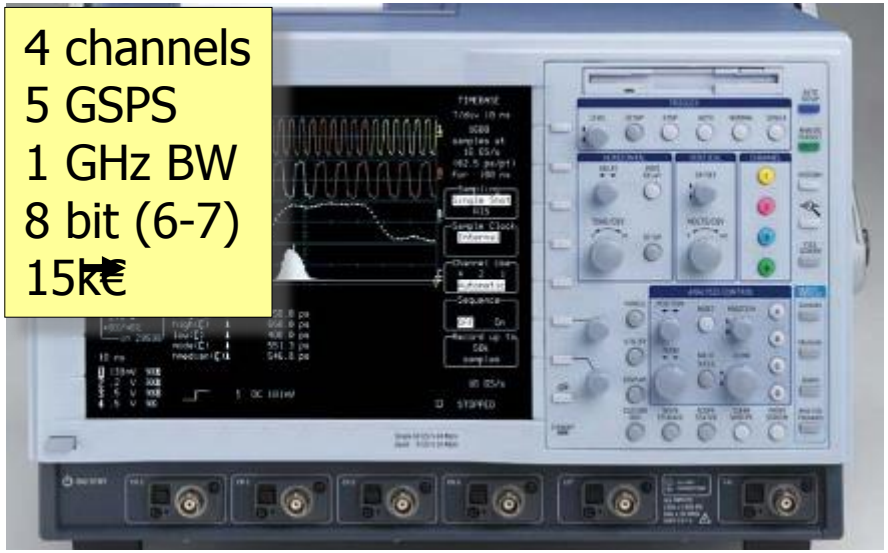


1.8 GHz!

24x1.8 Gbits/s

1/10 k€/ch

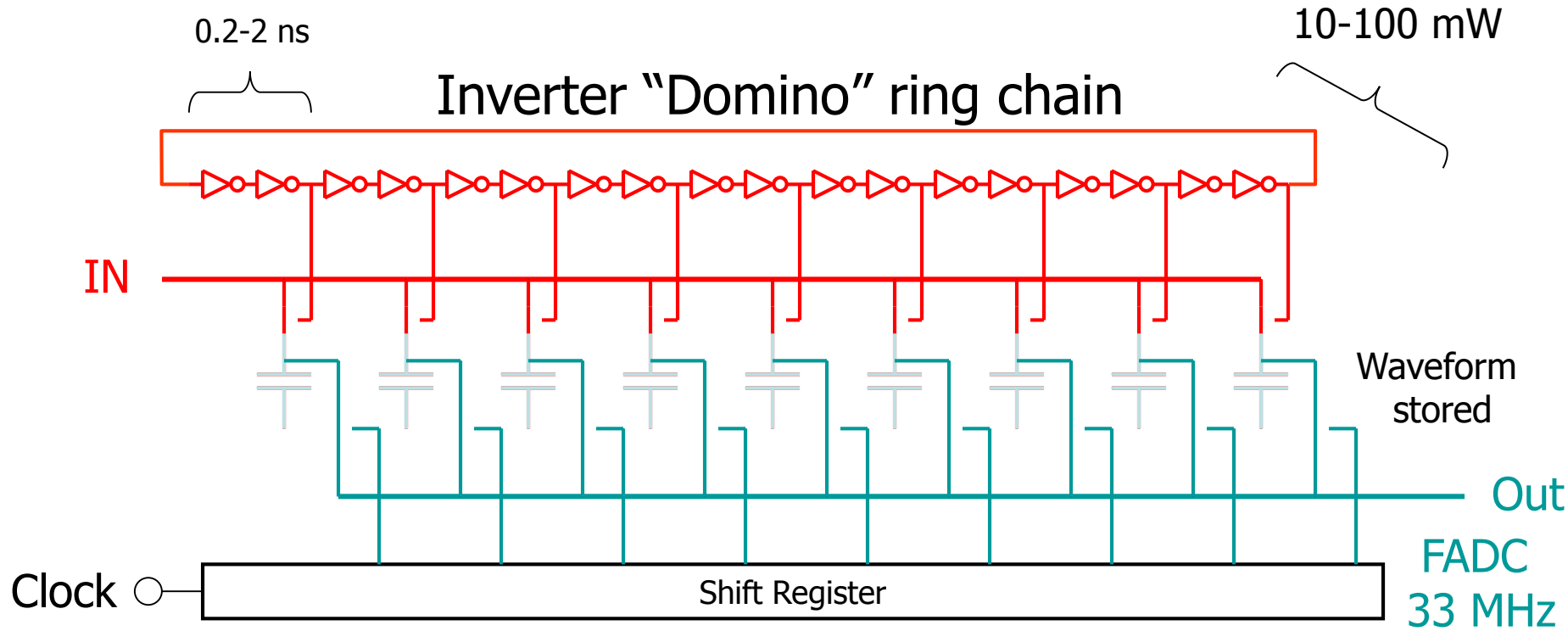
PX1500-4:
2 Channel
3 GS/s
8 bits

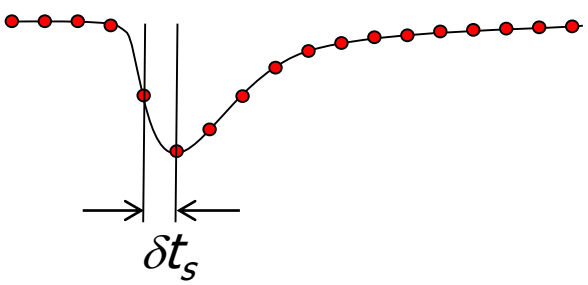


4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15k€

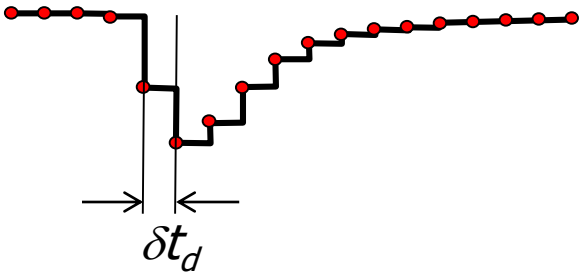
4 channels
5 GSPS
1 GHz BW
11.5 bits
900€
USB Power

Switched Capacitor Array (Analog Memory)

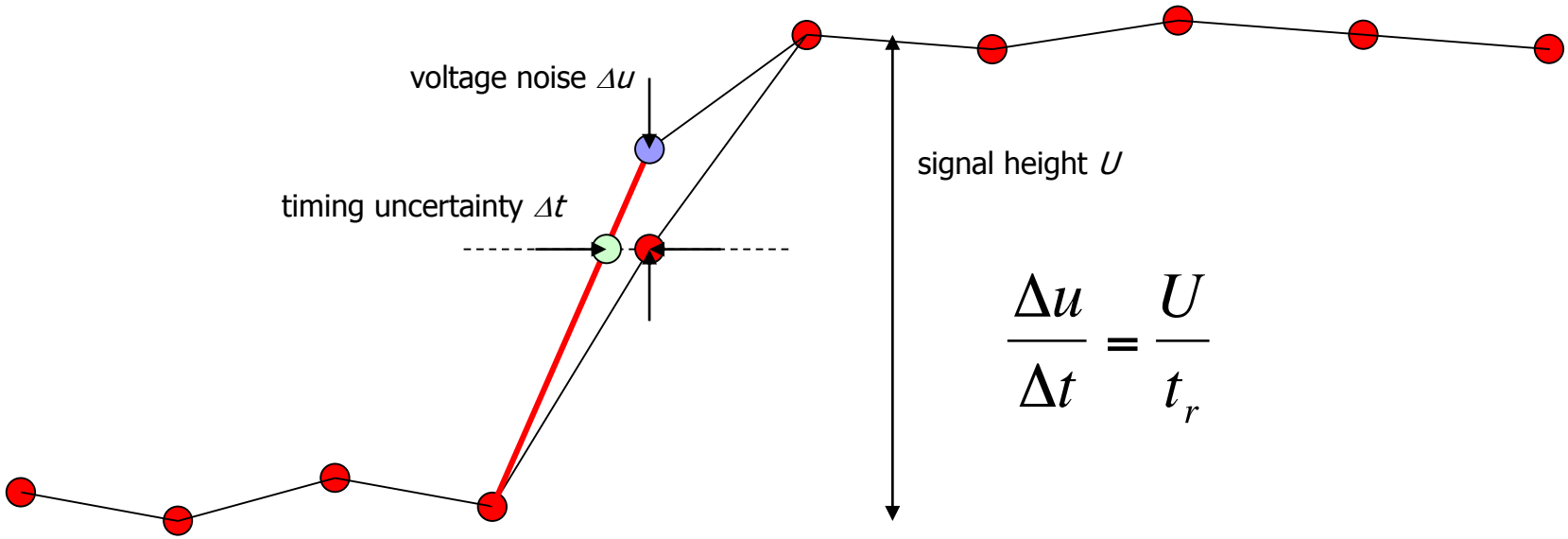




"Time stretcher"
GHz → MHz



How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

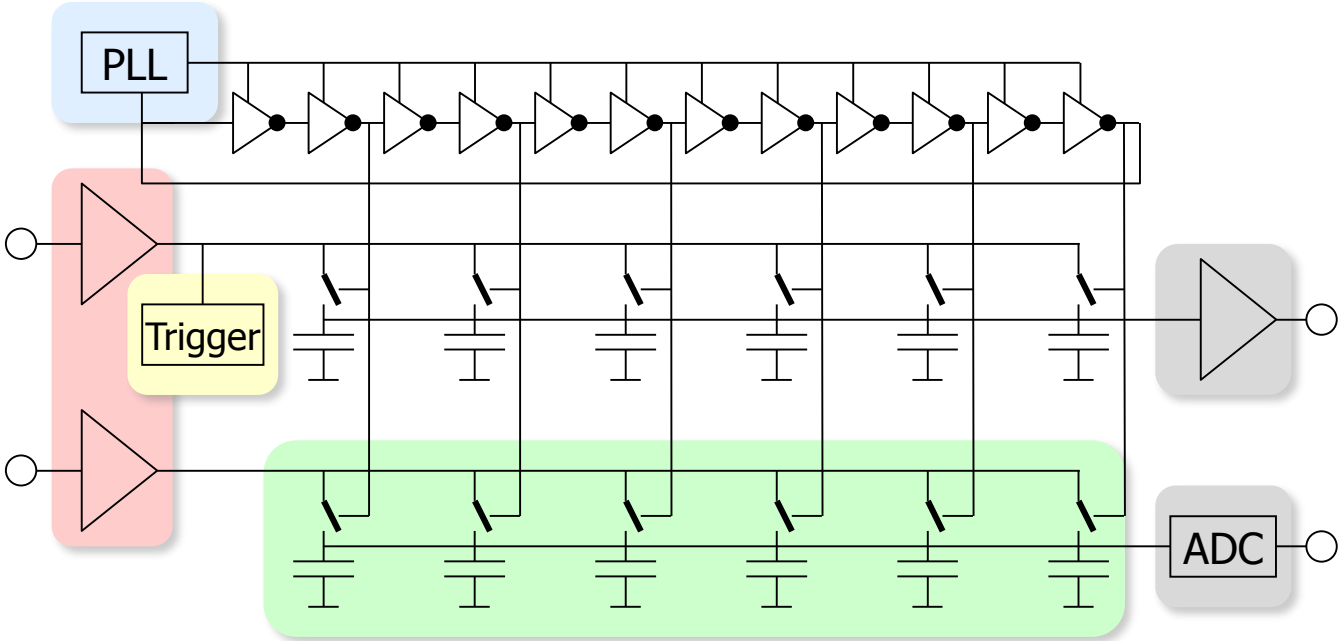
$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

Design Options

- CMOS process (typically 0.35 … 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



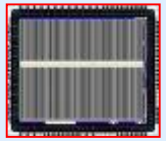
Switched Capacitor Arrays for Particle Physics

G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

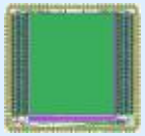
STRAW3 LABRADOR3 TARGET

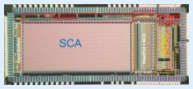


- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

www.phys.hawaii.edu/~idlab/

AFTER SAM NECTAR0





- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

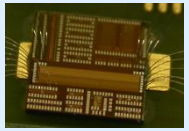
matacq.free.fr

PSEC1 - PSEC4

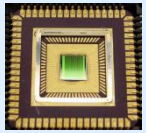
- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

psec.uchicago.edu

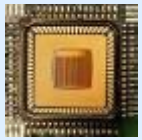
DRS1 DRS2 DRS3 DRS4



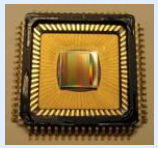
2002



2004



2007



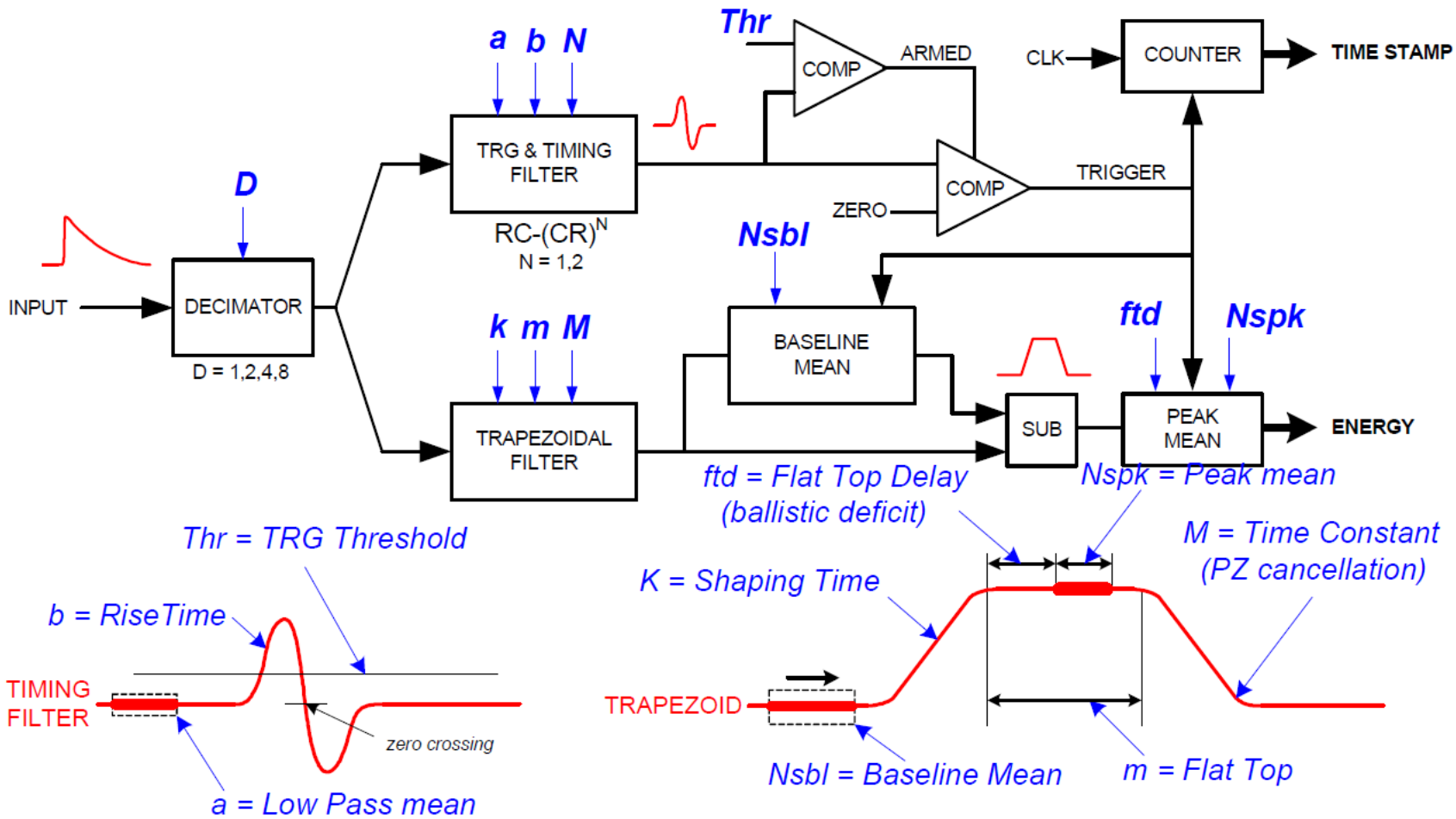
2008

- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

Stefan Ritt
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

Digital Pulse Processing (DPP)



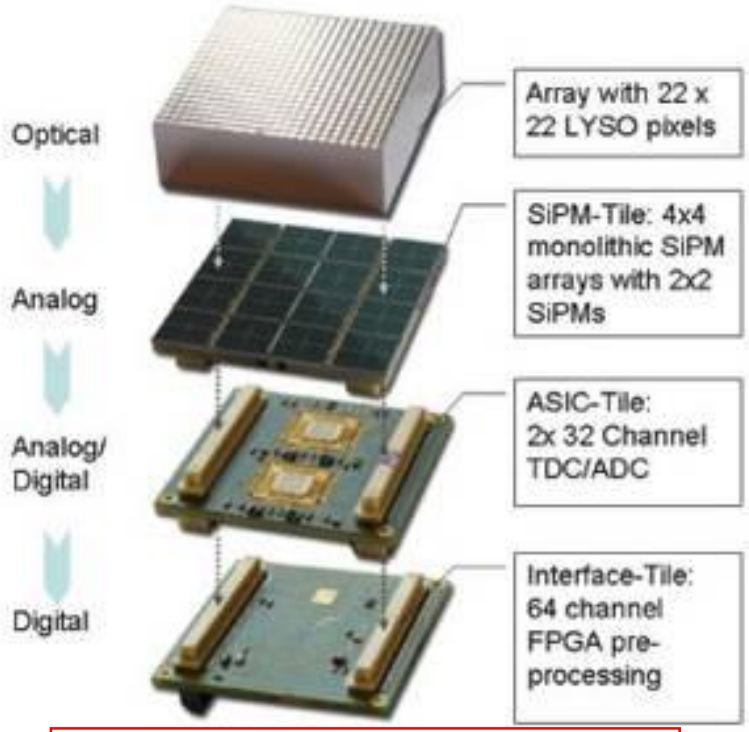
C. Tintori (CAEN)
V. Jordanov *et al.*, NIM **A353**, 261 (1994)

Comments

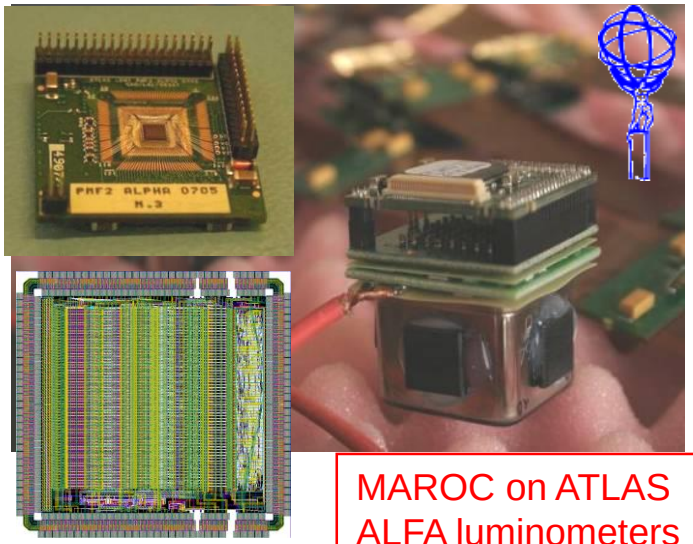
- Trends for SCAs
  - Reduce dead time
  - increase analog bandwidth
  - Increase depth, give more latency
  - Include high speed low noise preamps (NECTAR…)

- Comments
  - Unbeatable for pulse shape analysis or discrimination or if you don't know what you want to measure
  - Ultra low timing measurements (ps)
  - More power hungry than dedicated front-end (many CdV/dt…)
  - rarely optimal for large systems

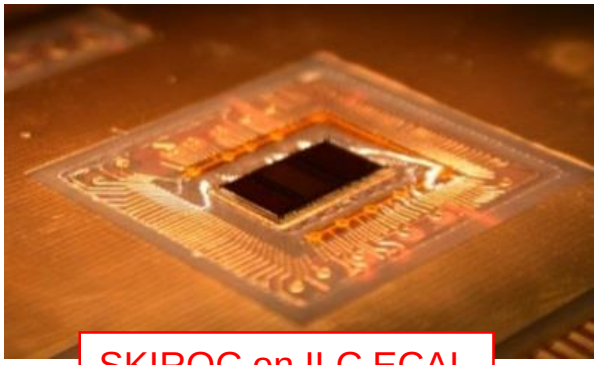
Electronics moves onto detectors



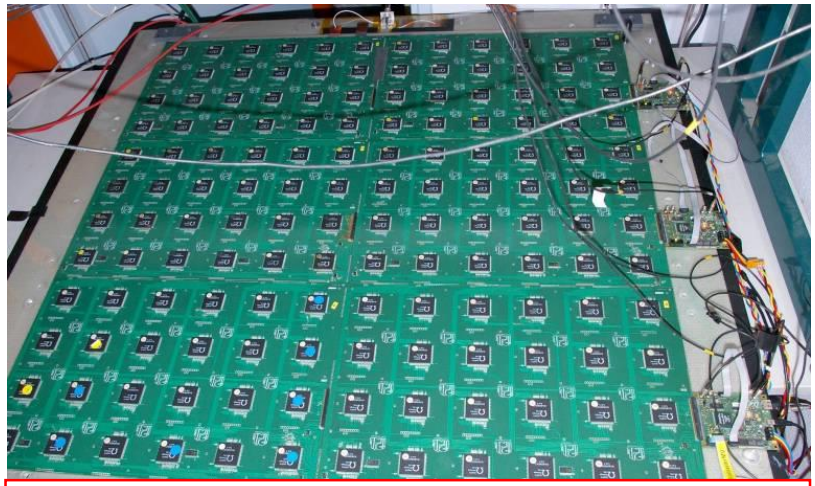
PET hyperimage project [P. Fisher]



MAROC on ATLAS ALFA luminometers



SKIROC on ILC ECAL



1m² RPC detector for ILC DHCAL [I. Laktineh]

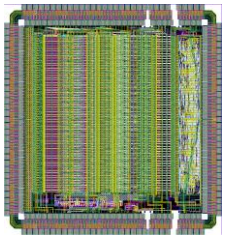
Example of SoC : OMEGA « ROC chips »

- Use of Silicon Germanium 0.35 µm BiCMOS technology since 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

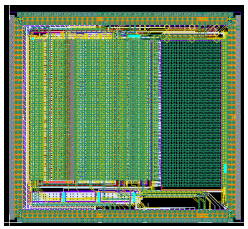
http://omega.in2p3.fr

Chip	detector	ch	DR (C)
MAROC	PMT	64	2f-50p
SPIROC	SiPM	36	10f-200p
SKIROC	Si	64	0.3f-10p
HARDROC	RPC	64	2f-10p
PARISROC	PM	16	5f-50p
SPACIROC	PMT	64	5f-15p
MICROROC	µMegas	64	0.2f-0.5p
PETIROC	SiPM	32	10f-200p

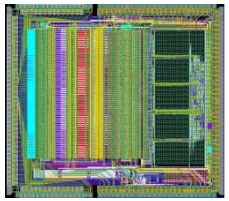
MAROC3



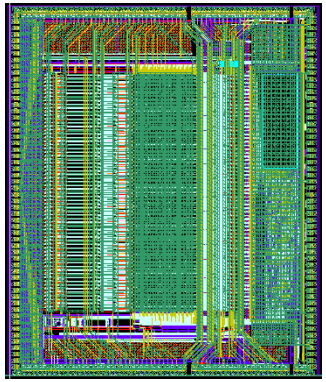
HARDROC2



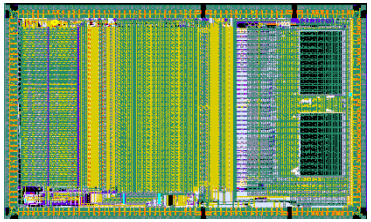
MICROROC1



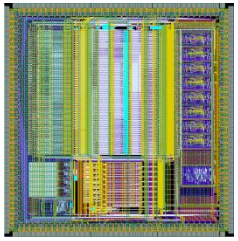
SKIROC2



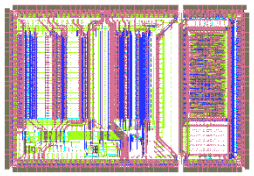
SPIROC2



SPACIROC

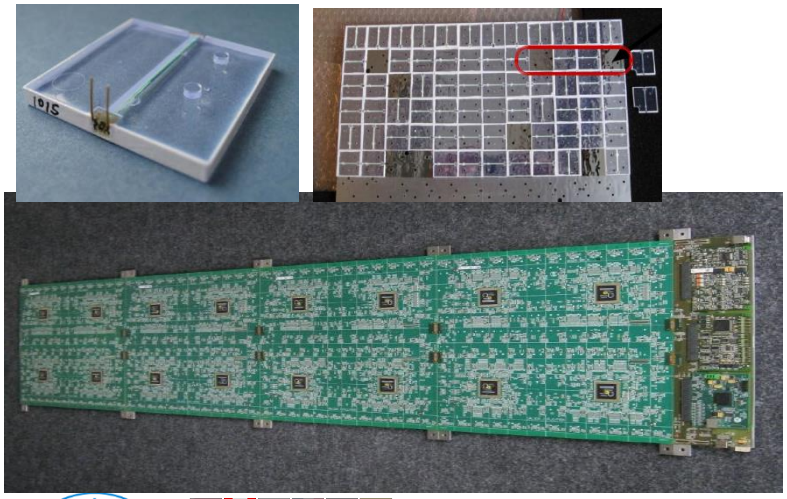


PARISROC2

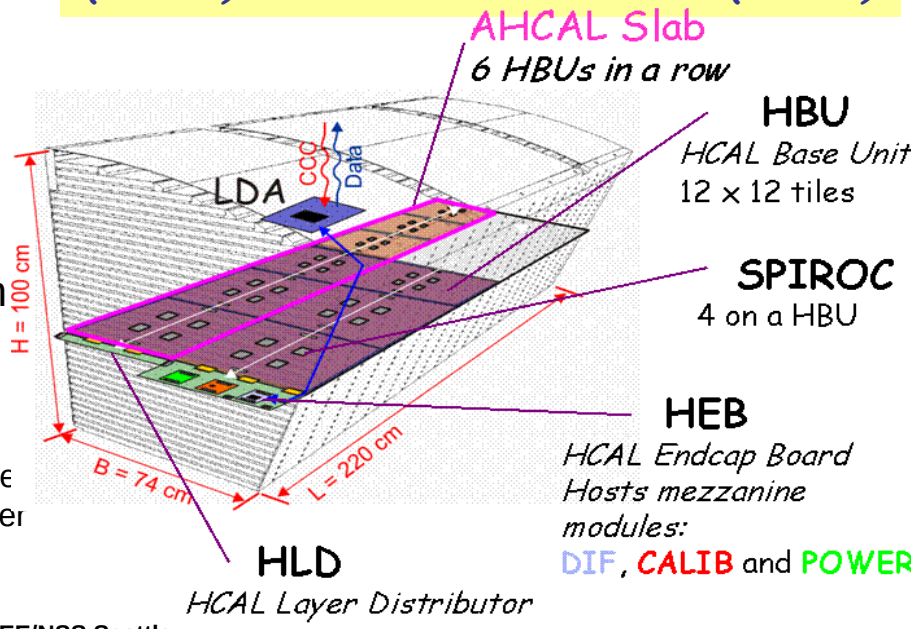


Example : SPIROC for SiPM

- SPIROC : Silicon Photomultiplier Integrated Readout Chip to read out the analog hadronic calorimeter for CALICE (ILC)
- **Ultra low-power 36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits, 1 pe to 2000 pe**
  - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
  - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - 4kbytes internal memory and daisy chain readout

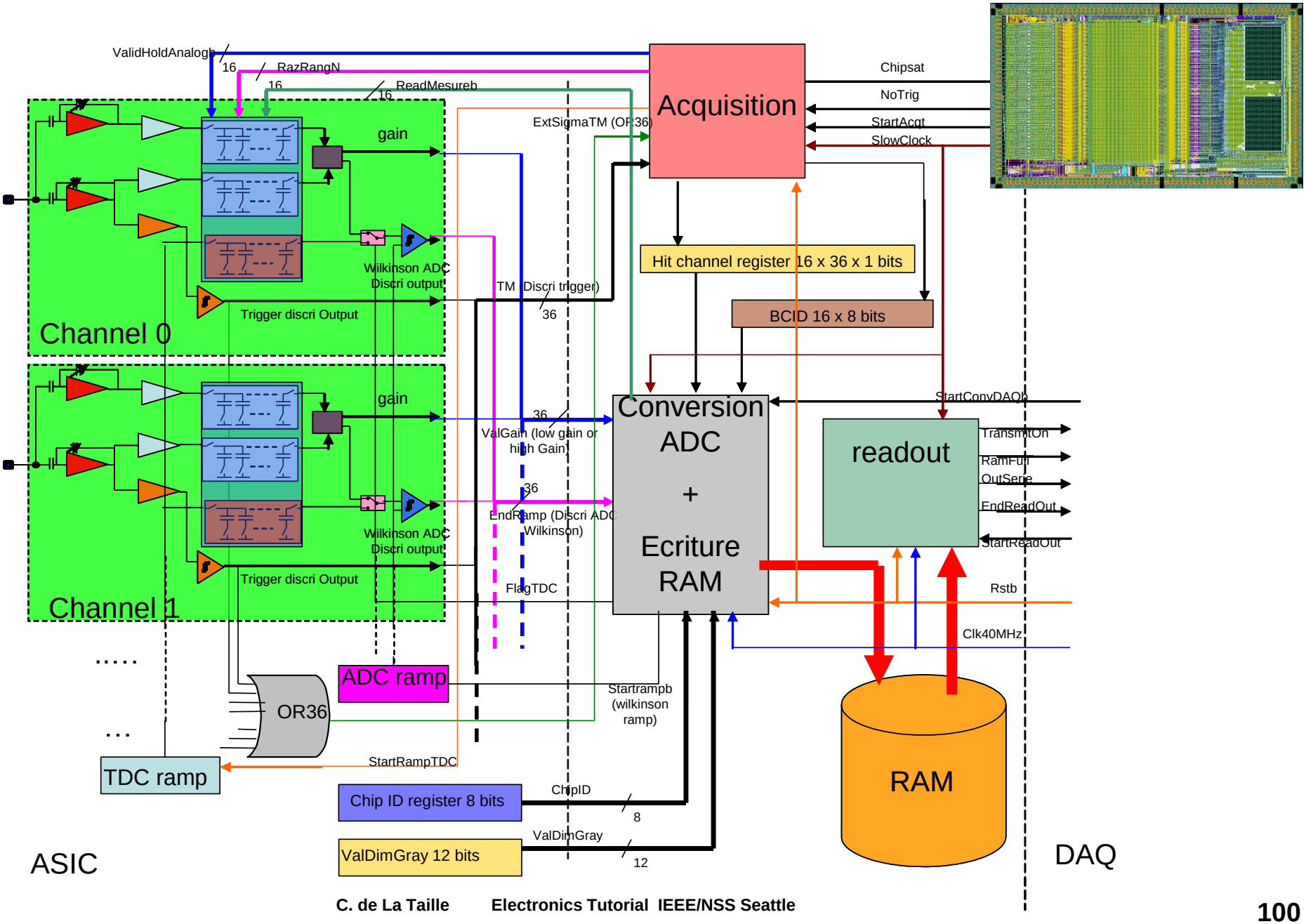


(0.36m)² Tiles + SiPM + SPIROC (144ch)



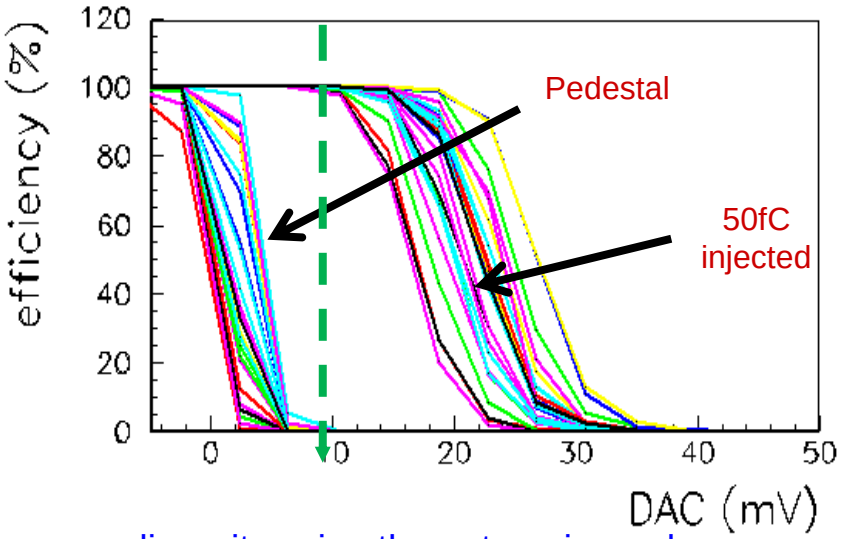
M. Bouchel et al. "SPIROC (SiPM integrated read-ou chip): Dedicate very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out," JINST, C01098 (2011).

SPIROC architecture

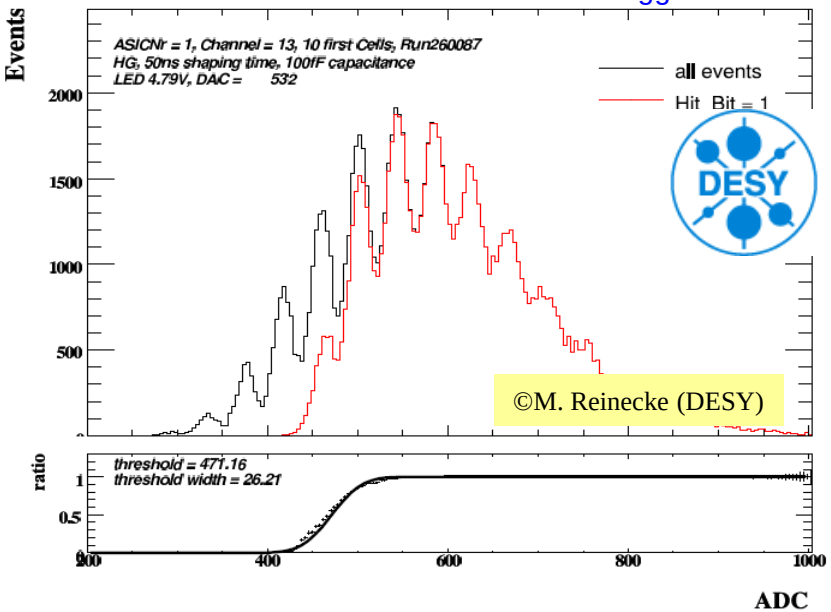


SPIROC: trigger efficiency measurements

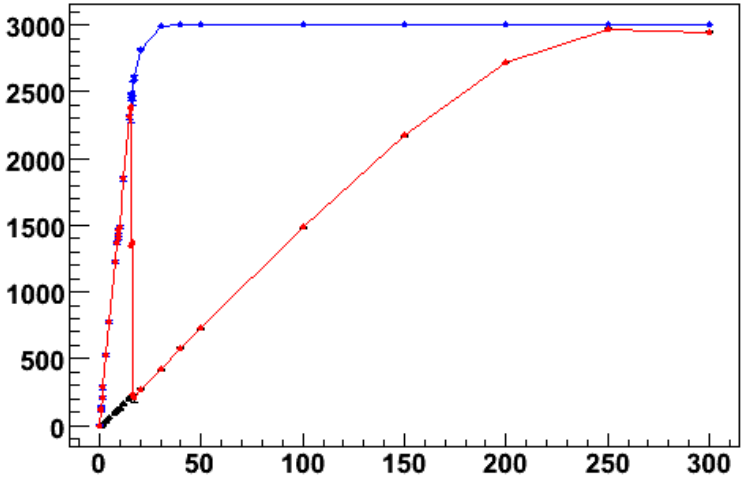
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



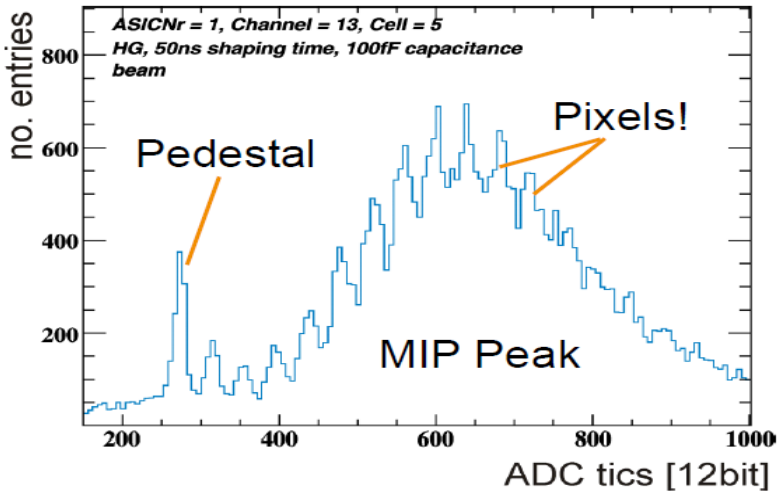
SiPM SPECTRUM with Autotrigger



linearity using the auto gain mode and internal ADC



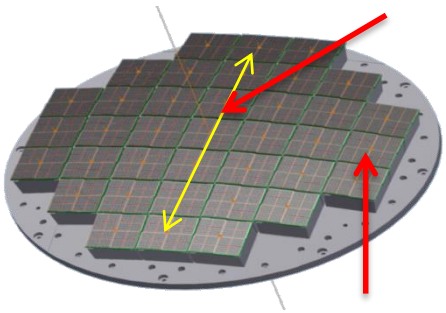
MIP response in DESY
6 GeV electron testbeam



PDM Electronics

FOV = 9.6°

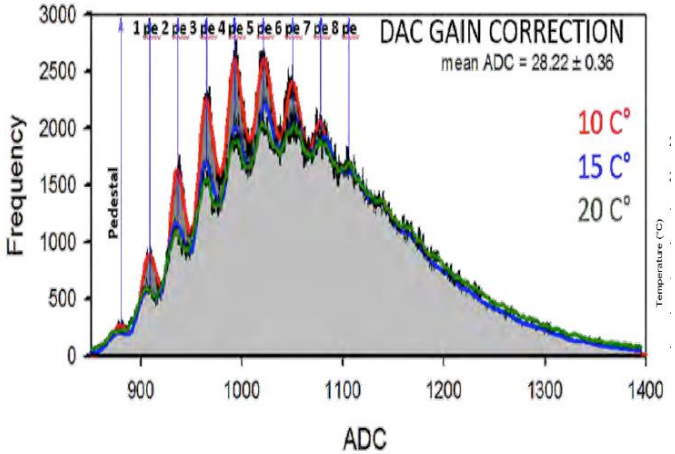
Ø = 350mm



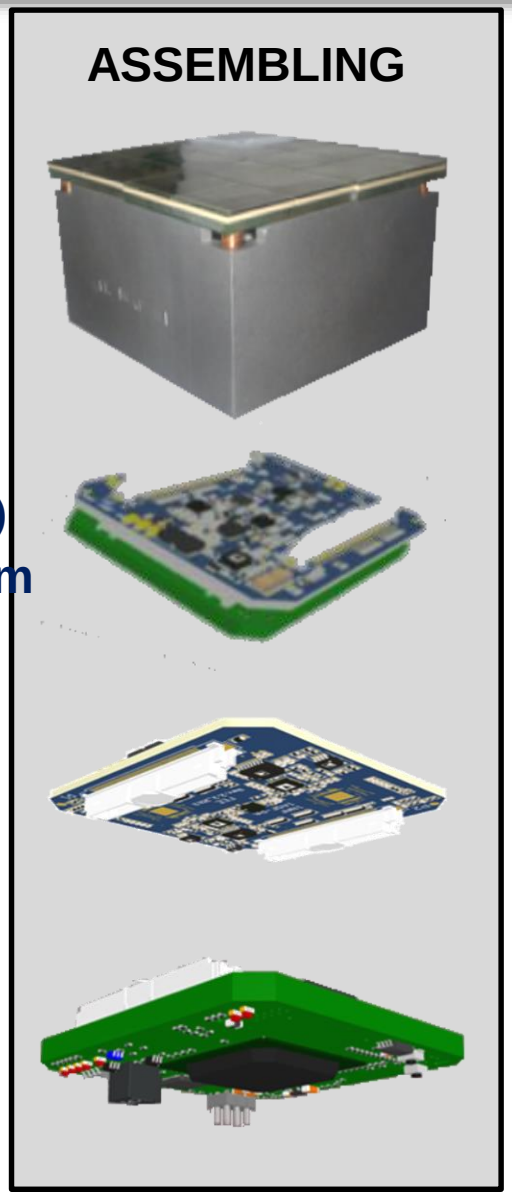
Photon Detection Module (PDM)

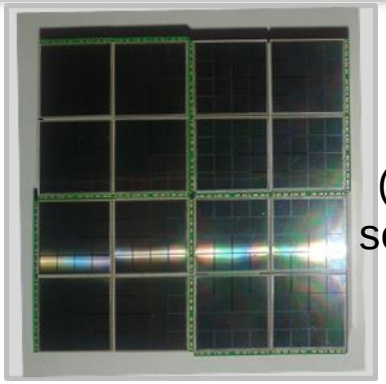
Pixel = 0.17° → 6.2 x 6.2 mm

© O. Cataneo INAF Palermo

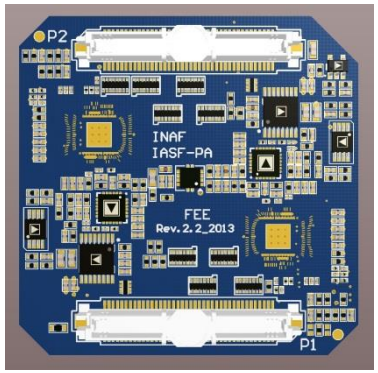


ASSEMBLING

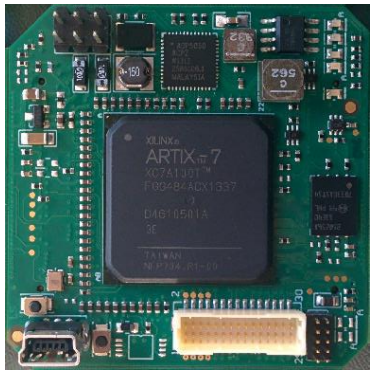




SiPM board (9 +1 temperature sensors embedded)



Front-End board (2 CITIROC ASIC)

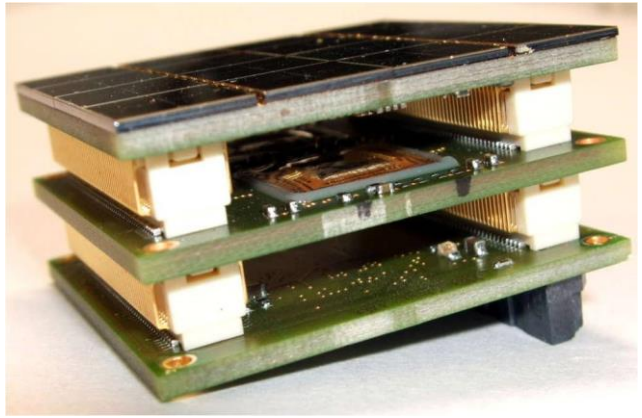


PDM FPGA Board (XILINX ARTIX 7)

PET Hyperimage

- PET/MRI projekt
  - P. Fischer et al. Heidelberg, Philips, Aachen, FBK Trento
- 40-channel system on chip for readout of the detectors that generate low voltage (several mV) signals
- Combined high precision time (~14 ps) and energy measurements (signal integral = energy)
- Time of flight measurements with energy discrimination
- Particle recognition, by mass measurement
- Medical imaging (SiPM based PET)

- [M. Ritzert…: "*Compact SiPM based Detector Module for Time-of-Flight PET/MR*" on IEE NPS Real Time Conference



Conclusion

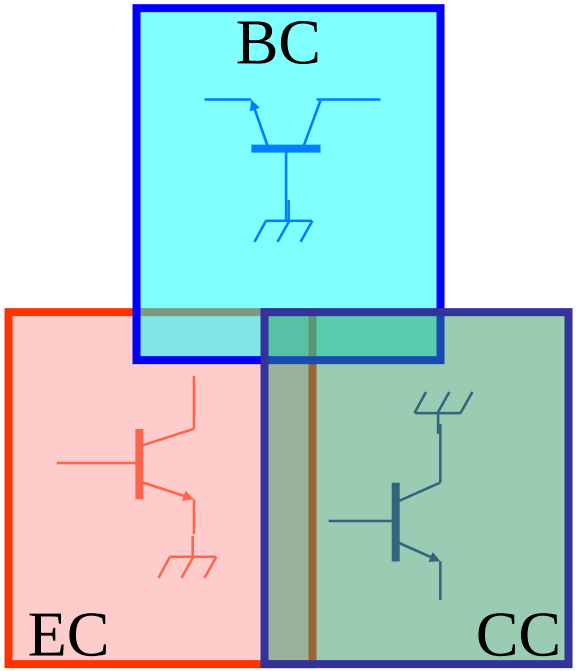
- Have fun designing electronics for future detectors !

Basic design in analog electronics :

- Three basic bricks
  - Common emitter (CE)
  - Common collector (CC)
  - Common base (BC)

- Numerous composites
  - Darlington
  - Paraphase
  - Cascode…

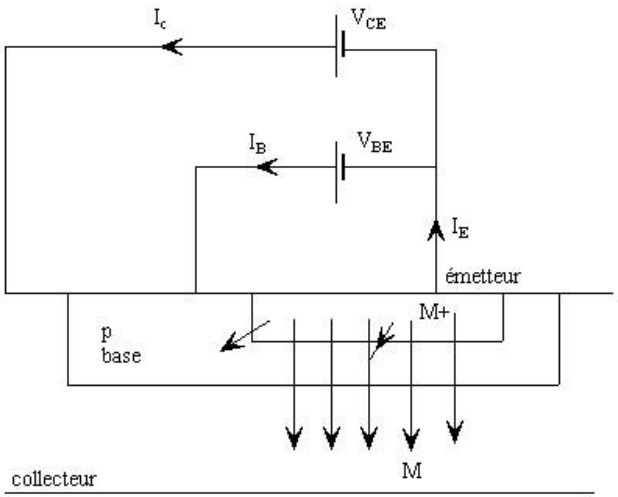
- Simple models
  - hybrid π model
  - Similar for bipolar and MOS
  - Essential for design
- + Powerful simulation tools
  - Spice, Spectre, Eldo…



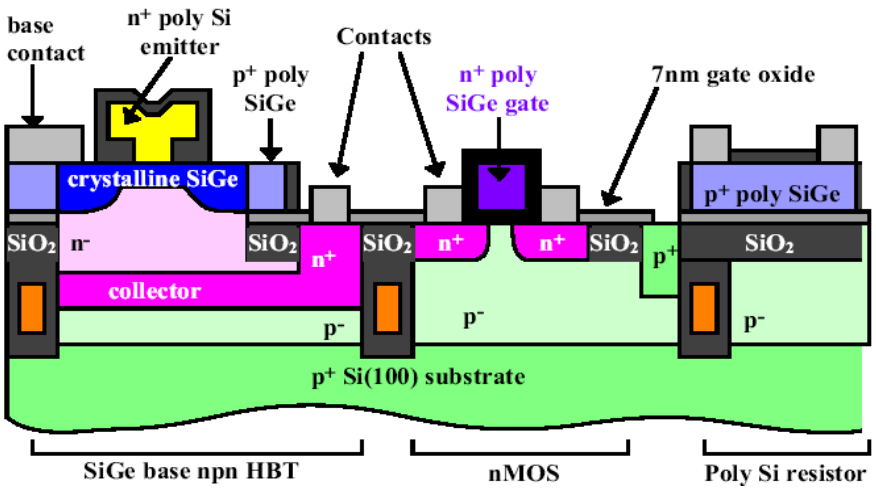
The *Art* of electronics design

Components : bipolar transistors (1)

- Principle of operation :
  - Forward bias of base emitter junction injects carriers which are swept in the collector due to the high collector-base electric field
  - collector current (I_C) controlled by base-emitter voltage (V_{BE})
  - Transconductance device : $g_m = \partial I_C / \partial V_{BE}$



First transistor (1949)
(Brattain-Bardeen Nobel 56)



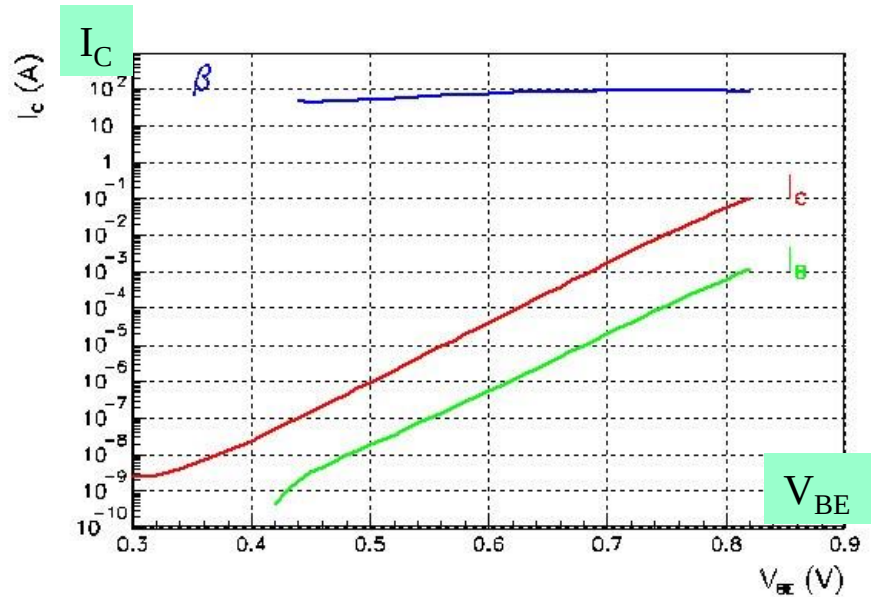
SiGe Bipolar in 0.35µm monolithic process

Components : bipolar transistors (2)

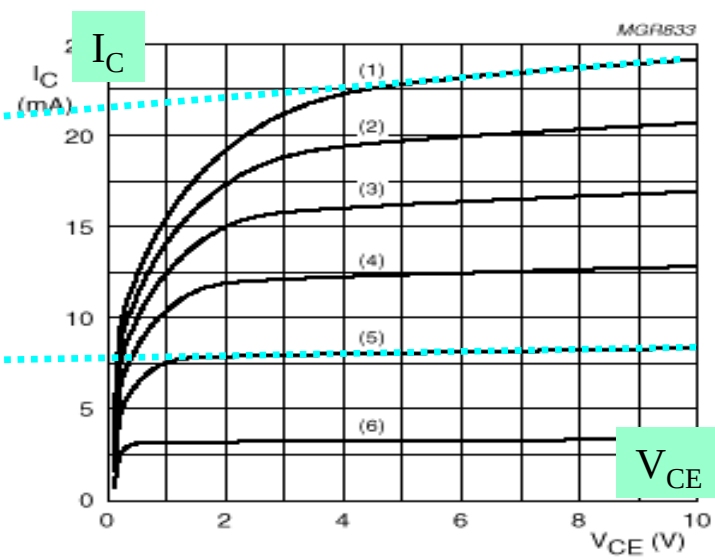
- **State equation :**

$$I_C = I_S \exp(V_{BE}/U_T)$$

  - $U_T = kT/q = 26$ mV : thermal potential
  - Is = 10^{-16}-10^{-14} A : technological param size
- Very wide validity : nA -> mA
- small input (base) current I_B
- $I_B = I_C/\beta_0$ β_0 >>1 is the current *gain : a* ve misleading term !

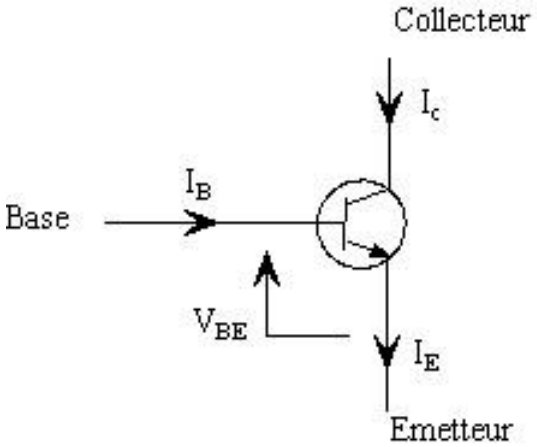


- **Early effect**
  - Very small dependance of I_C with collector voltage (V_{CE})
  - $I_C(V_{CE})$ are straight lines which cross at the same « Early » voltage V_E (20-200V)



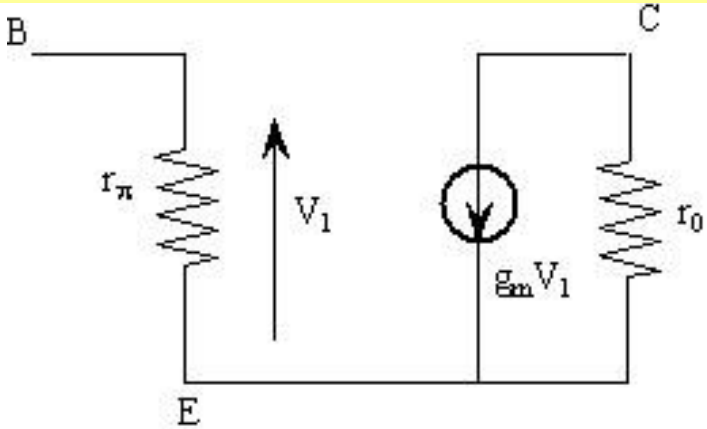
Small signal model

- **Equivalent circuit around bias point**
  - Signal = small variation around DC operating point (« bias point »)
  - => Linearisation : signal $v_{in} << V_{BE}$
  - $V_{BE} \rightarrow V_{BE} + v_{in}$ => $I_C = I_C (1 + v_{in}/U_T + \ldots)$
  - Tranconductance : $\mathbf{g_m} = \partial I_C / \partial V_{BE} = I_C/U_T$
    - g_m depends only on bias current I_C and $U_T = kT/q$
    - *Ex : $I_C = 1$ mA => $g_m = 1mA/26mV = 40$ mA/V*



Schematic drawing of NPN transistor

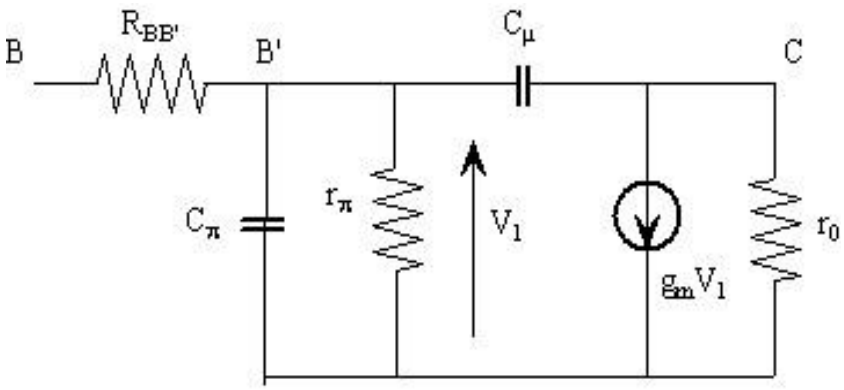
- **Input impedance = r_π**
  - Base current => Rin = $r_\pi = \partial V_{BE} / \partial I_B = \mathbf{b_0} / g_m$
  - Relatively large : r_π = 1-100 kΩ
    - *Ex : $I_C = 1$ mA ; $b_0=100$ => $r_\pi = 2.6$ kΩ*
- **Output impedance : r_0**
  - Early effect : Rout = $r_0 = \partial V_{CE} / \partial I_C = V_E/I_C$
    - V_E is the Early voltage = 10-100 V
  - Large value : 10k-10MΩ
    - *Ex : Ic=1 mA ; V_E=100V => r_0 = 100 kΩ*



Low frequency hybrid model of bipolar

Hybrid π model

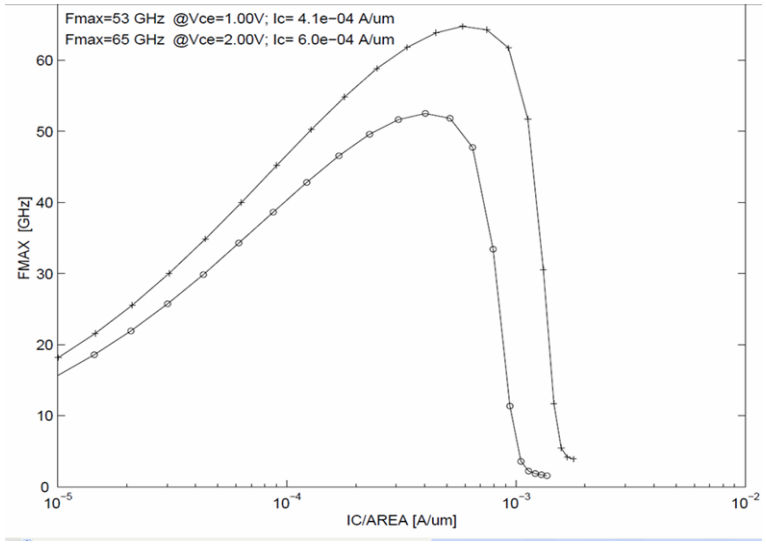
- Simple hybrid model :
  - Voltage controlled current source $g_m v_{BE}$
  - Transconductance $g_m = I_C/U_T$
  - Large input resistance $r_\pi = \beta_0 / g_m$
  - Large output resistance $r_0 = V_A/I_C$



High frequency hybrid model of bipolar

Frequency response

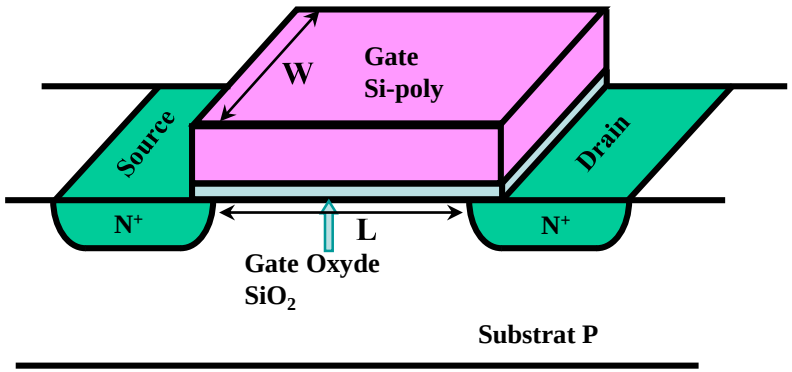
- Include capacitors :
  - Base-emitter junction C_π
  - Base collector junction Cμ
- => β varies with frequency :
  - $\beta(\omega) = g_m z_\pi(\omega)$
- $\beta(\omega) = \beta_0 / [1 + j\,\beta_0(C_\pi + C_\mu)/g_m]$
- $\beta(f) = 1$ for $f = f_T$ (transition frequency)
- f_T is a function of I_C but asymptotic to a max F_T

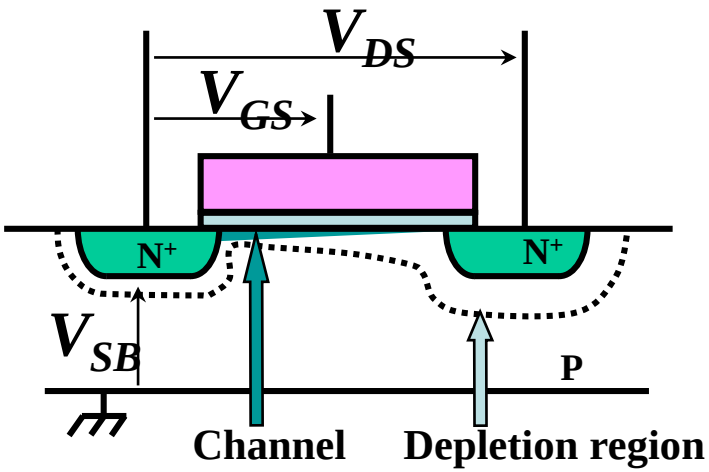


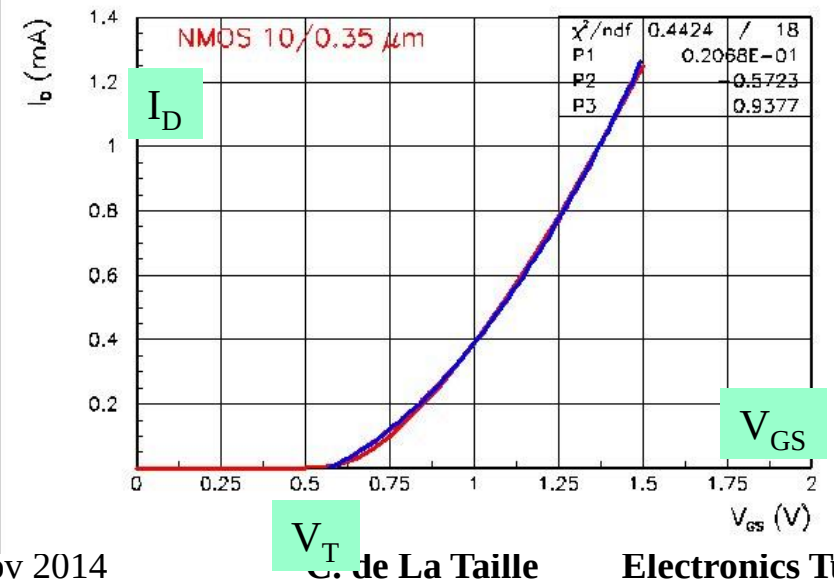
SiGe Bipolar Ft as a function of current

Components : MOS transistors

- Strong inversion :
  - quadratic approximation
  - $I_D = ½\ \mu_n C_{ox}\ W/L\ (V_{GS}-V_T)^2$
    - V_T : threshold voltage : technology dépendant
    - μ_n carrier mobility, C_{ox} gate thickness
    - W and L : dimensions = "designer's choice"
  - Voltage controlled current source

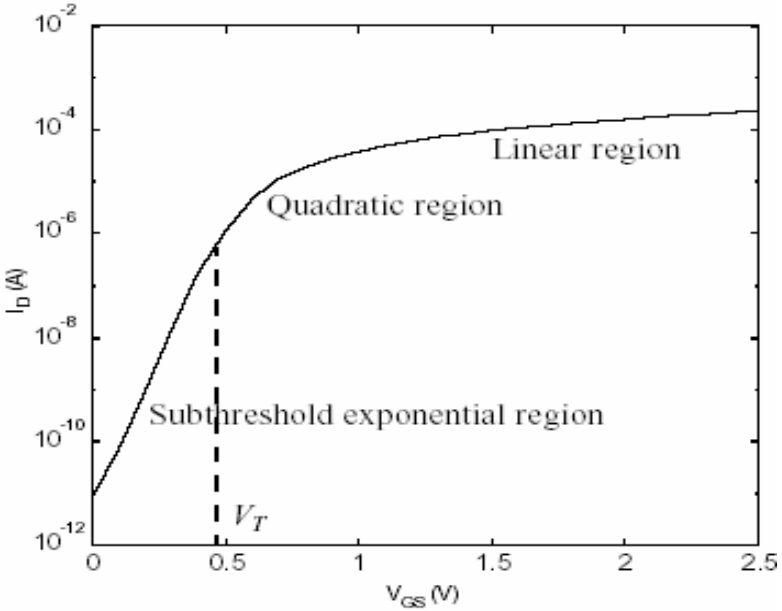




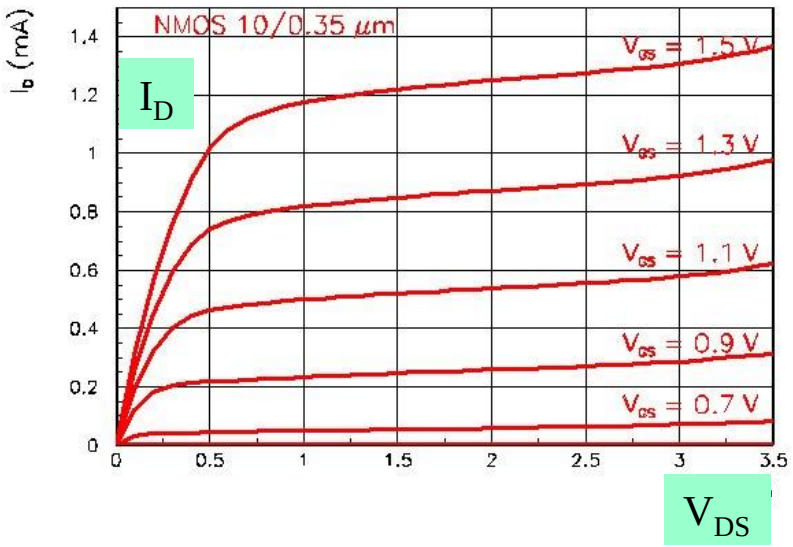


Components : MOS transistors

- **Weak inversion :**
  - **exponential law**
  - when V_{GS} close to V_T
  - $I_D = I_{D0}\ \mathbf{exp}(V_{GS}/n\mathbf{U_T})$
    - $(1 < n < 2)$
  - Similar to bipolar with $\beta_0 \to \infty$



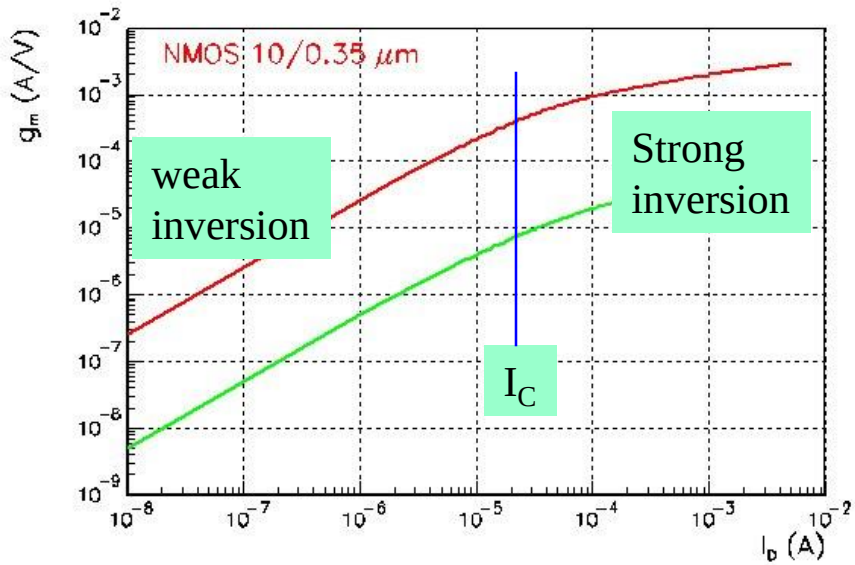
- **Early effect**
  - Small dependance of I_D with V_{DS}
  - Similar to bipolar transistor, but smaller V_A



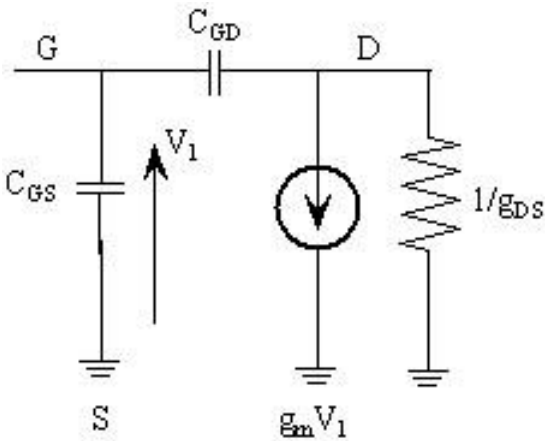
- **Body effect**
  - Effect of back gate : change in effective channel thickness
  - MOS is a 4 terminals device

MOS hybrid π model :

- **Small signal equivalent circuit**
  - Voltage-controlled (V_{GS}) current sourc
  - Transconductance : $\mathbf{g_m} = \partial I_D / \partial V_{GS}$
    - Strong inversion : $g_m = \mu_n C_{ox}\ W/L\ I_D)^{1/2}$
    - Weak inversion : $g_m = I_D / nU_T$
  - Input impedance : C_{GS}
  - Output impedance : $1/g_{DS} = V_E / I_D$
    - V_E : Early voltage $V_E = \alpha\ L$
  - Capacitance :
    - Gate-Source : $C_{GS} \sim 2/3$ Cox W L
    - Gate-Drain : $C_{GD} \sim 1/3$ Cox W L



- Similar hybrid π model as the bipolar
  - g_m remains g_m (but smaller)
  - $r_\pi \rightarrow \infty$
  - $r_0 \rightarrow 1/g_{DS}$

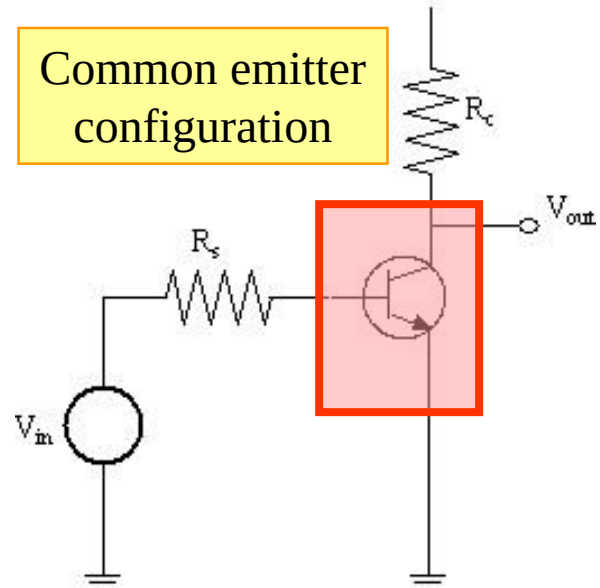


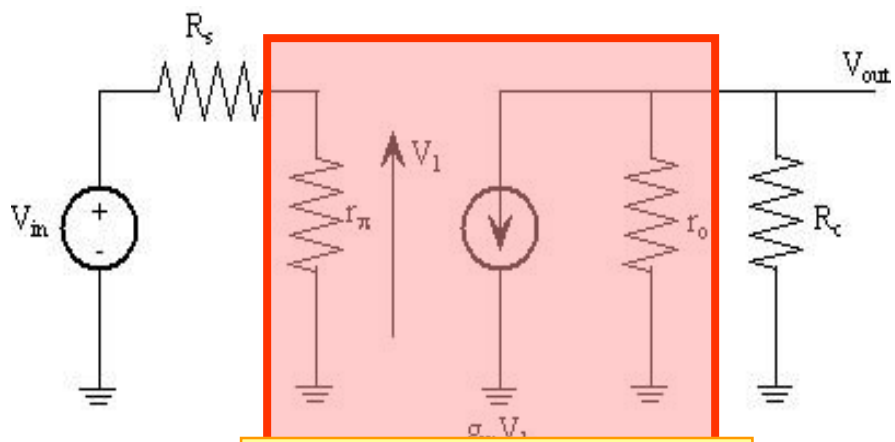
Common emitter (CE) configuration

- Emitter common to input and output
  - Input on the base
  - Output on the collector
  - "common source" with MOS

- Low frequency characteristics
  - Input impedance Rin = r_π $(=\beta_0/g_m)$
  - Output impedance: Rout = r_0 $(=V_A/I_C)$
  - Voltage gain : $G = v_{out}/v_{in} = - g_m R_L$
  - Inverting amplifier

- ***Transconductance stage***
  - Large Zin : voltage sensitive input
  - Large Zout : current driven output
  - Transconductance g_m determined by bias current I_C

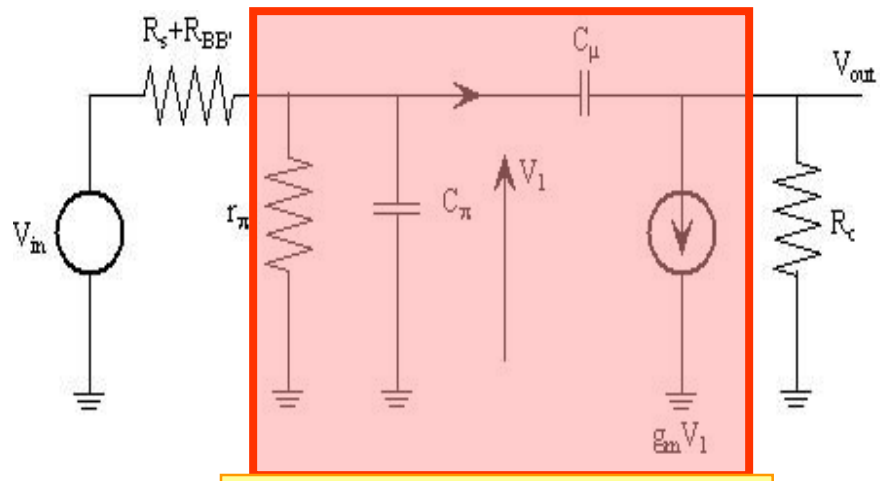




Equivalent circuit of CE

Common emitter frequency response

- Frequency response
  - Include capacitors : Cπ, Cμ
  - Effect of C_μ: Miller effect
  - = apparent input capacitance C_{Mi}
  - $C_{Mi} = (1 + g_m R_L) C_\mu$
  - Gain : $Av = -g_m R_L / [1 + j\omega R_S (C_\pi + C_{Mi})]$
  - *Ex : R_S=1 kΩ R_L=20kΩ g_m=1 mA/V C_π=2.5 pF C_μ=0.5 pF => C_{Mi} = 10 pF tau=12.5ns*

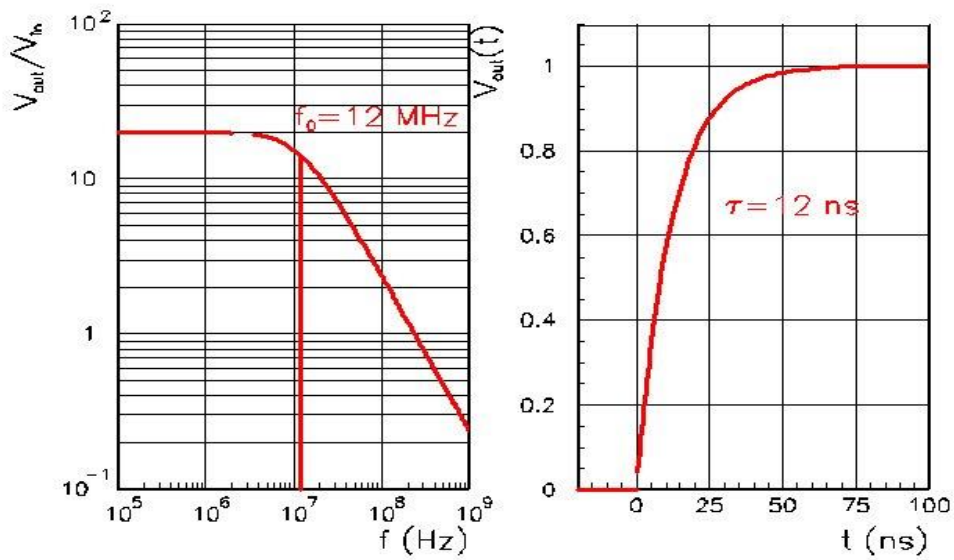


Frequency response of CE

- Time response
  - $H(t) = \mathcal{F}^{-1} \{ 1/j\omega \; R/(1+j\omega RC) \}$

    $= R [1 - \exp(-t/\tau)]$
  - $\tau = R_S(C_\pi + C_{Mi})$
  - Similar calculation as photodiode preamp

- Slow configuration



Common collector (CC) :

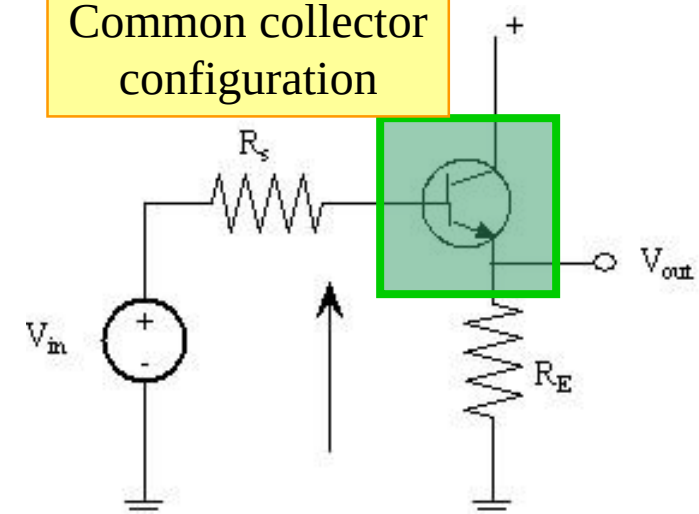
- Collector common to input and output
  - Input on the base
  - Output on the emitter
  - = Common drain for MOS

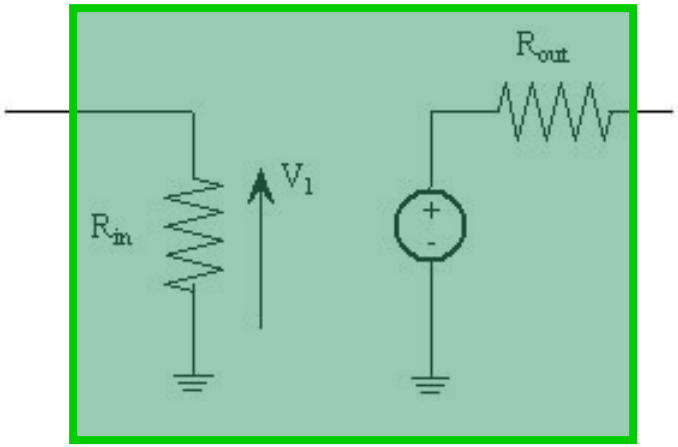
- Low frequency characteristics
  - Input impedance Rin = $r_\pi + \beta_0 R_E$
  - Output impedance: Rout = $R_S/\beta_0 + 1/g_m$
  - Voltage gain : Av = $v_{out}/v_{in} = 1/(1+1/g_m R_E) \leq 1$
  - Non inverting

- **Voltage follower or "emitter follower"**
  - Large Zin : voltage sensitive input
  - Small Zout : voltage driven output
  - Unity gain buffer : "the emitter follows the base"

- **Frequency response : ~F_T**
  - Small apparent input capacitance

Common collector configuration





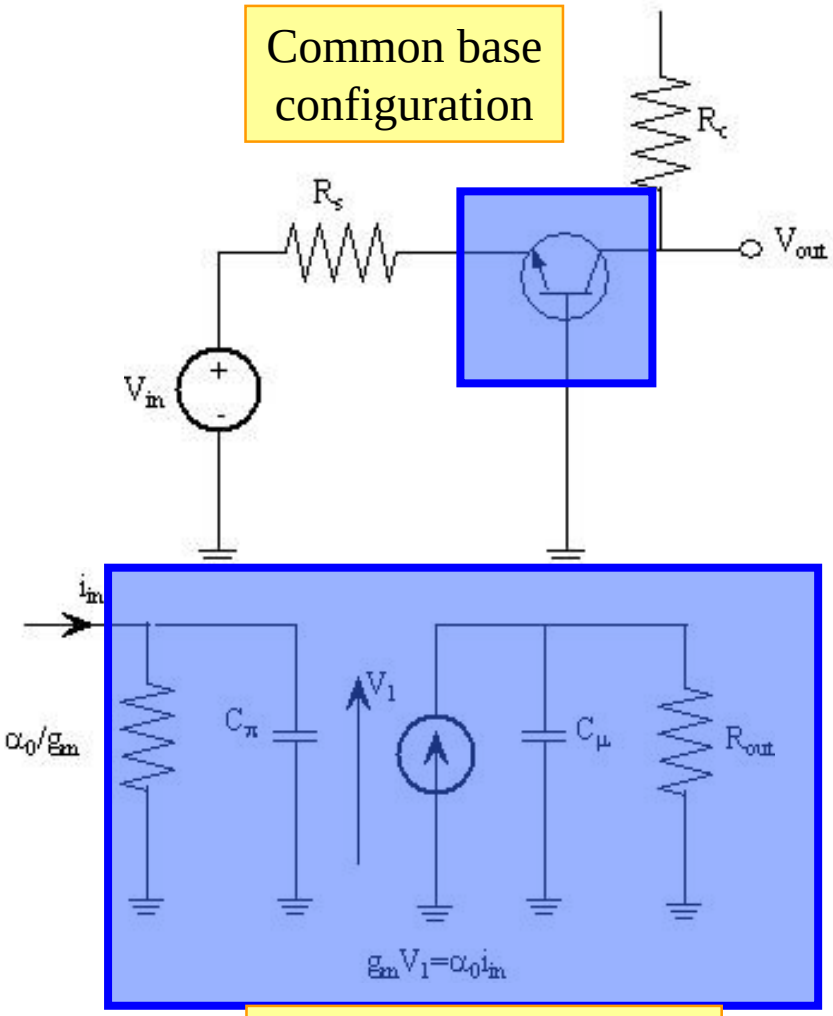
Equivalent circuit of CC

Common Base (CB) :

- Collector common to input and output
  - Input on the emitter
  - Output on the collector
- Low frequency characteristics
  - Input impedance Rin = $1/g_m$
  - Output impedance: Rout = $(1+g_m R_S)r_0$
  - Current gain : $A_i \sim 1$
  - Non inverting

- **Current conveyor**
  - Small Zin : current sensitive input
  - Large Zout : current driven output
  - Unity gain current conveyor

- Frequency response : $\sim F_T$
  - Very fast
  - Excellent isolation input/output

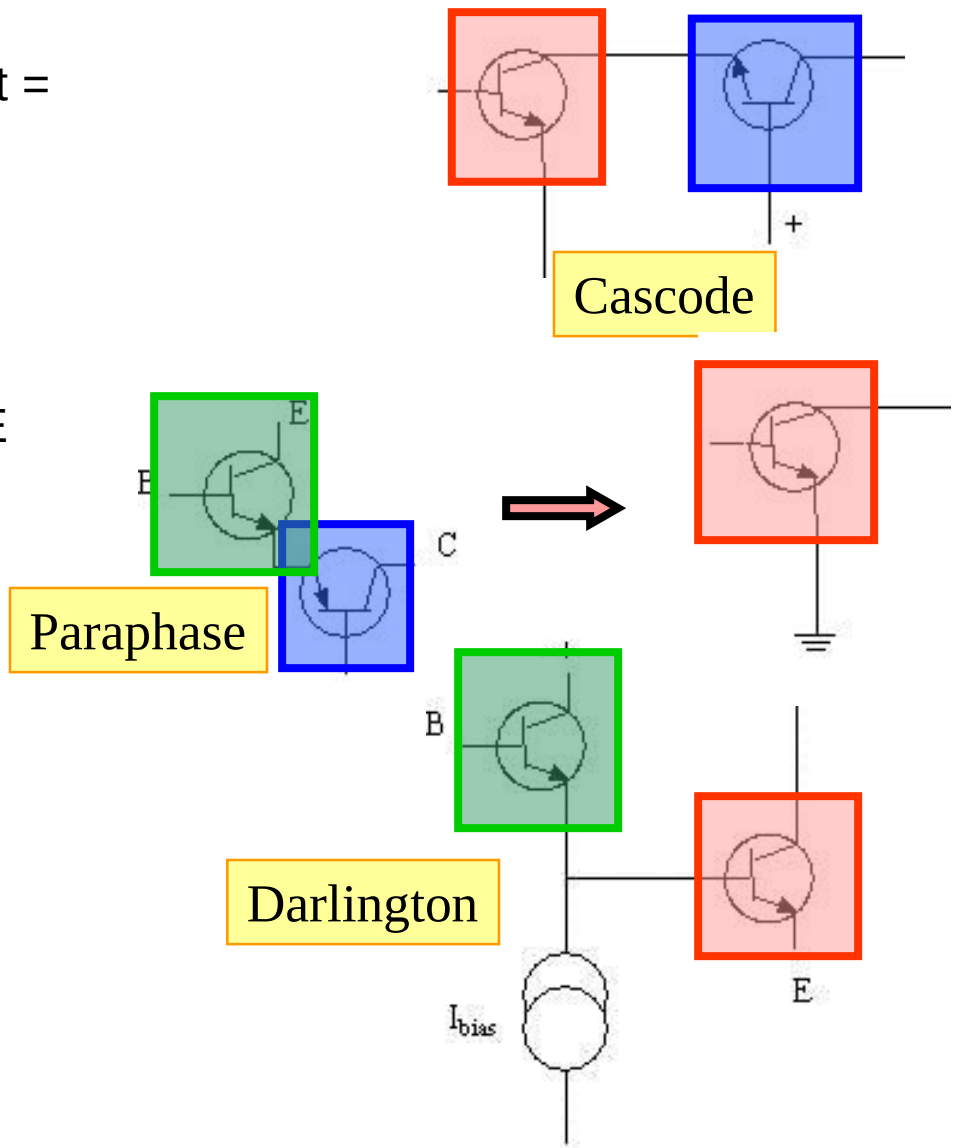


Example : simple composites :

- Cascode = CE + CB
  - Equivalent to CE
  - Larger output impedance Rout = $(1+g_{m2}/g_{DS1})/g_{DS2}$
  - *No Miller effect*

- Paraphase = CC + CB
  - Equivalent to non-inverting CE
  - Transconductance : $g_m/2$

- Darlington = CC + CE
  - Equivalent to CE
  - Larger input impedance
  - *Reduced Miller effect*

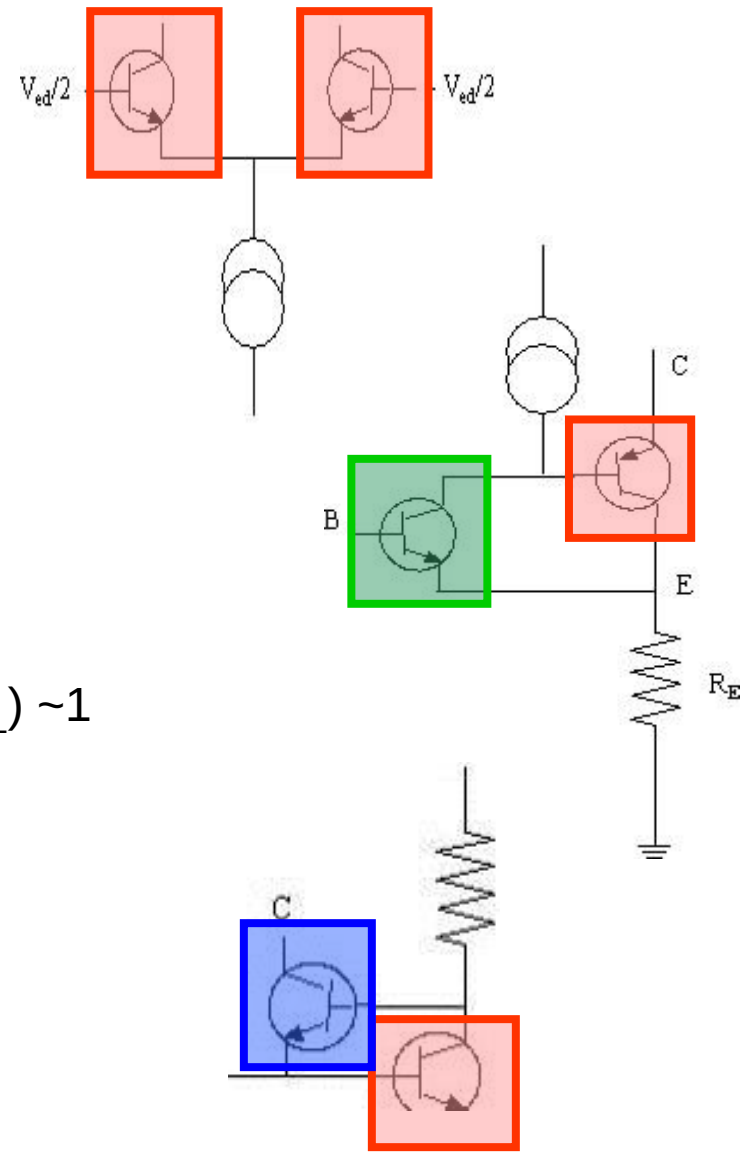


more composites

- Differential pair
  - Similar to common emitter
  - Input impedance : Rin = $2r_\pi$
  - Transconductance : $i_{out} = g_m/2\ v_{ind}$
  - Conversion differential / common mode

- White follower : CC + EC
  - Closed loop composite
  - Input impedance : Rin = $\beta_1\ \beta_2\ R_E$
  - Output impedance : Rout = $(R_S + r_{\pi 1})/\ \beta_1\beta_2$
  - Voltage gain : Av = v_{out}/v_{in} = $1/(1+Rout/R_L)$ ~1
  - => super voltage follower

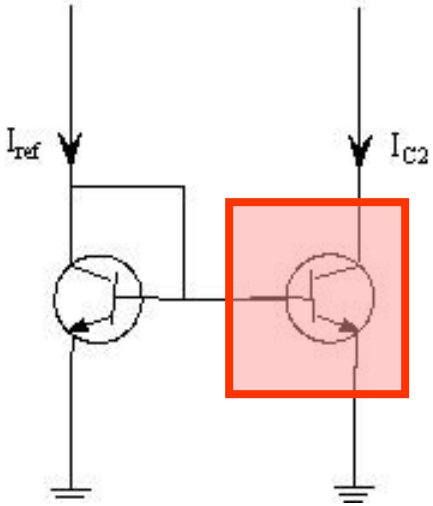
- "Super common base"
  - Input impedance : Rin = $1 / g_{m1}g_{m2}R_C$
  - => super current conveyor



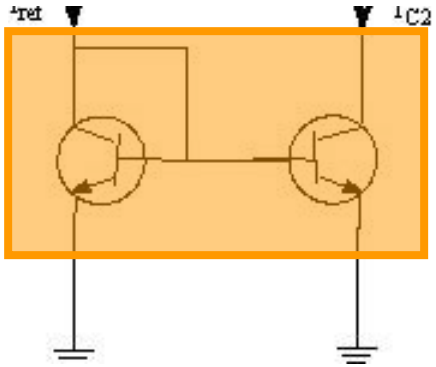
Current mirrors

- Several functions
  - Biasing : current source
  - Active load = high virtual resistor
  - Current amplifier

- Simple mirror characteristics :
  - Same V_{BE} => same current
  - Input impedance : $R_{in} = 1/g_{m1}$
  - Output impedance : Rout = $1/r_{02}$
    - Can be increased with composites
  - Current ratio : $I_{C2}/I_{C1} = 1$
    - Can be increased by changing the area
  - Several copies can be made



Current mirror



Current conveyor

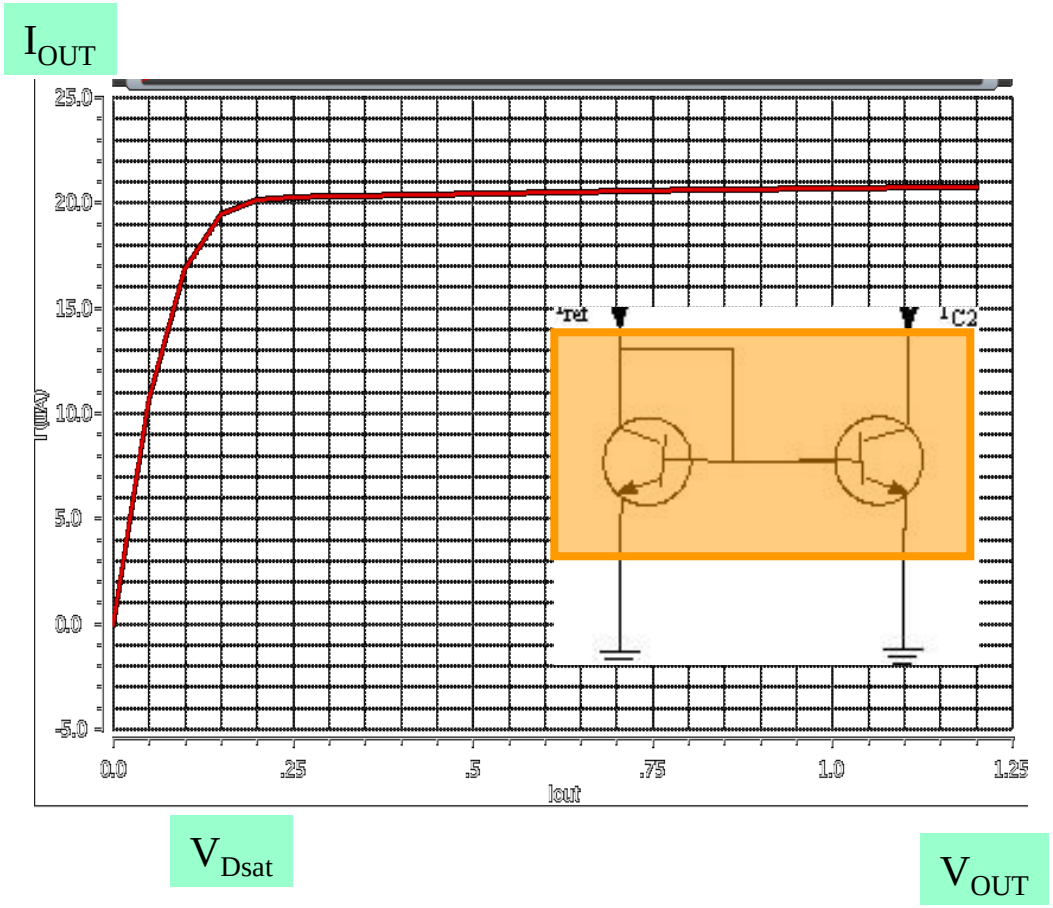
- Small Zin : current sensitive input
- Large Zout : current driven output
- Unity gain current conveyor

Output characteristics

- Output impedance
  - Limited by r0 $1/g_{DS}$
  - Can be improved by cascode or emitter degeneration
- Output swing
  - Limited by V_{Dsat} : MOS in triode region
  - In bipolars down to few U_T
- Matching
  - Systematic mismatch : Early effect, beta…
  - Random mismatch :

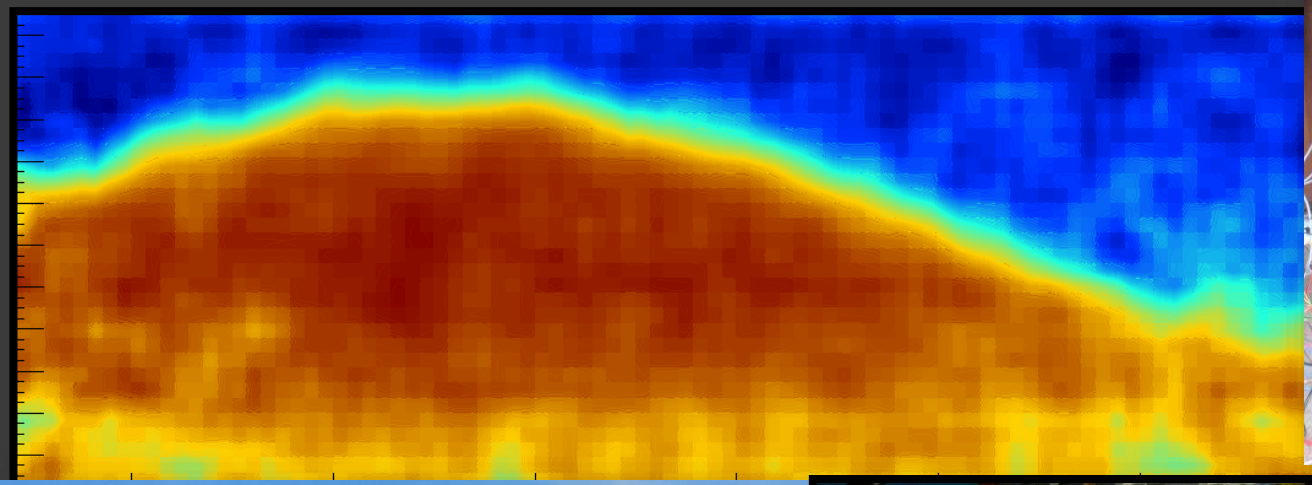
    $\Delta V_T = A / \sqrt{WL}$

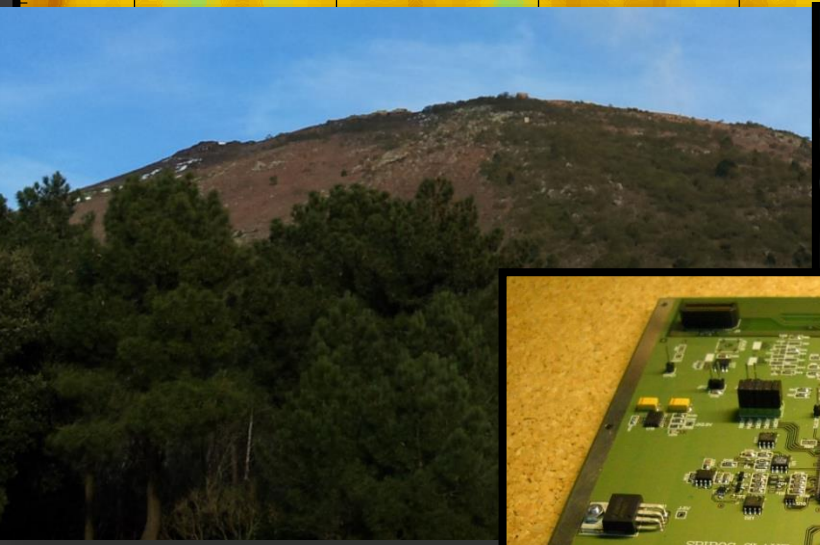
    A ~10 mV*µm

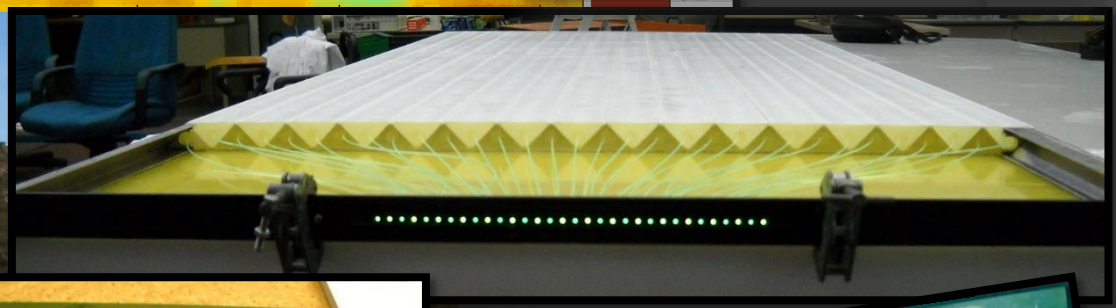


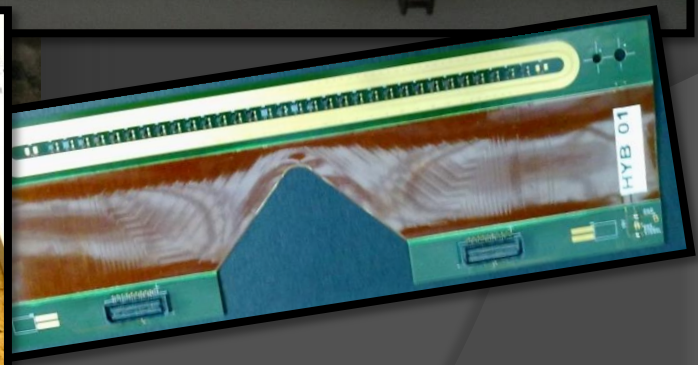
Output current of current mirror

The “Shadow” of the Vesuvius





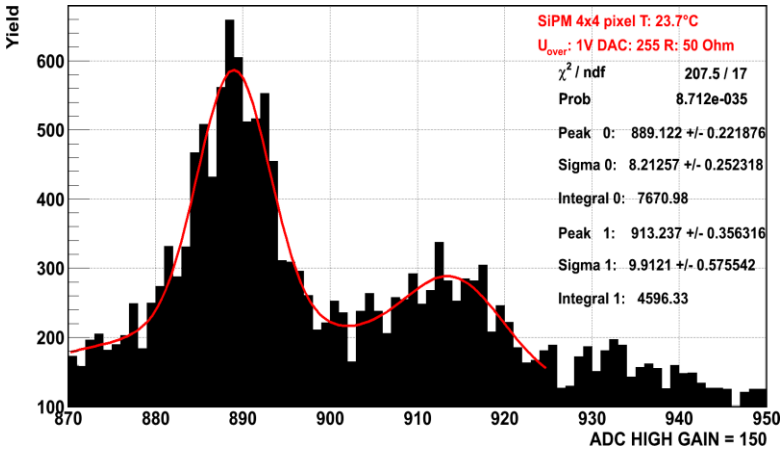


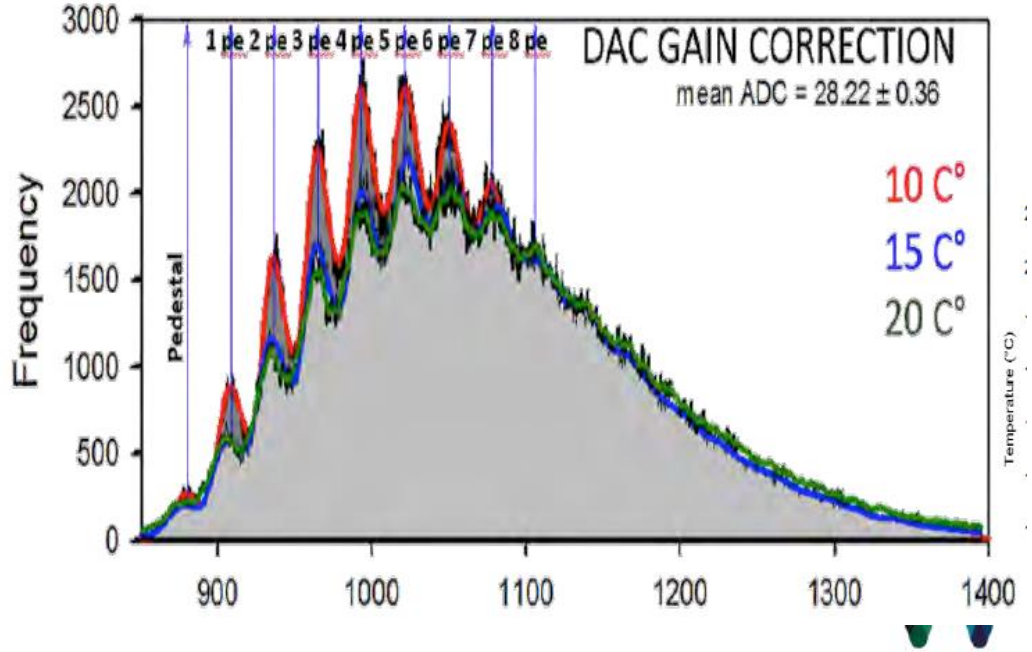


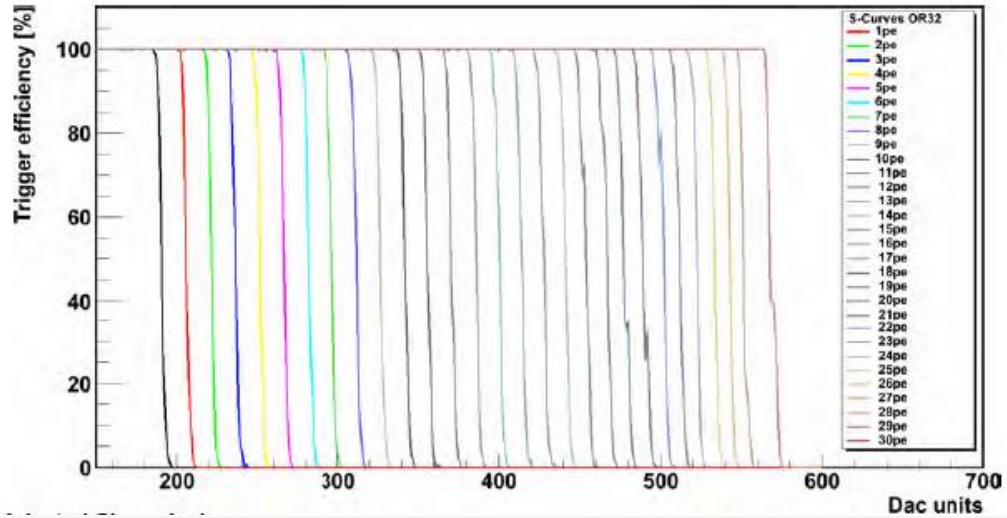
© P. Strolin INFN Napoli

CITIROC: Trigger Linearity

Gain premplifier =4*25fF ≈ 150 nom.
Shaping Time = 50ns
Steps of 1,2,3,4,5,6,7,8,9,10 pe



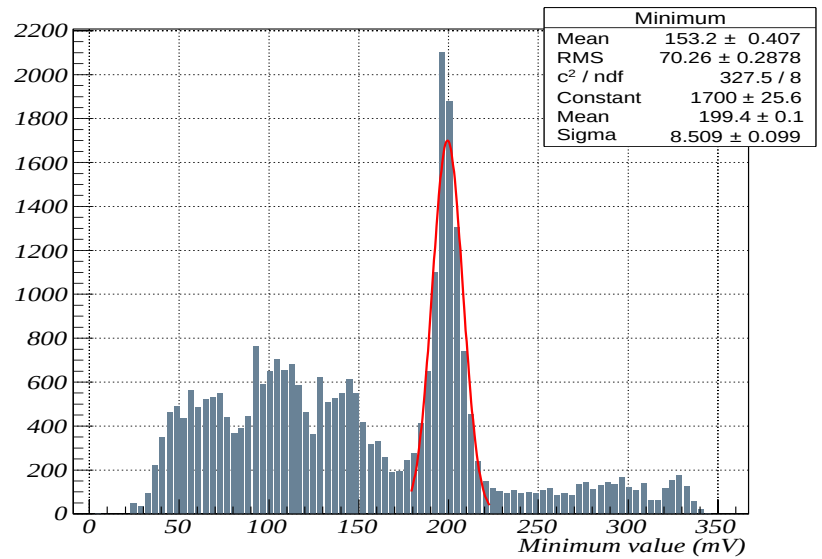




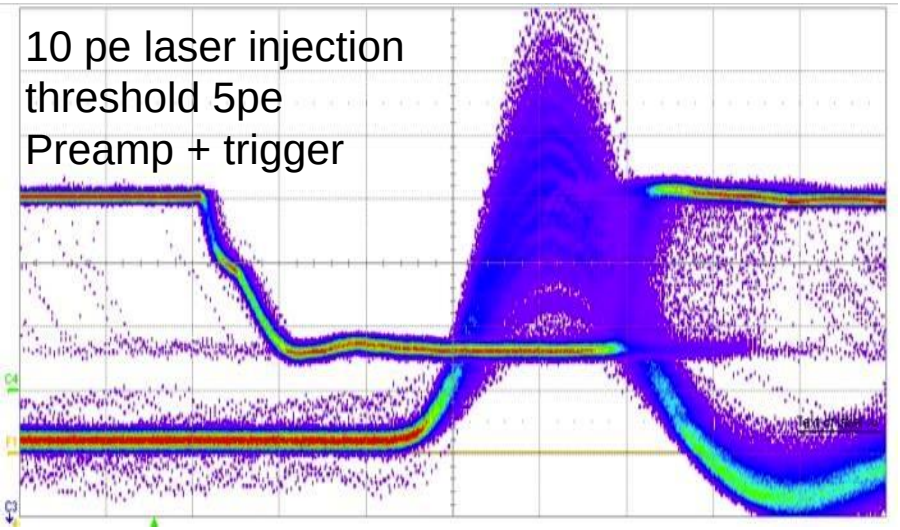
SiPM 4 pixel High Gain =150
Shaping Time = 50ns
delay time = 38 x 2.5 ns
Temp = 23.7 °C U_{over} = 1V
Resistance = 50 Ohm
Threshold = 922 DAC ~50% of 1 plateau

PETIROC1: Triggers on first pe

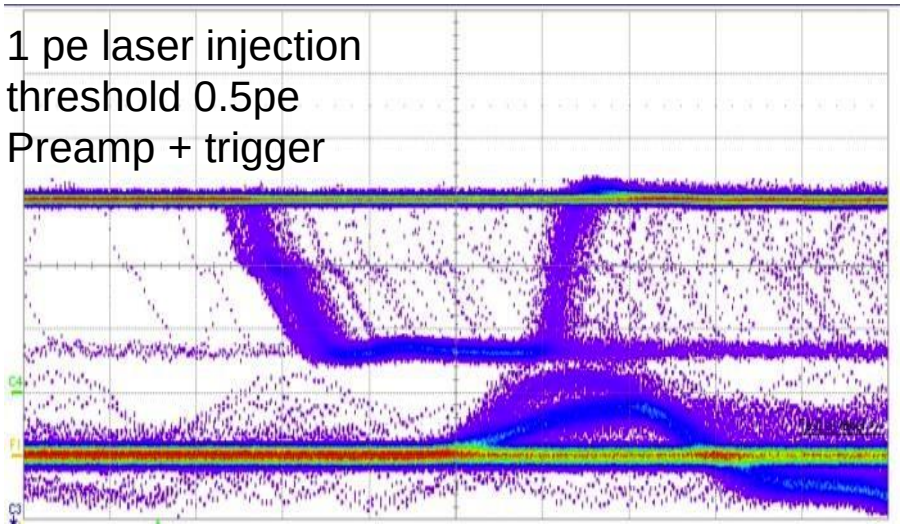
- Tests on EPTIROC1 (analog version of PETIROC2)
- 1x1mm SiPM Hamamatsu
- Laser for low light injection
  - 405nm, Jitter : 28 ps FWMH
- Petiroc can trigger on first photoelectron
- Petiroc is low noise : single photon identification



2 ns/div



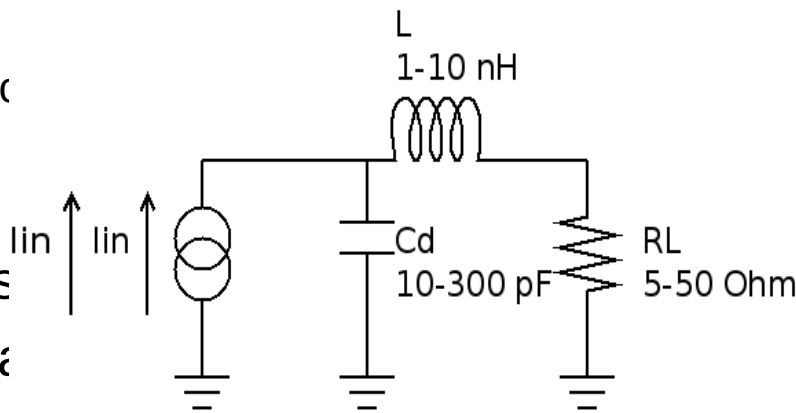
2 ns/div

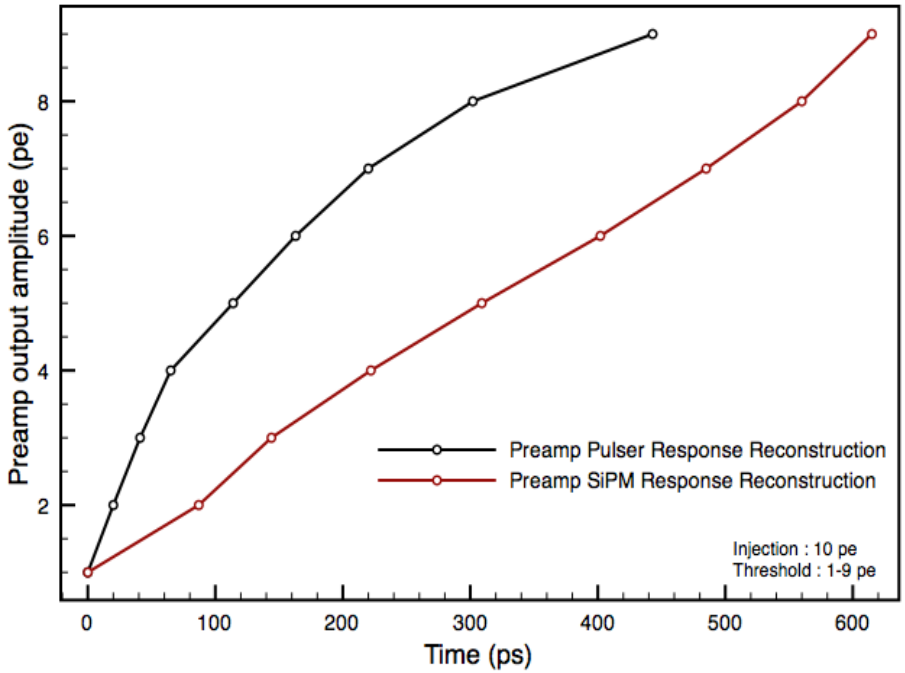


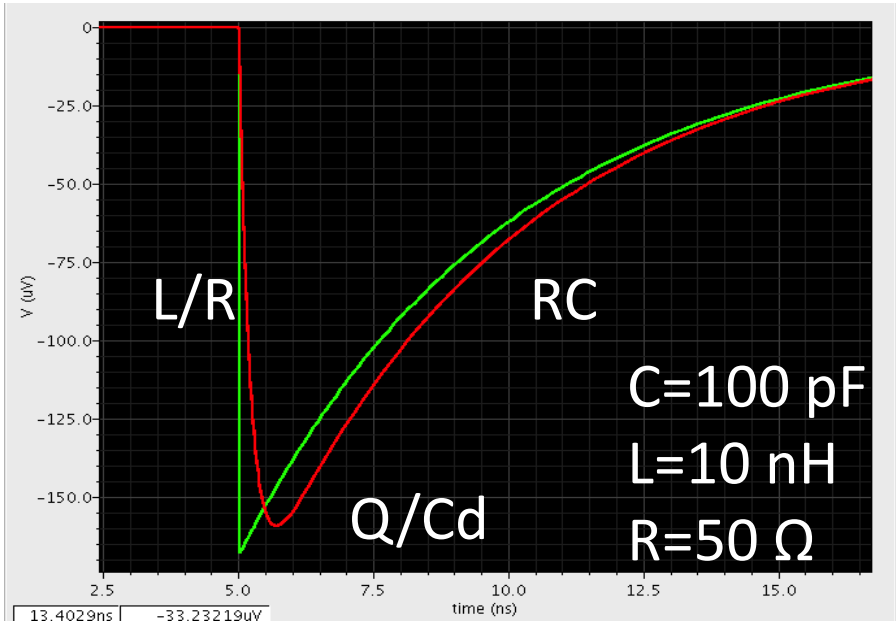
2 ns/div

Petiroc : bandwidth issues

- Pulser vs SiPM comparison
- SiPM is significantly slower than Petiroc
  - Pulser with 100pF injection capacitance, 10pe injec
  - SiPM illuminated with laser pulse, 10pe measured
  - Threshold from 1pe to 9pe
- Petiroc bandwidth meas. : 877MHz with puls
- With SiPm: limitation due to the stray inducta







ANALOG CIRCUIT DESIGN

Paul O’Connor

Analog Design

- Electronic Design Automation Tools and Foundry Access
- Analog CMOS Circuit Design
- Packaging, Interconnect and Systems Issues

Paul O'Connor, Brookhaven National Laboratory

IEEE Nuclear Sciences Symposium/Medical Imaging Conference

November 8, 2014

Design steps

- Specification
- Feasibility study
  - *technology selection*
  - *block definition, partitioning*
  - *die size estimate*
- Initial behavioral design
  - *user-developed high-level models and hand calculations*
- Schematic design and simulation*
- Physical design*
  - *Transistors and passives, modules, interconnect, signal and power routing, pad frame*
  - *Automatic layout generators, place-and-route tools where appropriate*
- Layout verification*
  - *Design rule check (DRC)*
  - *Electrical rule check (ERC)*
  - *Layout-vs-schematic (LVS)*
- Parasitic extraction and post-layout simulation*
  - *Nominal and corner process, voltage, and temperature*
  - *Full-chip simulation (transistor-level may be prohibitive)*

** Foundry's Process Design Kit (PDK) needed*

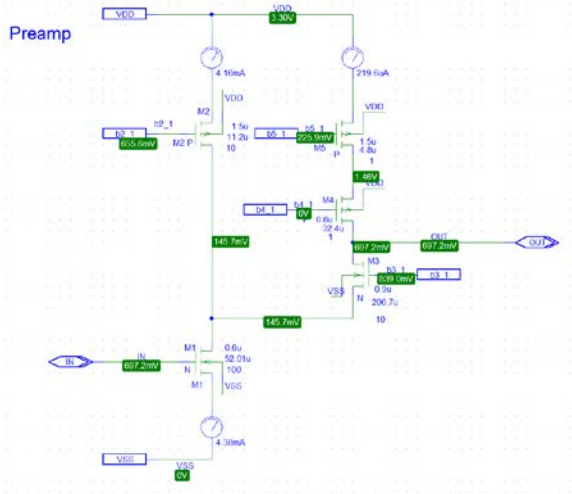
Electronic Design Automation (EDA)

- Commercial end-to-end tool chains:
  - *Cadence, Mentor Graphics, Synopsys, Magma: major providers*
  - *Tanner, Silvaco, Zeni-EDA: lower cost of entry*
- Many specialized point tools (RF, memory, image sensor, MEMS, ...)
- Public domain: *embedded.eecs.berkeley.edu/pubs/downloads* is a good starting point. See also opencircuitdesign.com/magic/ for Magic, a VLSI Layout Editor.

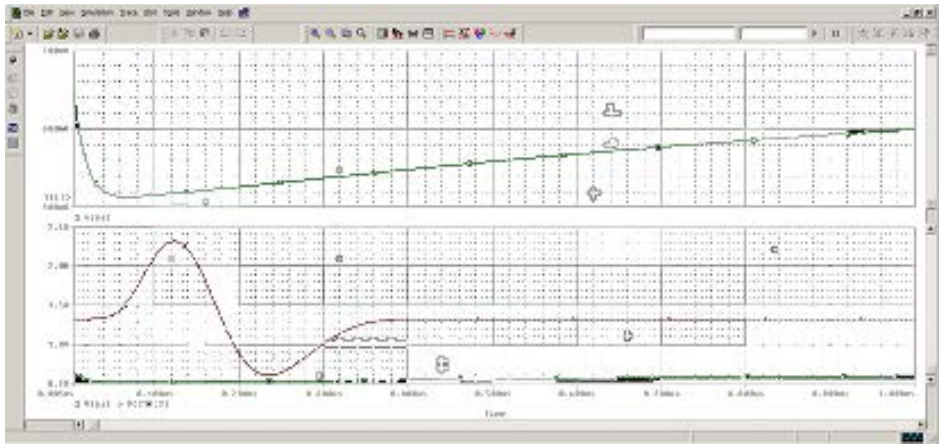
Essential tools for circuit-level design

- Transistor-level circuit simulator
  - *Matrix solution of network equations of your circuit*
  - *PSPICE, HSPICE, SPECTRE are the standards*
  - *inputs: circuit topology, device models, source driving functions*
  - *Outputs:*
  - *DC bias point, source sweep, temperature sweep*
  - *Frequency sweep using linearized model of active devices*
  - *Noise analysis in freq. domain*
  - *Time sweep*
  - *Monte-Carlo facility, samples from user-defined parameter distributions*
- Transistor models
  - *Strike a balance between*
    - Accurate in all transistor operating regions
    - Physics-based
      - Surface-potential based
      - Inversion charge based
    - Computational efficiency
    - Simple parameter extraction methodology
  - *Recent interest in CMOS for high-frequency RF applications and imagers has led to improved analog models*
  - *BSIM, EKV, MOS9 for advanced CMOS*
  - *Usually supplied by foundry*

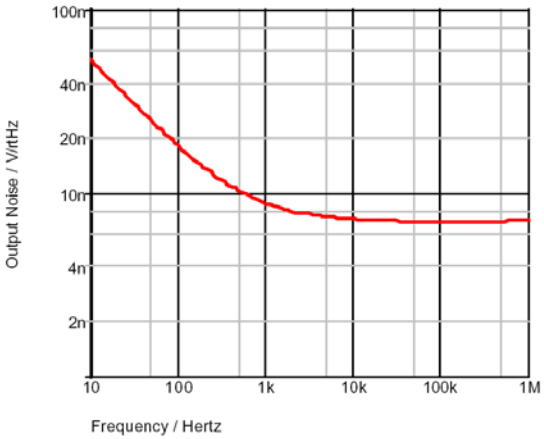
SPICE input & outputs



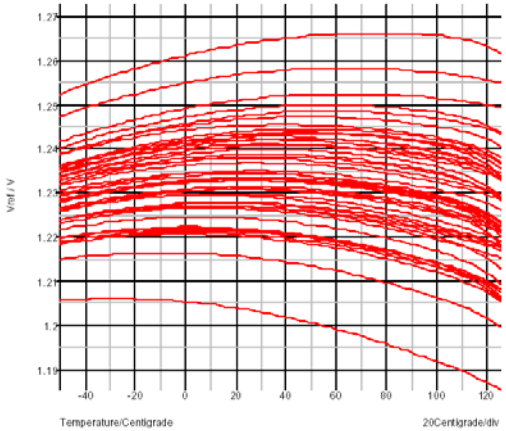
Schematic entry with backannotated node voltages and currents



Transient analysis result: voltages vs. time



Noise analysis: equivalent input noise density vs. frequency



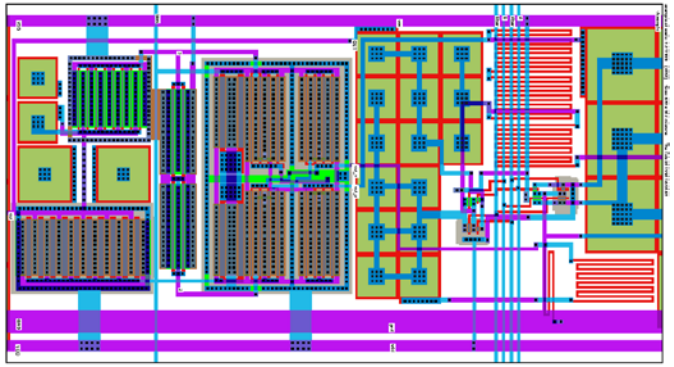
Monte Carlo analysis: node voltage vs. temperature, 50 runs from parameter distribution

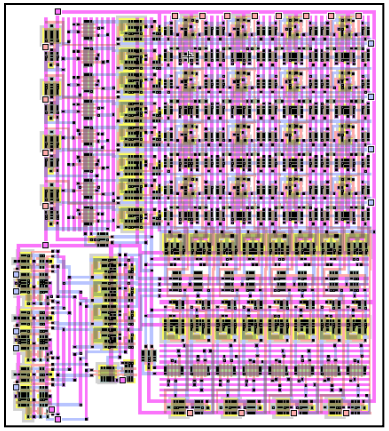
EDA tools for physical design

- Chip layout (full custom, no pre-designed blocks)
  - *Polygon-level mask editor with built-in process knowledge*
- Design rule checker
  - *Checks mask geometry, flags violations of foundry design rules*
- Connectivity verification
  - *Layout-to-schematic network comparison*
- Parasitic extraction
  - *Find capacitance, resistance associated with interconnect lines on chip*

Layout with MAGIC

500μm



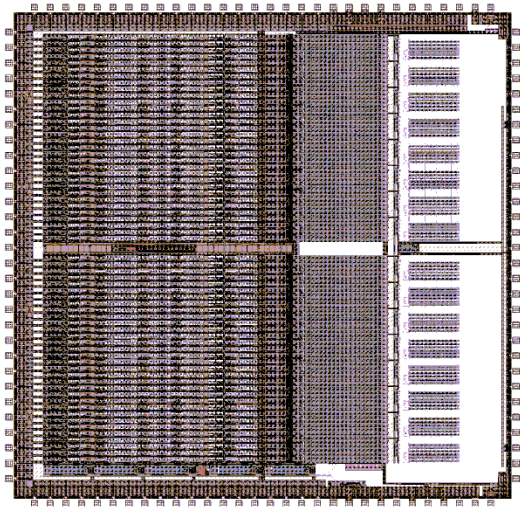


Analog and digital layout, 1.2μm CMOS

```
****** top level cell is ./preampflat.ext
C1 IN 2 5.00932e-13
Cxxnull 2  vss  1.323e-13
M1  BGND  IN  1  GND!  nch M=48  W=87.6U L=1.2U GEO=3
M2  1  VB1  Vdd  Vdd  pch M=2  W=42.0U L=3.0U GEO=3
M3  3  VB1  Vdd  Vdd  pch  W=30.0U L=3.0U GEO=3
M4  VSS  2  3  Vdd  pch  W=12.0U L=1.8U GEO=3
M5  2  BGND  1  Vdd  pch M=6  W=83.4U L=1.2U GEO=3
M6  2  VB2  VSS  GND!  nch  W=199.8U L=40.2U GEO=3
M7  VSS  VB2  OUT  GND!  nch M=3  W=199.8U L=40.2U GEO=3
M8  OUT  3  Vdd  GND!  nch M=24  W=87.6U L=1.2U GEO=3
R1 IN 3 57166.5
C3  9_2072_18#  OUT  1.0F
C4  9_226_18#  BGND  1.0F
C5  1  VSS  2.3F
C6  BGND  IN  8.6F
C7  Vdd  3  3.0F
C8  9_720_18#  BGND  1.0F
C9  1  IN  5.3F
C10  BGND  Vdd  1.8F
C11  OUT  3  4.2F
C12  Vdd  VSS  1.1F
C13  OUT  VB2  3.8F
C14  VSS  VB2  6.2F
C15  9_1806_18#  OUT  1.0F
C16  OUT  VSS  2.6F
C17  BGND  VSS  4.3F
C18  Vdd  VB1  1.1F
C19  1  GND 404.4F
C20  2  GND 79.6F
C21  3  GND 98.5F
C22  9_2072_18#  GND 1.0F
C23  VSS  GND 439.1F
C24  Vdd  GND 447.6F
C25  BGND  GND 449.7F
C26  9_226_18#  GND 1.0F
C27  9_720_18#  GND 1.0F
C28  OUT  GND 275.9F
C29  IN  GND 149.9F
C30  9_1806_18#  GND 1.0F
C31  VB1  GND 23.2F
C32  VB2  GND 96.3F
.END
```

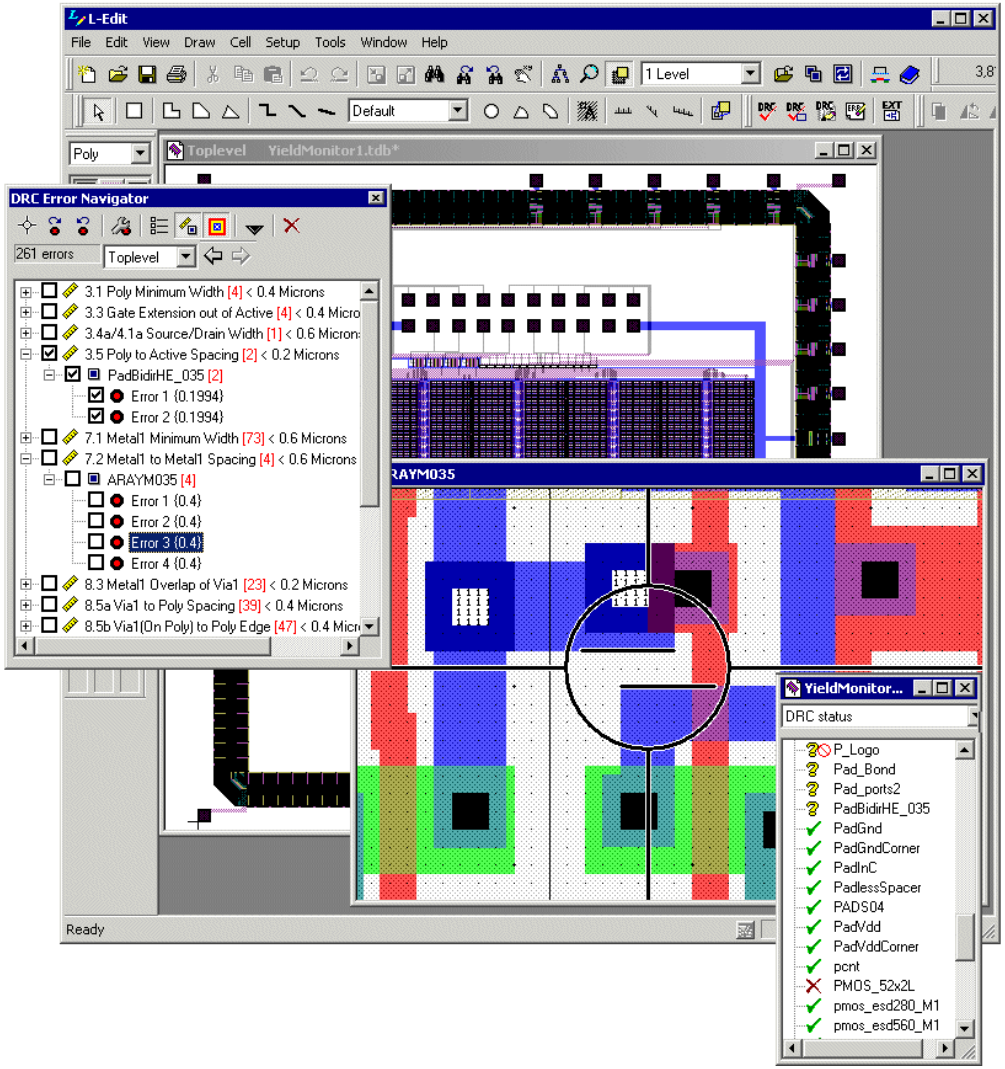
Circuit netlist extracted from layout w/ parasitic capacitances

6 mm



Mixed-signal circuit, 6×10^5 transistors, 0.25μm CMOS

Graphical Design Rule Check



Multiproject services for low-cost prototyping

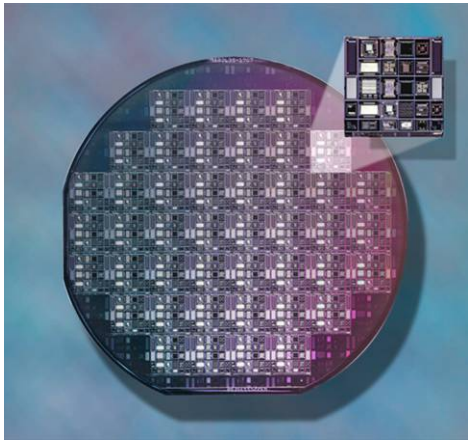
- Organize regularly-scheduled multiproject runs (MPW)
- Collect and merge designs and provide production-compatible masks to foundry
  - *share costs among users*
    - mask-area weighted
- Access to latest production processes from major foundries
  - *CMOS, BiCMOS, SiGe, CIS, (GaAs, InP, MEMS)*
- User support:
  - *design kit*
  - *models*
  - *parametric process data*
    - process control monitor and reference design probed after each MPW run
    - statistical process database
    - quality/yield monitor
  - *access to wafer thinning, dicing, wirebonding, and packaging services*
  - *low-volume production*

Multiproject services

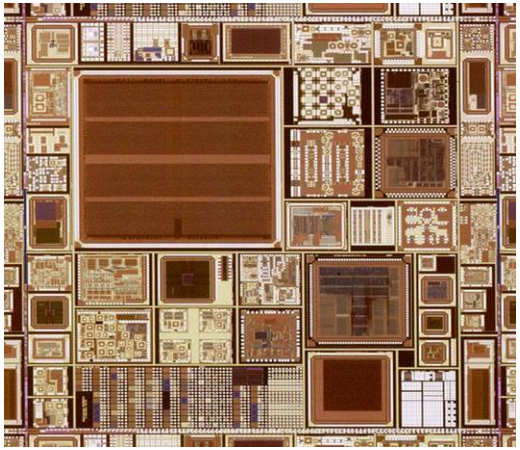
- Multi-foundry:
  - *MOSIS* *www.mosis.org*
  - *Europractice* *www.imec.be/europractice*
  - *Canadian Microelectronics* *www.cmc.ca*
- Foundry-based:
  - *TSMC* *www.tsmc.com*
  - *Global Foundries* *www.globalfoundries.com*
  - *XFAB* *www.xfab.com*
  - *Austria Microsystems* *www.austriamicrosystems.com*
  - *TowerJazz Semicond.* *www.jazzsemi.com*

MPW examples

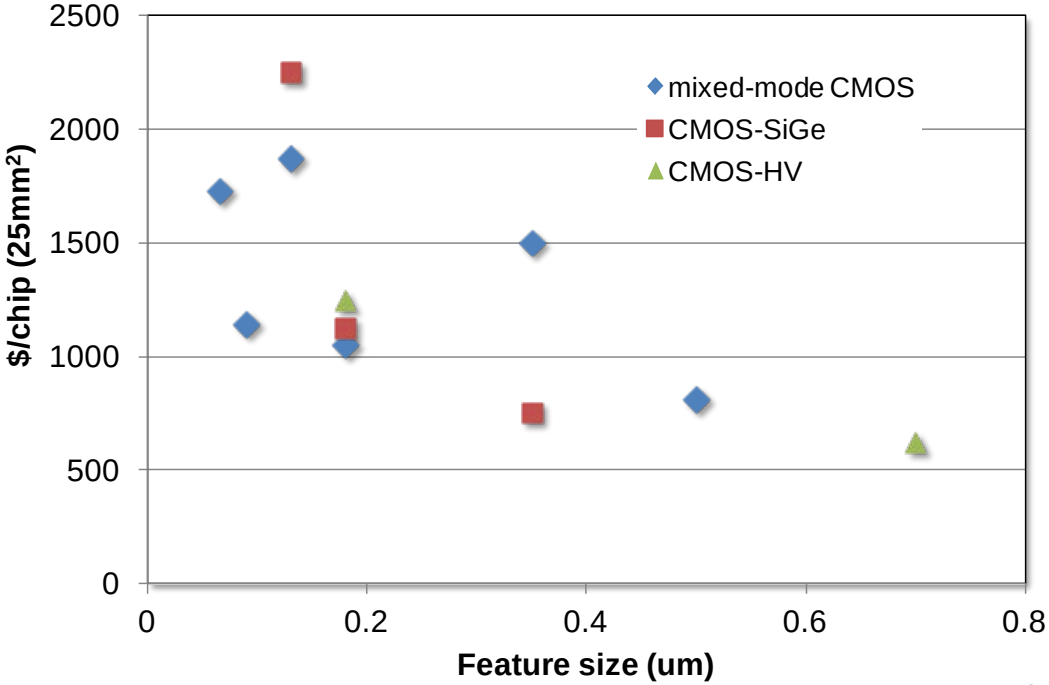
wafer



reticle (0.18μm CMOS)



Cost comparison



MOSIS 2014 MPW schedule

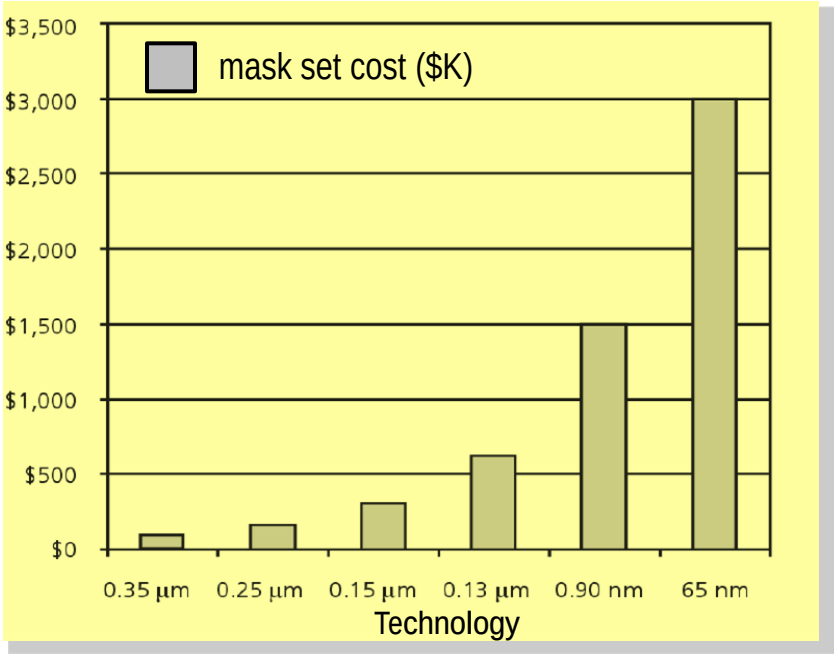
www.mosis.org

Example: foundry MPW schedule

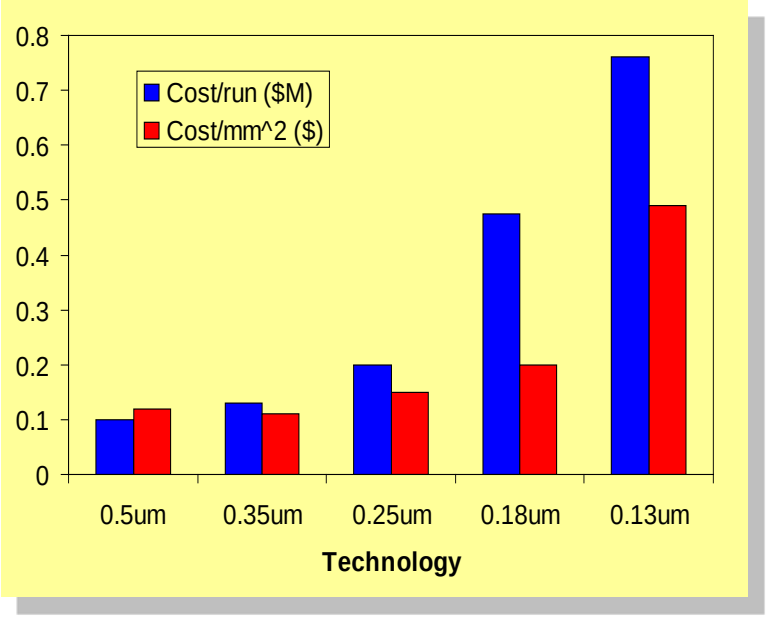
Technology Node	2012											
	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
20nm									●			
28nm		●				●					●	
40nm	●			●			●			●		
65nm		●	●			●		●		●		●
0.13um/0.11um	●		●		●		●		●		●	
0.18um	●	●		●	●	●	●		●	●	●	●
0.35um			●		●		●		●			●

Costs

Mask set

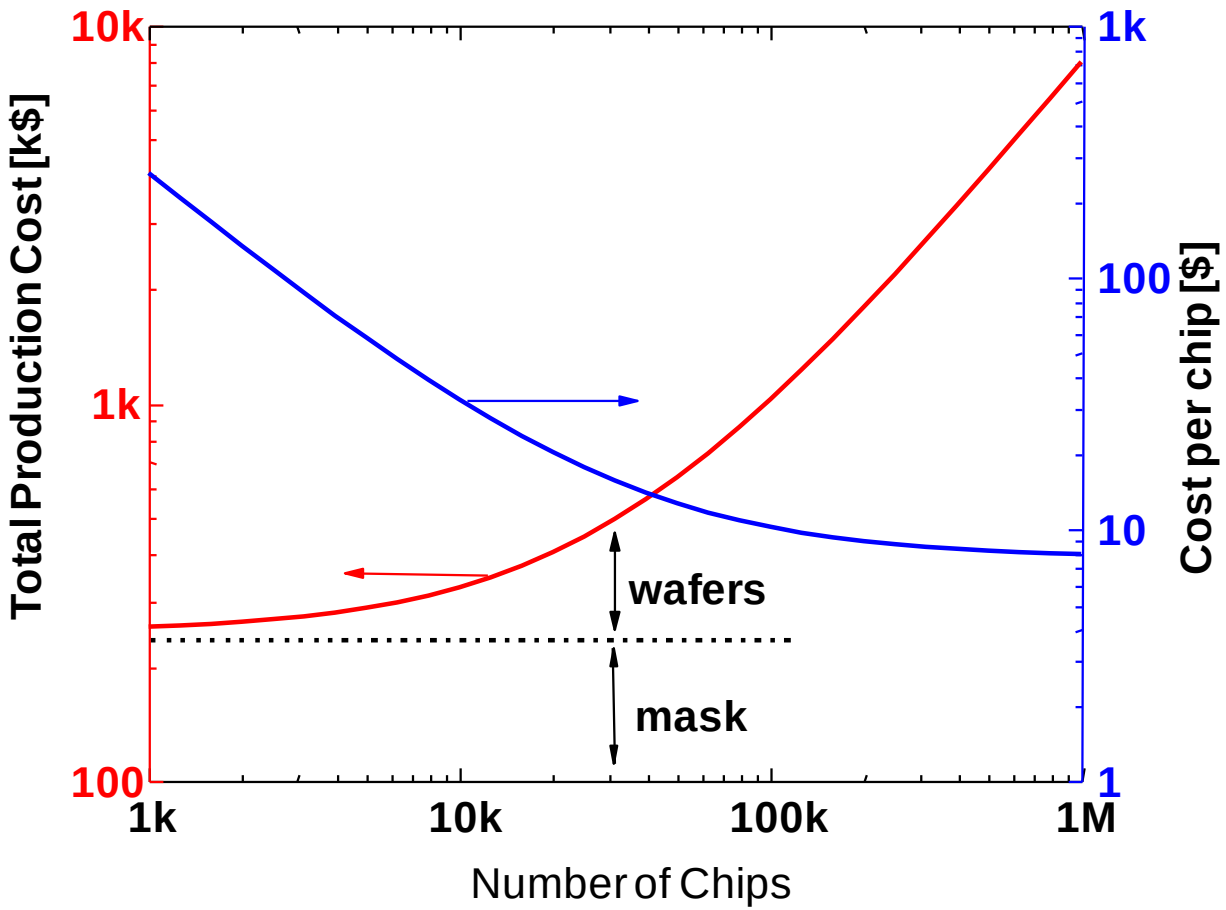


Engineering run

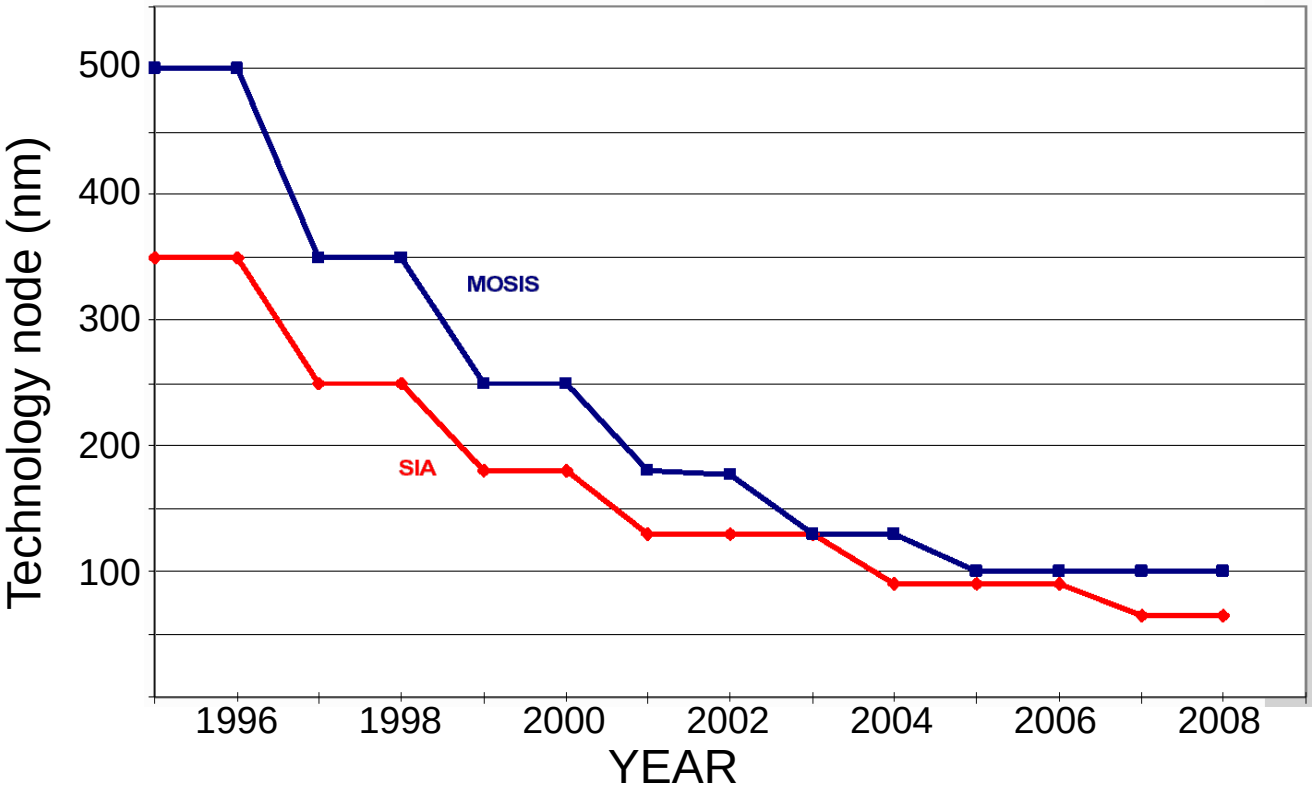


(typical engineering run = 20 wafers)

Cost of volume fabrication



Technology introduction roadmap
MOSIS and Semiconductor Industry Association



www.mosis.org
public.itrs.net

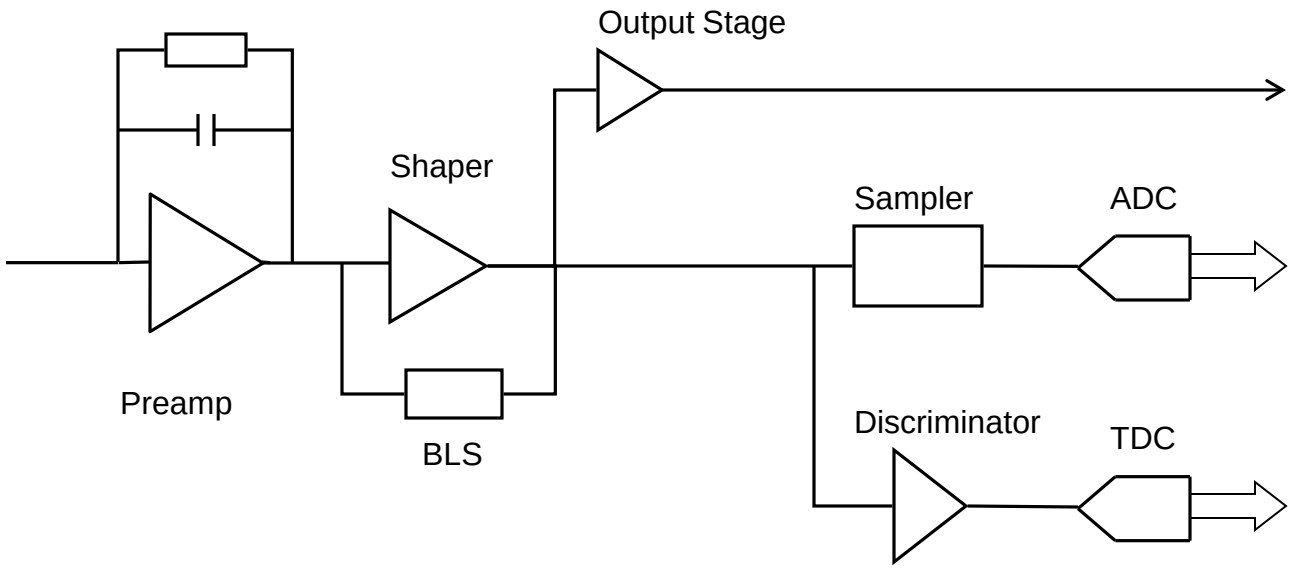
Analog CMOS Circuit Design

Paul O'Connor, Brookhaven National Laboratory

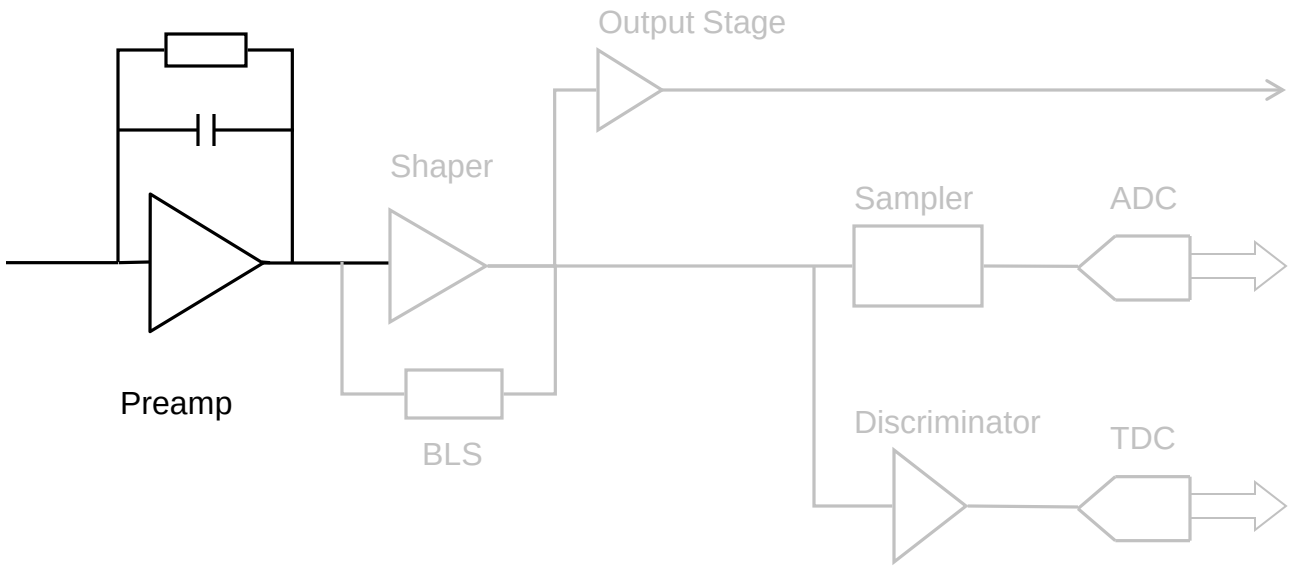
IEEE Nuclear Sciences Symposium/Medical Imaging Conference

November 8, 2014

Signal Chain Block Diagram



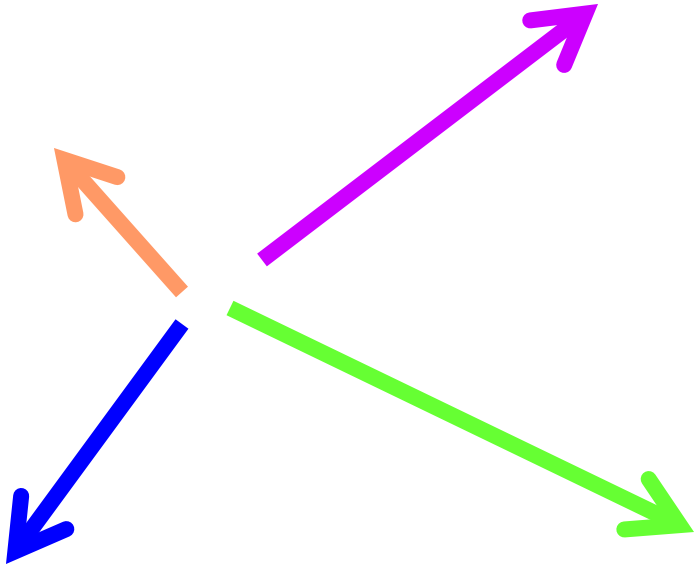
Charge Sensitive Preamplifier



MOS charge amplifier design

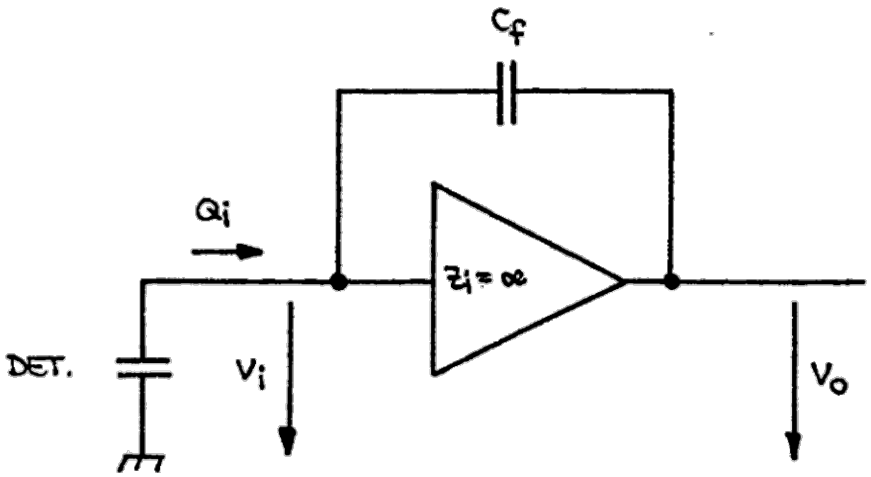
- Key parameters:
  - C_{det} , I_{det} , Q_{max} *(detector)*
  - *Rate*, P_{diss} *(system)*
  - f_T , K_F , I_{in} *(technology)*

- Key design decisions
  - *NMOS/PMOS*
  - L_g
  - C_{gs}/C_{det}
  - *Reset system*
  - *Weighting function*



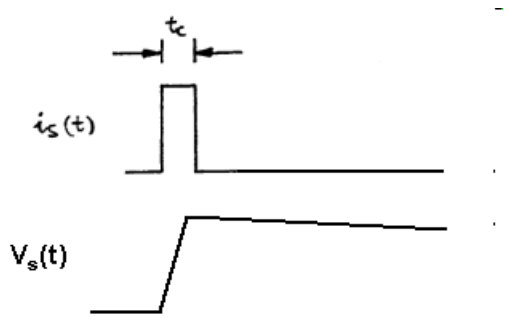
Low noise charge amplification

- Charge sensitive configuration (active integrator)



for $Z_{in}, |A_V| \to \infty$

$$V_s = \frac{\int i_s(t)dt}{C_f} = \frac{Q_s}{C_f}$$



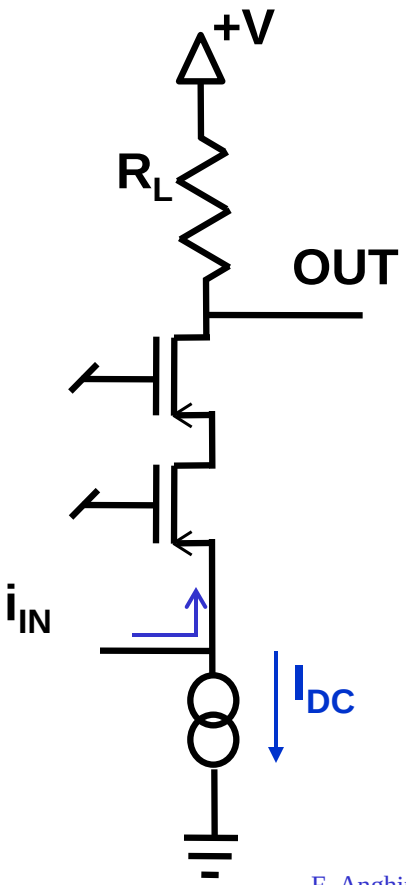
Gain <u>insensitive</u> to C_{det} and A_V

Best for

- *low power*
- *moderate rates*
- *high linearity*

Low noise charge amplification

- Common gate configuration (current amplifier)



$$Z_{in}=1/g_{mb}$$

$$\tau \sim R_L * C_L$$

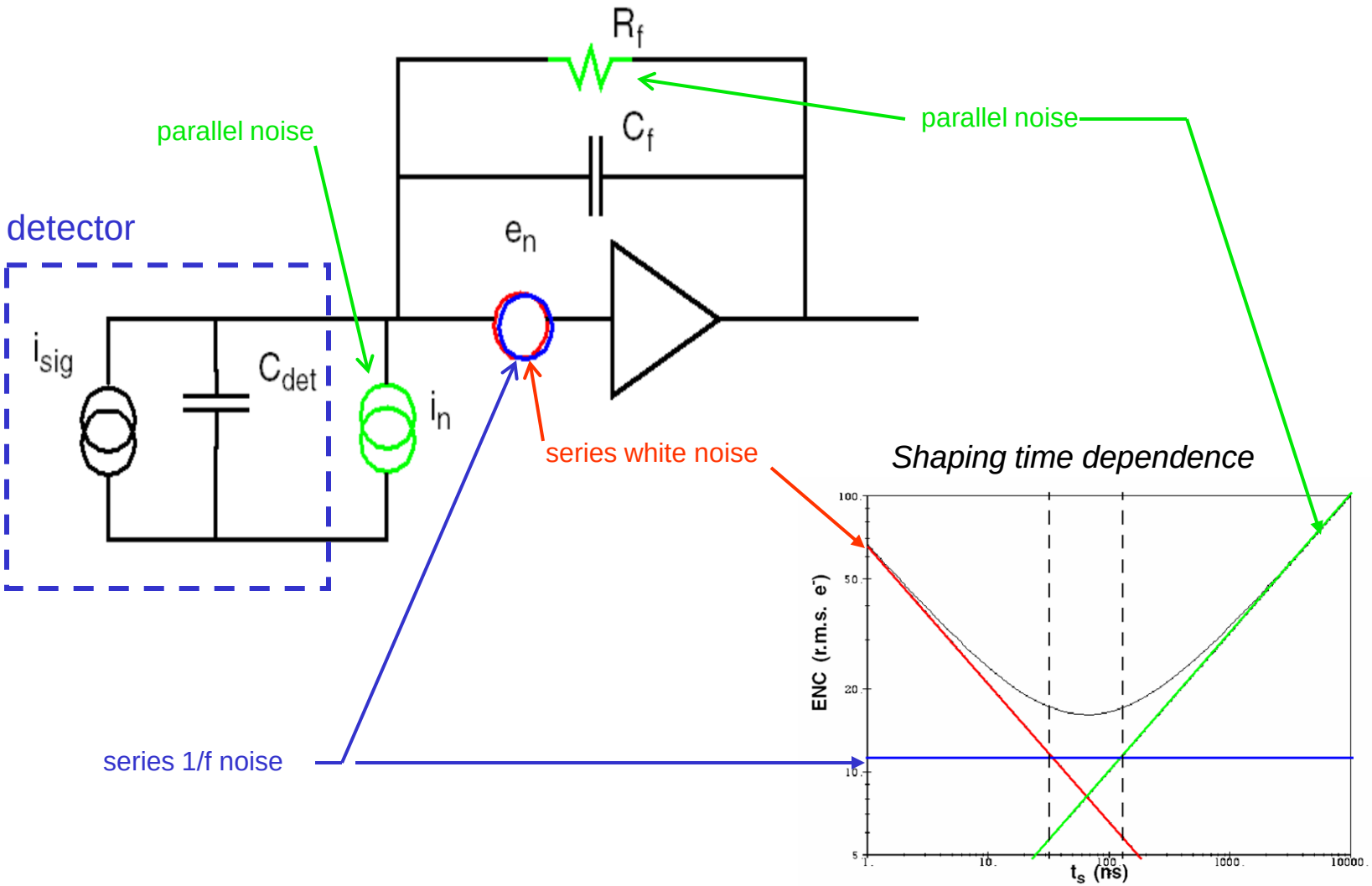
$$V_{OUT} = i_{in} * R_L$$

Best for

- *fast risetime*
- *high rates*
- *controlled, low input impedance*

F. Anghinolfi et al, "NINO, an ultra-fast, low-power, front end amplifier discriminator for the Time-of-Flight detector in the ALICE experiment",NIM A533 (2004), 183-187

Charge amplifier noise sources



Equivalent Noise Charge ENC

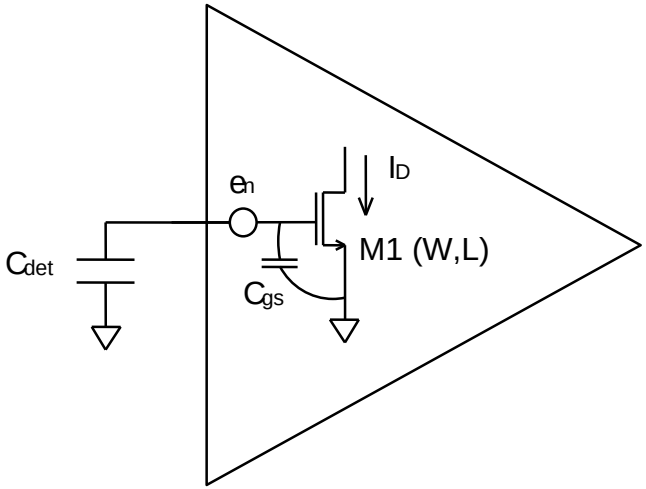
$$ENC^2 = \tfrac{1}{2}\, e_{nw}^2 C_{in}^2 A_1/\tau + \pi C_{in}^2 A_f A_2 + q I_0 A_3 \tau$$

e_{nw}	*series white noise spectral density, nV/√Hz ~ $1/g_m$*
C_{in}	*includes contribution from detector, parasitics, and input transistor*
τ	*characteristic shaping time*
I_0	*leakage current + resistive elements*

Noise optimization:

- Shaping time and detector capacitance dictated by the application
- Determine magnitude of parallel noise
- Determine power (drain current) allocation for the front end
- Choose an amplifier topology
- Dimension the input MOSFET

Dimensioning the input MOSFET for minimum noise



$$ENC^2 = \left(C_{det} + C_{gs}\right)^2 \cdot \left(\frac{4kT\gamma}{g_m \cdot t_m} + \frac{K_F}{C_{gs}}\right)$$

white 1/f

Choose minimum L for best g_m/C_{gs} ratio

Increasing M1 width makes e_n smaller while C_{gs} gets larger

$\Rightarrow$ ***optimum width for M1 must exist***

1/f noise:

$$C_{gs,opt} = C_{det}$$

White -- two cases :

I. Fixed V_{gs} (fixed current density, fixed f_T)

$$g_m \propto C_{gs}$$

$$C_{gs,opt} = C_{det}$$

II. Fixed I_D (practical case)

$$g_m \propto C_{gs}^{1/2} \text{ [strong inversion]}$$

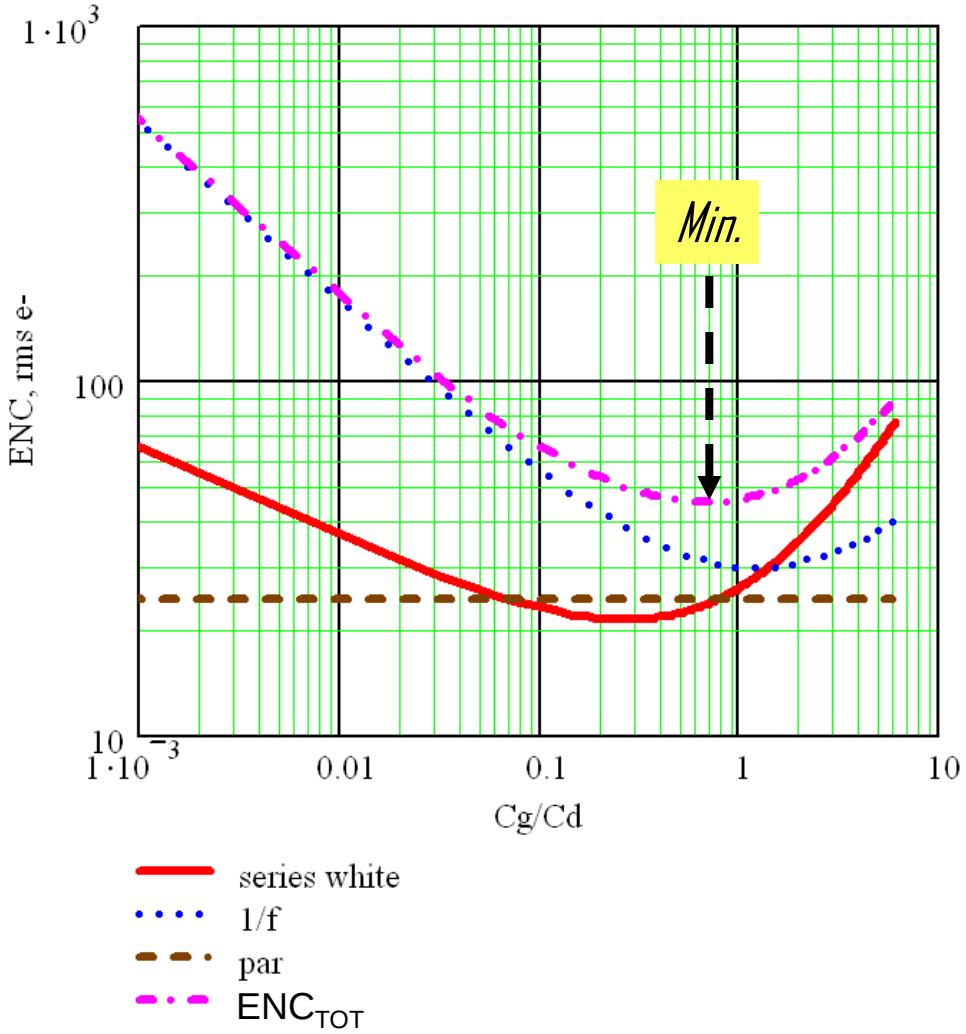
$$C_{gs,opt} = C_{det}/3$$

P. O'Connor, G. De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", NIM A480 (2002), 713 - 725

Composite noise

- C_{det} = 3 pF
- t_p = 0.5 μs
- P_{diss} = 1 mW
- I_{leak} = 100 pA
- Technology: 0.35 μm NMOS

- *Optimum width for series noise is a compromise between white and 1/f components*



Optimizing the input MOSFET using advanced models

Series noise "capacitive match" problem:

$$ENC^2 = ENC_{sw}^2 + ENC_f^2$$

$$ENC_{sw}^2 = \frac{a_1}{2\tau_p} e_{n,sw}^2 (C_d + C_{in})^2$$

$$e_{n,sw}^2 = \frac{4kTn\gamma}{g_m}$$

$$ENC_f^2 = a_2 \pi \frac{K_F}{C_{ox} WL} (C_d + C_{in})^2$$

γ and g_m depend on region of operation:

	γ	g_m
weak	1/2	qI_D / nkT
strong	2/3	$\sqrt{2\mu C_{ox} \frac{W}{L} I_D}$

How to handle moderate inversion?

G.De Geronimo, P.O'Connor , V. Radeka and B. Yu, "Front-end electronics for imaging detectors", *Nuclear Instrum. Methods* A471 (2001) 192-199

P. O'Connor and G.De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", *Nuclear Instrum. Methods* A484 (2002) 713-725

L. Fabris, P. Manfredi, "Optimization of front-end design in imaging and spectrometry applications with room temperature semiconductor detectors", *IEEE Trans Nucl. Sci*., 49 (4) ,1978 –1985, Aug. 2002

M. Manghisoni, L. Ratti, V. Re, and V. Speziali, "Submicron CMOS Technologies for Low-Noise Analog Front-End Circuits", *IEEE Trans. Nucl. Sci.* 49,1783-1790, Aug. 2002

Simplified EKV model for hand calculations

- substrate-referenced compact MOS model
- small, physics-based parameter set
- continuous modeling of weak to strong inversion
- simple set of equations valid for saturation:

Inversion coefficient $i = I_D / I_0$

$$I_0 = 2n\beta \cdot U_T^2 \qquad \beta = \mu \cdot C_{ox} \frac{W}{L} \qquad U_T = \frac{kT}{q}$$

Interpolation function :

$$f(i) = \frac{1}{2}\left(\sqrt{1+4i}+1\right)$$

$$\frac{g_m}{I_D} = \frac{1}{n \cdot U_T} \frac{1}{f(i)}$$

$$\frac{C_{GS}}{WLC_{ox}} = \frac{1}{\frac{3}{2} + \frac{f(i)}{i}}$$

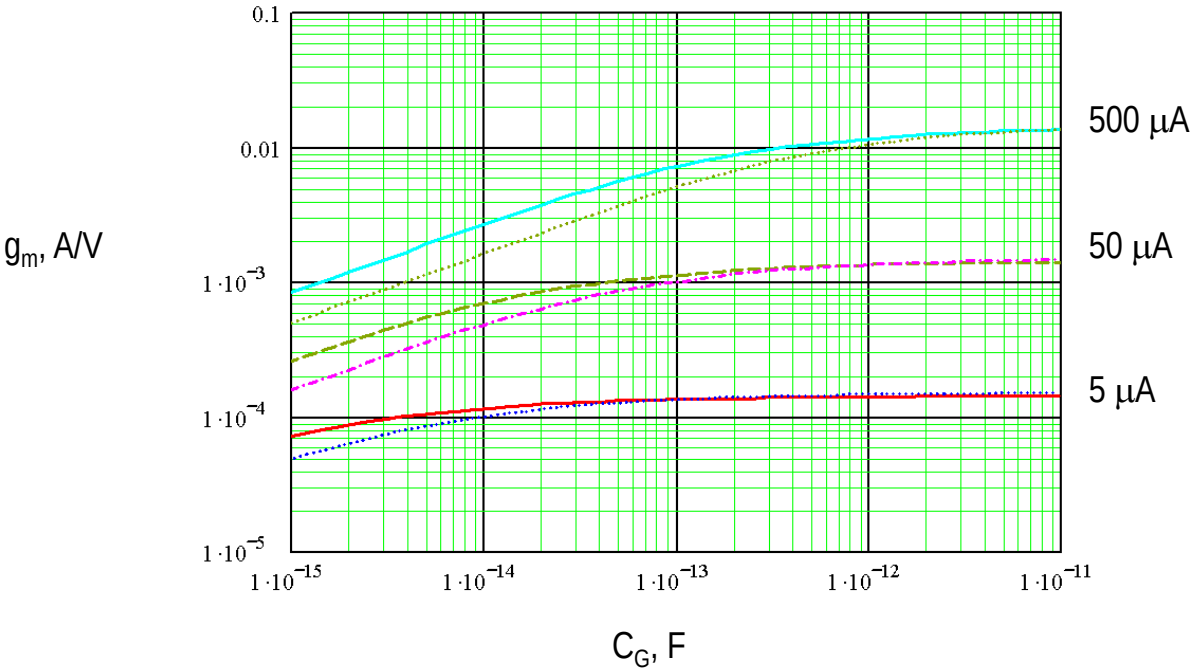
$$\frac{S_{th}}{4kTng_m} = \frac{\frac{1}{2} + \frac{2}{3}i}{1+i} \equiv \gamma$$

short-channel effects not modeled

C. Enz, F. Krummenacher, E. Vittoz, “An Analytical MOS Transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications”, *Analog Integrated Circuits and Signal Processing* 8, 83-114 (June 1995)

g_m vs. C_G vs. scaling

L := .18μ



NMOS (upper) PMOS (lower)

Strong inversion:

$g_m \sim \sqrt{C_G}$

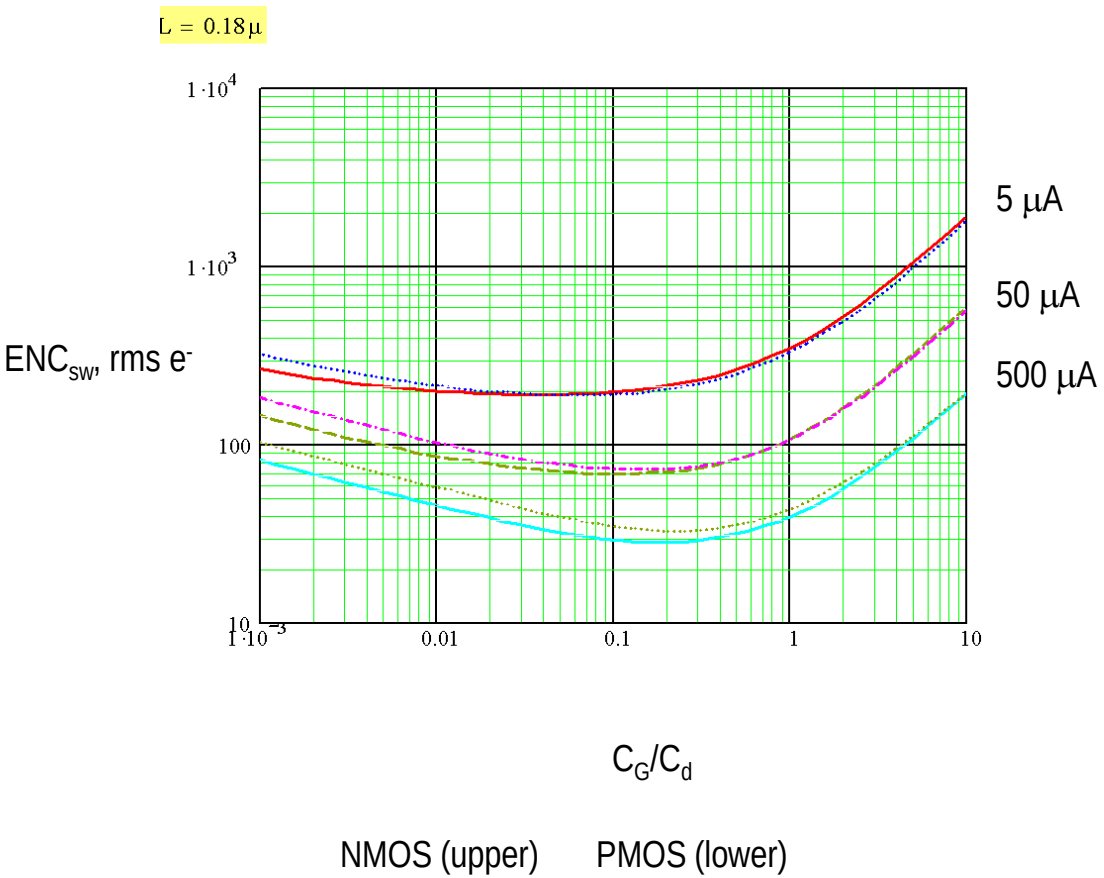
$g_{m,n} \sim 3g_{m,p}$

Weak inversion:

$g_m \sim const.$

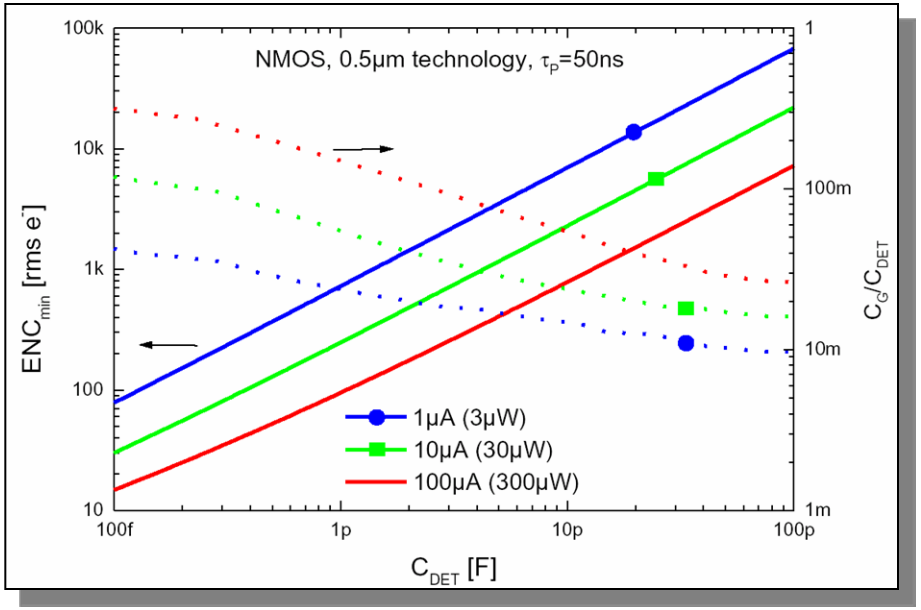
$g_{m,n} = g_{m,p}$

White series noise vs. C_G/C_d vs. scaling

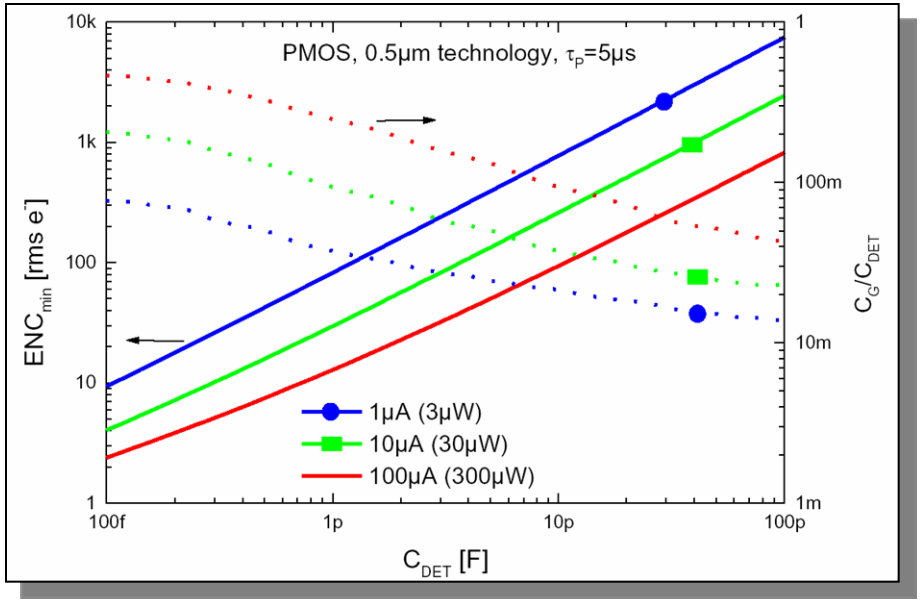


White series ENC, $C_{G,opt}/C_{DET}$ vs. C_{DET}

NMOS



PMOS



For fixed power budget,

$$ENC \propto \begin{cases} C_{DET}, \text{ weak inversion} \\ C_{DET}^{3/4}, \text{ strong inversion} \end{cases}$$

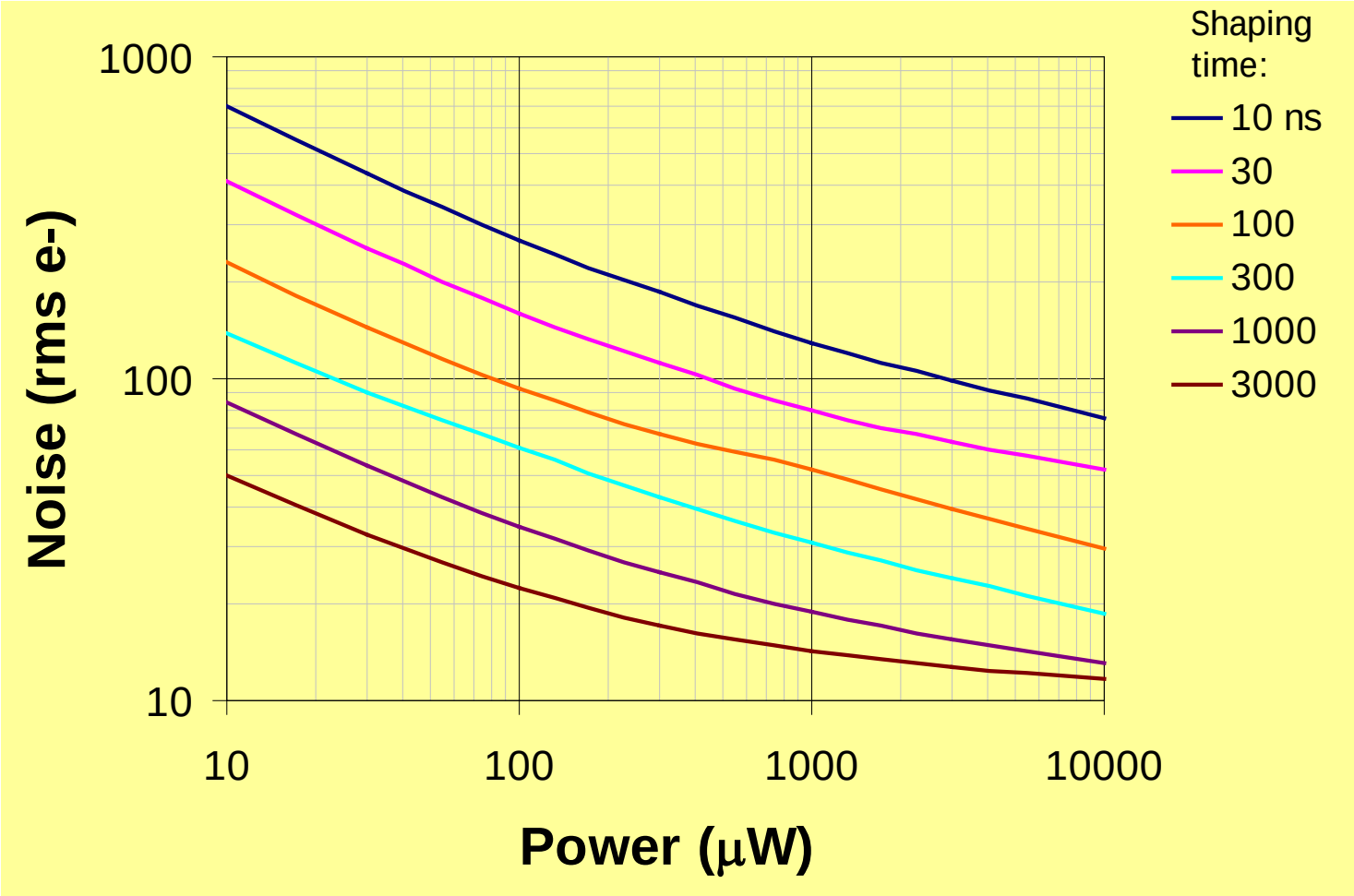
Power allowed to scale with C_{DET}:

$$ENC \propto C_{DET}^{1/2}$$

De Geronimo et al. , NIM A 471 (2001) 192 - 199

Optimized noise vs. power

(MOSFET optimized at each power level and shaping time)

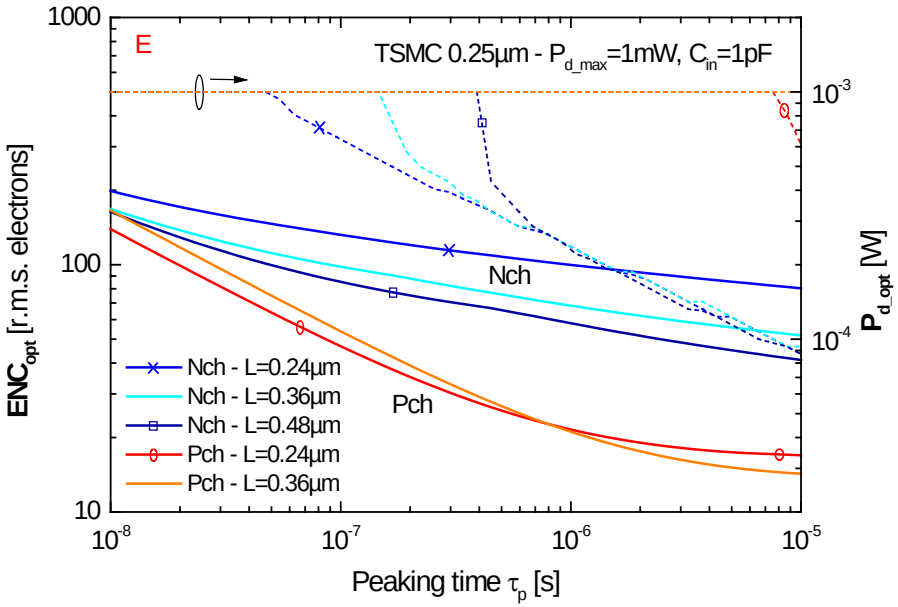


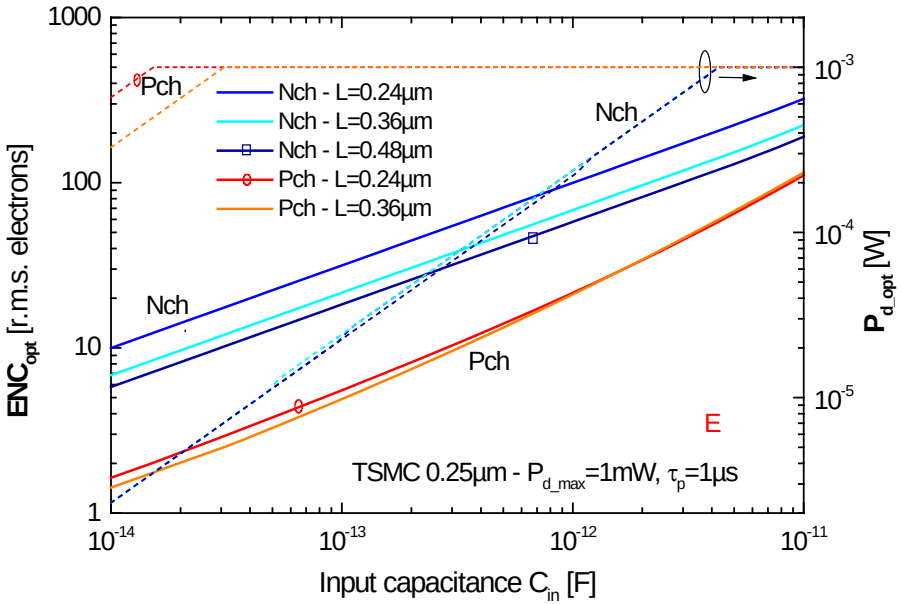
Note:

$$\left|\frac{PdN}{NdP}\right| \leq 0.4$$

Cd = 1pF
0.25 μm CMOS

0.25μm CMOS optimized noise/power





Enhanced noise model incorporates:

- *Gate capacitance bias dependence*
- *Gate-source and gate-drain overlap capacitance*
- *Length-dependent 1/f noise coefficient*
- *$1/f^{\alpha}$ behavior of low-frequency noise*

$L > L_{min}$ in most cases

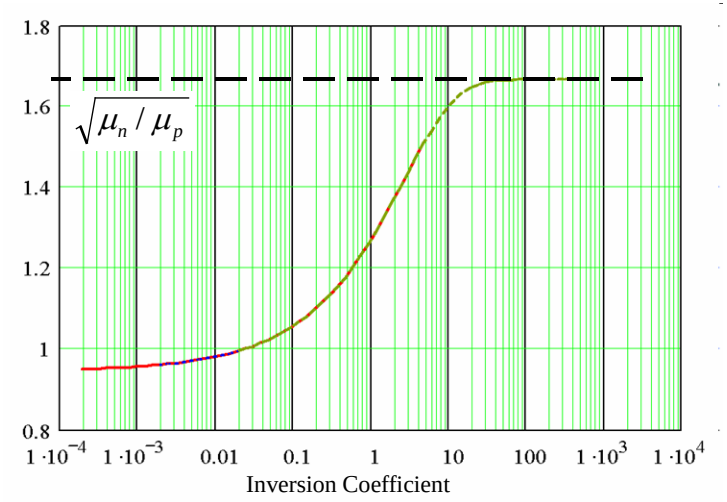
$P < P_{max}$ with C_d small and 1/f noise dominant

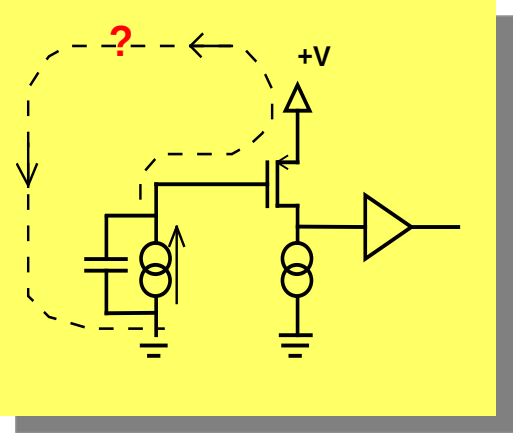
G. De Geronimo, P. O'Connor, IEEE Trans. Nuc. Sci.52,3223-3232 (2005)
G. De Geronimo, "Low Noise Electronics for Radiation Sensors", in *Medical imaging: Principles, Detectors, and Electronics*, ed. K. Iniewski, Wiley (2009)

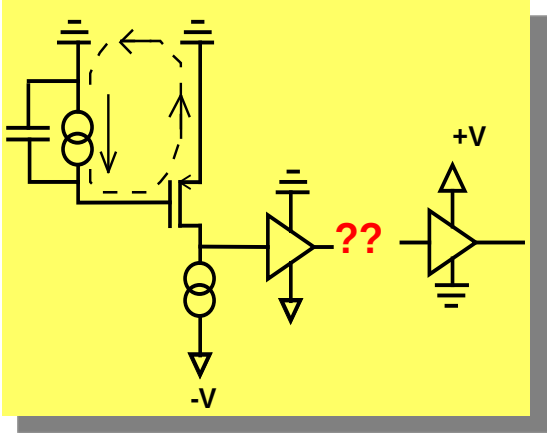
Choice of PMOS vs. NMOS

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse* V_{BS} *to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin* t_{ox}
- *Single-supply operation of PMOS-input preamp awkward:*

g_{mn}/g_{mp} vs IC







Minimum series noise

- Input MOSFET fully optimized:

$$ENC_{sw,opt} \approx \sqrt{kTC_{\det}}\sqrt{\frac{\tau_{el}}{t_m}}$$

$$ENC_{1/f,opt} \approx \sqrt{K_F C_{\det}}$$

τ_{el} = electron transit time under the gate $= C_{gs} / g_m$

- Key ingredients for low series ENC:
  - *low* C_{det}
  - *long* t_m
  - *short* τ_{el}
  - *low* K_F

Gate resistance noise

- Polysilicon gate is resistive:
  - ρ_{poly} **25 Ω/sq.**
  - $\rho_{silicided\ poly}$ **4 Ω/sq.**

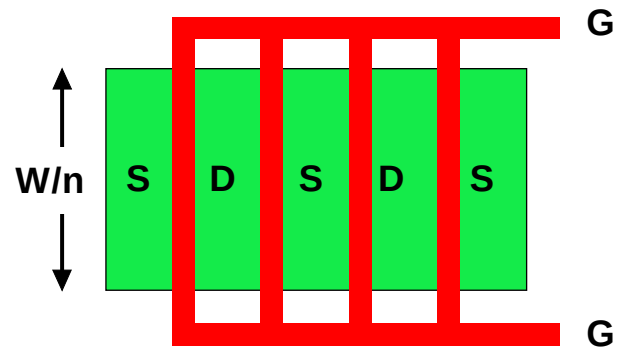
resistance of non-interdigitated gate:

$$R_g = \rho_{poly} \cdot \frac{W}{L}$$

series noise due to gate resistance:

$$e_{ng}^2 = 4kT \cdot R_{eq}$$

FET with interdigitated layout



n gate fingers
n = 4

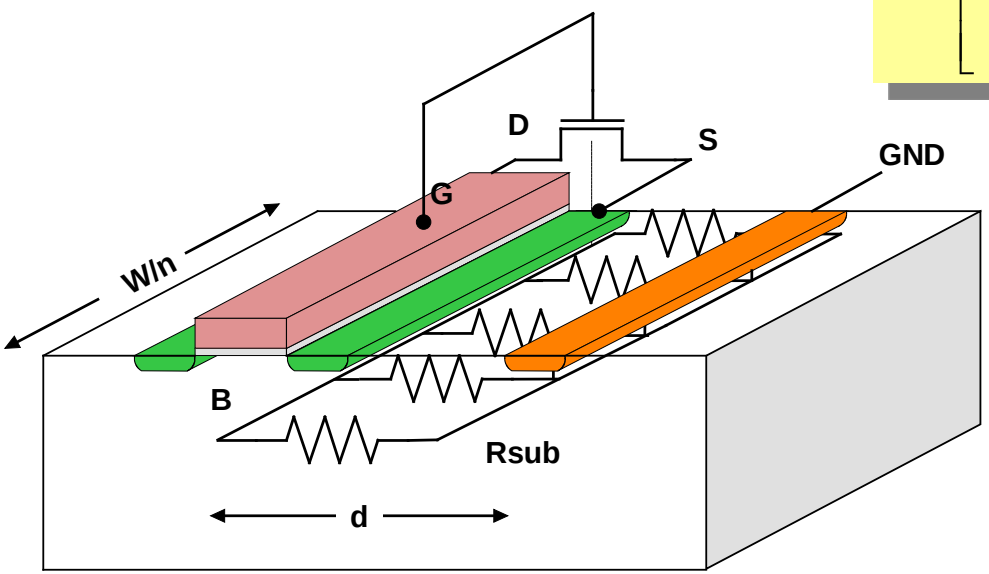
Layout	Req driven one end	Req driven both ends
Single finger	Rg/3	Rg/12
Interdigitated n fingers	$Rg/3n^2$	$Rg/12n^2$

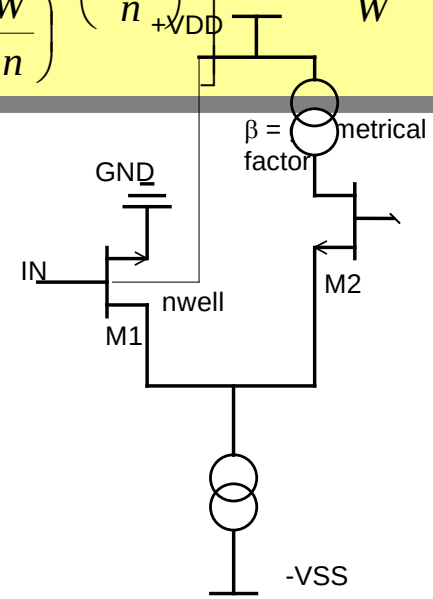
Bulk resistance noise

- Resistive substrate couples to the channel via the back transconductance g_{mb}.
- Substrate resistance is distributed.

leads to noise in the channel:

$$i_{db}^2 = \left[4kT \cdot n \cdot \beta \frac{d}{\left(\frac{W}{n}\right)} \cdot \left(\frac{g_{mb}}{n}\right)^2 \right] = 4kT\beta \frac{d}{W} g_{mb}^2$$

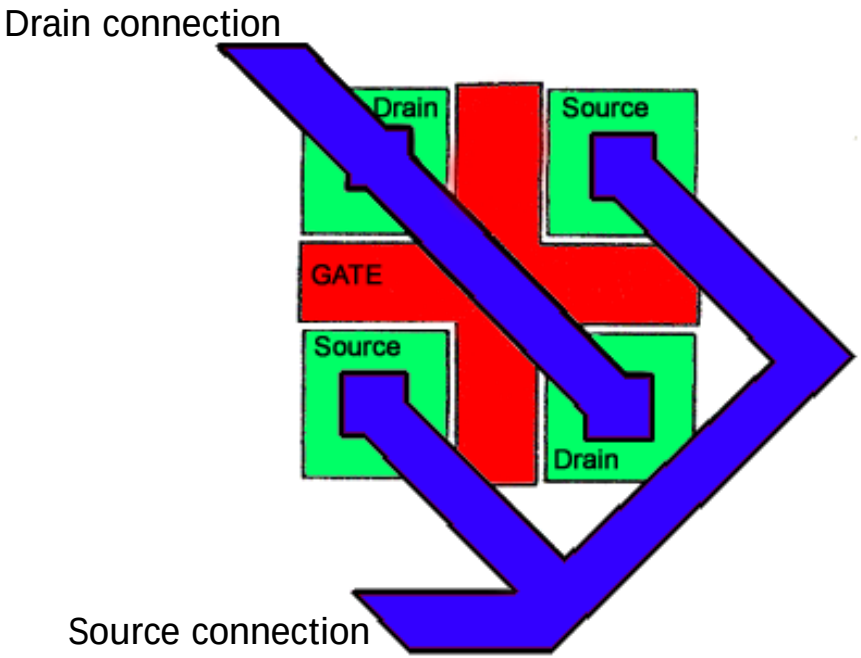




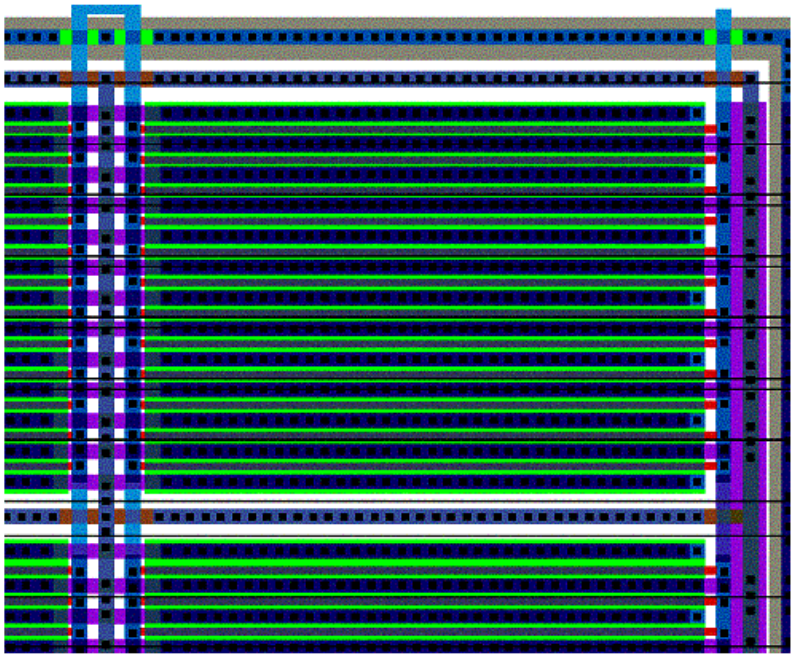
- Minimize by reverse biasing the source-substrate junction.

Layout techniques to reduce gate and bulk resistance noise

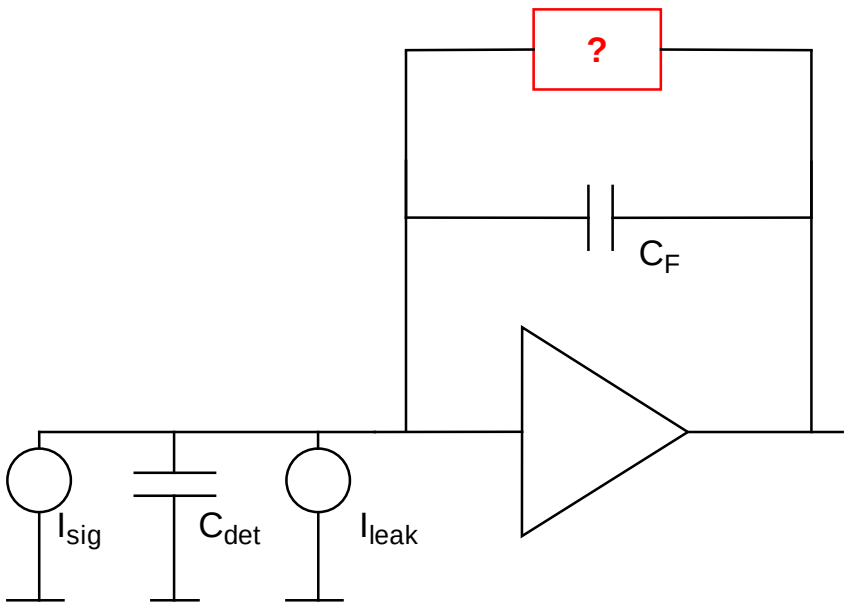
Waffle iron layout



Substrate contacts, guard ring, multiple gate fingers contacted both ends

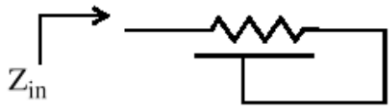


Preamp reset – requirements



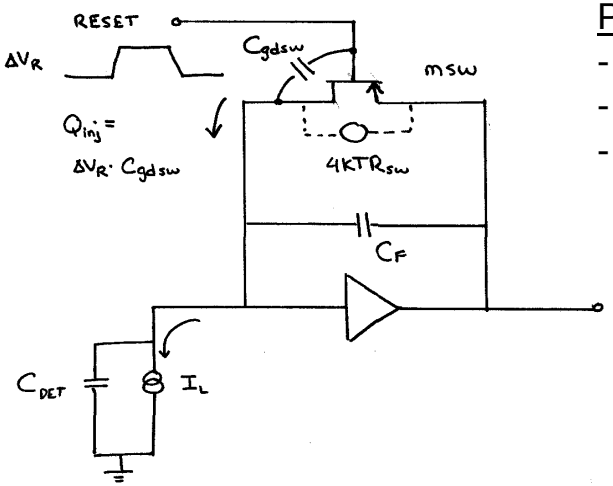
- all charge preamplifiers need DC feedback element to discharge the input node and stabilize the bias point
- usually, a resistor in the MΩ – GΩ range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - *insensitive to process, temperature, and supply variation*
  - *low capacitance*
  - *lowest possible noise*
  - *linear*

Preamplifier reset – monolithic techniques (1)



$$i_n^2 = \frac{4kT}{Re\{Z_{in}\}}$$

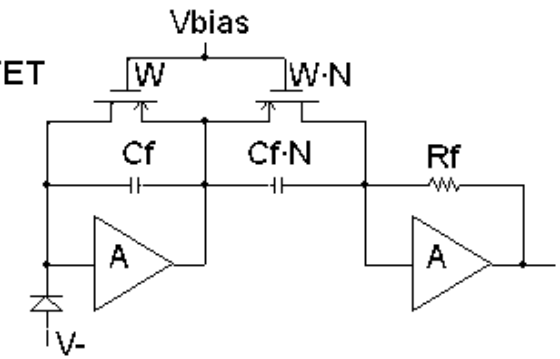
Physical resistor
- always accompanied by parasitic capacitance
- de-stabilizes circuit and increases noise
- noise higher than 4kT/R by factor ~ RC/t_m



Pulsed reset by MOS switch
- sampled noise $\sqrt{kTC_F}$
- Q_{inj} noise from switch control voltage
- leakage current integrates on output node $dV_{out}/dt = I_L/C_F$

Preamplifier reset – monolithic techniques (2)

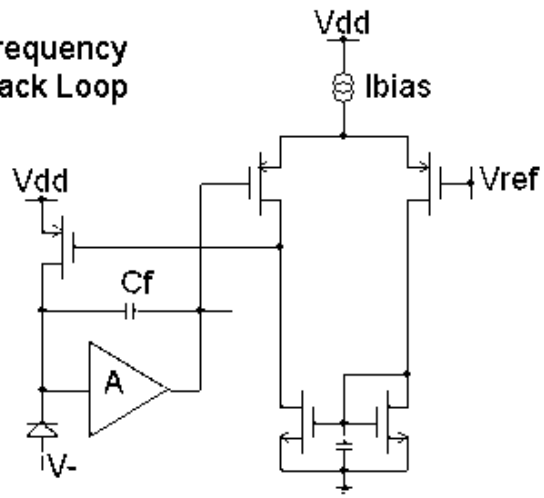
Single MOSFET



O'Connor et al., TNS v44 n3 (1997)
De Geronimo et al., NIM A421 (1999)
De Geronimo et al., TNS v47 n4 (2000)

- provides effective current gain -N
- full compensation (high linearity)
- minimum noise (thermal)
- requires baseline stabilization
- can be realized in multiple stages

Low Frequency Feedback Loop

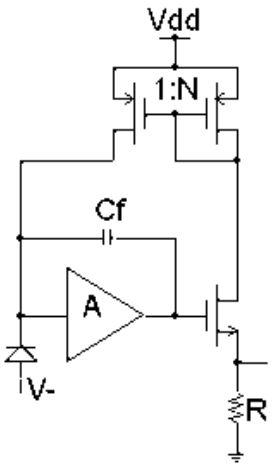


Krummenacher, NIM A350 (1991)
Ludewigt et al., TNS v41 n4, (1994)
Vandenbussche et al., TNS v45, n4 (1998)
Manfredi et al., Nucl.Phys.B 61B, Proc.Suppl. (1998)

- noise can be high
- requires baseline stabilization at high rates
- compensation an issue

Preamplifier reset – monolithic techniques (3)

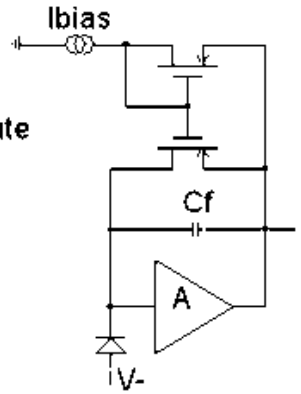
R-Scaling



Santiard et al., CERN-ECP/94-17 (1994)
Chase et al., NIM A409 (1998)
Sampietro et al., Elec.Lett. v34 n19 (1998)

- noise can be high (large values of R and N required)
- linearity an issue
- parasitic capacitor an issue
- compensation available in some configuraitions
- requires baseline stabilization

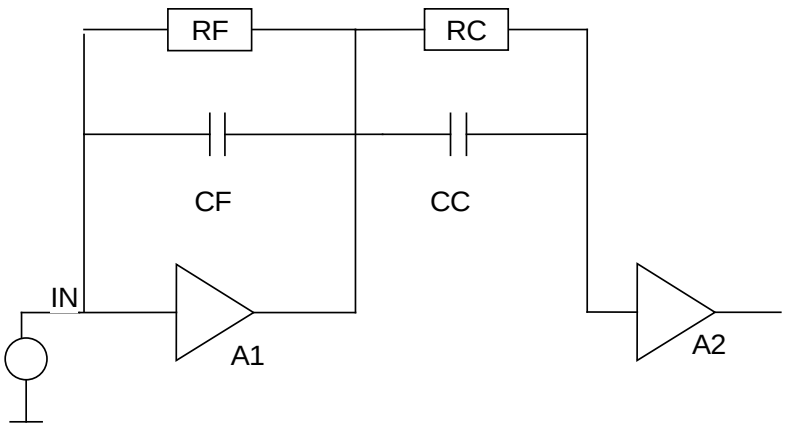
Slew-rate Limited



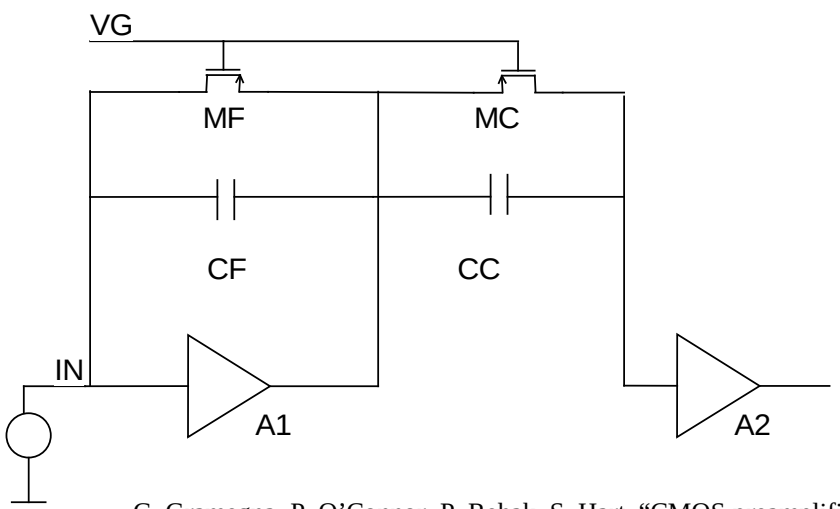
Blanquart et al., NIM A395 (1997)
Blanquart et al., NIM A439 (2000)

- MOSFET operates in saturation only when there is signal activity
- noise can be high (it requires Ibias > Idet)
- parasitic capacitor an issue
- suitable for Time-Over-Threshold processing techniques
- requires baseline stabilization at high rates
- linearity an issue
- compensation an issue

Nonlinear pole-zero compensation



- Classical
  - *RF · CF = RC ·CC*
  - *Zero created by RC,CC cancels pole formed by RF, CF*

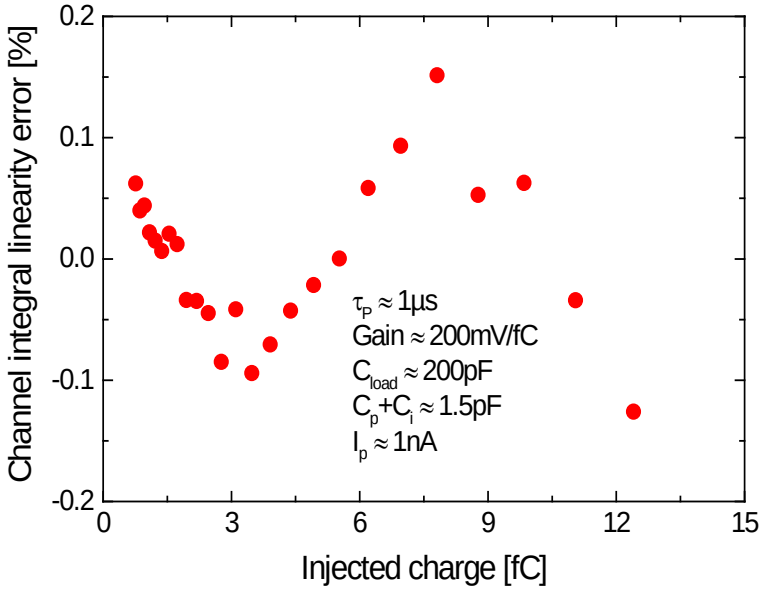


- IC Version
  - *CC = N · CF*
  - *$(W/L)_{MC} = N \cdot (W/L)_{MF}$*
  - *Zero created by MC, CC cancels pole formed by MF, CF*
  - *Rely on good matching characteristics of CMOS FETs and capacitors*

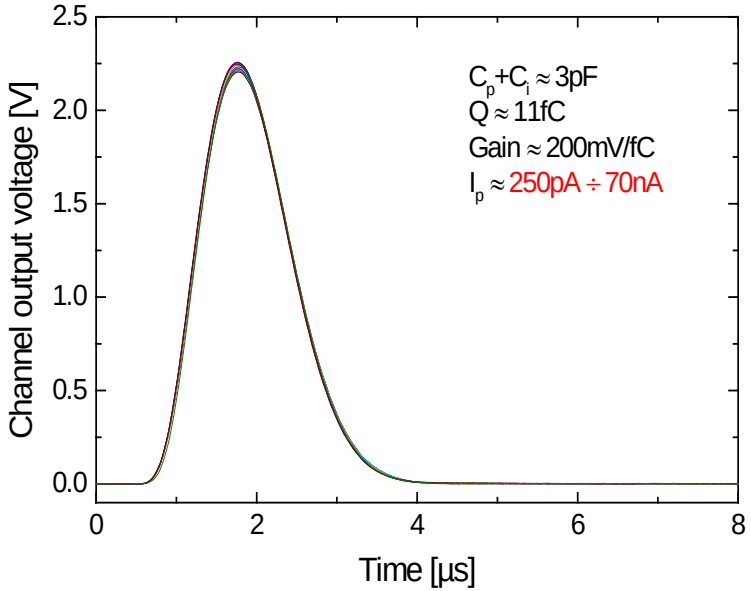
G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

Preamp reset with nonlinear PZ compensation – experimental results

linearity



output vs pixel leakage current

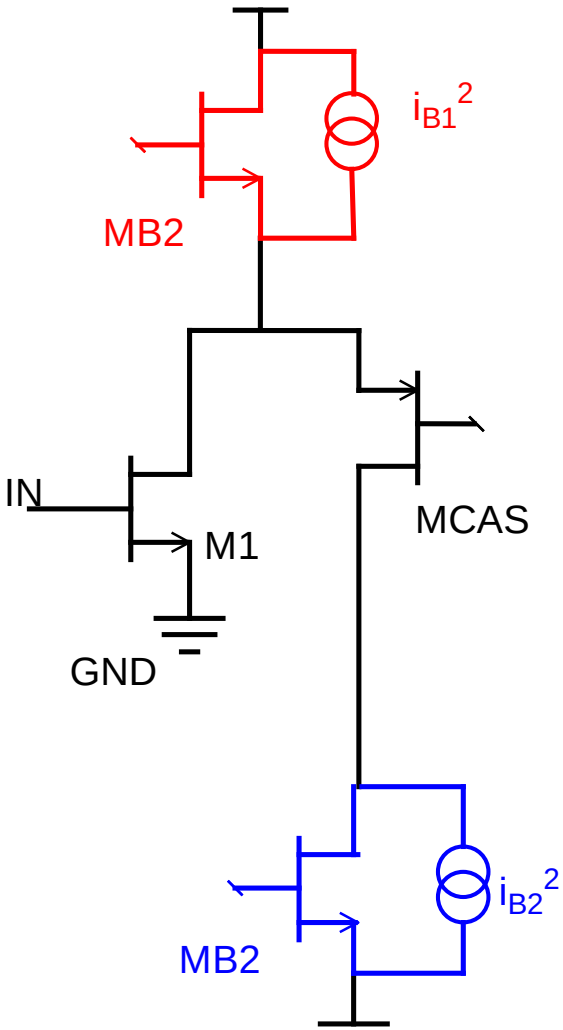


Compensated reset system

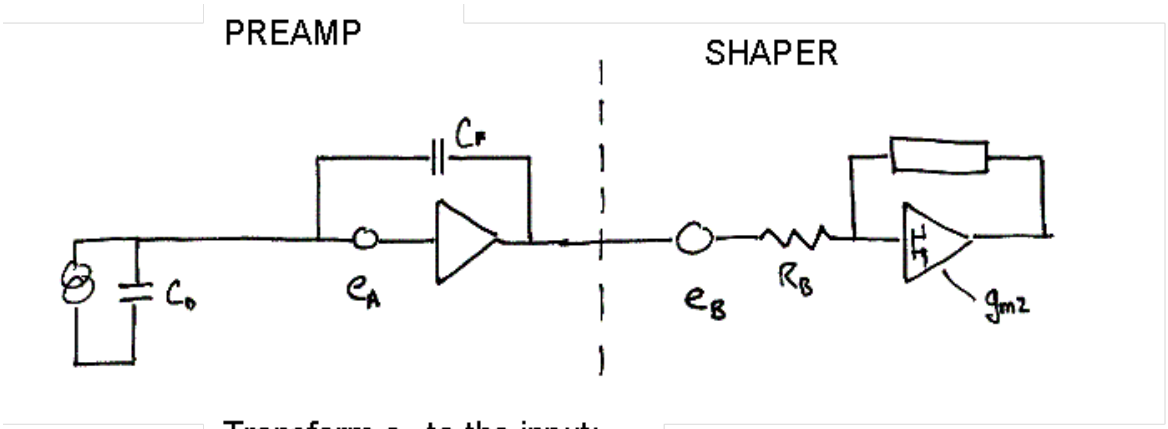
- Advantages:
  - *near theoretical noise contribution*
  - *accepts detector leakage current over wide range*
    - allows DC coupling of detector to preamp
  - *compensate the parasitic preamp feedback pole with a precisely matched zero*
    - allows crude single-element feedback
  - *insensitive to variations in supply voltage, temperature, and process*
  - *internal bias circuit needs no external adjustments*
    - same circuit works for any detector, gain, tp
  - *easy to implement programmable gain*
- Drawbacks:
  - *only works in one polarity*
  - *DC leakage amplified by same factor as signal*
    - requires BLR in 2nd stage
  - *large area consumption*

Secondary noise sources in the preamp

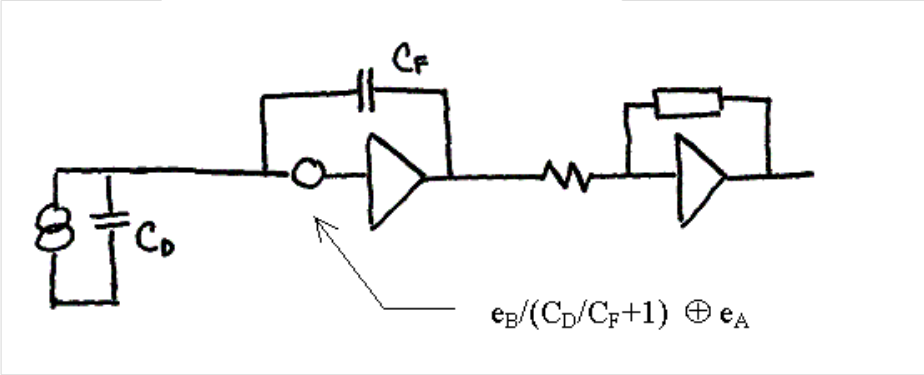
- i_{B1}^2 and i_{B2}^2 are effectively in parallel with the input transistor
- Their contribution to input (white) thermal series noise is $(g_{mB1,2}/g_{m1})^2$.
- We minimize their g_m w.r.t. that of M1
- $g_{mB1,2} = \sqrt{2\mu C_{ox} W I_D / L}$
- use <u>low</u> W/L (i.e. long-gate) devices with large or degenerate with source resistor.
- Keep W/L as small as possible (thus V_{gs}-V_T large) while keeping $V_{DS} > V_{gs}$-V_T.
- Various ways to optimize.



Second-stage noise

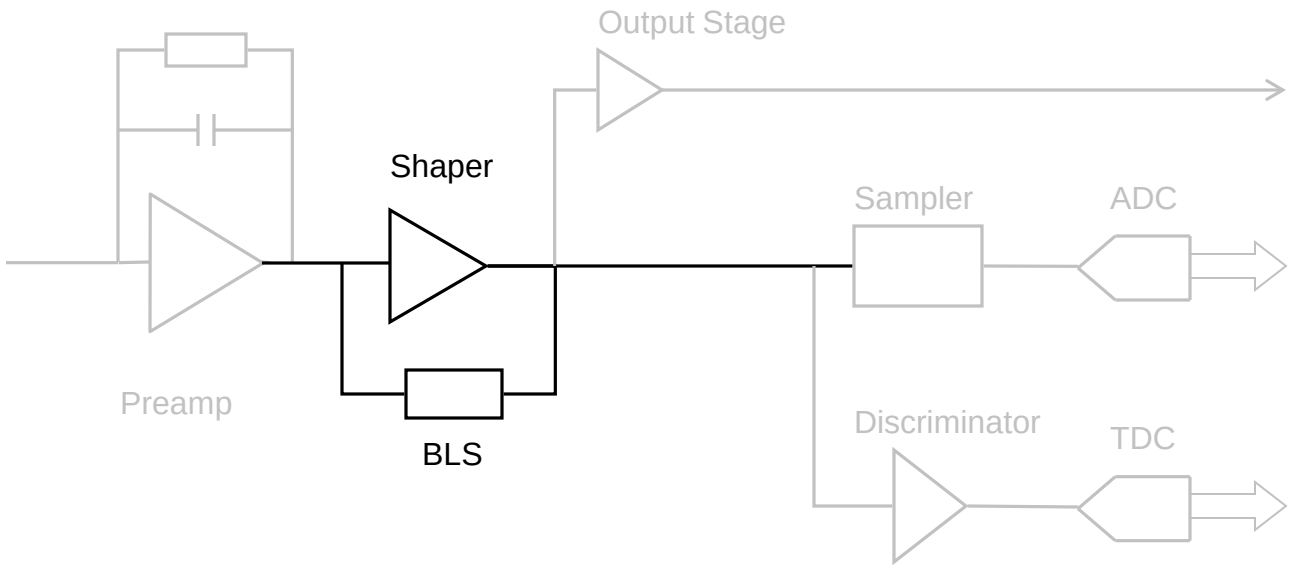


Transform e_B to the input:



$$\frac{ENC_B}{ENC_A} = \frac{C_F}{C_D} \cdot \left(\frac{R_B}{R_A}\right)^{1/2}$$

Shaper and baseline stabilizer

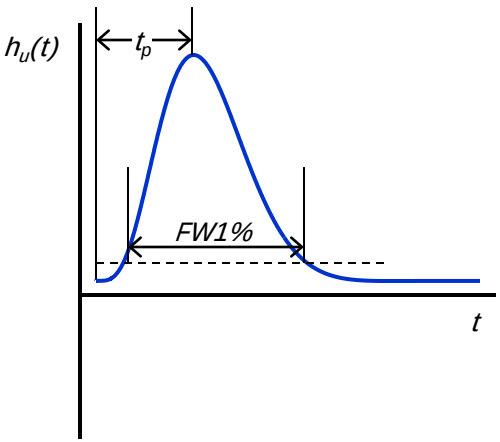


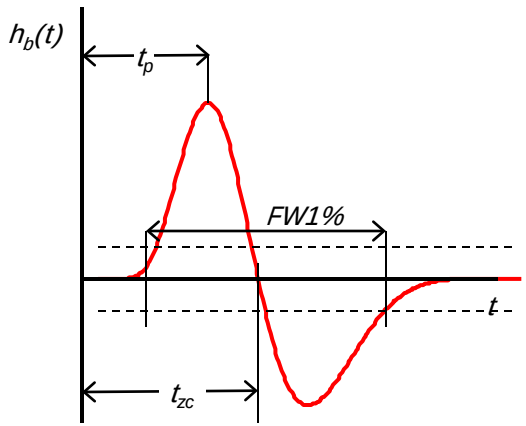
Integrated shaping amplifiers

- Limits the bandwidth for noise
- Gives controlled pulse shape appropriate for rate
- Control baseline fluctuations
- Set slope at threshold crossing for timing
- Bring charge-to-voltage gain to its final value
- By its saturation characteristics, sets upper limit on Q_{in}

- Feedback circuits give the most stable and precise shaping
  - *At the expense of power dissipation*
  - *Poor tolerance of passives limits accuracy of the poles and zeros*
- High-order shapers give the lowest noise for a given pulse width

Shaper Characteristics





first and second moments

$$\int_{-\infty}^{\infty} |h(t)|^2 \, dt$$

$$\int_{-\infty}^{\infty} |h'(t)|^2 \, dt$$

slope at threshold crossing

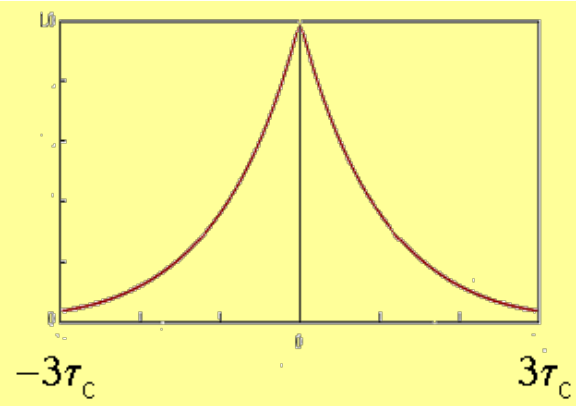
$$h'(t_{TC})$$

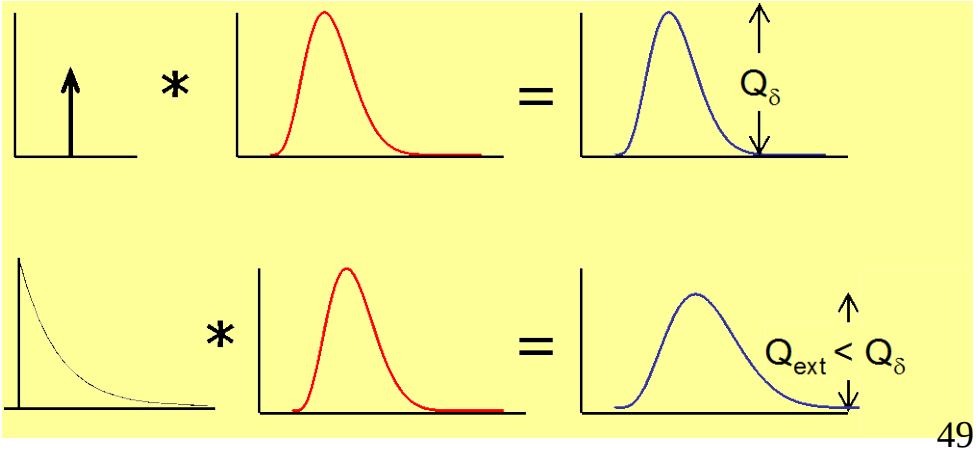
$$\text{where } h(t_{TC}) = V_{th}$$

Pulse shaper – matched filter with compromises

- calculation of matched filter
  - *incomplete knowledge of noise spectrum*
  - *incomplete knowledge of input waveform*
- exact transfer function difficult to realize in practice
- optimum filter requires a long time to respond
  - *pileup ⇔ limited rate capability*
- "ballistic deficit"
  - *input charge is not a δ-function*
  - *width of impulse response must be >> duration of input charge waveform*

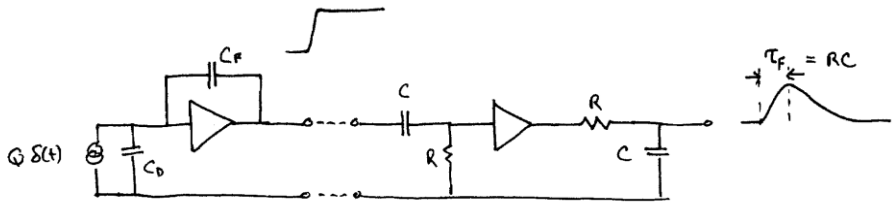
constraints:
- noise corner
- rate^{-1}
- charge collection
- preamp decay





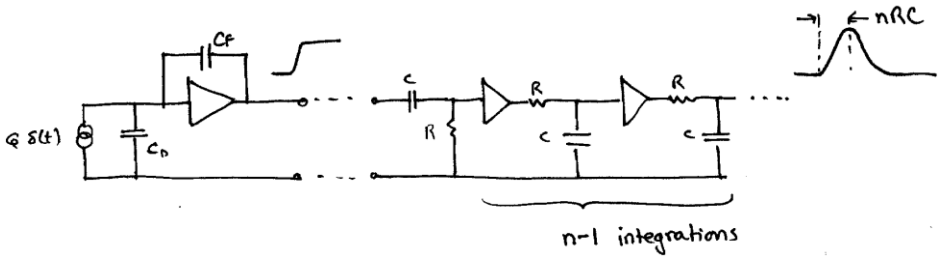
Pulse shaping filters with real poles

Simplest filter: CR-RC

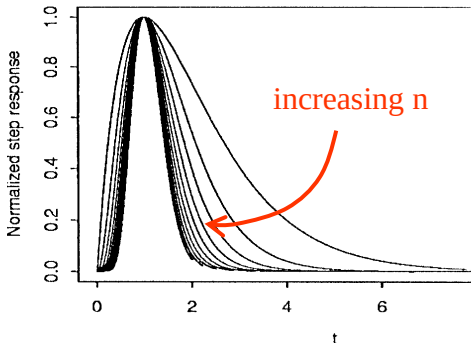


- asymmetric response

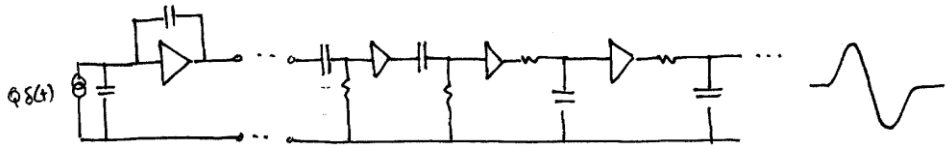
CR-RC^n, unipolar semiGaussian



- Identical real poles
- Symmetry improves with order n:



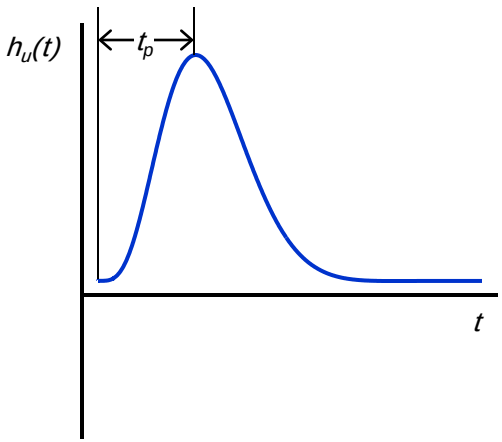
CR^2-RC^n, bipolar semiGaussian



- Area-balanced
- Derivative of CR-RC^n

Properties of real-pole semiGaussian shapers

unipolar CR-RC^n

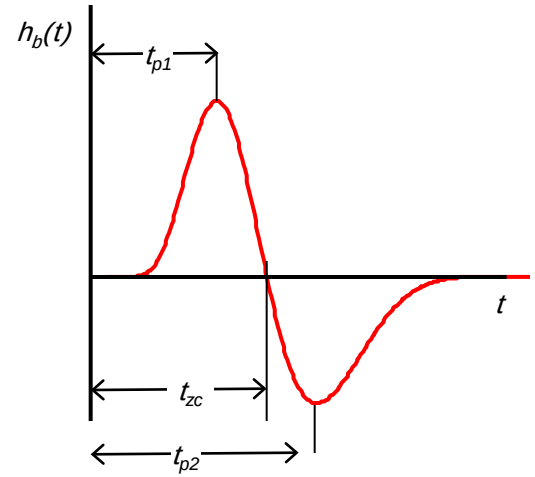


$$H_u(s) = \frac{s\tau}{(1+s\tau)^{n+1}}$$

$$h_u(t) = \frac{1}{n!}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-t/\tau}$$

$$t_p = n\tau$$

bipolar CR^2-RC^n



$$H(s) = \frac{(s\tau)^2}{(1+s\tau)^{n+2}} \qquad \omega_{\max} = \frac{2}{n\tau}$$

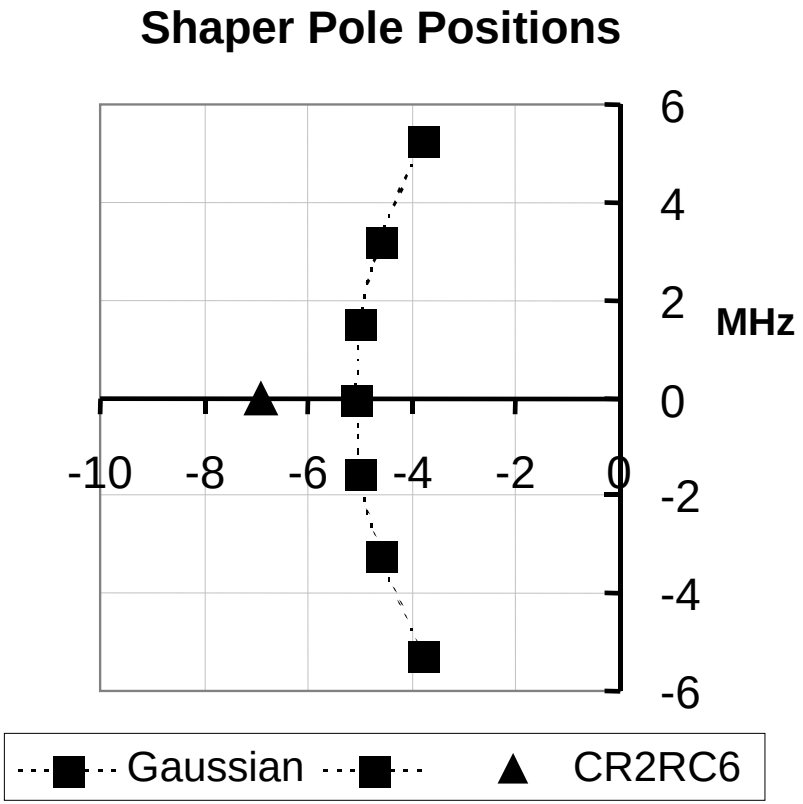
$$h(t) = \frac{1}{(n+1)!\tau}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-t/\tau}\left[t-(n+1)\tau\right]$$

$$t_{p1} = (n+1-\sqrt{n+1})\tau$$

$$t_{zc} = (n+1)\tau$$

$$t_{p2} = (n+1+\sqrt{n+1})\tau$$

Complex pole approximation to Gaussian pulse



Ohkawa synthesis method (Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers")

For given filter order, gives closest approx. to a true Gaussian

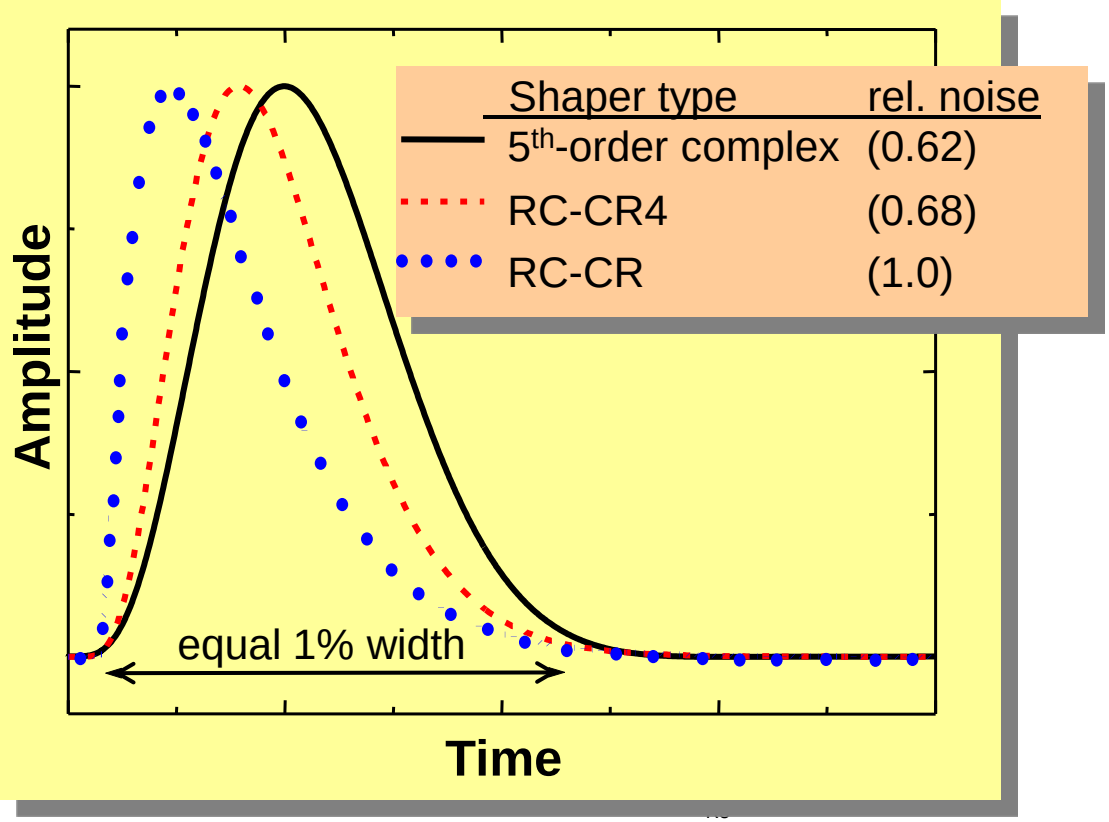
More symmetrical than CR-RC^n filter of same order for same peaking time

Noise weighting functions:

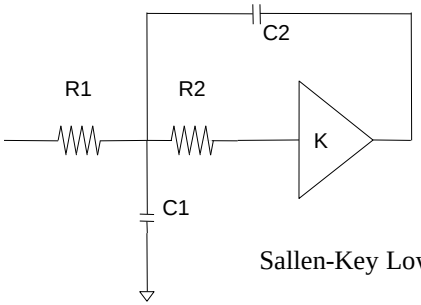
$I_{1,complex}/I_{1,CR\text{-}RC} = 1.18$ **series**

$I_{2,complex}/I_{2,CR\text{-}RC} = 0.81$ **parallel**

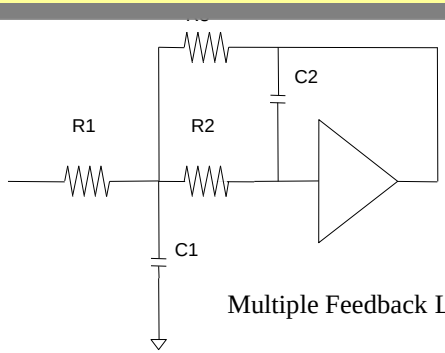
Shaper optimization



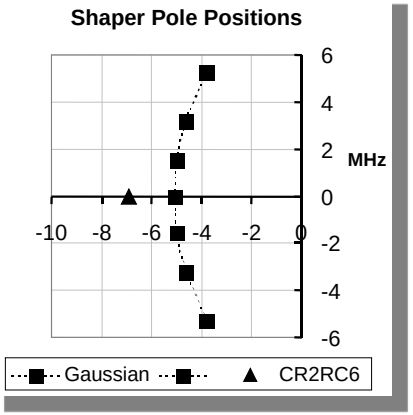
- For a given rate-handling capability, high-order shapers have lower noise.
- Adding an extra shaper stage can reduce noise more than putting the equivalent amount of power into the preamp.
- For a given shaper order, complex pole constellation using second- or third-order active filter topologies minimizes noise.



Sallen-Key Lowpass



Multiple Feedback Lowpass

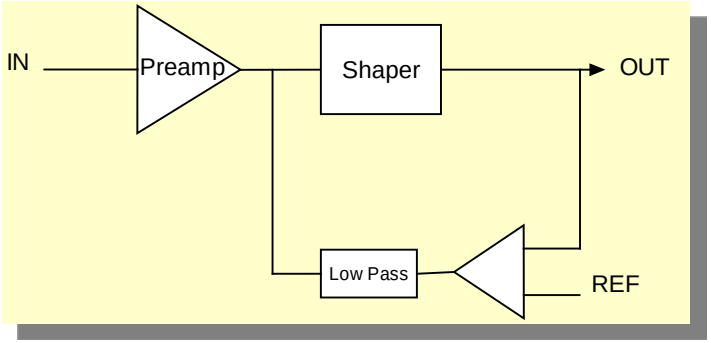


Baseline stabilization

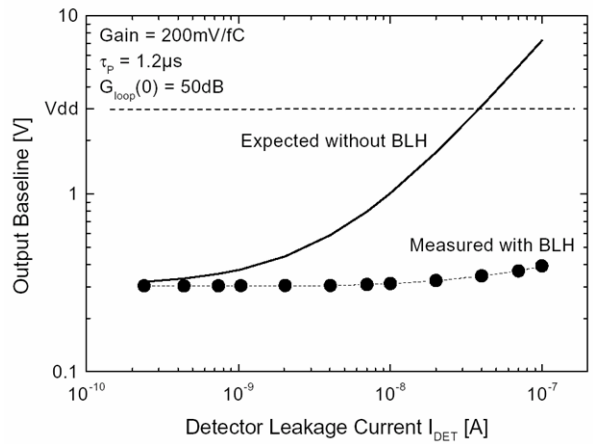
Baseline can move due to:

1. DC coupling to detector with variable leakage
2. Temperature and power supply drift
3. Rate fluctuations in a system with AC coupling

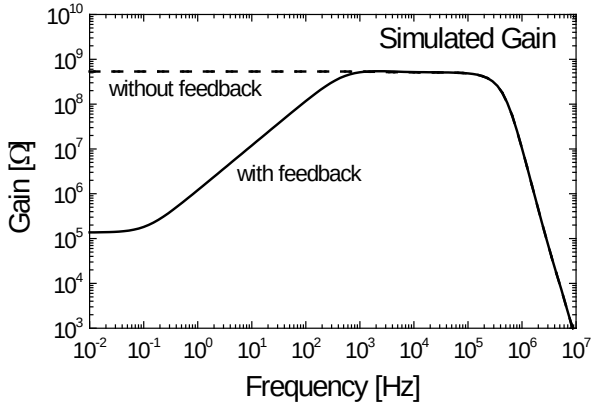
(1) and (2) can be prevented by low frequency feedback circuit:



Result:



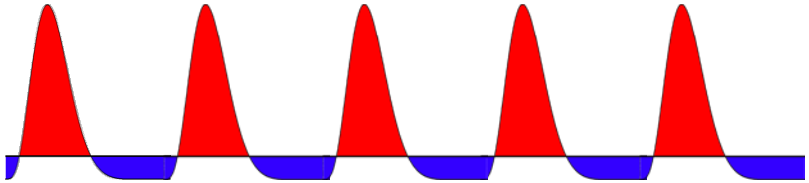
But this introduces unintended AC coupling:



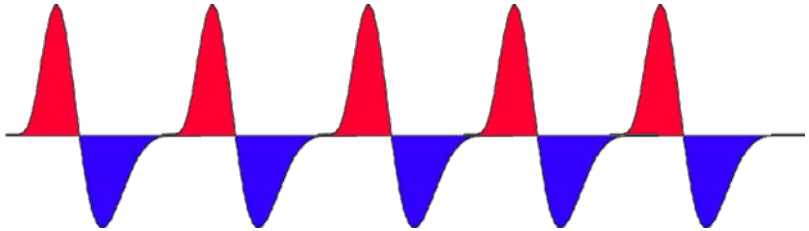
Compensate with nonlinear element or gating of the feedback circuit

Area balance after AC coupling

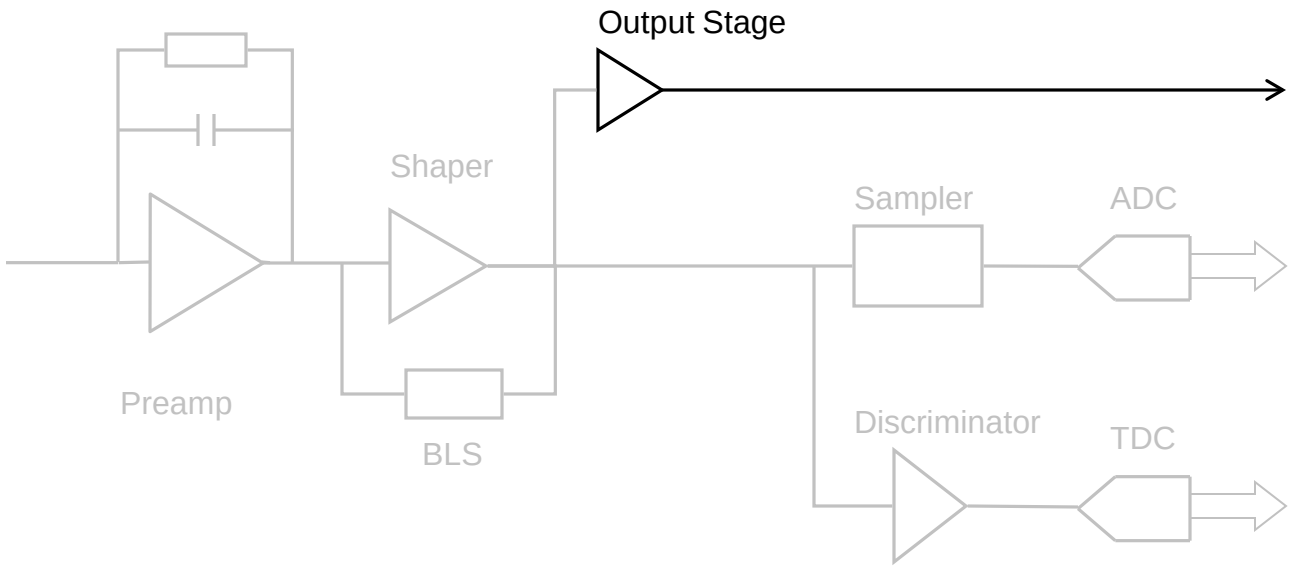
- Unipolar pulse:
- baseline displaced below 0
- instantaneous rate fluctuations cause baseline to wander



- Bipolar pulse:
- each pulse is area balanced, no detrimental effect of AC coupling
- penalty is higher noise, longer occupancy per pulse

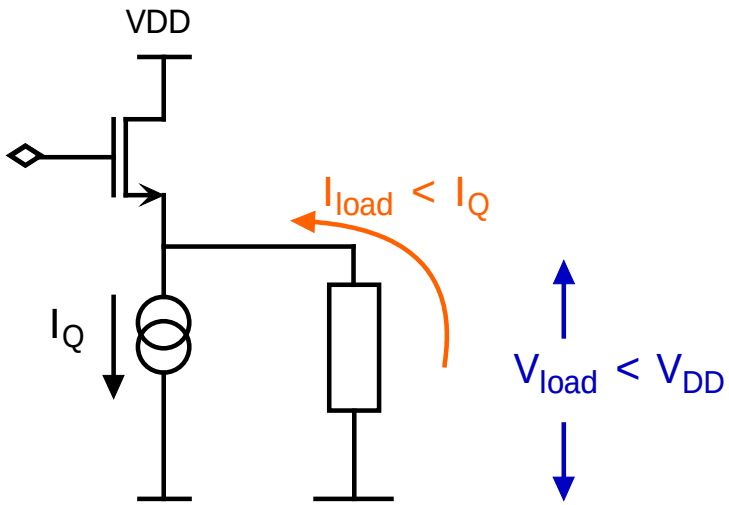


Output stage

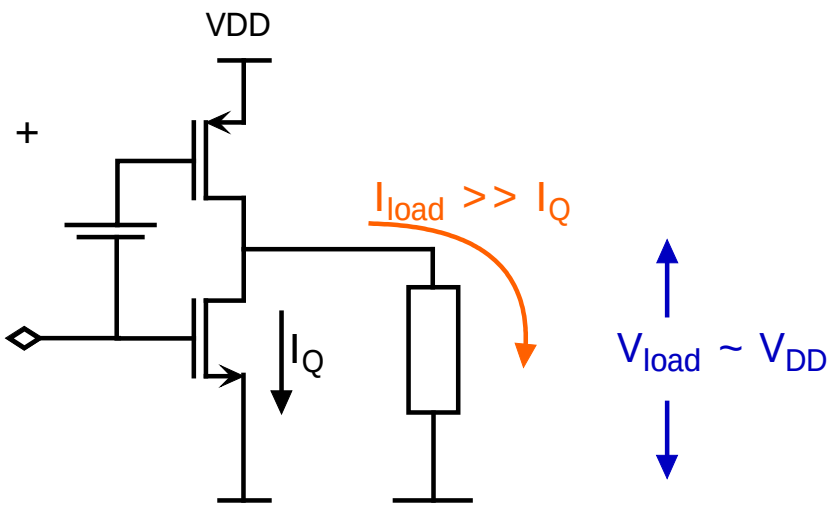


Output driver

source follower



class AB common source

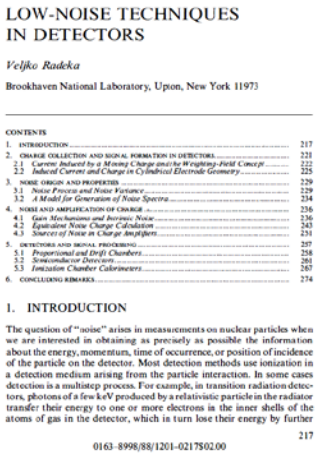


- class A: high standing current
- can't swing rail-to-rail

- class AB stage can source or sink currents >> quiescent current
- common-source stage can drive rail-to-rail

Hogervorst ref.

Further Reading



LOW-NOISE TECHNIQUES
IN DETECTORS

Veljko Radeka

Brookhaven National Laboratory, Upton, New York 11973

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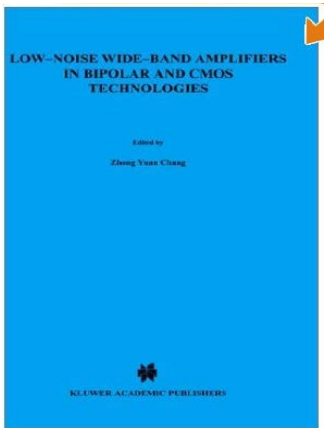
1. INTRODUCTION

The question of "noise" arises in measurements on nuclear particles when we are interested in obtaining as precisely as possible the information about the energy, momentum, time of occurrence, or position of incidence of the particle on the detector. Most detection methods use ionization in a detection medium arising from the particle interaction. In some cases detection is a multistep process. For example, in transition radiation detectors, photons of a few keV produced by a relativistic particle in the radiator transfer their energy to one or more electrons in the inner shells of the atoms of gas in the detector, which is turn lose their energy by further

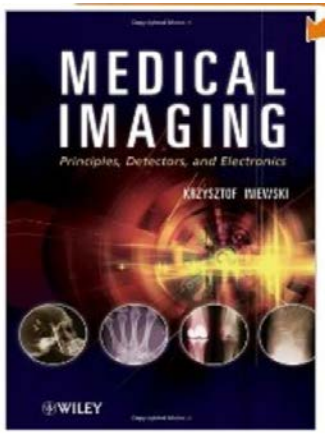
217

0163-8998/88/1201-0217$02.00

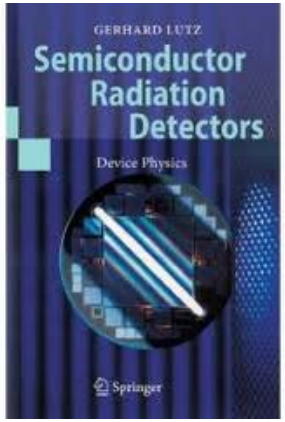
V. Radeka, "Low-noise Techniques in Detectors", *Ann. Rev. Nucl. Part. Sci.* 38, 217-77 (1988)



Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies, ed. Z. Chang, Springer1990

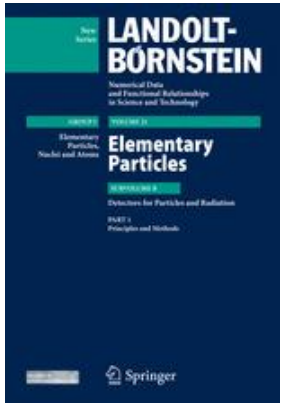


G. De Geronimo, "Low-noise Electronics for Radiation Sensors", Ch. 6 in *Medical Imaging: Principles, Detectors, and Electronics*, ed. K. Iniewski, Wiley 2009



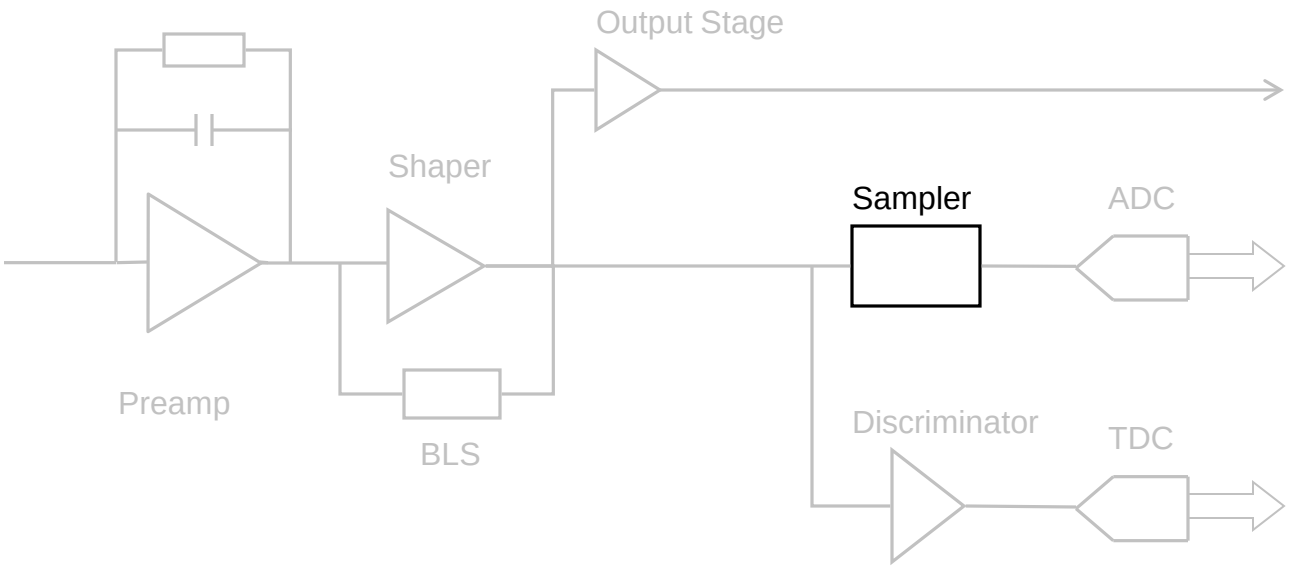
G. Lutz, *Semiconductor Radiation Detectors*, Ch. 7, Springer, 2007

P. Grybos, *Front-end Electronics for Multichannel Semiconductor Detector Systems*, Eucard editorial series on Accel. Science and Technology, 2010



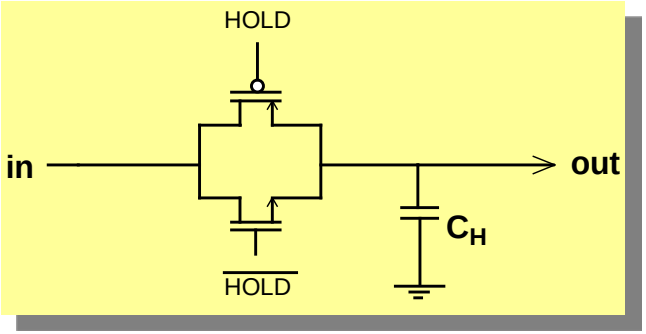
V. Radeka, "Signal Processing for Particle Detectors", Ch. 6 in *Detectors for Particles and Radiation. Part 1: Principles and Methods*, Springer, 2011

Analog sampling



Candidate sampling/memory cells in CMOS

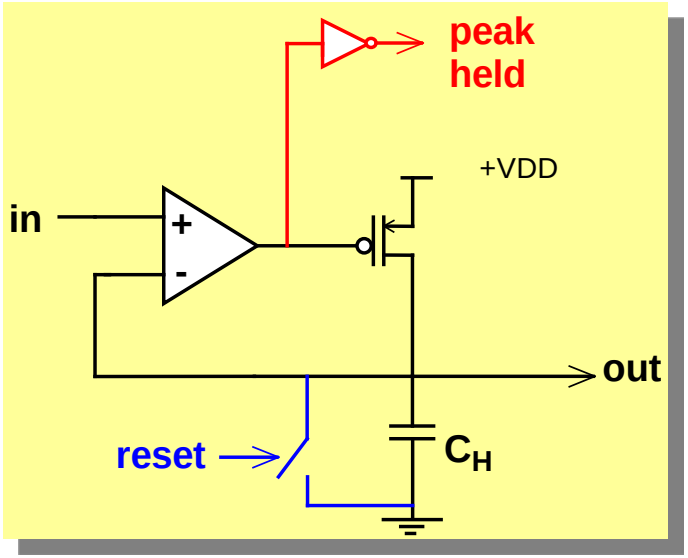
Sample/hold using switched capacitor



- small
- low-power

- timing of hold signal: needs CFD for walk-free operation
- switch charge injection
- poor drive capability: needs output amp

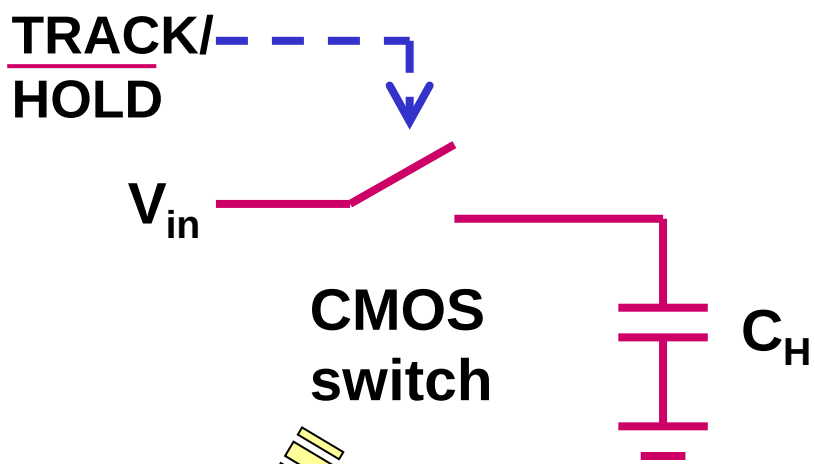
Peak Detector (PD)

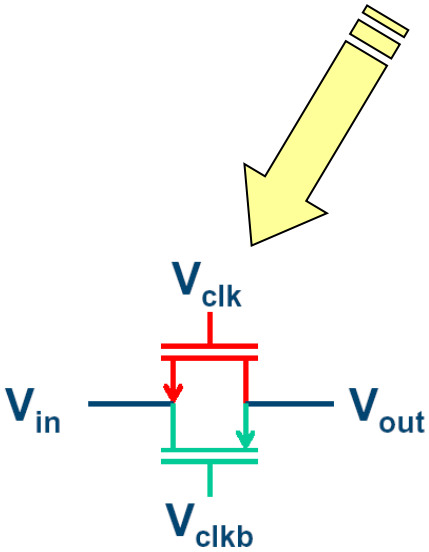


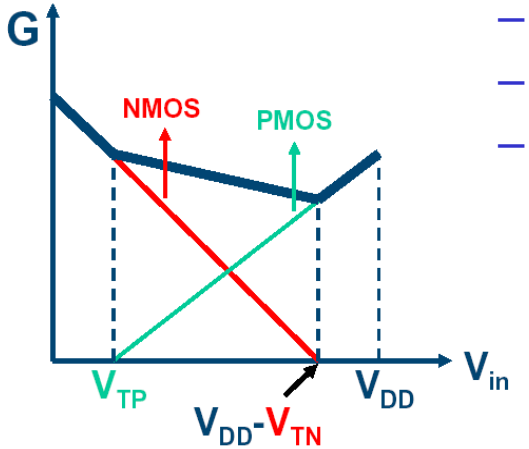
- self-triggered
- timing output
- feedback loop

- deadtime until readout reset
- poor drive capability
- accuracy impaired by opamp offsets, CMRR, slew rate

Switched-capacitor track-and-hold







CMOS switch:

- *low I_{off}*
- *high G_{on}, $0 < V_{sig} < V_{DD}$*

MOS/MIM capacitor:

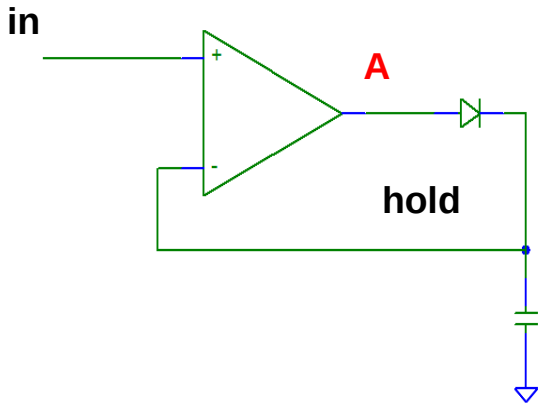
- *well-matched*
- *low leakage*
- *linear*

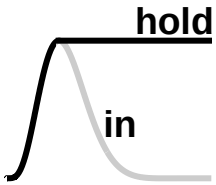
Design tradeoffs:

- *speed – droop rate*
- *speed – charge injection*
- *speed – clock feedthrough*
- *low voltage limits*

CMOS Peak Detector

Classical peak detector





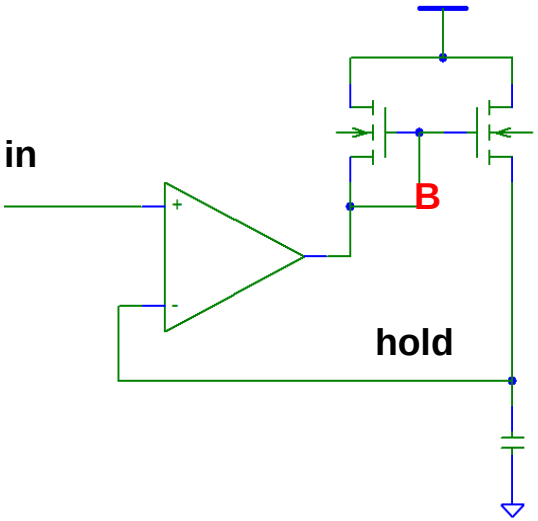
Diode replaced by current mirror acting as rectifying and loop-stabilizing element.

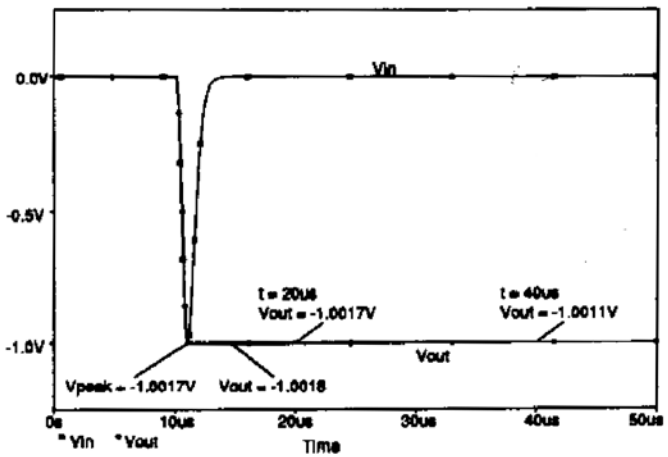
Reduced charge injection from sharp transient at node A(B).

$\Delta V_A = V_P$; $\Delta V_B = V_{th} << V_P$

Accuracy, speed, and dynamic range limited.

Improved CMOS version



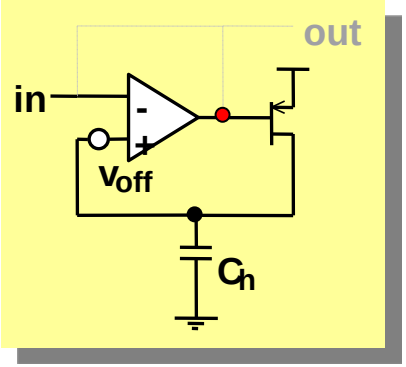


M. W. Kruiskamp, D. M. W. Leenaerts, IEEE Trans. Nuclear Sci., 41(1) 295 (1994)

The two-phase peak detector concept

Write phase

• behaves like classical configuration



Read phase

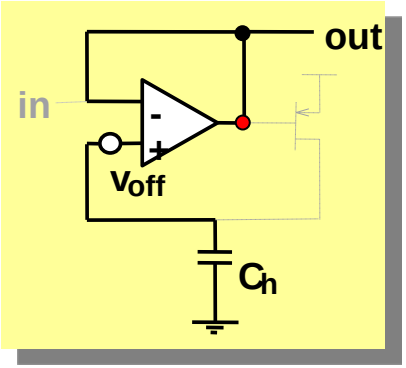
• op-amp re-used as buffer

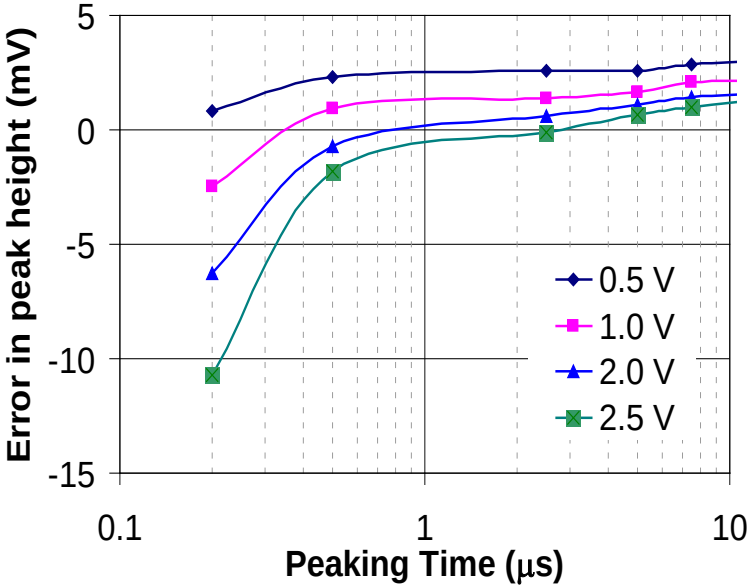
• **offset** and **CMMR errors canceled**

• enables **rail-to-rail** sensing

• good **drive capability**

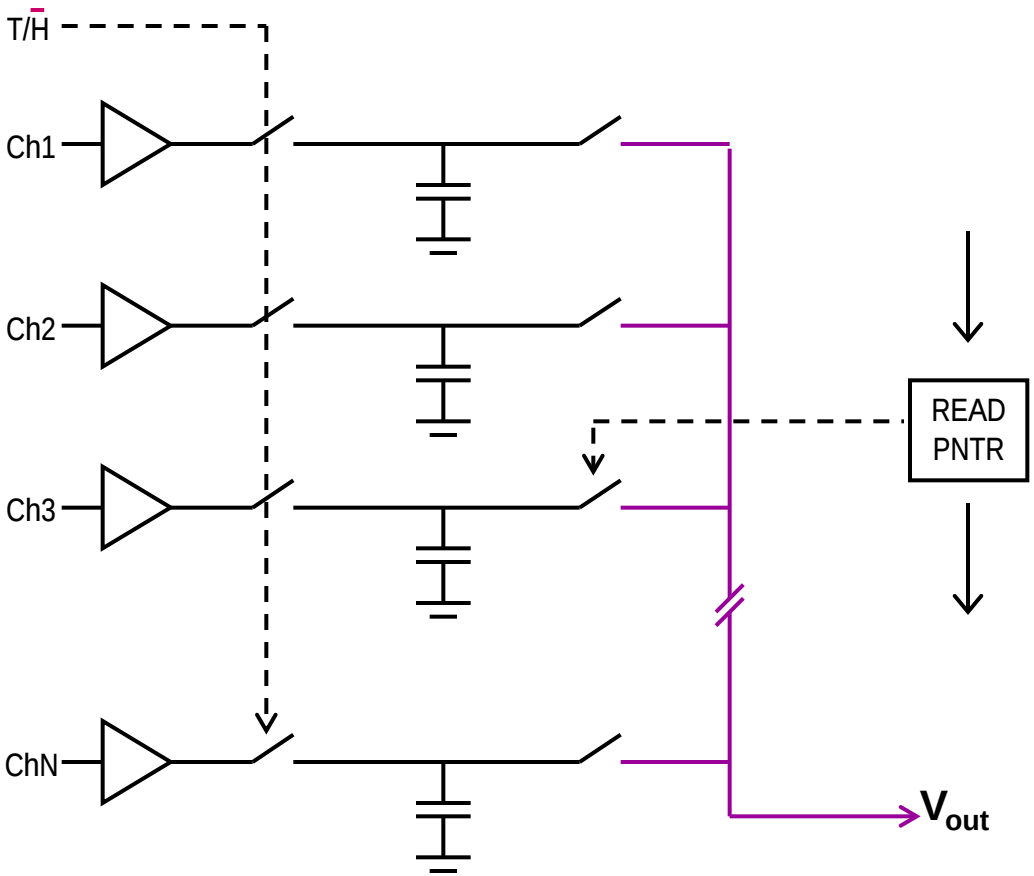
• **self-switching** (peak found)





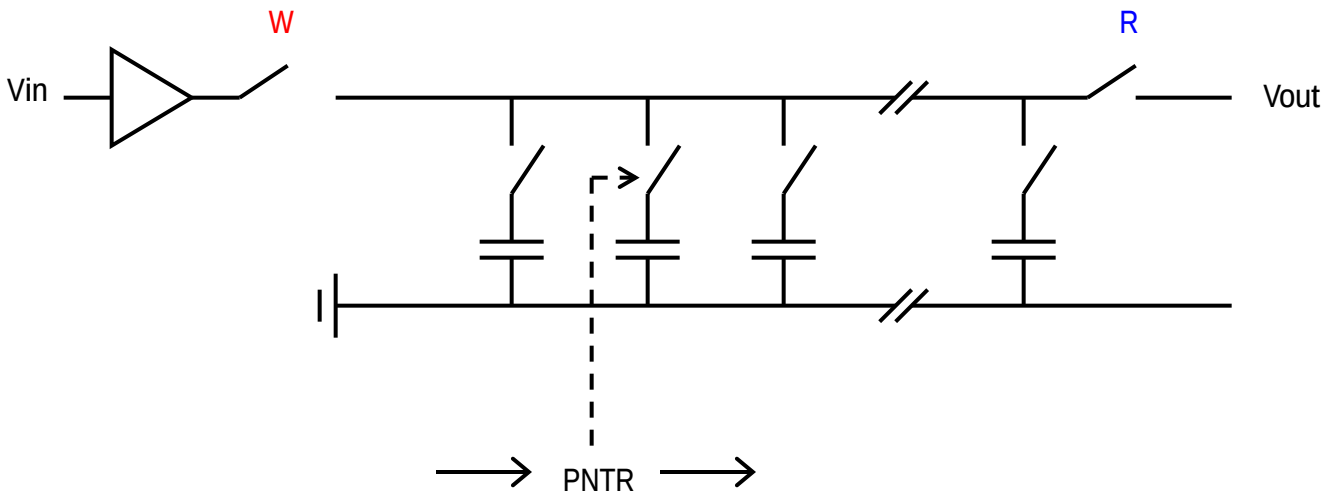
P. O'Connor, G. De Geronimo, A. Kandasamy,, IEEE Trans. Nucl. Sci. 50(4), 892 (2003)
G. De Geronimo, P. O'Connor, A. Kandasamy, Nucl. Instr. Meth. A484, 533 (2002)

Track/hold array + N-to-1 multiplexer

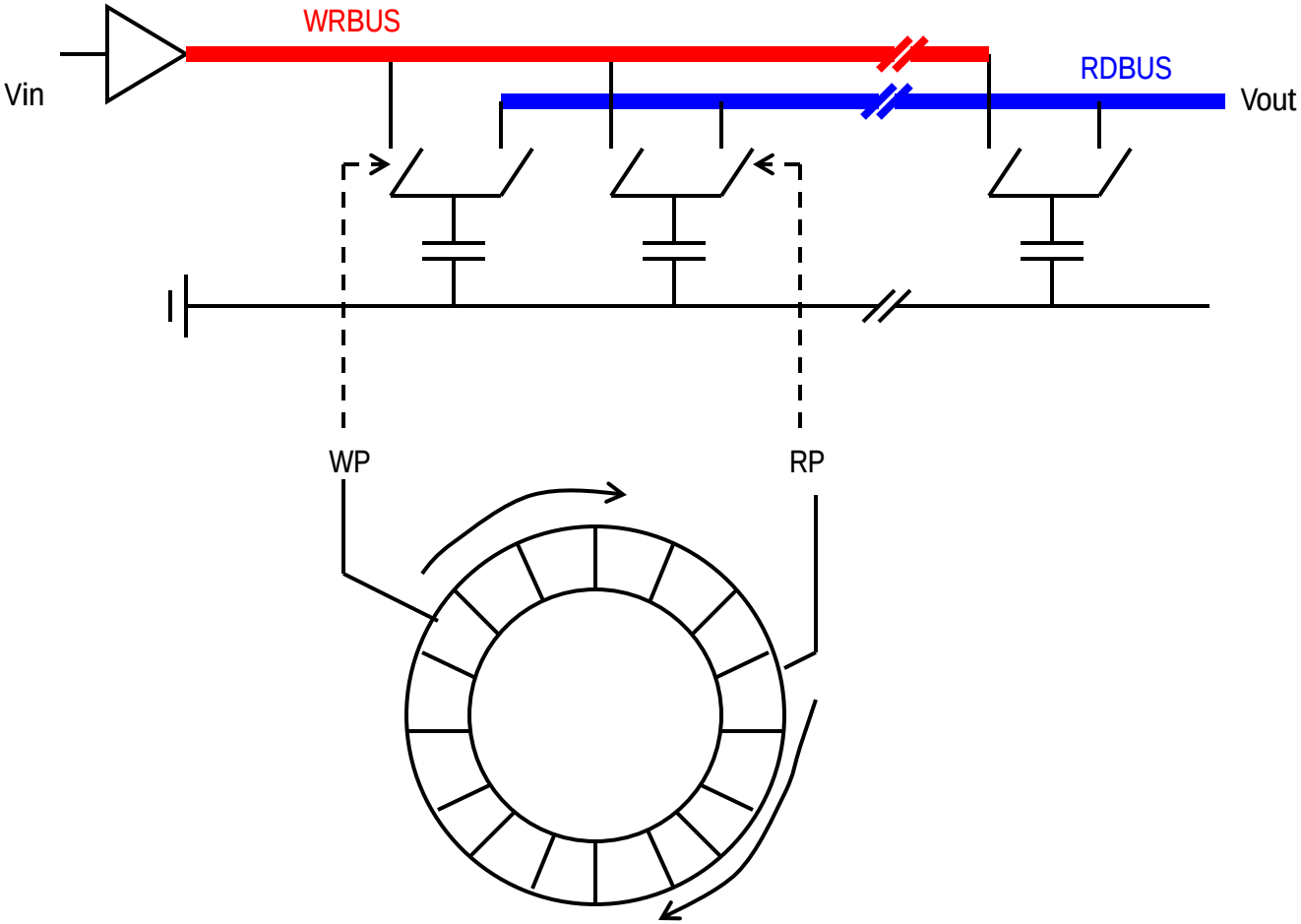


- tradeoff of multiplexing ratio, deadtime
- good channel-channel matching
- requires external signal to control track/hold

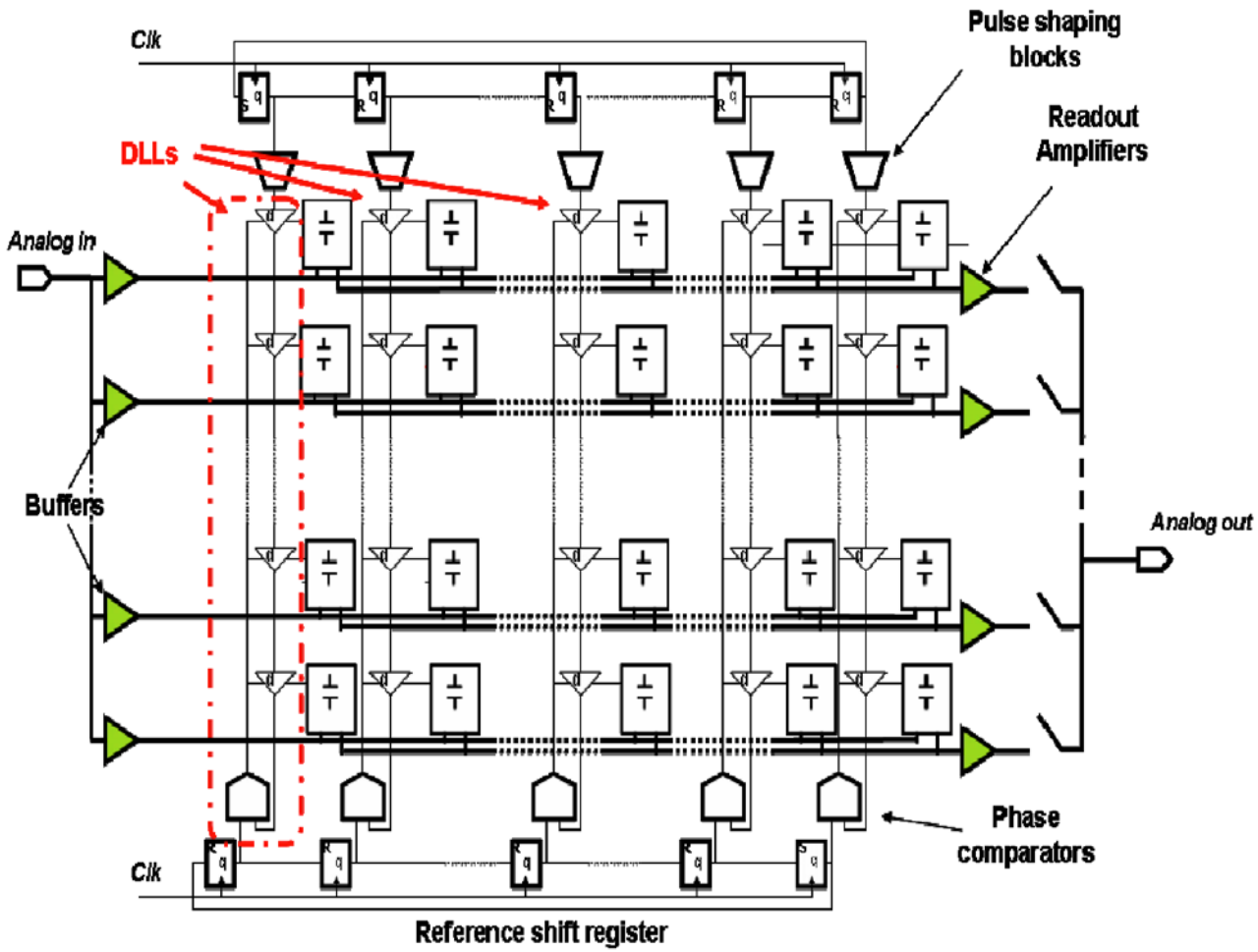
Switched-capacitor array waveform recorder



Deadtimeless SCA with simultaneous R/W



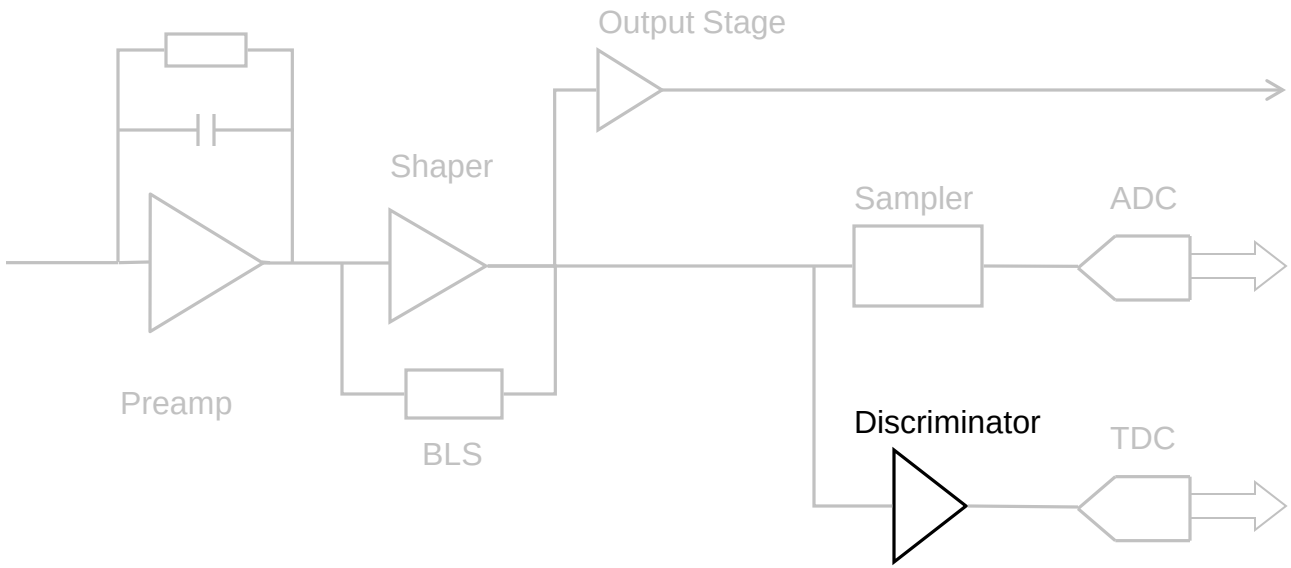
Fast matrix-organized SC memory



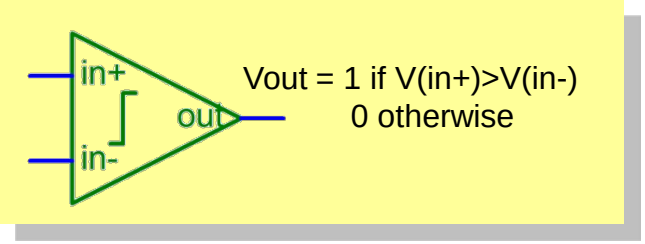
- *Delay-locked loop fine time sampling*
- *250MHz analog bandwidth*
- *sampling frequency 1 – 2.5 GHz*
- *400μV fixed-pattern noise*
- *readout rate 90ns/cell*

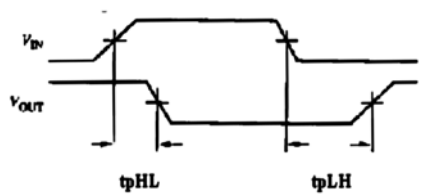
E. Delagnes et al., "A Multigigahertz Analog Memory with Fast Read-out for the H.E.S.S.-II Front-End Electronics", IEEE Nucl. Sci. Symposium Conf. Record, 2006

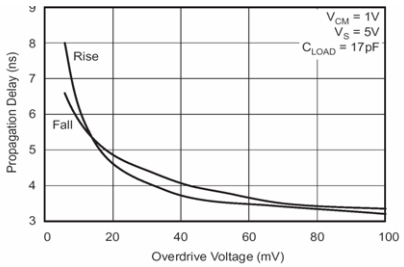
Discriminator



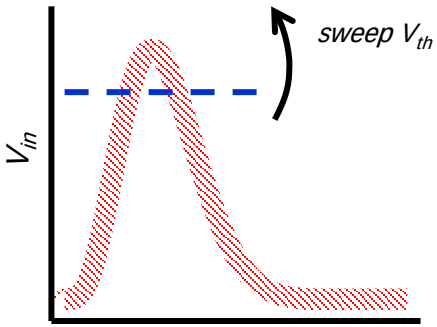
Discriminator properties and applications

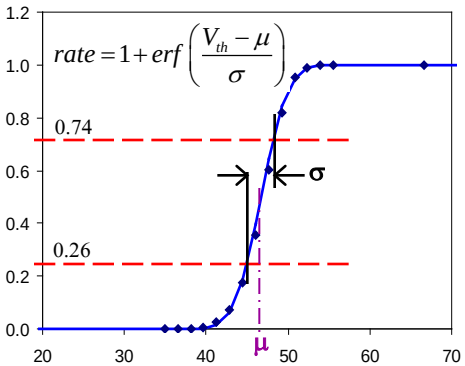






- Characteristics
  - *propagation delay*
    - vs. overdrive
    - vs. risetime (of input wfm)
    - vs. load capacitance
  - *hysteresis*
  - *recovery from saturation*

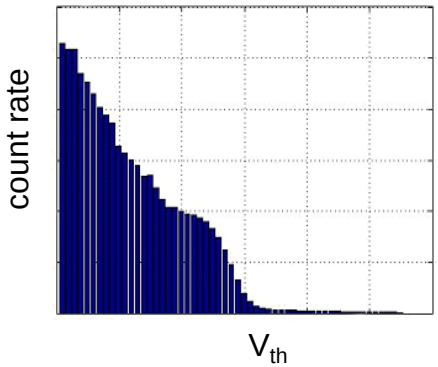


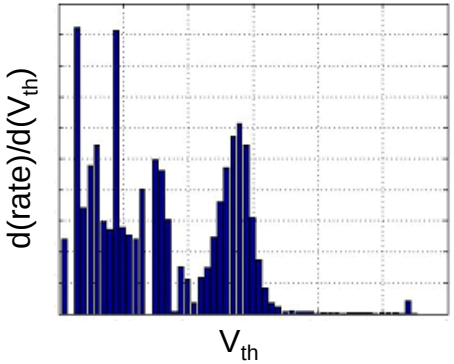


- Used for
  - *hit detection (YES/NO)*
  - *trigger*
  - *amplitude windowing*
  - *amplitude spectra (by threshold sweep)*
  - *time interval marker*

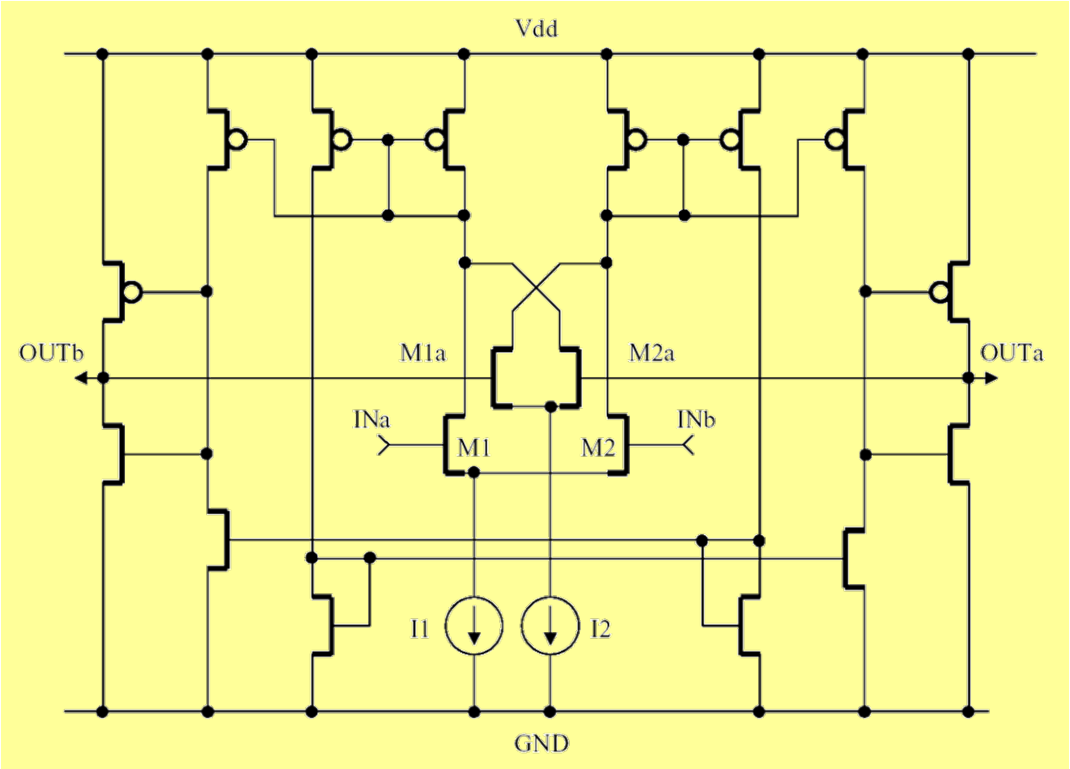
Noise hit rate in threshold detection:
System bandwidth B, rms noise σ ➔

$$f_{noise} \approx 0.6B\exp\left(-\frac{V_{th}^2}{2\sigma^2}\right)$$



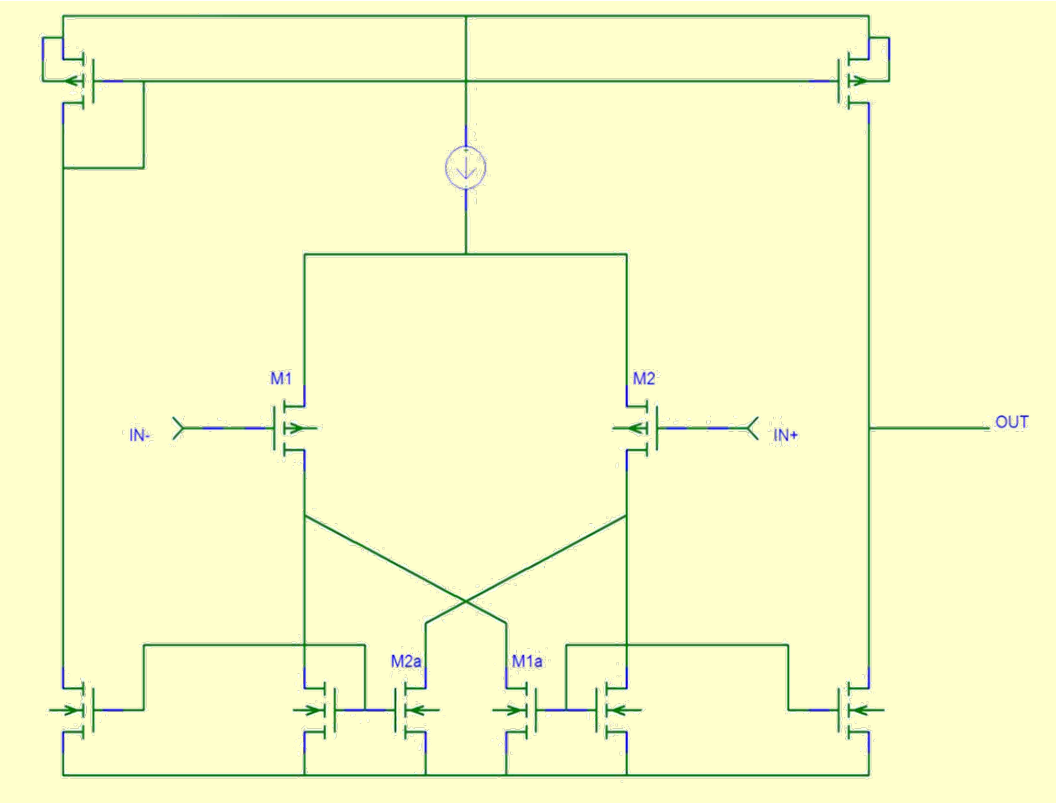


CMOS discriminator topologies (1)



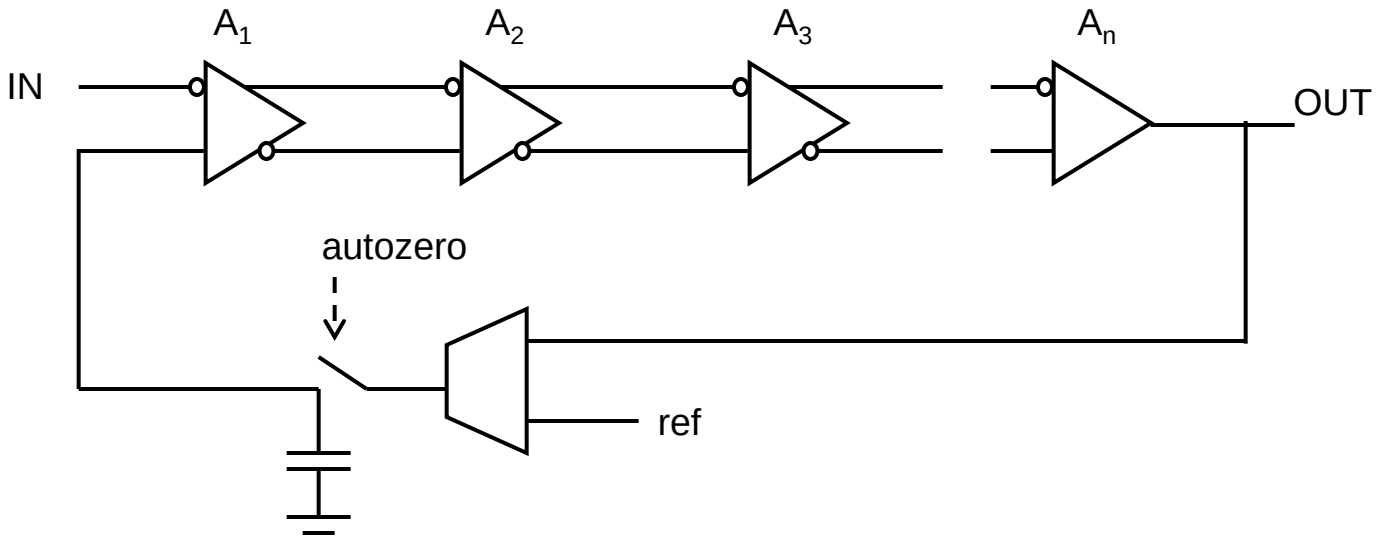
- Main differential pair M1-M2 plus dual current mirrors provide gain ~ 500
- Cross-coupled pair M1a, M2a provide positive feedback.
- Hysteresis level adjustable by I2/I1 ratio.
- Balanced, fully differential circuit less prone to feedback oscillation.

CMOS discriminator topologies (2)

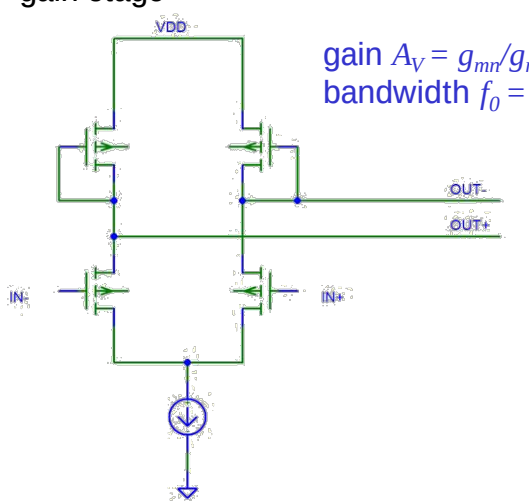


- Cross-coupled pair M1a, M2a provide positive feedback
- Hysteresis level adjustable by M1/M1a width ratio

Cascade topology



gain stage



gain $A_V = g_{mn}/g_{mp}$
bandwidth $f_0 = g_{mp}/2\pi C_{out}$

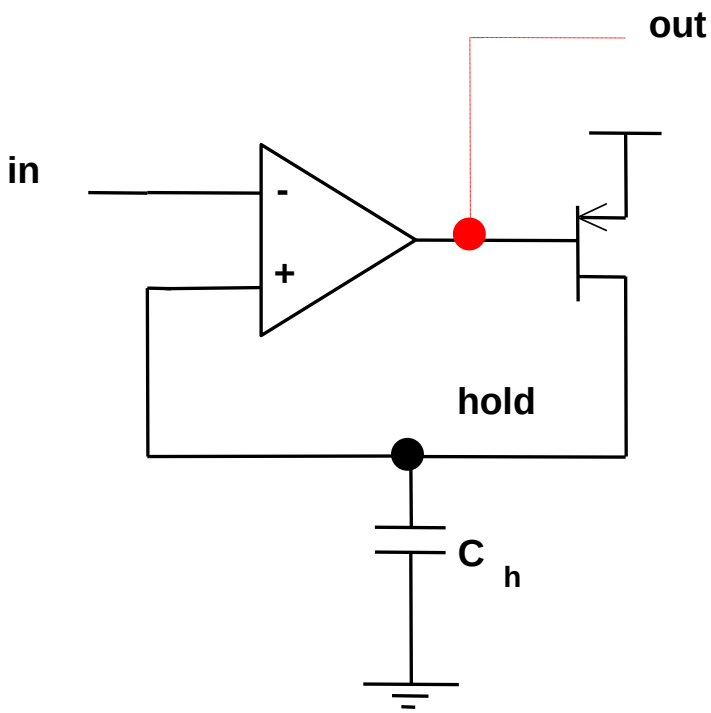
Overall gain A_V^n

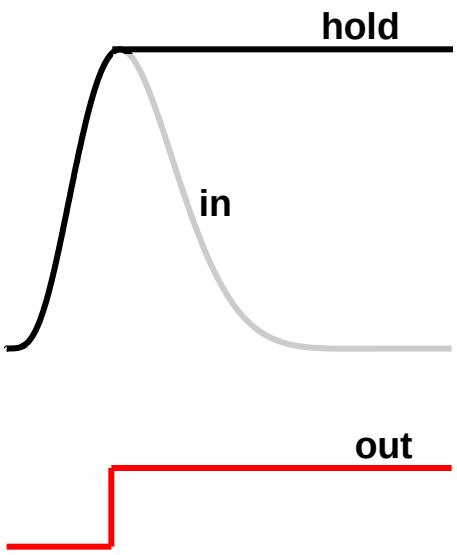
Overall BW $f_0\sqrt{2^{1/n}-1}$

- Cascade gain increases faster than bandwidth decreases as add more stages.
- Nonlinearities limit n to ~ 5 - 6 in practice.

M.L. Simpson et al., IEEE J. Solid-State Circuits 32(2), 1997 (198)
N. Paschalidis et al., IEEE Trans. Nuc. Sci. 49(3), 2002 (1156)

Peak detector as timing comparator

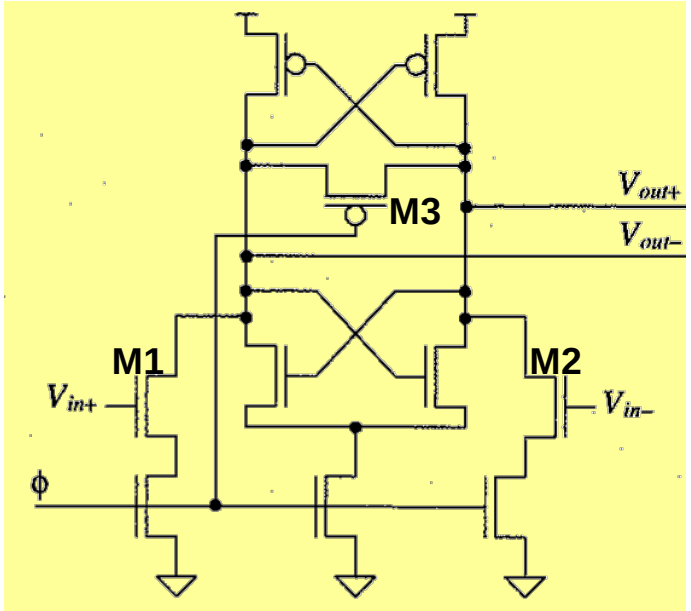




C_h may be precharged to threshold

V_{out} is free of time-walk

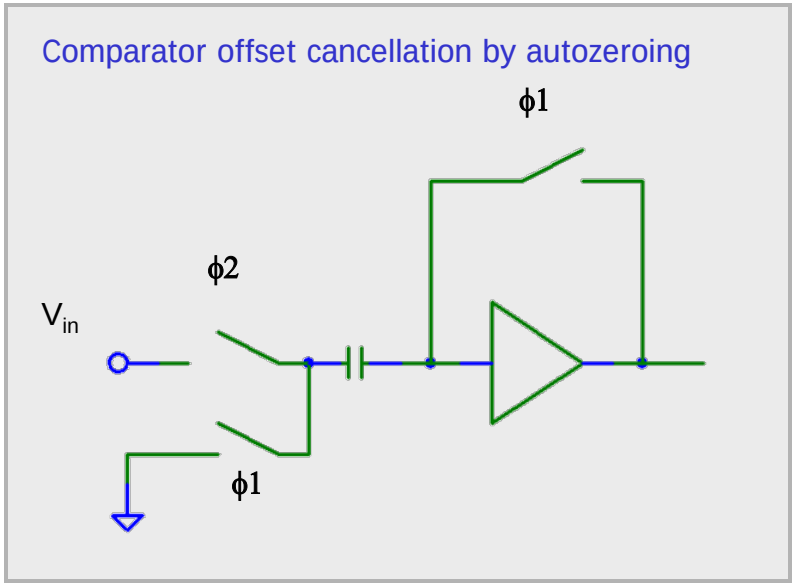
Clocked comparator



ϕ=0:
M3 holds latches in balanced condition

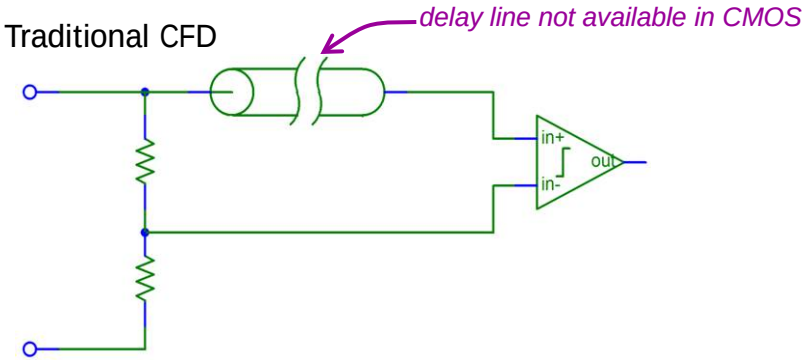
ϕ=1:
M3 OFF, M1/M2 unbalance latches, positive feedback gives rapid response

- This topology frequently used in ADCs.

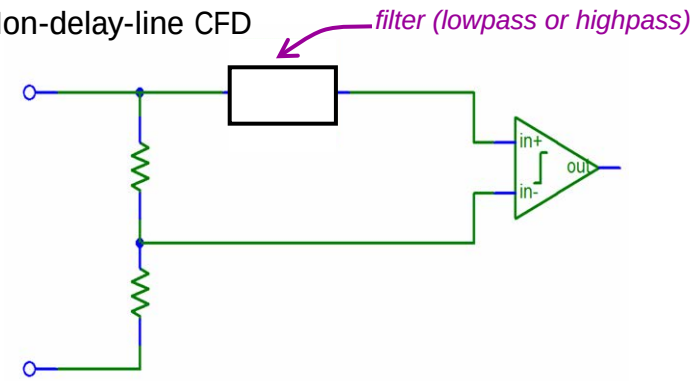


Non-delay-line constant fraction discriminators

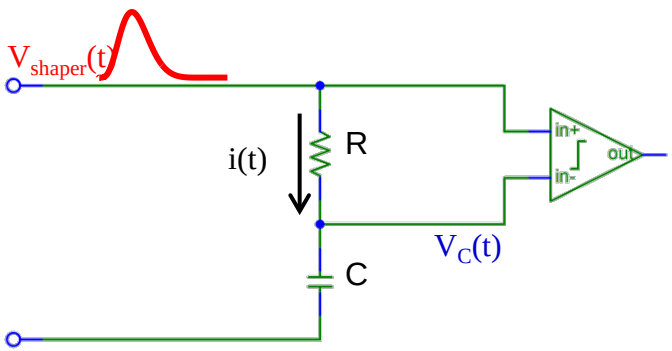
Traditional CFD

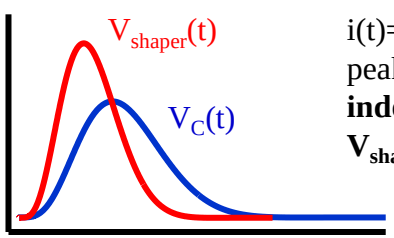


Non-delay-line CFD



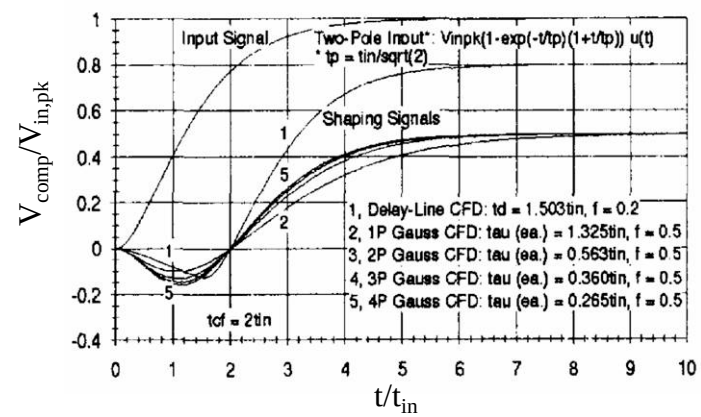
Simple monolithic implementation





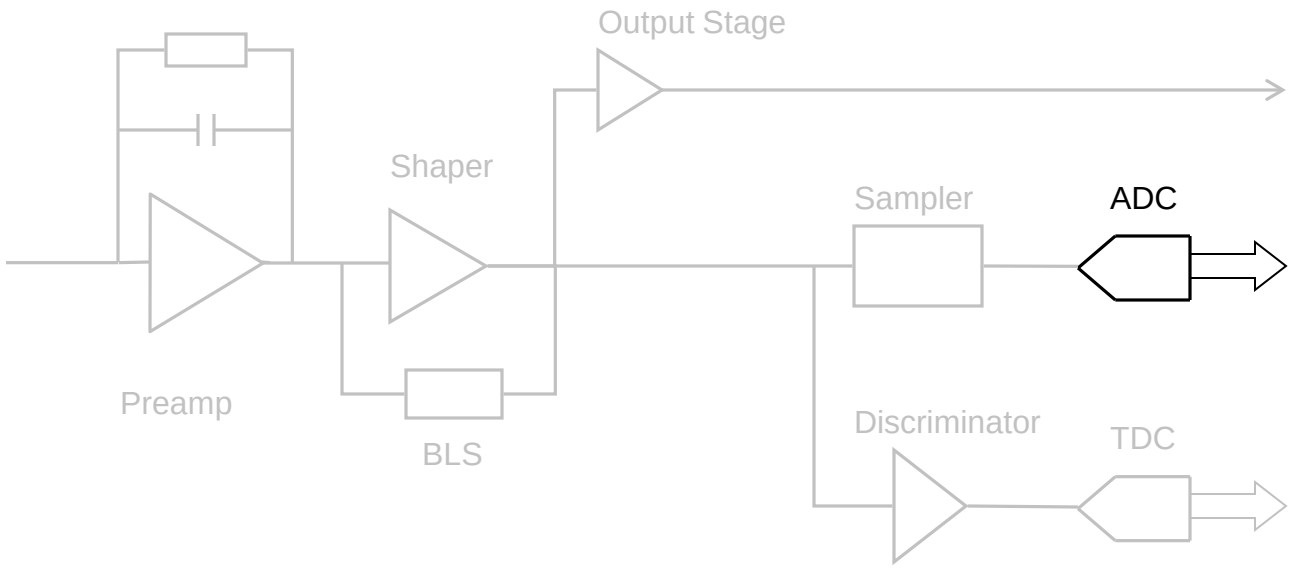
i(t)=0 when $dV_C(t)/dt=0$, i.e. at peak of lowpass waveform **independent of amplitude of $V_{shaper}(t)$**

Higher-order filter improves slope at zero-cross and leading-edge sensitivity

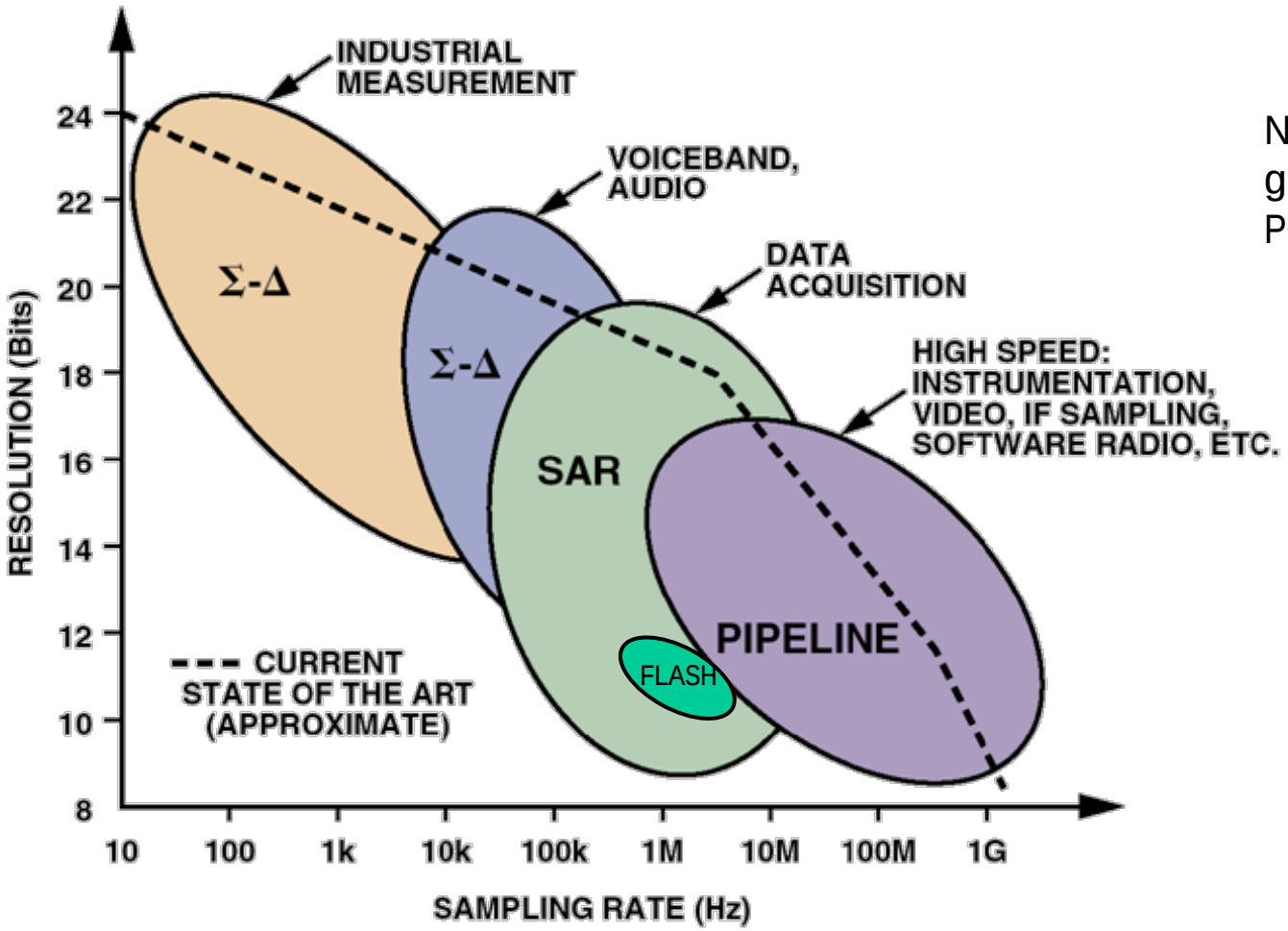


B.T. Turko, R.C. Smith, IEEE Trans. Nuc. Sci. 39(5), 1992 (1311)
C.H. Nowlin, Rev. Sci. Instr. 63(4), 1992 (2322)
D.M. Binkley, IEEE Trans. Nuc. Sci. 41(4), 1994 (1169)

Analog-to-digital converter (ADC)



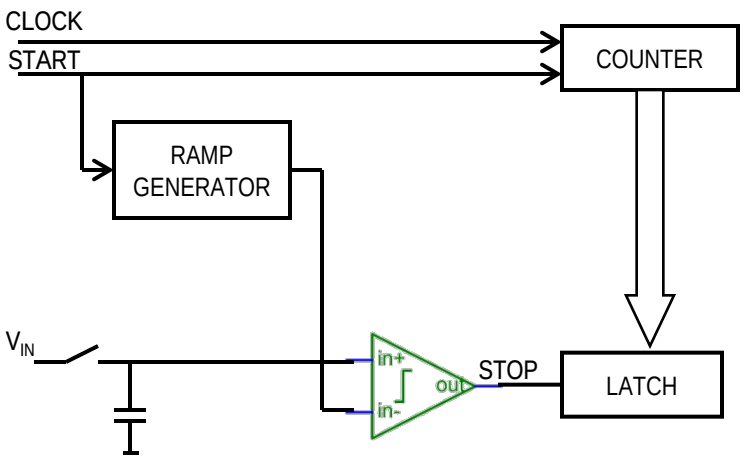
ADC architectures

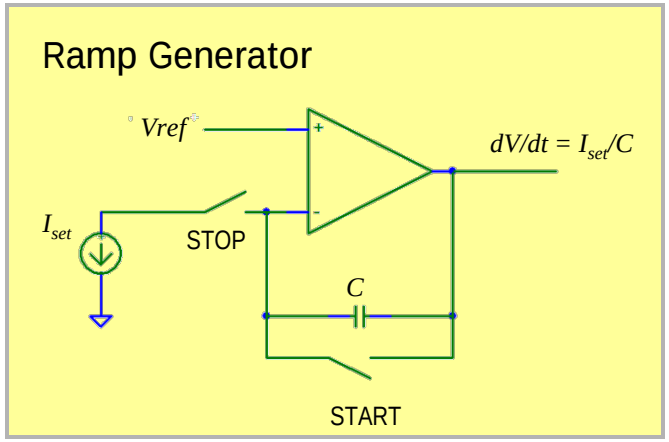


Not shown on this graph:
POWER dimension

W. Kester, Analog Dialogue 39(2), 2005 (11)

Single-slope (Wilkinson) integrator



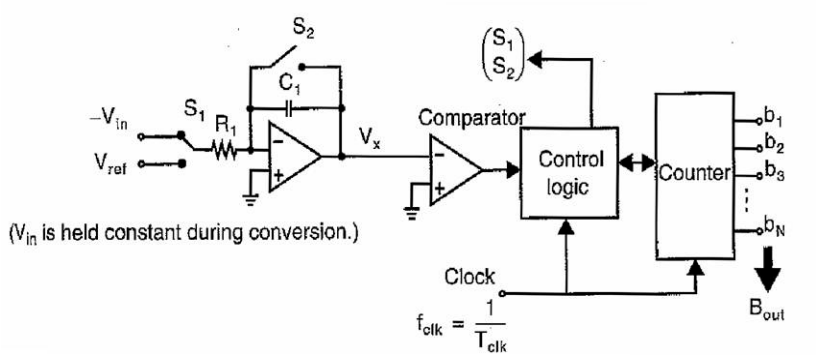


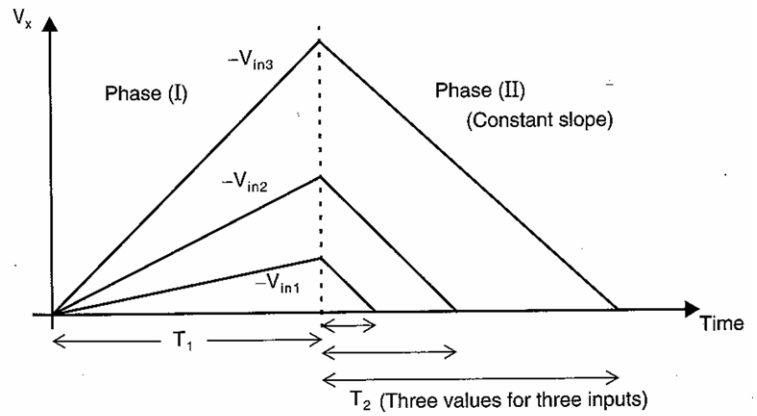
O. B. Milgrome, et al, "A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 4, pp. 771-5, 1992.

- Converts voltage into time interval
- N-bit conversion requires 2^N-1 clock cycles (worst case)
- Dual-edge clocked, Gray code counter improves speed performance
- good DNL
- Compact, low power
- Easily extended to multichannel systems
  - *counter, ramp generator common to all channels*
  - *Sample/hold, comparator, and output register per channel*

D. Wilkinson, Proc. Cambridge Philos. Soc. 46, 508 (1950)
See also Ann. Rev. Nucl. Part. Sci. 45, 1-40 (1995) for an historical description

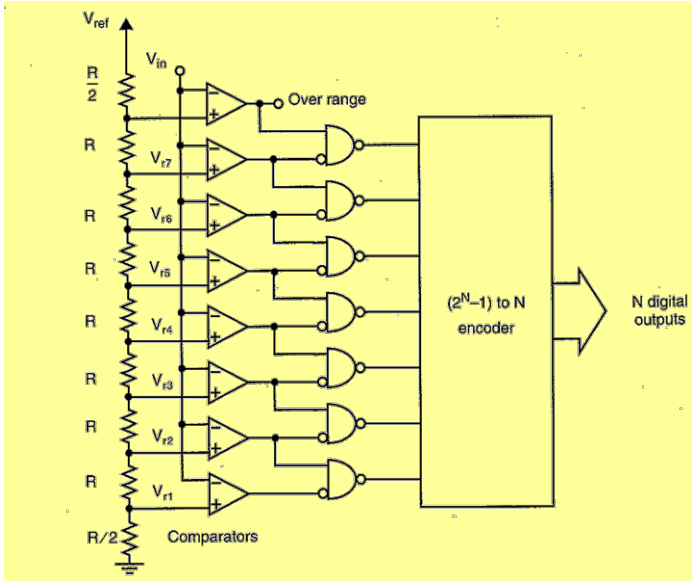
Dual-slope integrator



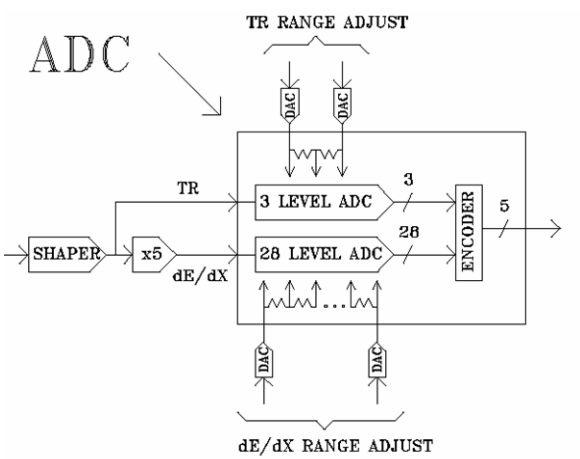


- Compare V_{in} to reference voltage by measuring time needed to charge/discharge C_1
- 2^N clock cycles per conversion, worst case
- Result independent of R_1,C_1, comparator offset
- Largely supplanted by oversampling Σ–Δ converters in most commercial markets

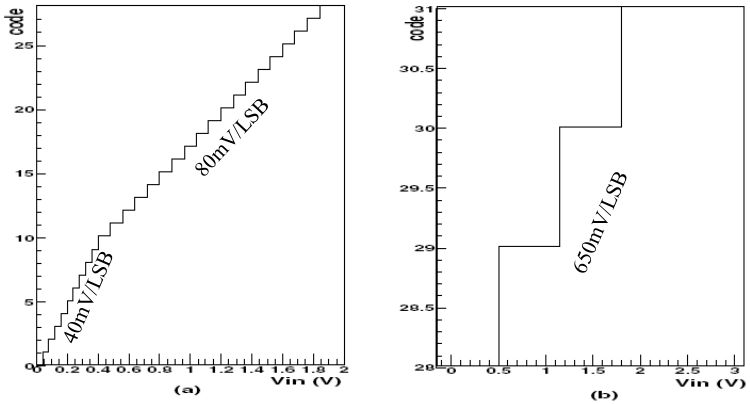
Flash converter



- N-bit converter requires 2^N-1 comparators and resistors
- Converts in one clock cycle (no latency)
- Comparator offset must be < $V_{FS}/(2^N)$
- Vin must be able to drive large dynamic load of comparator array
- Resistor string may be tapped for piecewise-linear transfer function

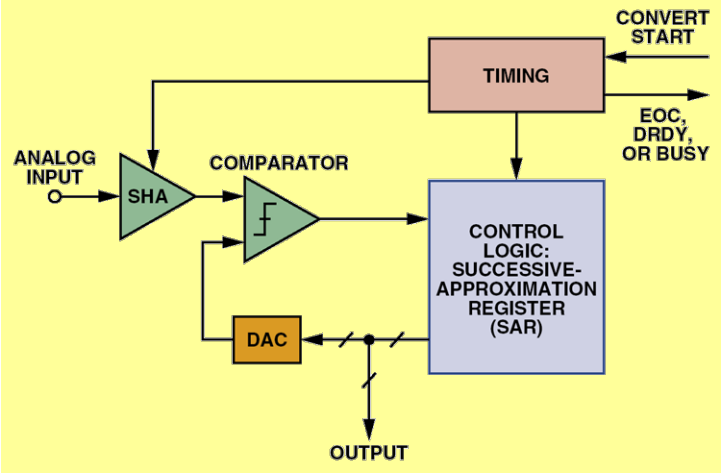


5 bit output
9 bit dynamic range



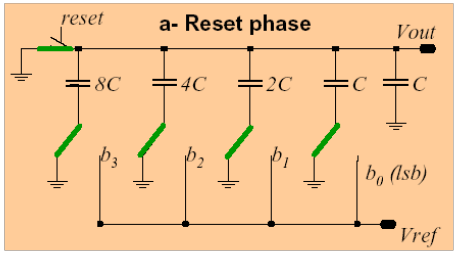
K. Barish et al., Nuclear Science Symposium Conference Digest IEEE, Nov. 2001, 604

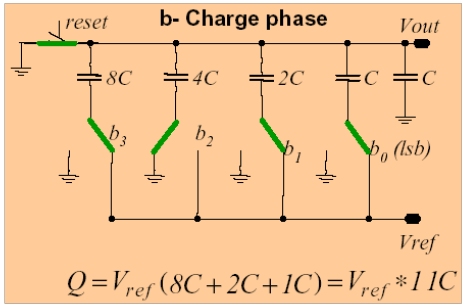
Successive Approximation (SAR) converter

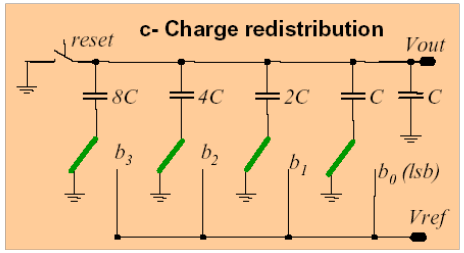


- Performs binary search using N-bit accurate DAC
- Charge-redistribution DAC gives 10 bit accuracy without calibration for typical 0.1% capacitor matching
- With digital autocalibration accuracy improves to 18-bit
- N-bit conversion requires N comparisons
- Sample-and-hold required at input so value to be converted does not change during the conversion time

Charge Redistribution DAC
Example: 4Bit DAC- Input Code 1011



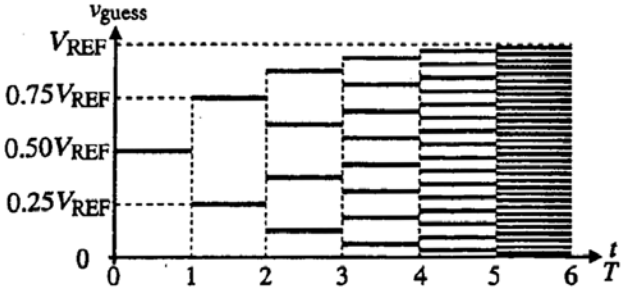




$$V_{ref} * 11C = V_{out} * 16C$$

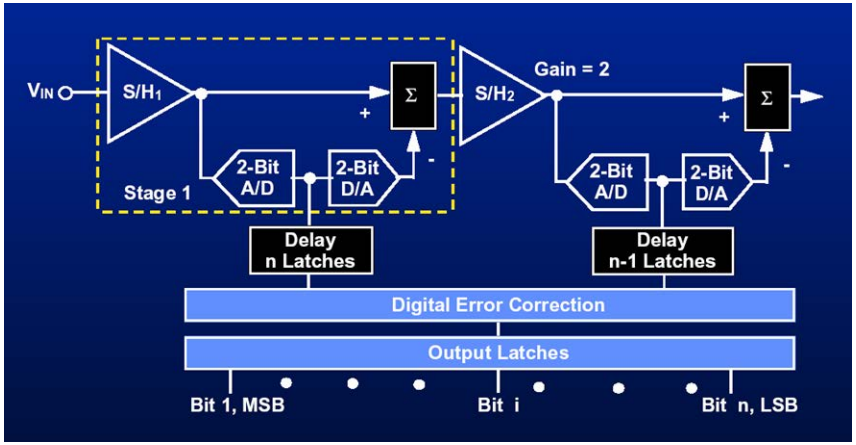
$$\rightarrow V_{out} = \frac{11}{16} V_{ref}$$

Binary search



In SAR converter, CDAC also combines functions of sample/hold and subtractor

Pipeline converter



- Cascade of N stages, each stage consists of a sample/hold, low resolution ADC and DAC, summing amplifier with gain-of-2
- Each stage converts one bit and passes the residue on to the next stage
- N samples being simultaneously processed
- High throughput, moderate complexity, low power
- Only first stage needs full accuracy
- Sub-converter nonidealities can be removed by digital error correction
- Latency of N clocks between sample and valid data
- Minimum clock rate because of droop of internal S/H's
- Cannot be operated in burst mode

Figure of merit for ADC: energy per conversion step

$$FOM_{ADC} = \frac{P_d}{2^{ENOB} \cdot f_s}$$

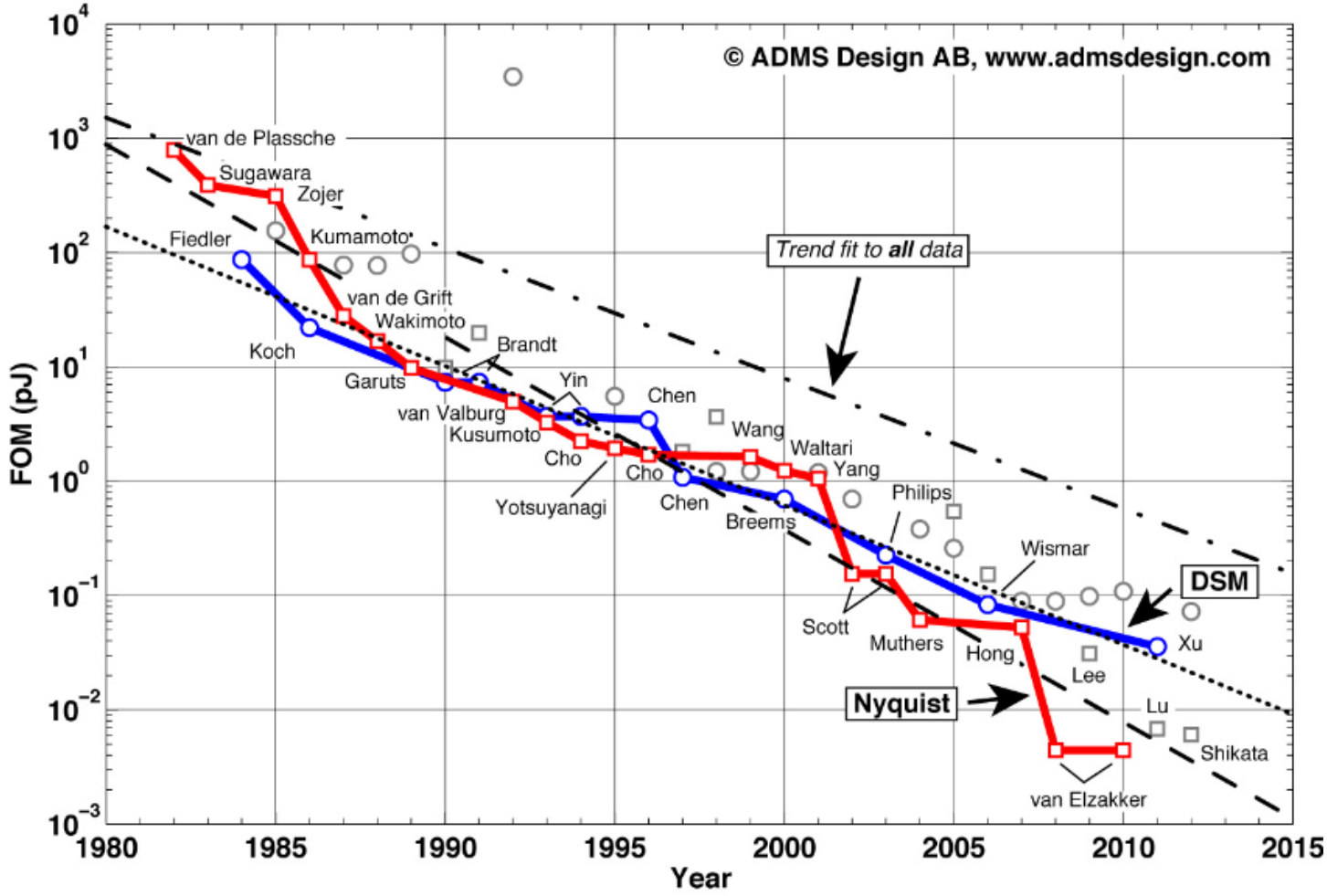
$\boldsymbol{P_d}$ = average power dissipation

$\boldsymbol{ENOB}$ = "equivalent number of bits" = $\log_2$(dynamic range)

$\boldsymbol{f_s}$ = sampling rate

Expresses the power efficiency of A-D conversion

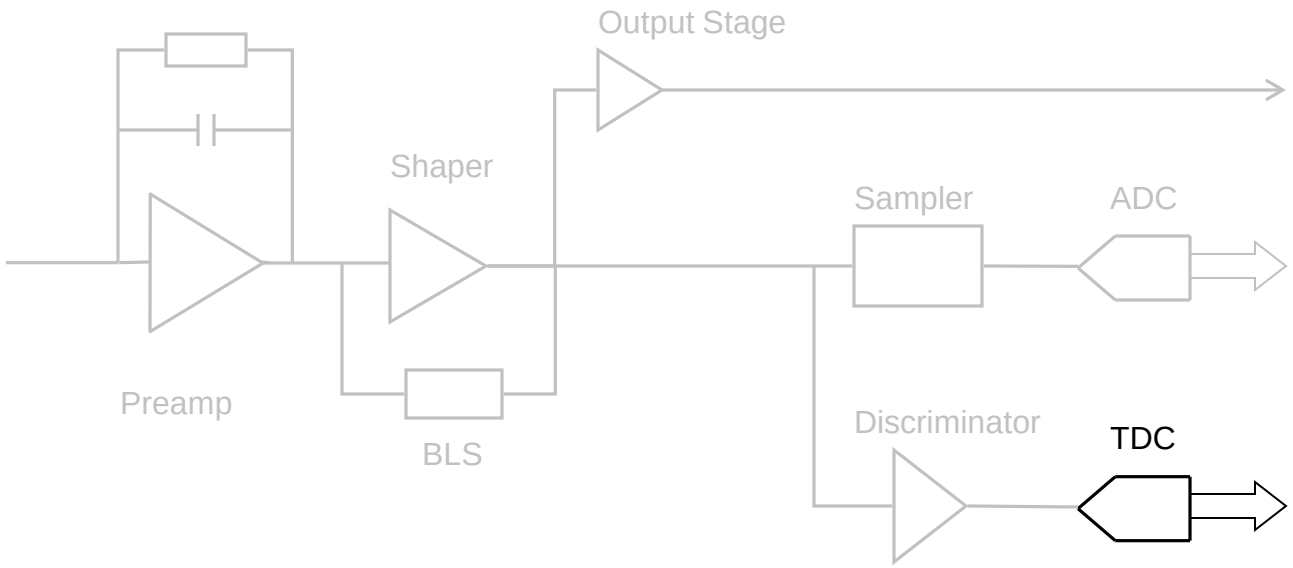
FOM_{ADC} trends – research publications



Performance doubling every ~31 months
cf. Moore's law for logic: 12 - 18 months

B. E. Jonsson, "ADC performance evolution: Walden figure-of-merit (FOM)," Converter Passion, Aug. 21, 2012, Available: http://converterpassion.wordpress.com

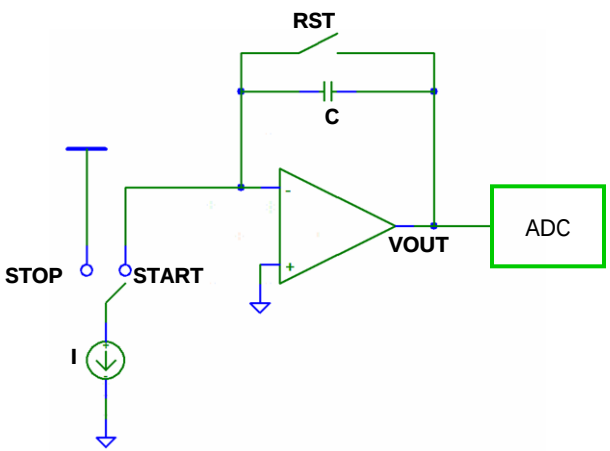
Time-to-digital converter (TDC)

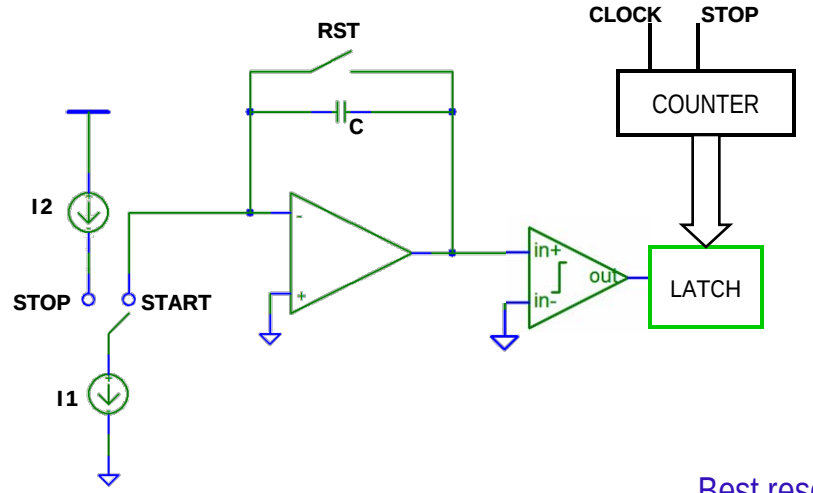


Time-to-amplitude converter (TAC)

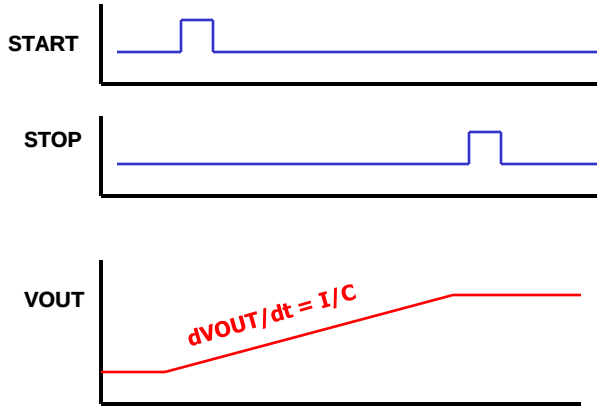
Const. current charges capacitor for time $\Delta T = T_{stop} - T_{start}$
Measure $V_{out} = I \times \Delta T / C$

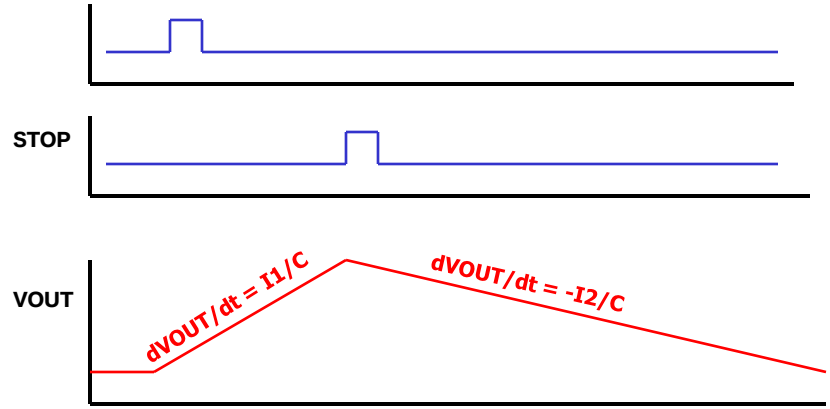
TAC + Wilkinson = TDC



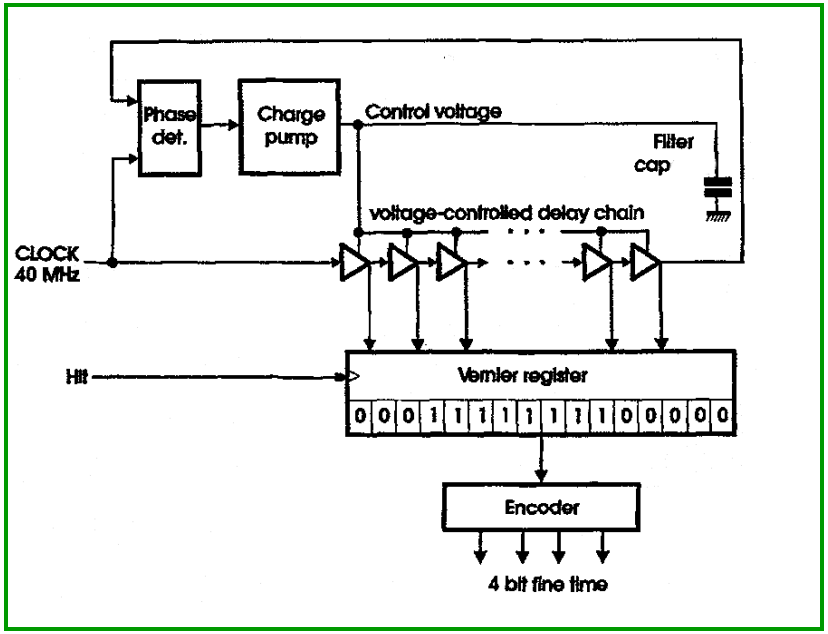


Best resolution ~ 30ps



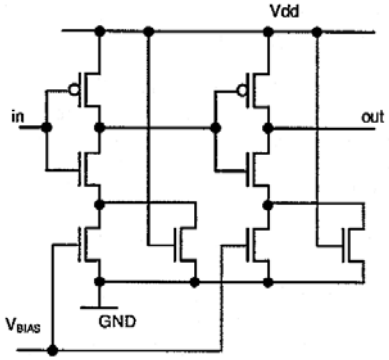


Delay-locked loop interpolator

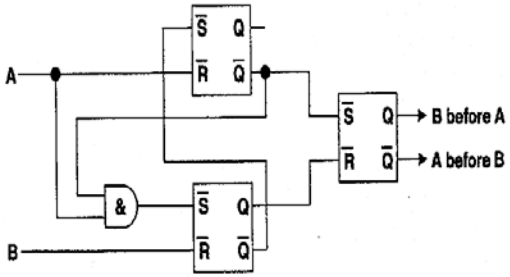


- Clock (START) signal propagated down a tapped, N-element delay chain
- Hit (STOP) freezes state of delay line
- Delay per stage stabilized to T_{ck}/N by phase-locking output to input, using voltage control of delay elements
- Resolution T_{ck}/N; dynamic range T_{ck}
- Extend dynamic range by coarse counter
- Resolution limited to unit gate delay of the technology
- Mismatch of delay elements ➔ nonlinearity
- Long delay lines more nonlinear
- Easily extended to multichannel systems:
  - *DLL common to all channels*
  - *Latch, encoder per channel*

Variable delay element



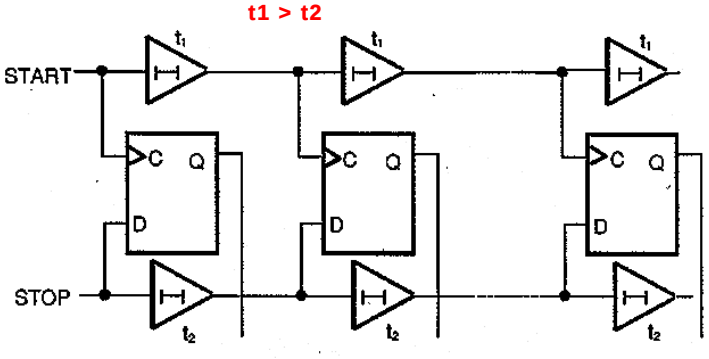
Phase detector



K. Barish et al., Nuclear Science Symposium Conference Digest IEEE, Nov. 2001, 604

Vernier techniques

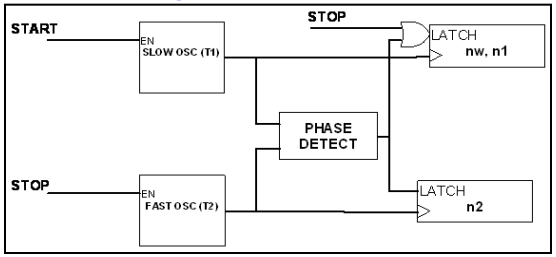
Vernier DLL

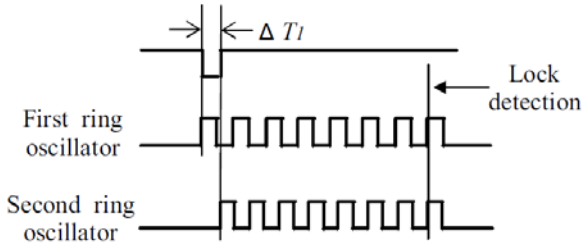


P. Dudek, IEEE Trans. Solid-State Circuits 35(2), 240 (2000)

- START and STOP signals propagate down separate delay lines
- START chain has longer element delay than STOP
- Measure the stage where STOP catches up to START
- Stabilize by controlling *difference* t_1-t_2 so that $N(t_1-t_2) = T_{ck}$
- Resolution LSB can be << t_{pd} of the technology
- Area increases linearly with dynamic range
- Less tolerant to mismatch than single DLL

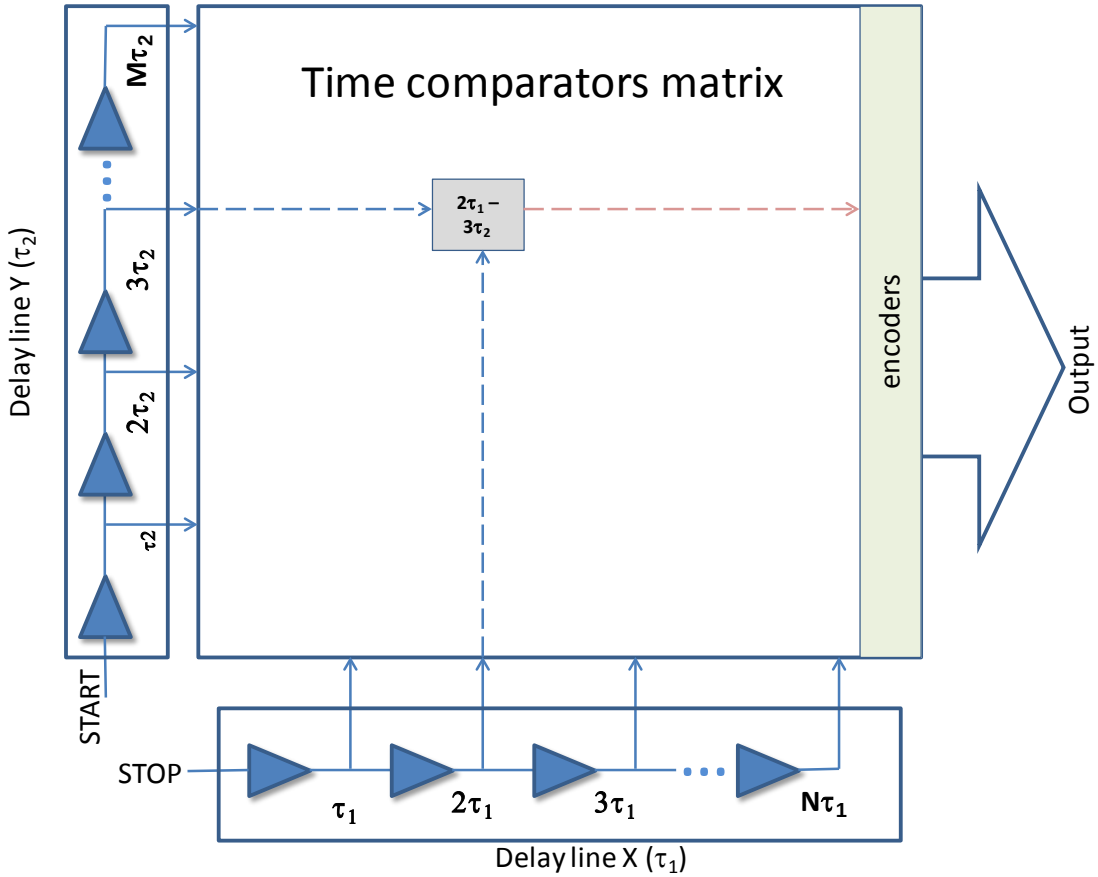
Two-ring oscillator





- START and STOP signals are used to enable triggerable oscillators having a small frequency difference
- START triggers the slower of the two oscillators, STOP triggers the faster one
- Resolution LSB is equal to the difference in period between the two oscillators T1-T2
- Counters record the number of periods of each oscillator between START and lock detection
- $\Delta T = (n_1 - n_2)T2 + n_1(T1-T2)$

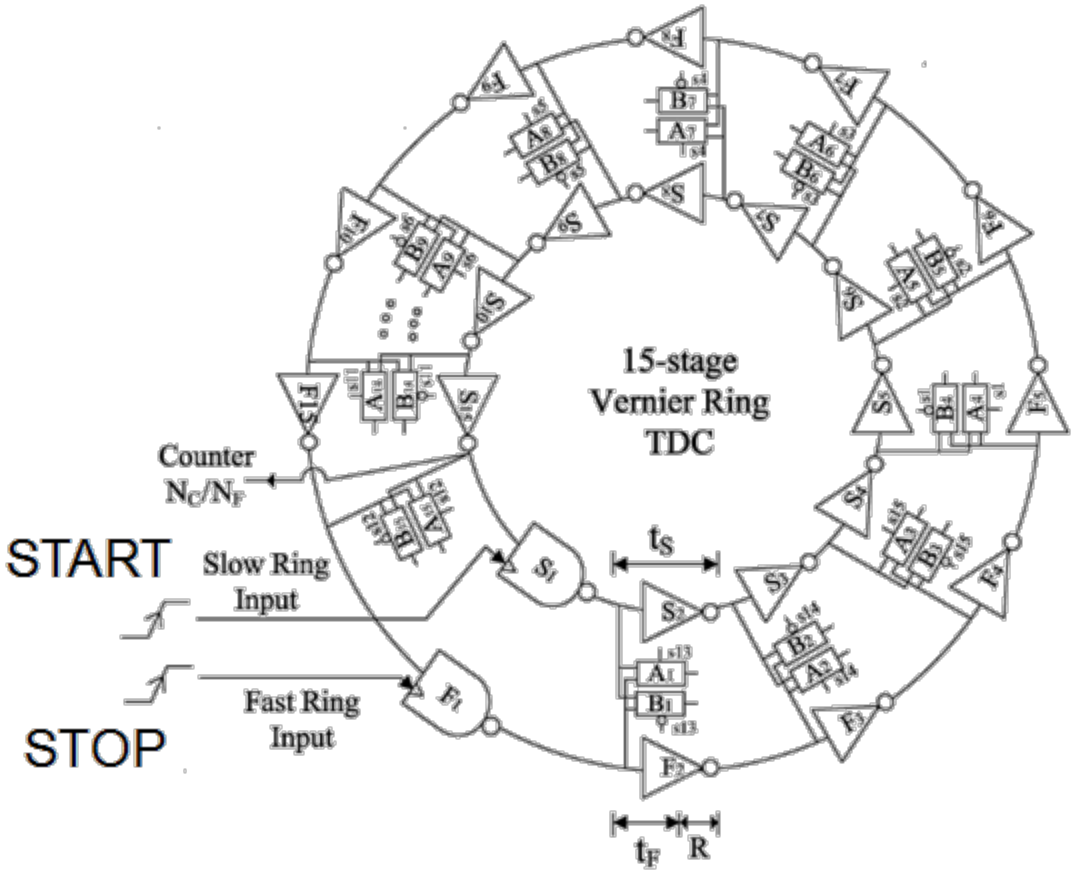
Two-dimensional vernier TDC



- Hybrid between single DLL and classical vernier TDC
- shorter length of delay lines to achieve same overall delay range and resolution
- performance achieved (65nm CMOS):
  - resolution: 5ps
  - range: 0.6ns, 7bit
  - power dissipation: 1.7mW

L. Vercesi et al., IEEE J. Solid-state Circuits 45, 1504-1512 (2010)

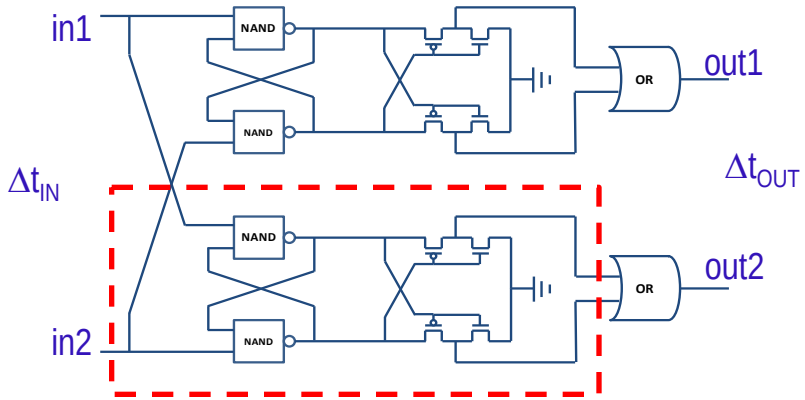
Cyclic vernier TDC for extended dynamic range



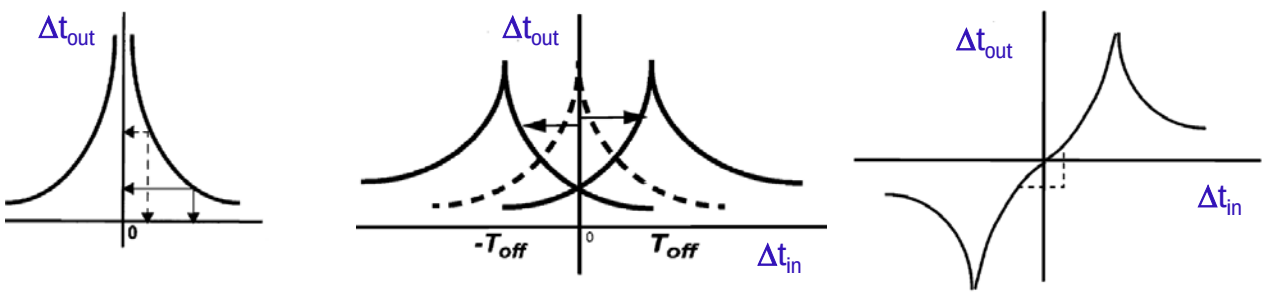
- delay cells are re-used for measuring large time intervals
- digital logic monitors number of laps and checks when STOP catches START
- good speed/dynamic range/area tradeoff
- performance achieved (130nm CMOS):
  - resolution: 8ps
  - range: 32.8ns, 12bit
  - power dissipation: 7.5mW

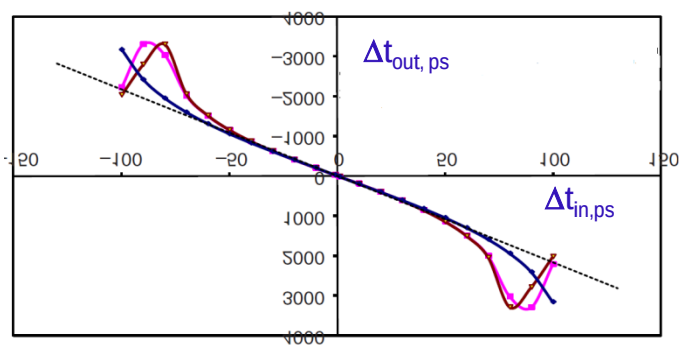
J. Yu et al., IEEE J. Solid-state Circuits 45, 830-842 (2010)

Time difference amplifier



- metastability of cross-coupled NAND latch can be used to make a ***time difference amplifier***
- output delay difference is logarithmic function of input delay difference
- by offseting and subtracting two metastable transfer functions, a quasi-linear relation between input and output time difference can be obtained.





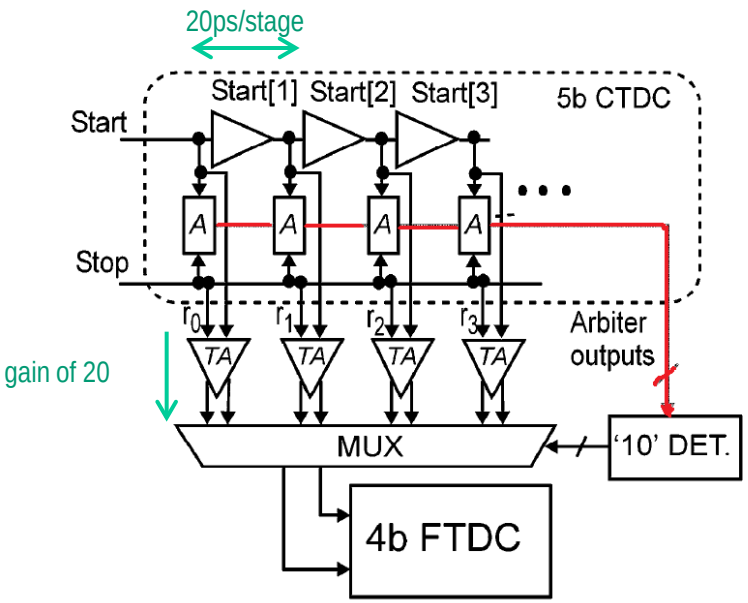
- gains of 2 – 20 over a range up to several hundred ps are possible

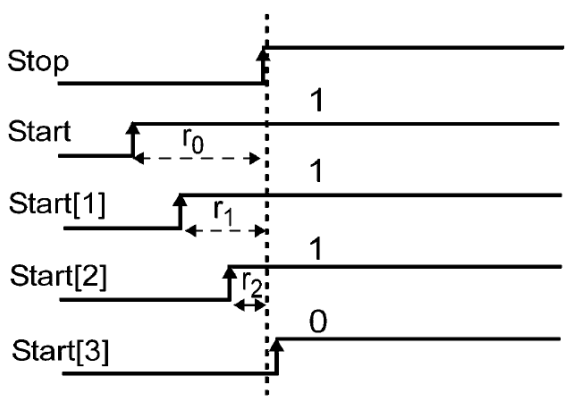
M. Lee, A. Abidi, "A 9b, 1.25ps resolution coarse-fine time-to-digital converter in 90nm CMOS that amplifies a time residue", IEEE J. Solid-State Circuits 43,769-777, 2008

A. Abas et al., "Time difference amplifier", Electronics Letters 38, 1437-8, 2004

A. Alahmadi et al., "Time difference amplifier with improved performance parameters, Electronics Letters 48, 2012

Coarse-fine TDC using time diff. amplifiers

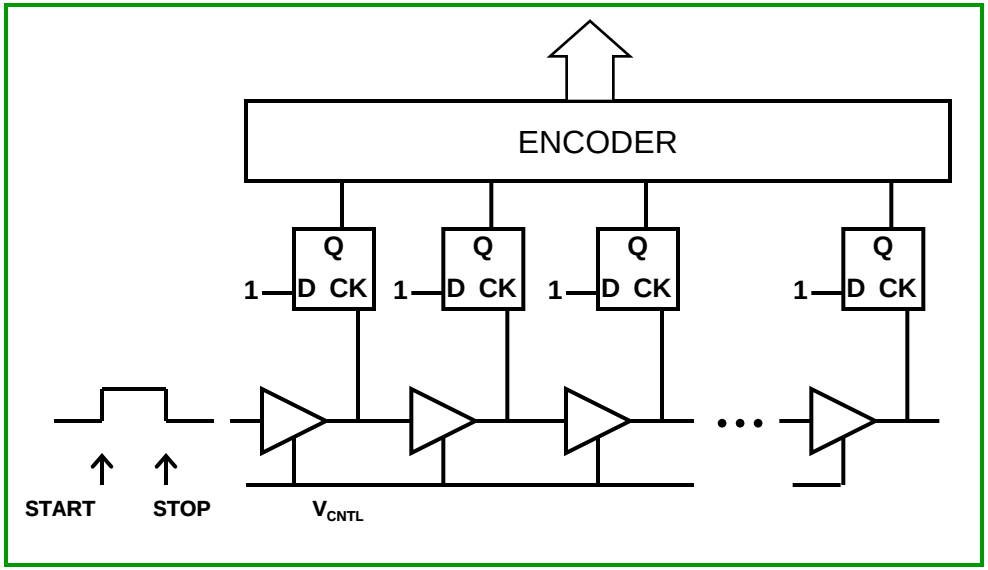




- similar in principle to SAR ADC
- make coarse measurement of time difference, then amplify the residue
- generate all possible residues (time cannot be stored) and select the correct residue for amplification
- performance achieved (90nm CMOS):
  - 1.25ps resolution
  - 640ps range (9b)
  - 3mW power dissipation
  - 0.6mm^2

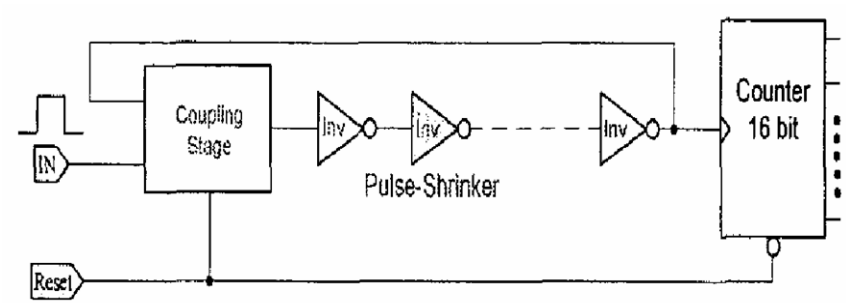
M. Lee, A. Abidi, "A 9b, 1.25ps resolution coarse-fine time-to-digital converter in 90nm CMOS that amplifies a time residue", IEEE J. Solid-State Circuits 43,769-777, 2008

Pulse-shrinking TDC



- Chain of pulse-shrinking elements
- Change of pulse width Δt per cell (stabilized)
- After n cells the pulse width shrinks to zero
- Cyclic version recirculates pulse through same shrinking element; count number of cycles until pulse vanishes
- Resolution LSB can be << t_{pd} of the technology
- Conversion time > time interval to be measured
- Both schemes can be combined with coarse counters to extend dynamic range

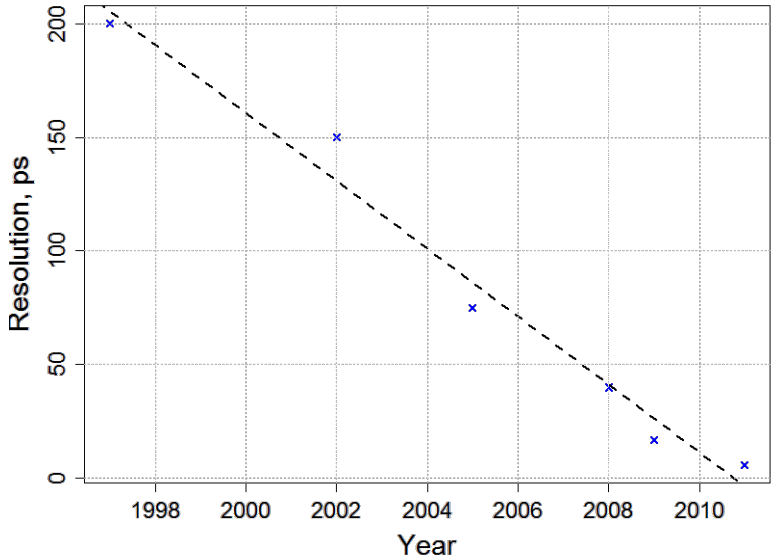
Cyclic version



E. Raisanen-Ruotsalainen, IEEE J. Solid State Circuits 30(9), 984 (1995)
S. Tisa et al., Proc. ISCAS 2003, p.465

TDC in FPGA

- Modern FPGAs take advantage of the latest CMOS technology ➔ gate delays below 100ps
- DLL-based or Vernier TDC can be programmed in firmware
- Place-and-route constraints and knowledge of the FPGA's clock distribution tree are necessary to achieve respectable nonlinearity
- Need to compensate for process, temperature, and voltage variations
- Abundance of gates and high-bandwidth I/O makes it easy to implement multiple channels, nonlinearity compensation, other digital functions.



1. J. Kalisz, R. Szplet, J. Pasierbinski, and A. Poniecki, "Field-programmable-gate-array-based time-to-digital-converter with 200-ps resolution," *IEEE Trans. Instrum. Meas., vol. 46, pp. 51–55, Feb.*1999.
2. M. S. Andaloussi, M. Boukodoum, and E. M. Adoulhamid, "A novel time-to-digital converter with 150 ps time resolution and 2.5 ns pulsepair resolution," in *Proc. 14th Int. Conf. Microelectronics, Dec. 11–13*, 2002, pp. 123–126.
3. D. Xie, Q. Zhang, G. Qi, and D. Xu, "Cascading delay line time-to-digital converter with 75 ps resolution and a reduced number of delay cells," *Rev. Sci. Instrum., vol. 76, no. 014701, 2005.*
4. J.Wu and Z. Shi, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay," in *Proc. IEEE Nuclear Science Symp. Conf. Rec., Oct. 19–25, 2008, pp. 3440–3446.*
5. S. Junnarkar, P. O'Connor, and R. Fontaine, "FPGA based self calibrating 40 picosecond resolution, wide range time to digital converter," in *IEEE Nuclear Science Symp. Conf. Rec., Oct. 19–25, 2008, pp.* 3434–3439.
6. C. Favi and E. Charbon, "A 17 ps time-to-digital converter implemented in 65 nm FPGA technology," in *Proc. ACM/SIGDA Int. FPGA Symp., Feb. 22–24, 2009, pp. 113–120.*
7. E. Bayer, M. Traxler, "A High-Resolution (<10ps RMS) 48-Channel Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA)", IEEE Trans. Nucl. Sci. 58, 1547-1552, 2011

Not in signal path, but important

- Power conditioning and distribution
- Bias circuits
- Electrostatic discharge protection
- Digital configuration switches
- Analog monitor
- DACs
  - *set comparator thresholds*
  - *trim channel-channel variations*
- Calibration pulser

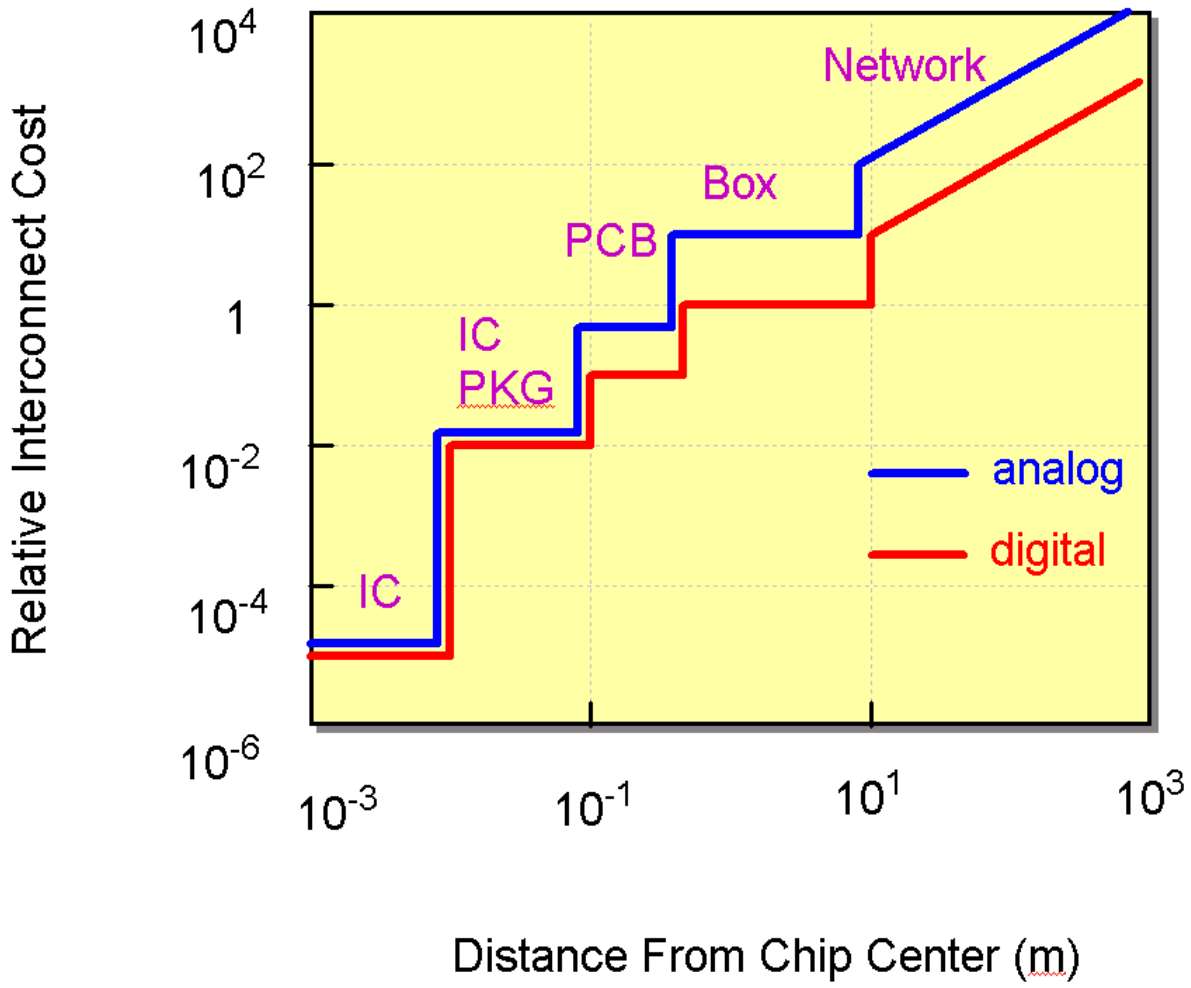
Packaging, Interconnect, and Systems Issues

Paul O'Connor, Brookhaven National Laboratory

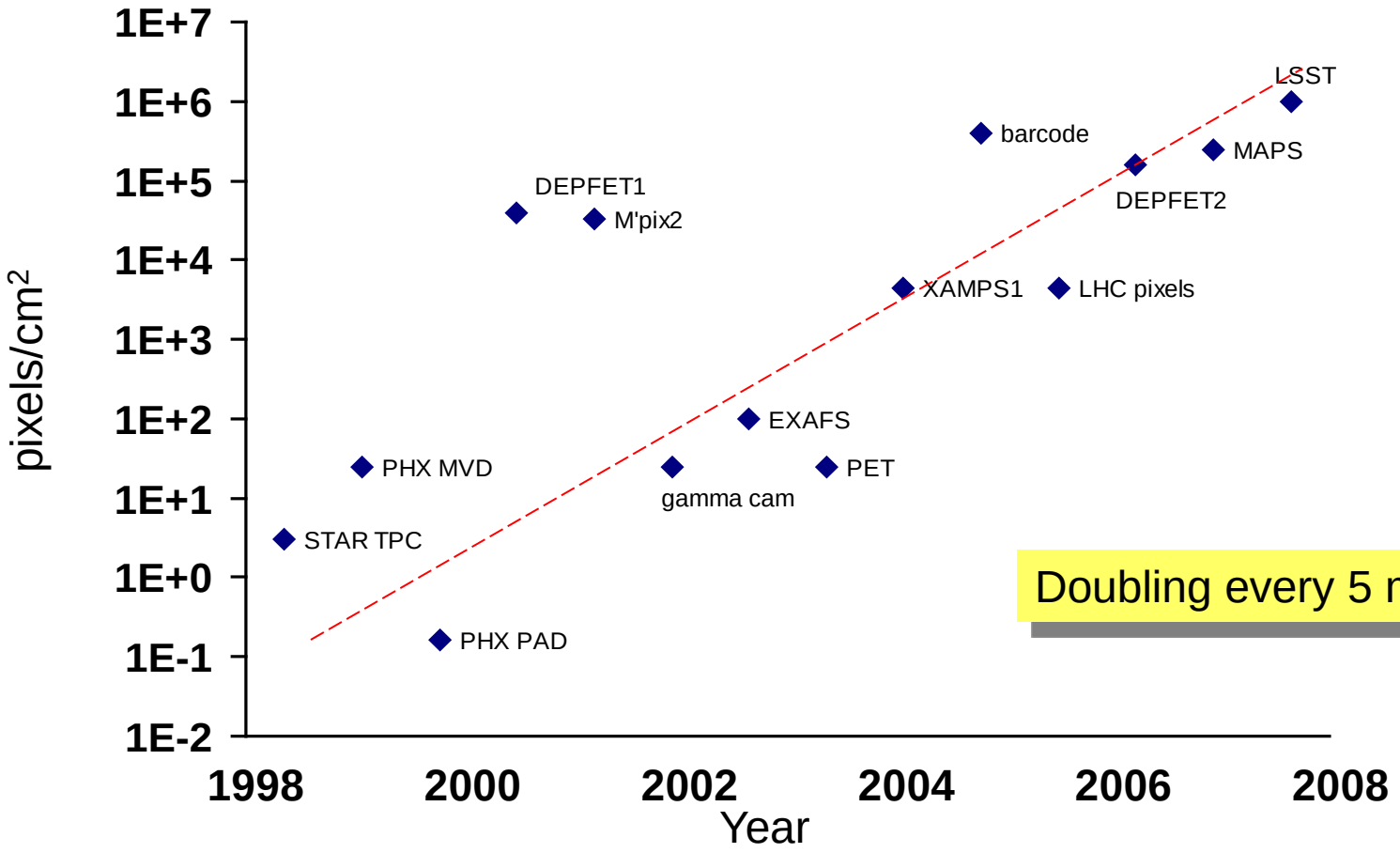
IEEE Nuclear Sciences Symposium/Medical Imaging Conference

November 8, 2014

Cost of interconnect



Pixel density



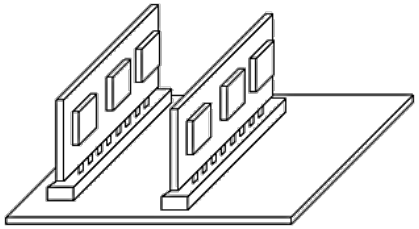
Doubling every 5 months

Interconnect issues in monolithic front ends

- Detector – Front End
  - Lowest possible capacitance for low noise
  - Maintain small form factor
  - Ease of assembly
- Front end – Data Acquisition
  - Analog processing to reduce the required level of digitization
    - *sampling*
    - *peak detection*
    - *multiplexing*
  - Efficient use of expensive “analog” interconnect

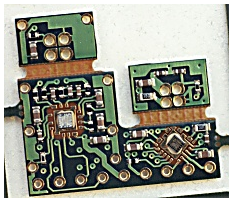
Detector – FE interconnect choices

- **board-to-backplane**
  - easy to test, repair
  - large boards possible
  - connector pins are failure points
  - coarse pitch and high capacitance (> 1pF)

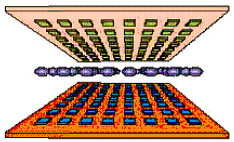


- **standard SMT package soldered to board (QFP or BGA)**
  - easy to test, difficult to repair
  - capacitance down to 0.2 pF for small packages
  - board area limited by reflow oven capacity

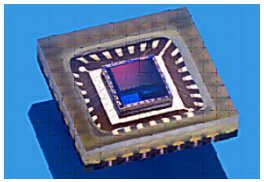
- **wirebonded chip-on-board**
  - difficult to test, assemble, and repair
  - board area limited by wirebonder
  - fragile
  - low capacitance (0.1 pF)

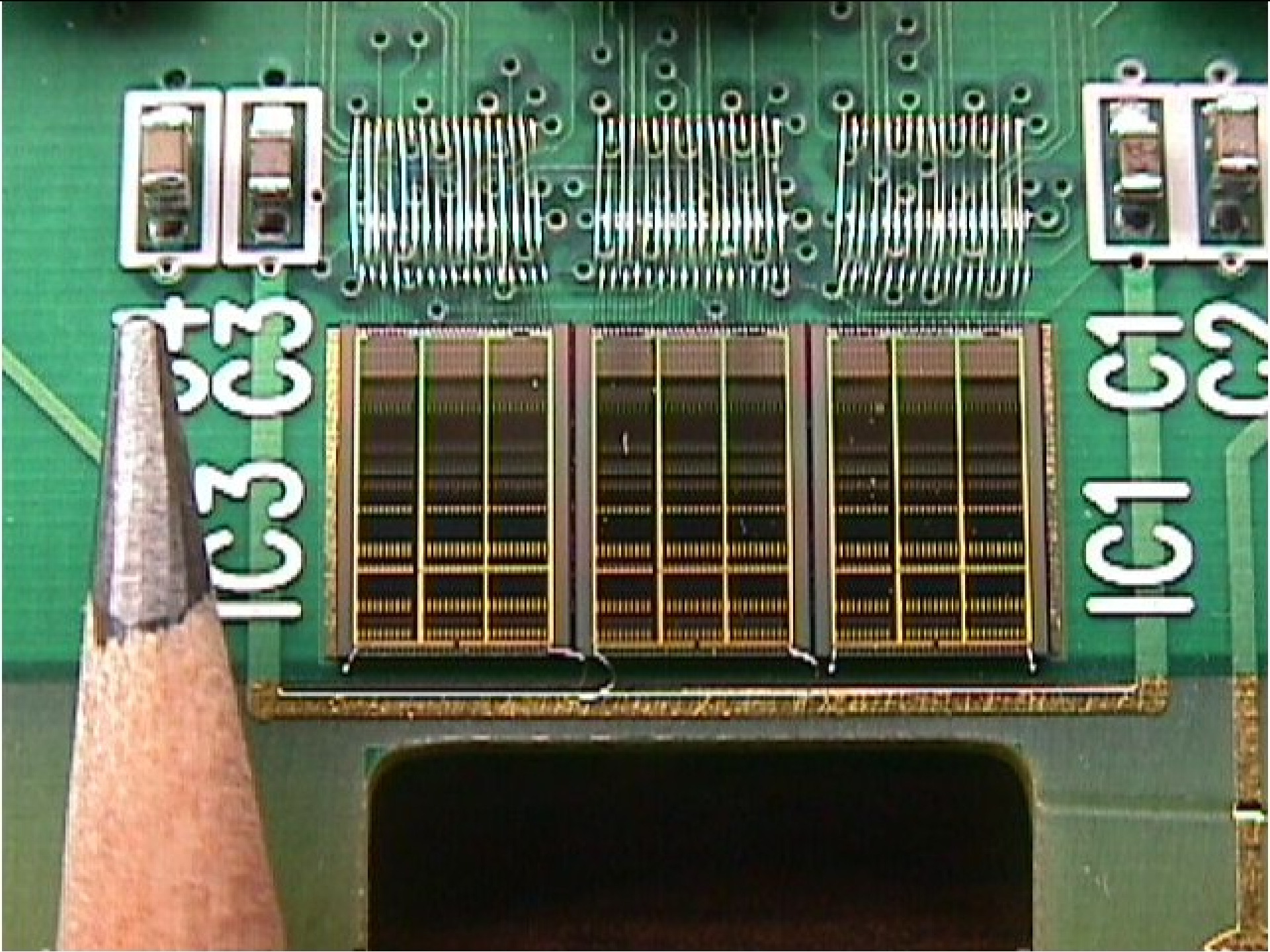


- **bump-bonded flip-chip**
  - can match pixels with pitch from ~30 – 1000 μm
  - difficult to test, assemble, and repair
  - circuitry has to fit in same area as pixel

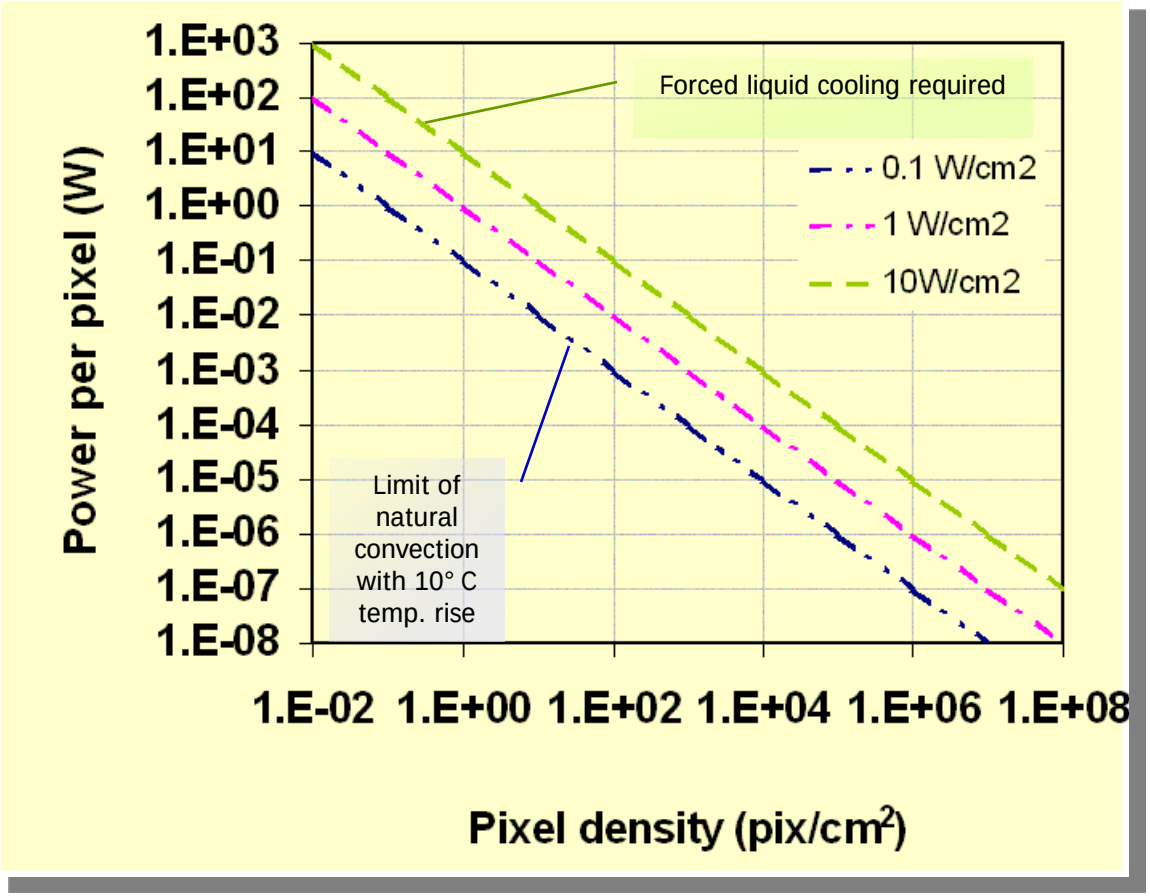


- **monolithic detector/electronics**
  - interconnect is created as part of the detector fabrication process
  - ultra-low capacitance (few fF)



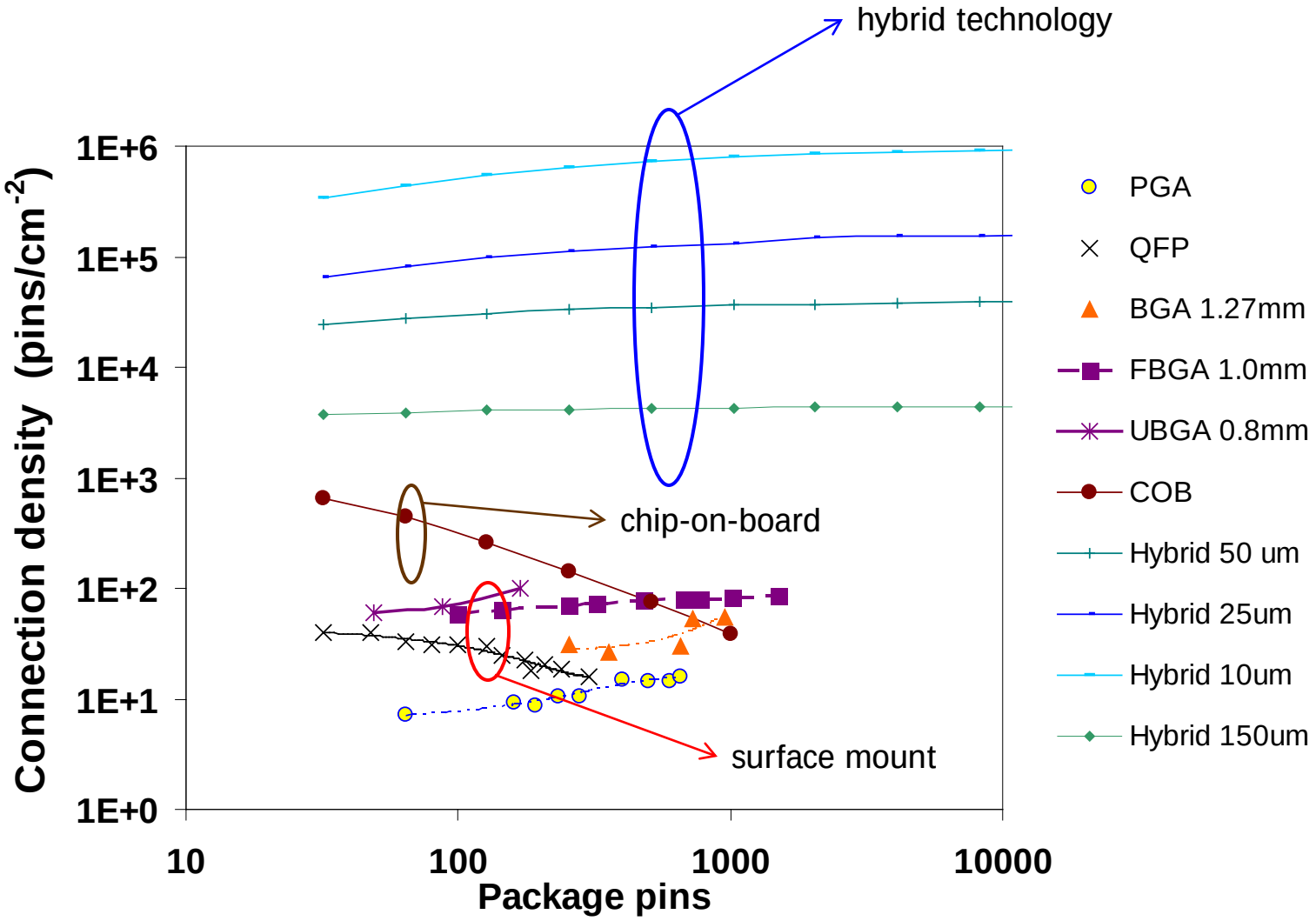

IC3
IC1

Power density



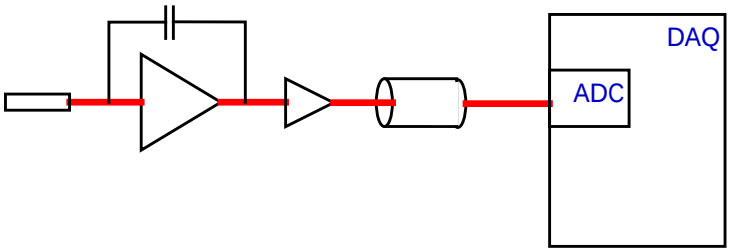
- On-detector power density is limited by cooling capability.
- Electronics for high-density detector must be extremely low power.

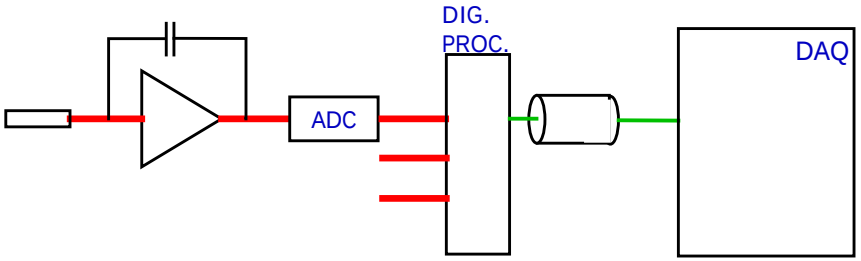
Packaging density

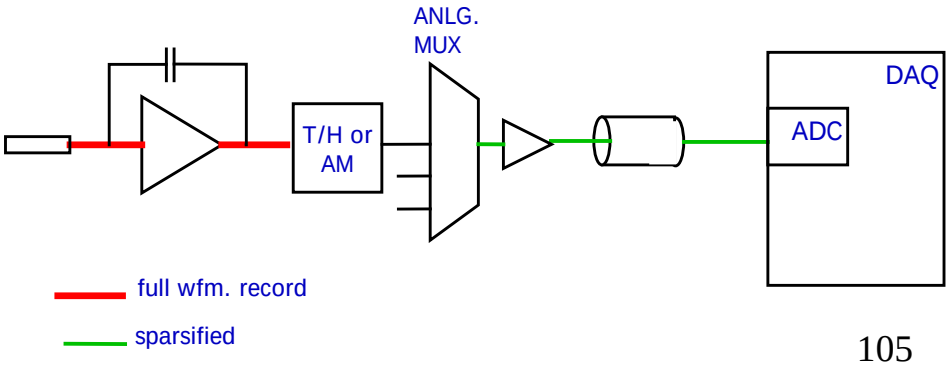


Front end – DAQ interconnect

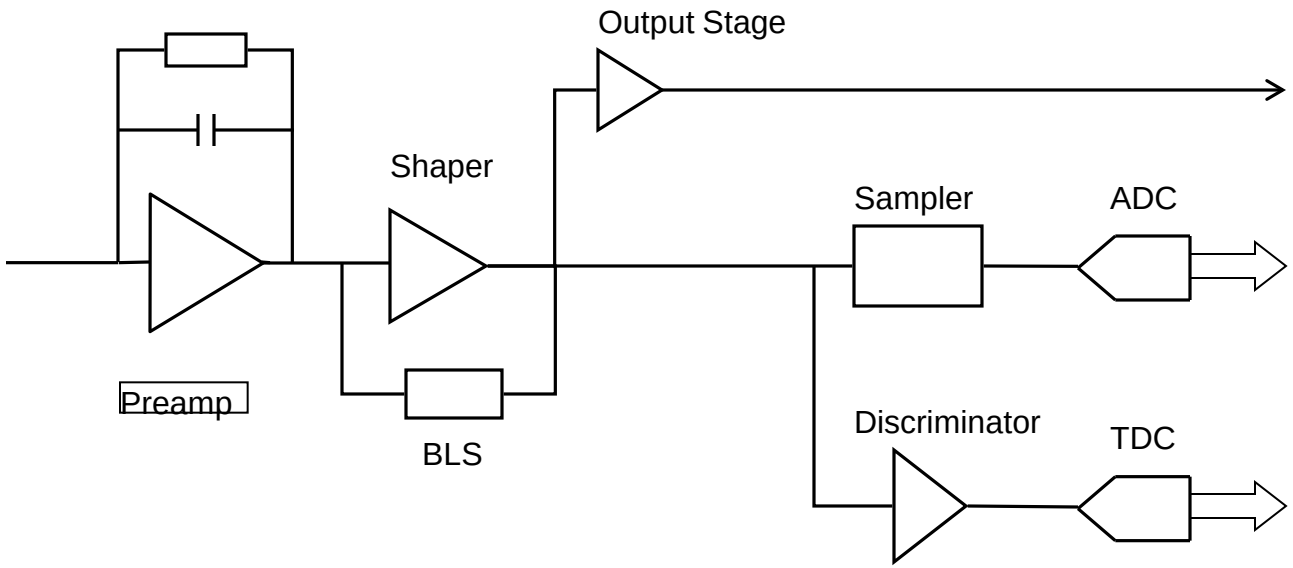
- High bandwidth analog interconnect is expensive and bulky.
- Due to the low occupancy, this interconnect bandwidth is mostly wasted.
- Digitizing every channel is inefficient in a low-occupancy system.
- Existing approaches to sampling and multiplexing are inefficient:
  - *track/hold needs trigger, incurs deadtime during readout*
  - *analog memory (SCA) deadtimeless but needs trigger, multiple samples, no sparsification, complex controller*







Putting it all together



Power Efficient Architecture

- Highest power functions:
  - *charge preamplifier*
  - *analog line driver*
  - *ADC*

- Staying within a power budget and achieving maximum performance involves careful tradeoff.

Figure of merit for charge amplifiers and ADCs

$$FOM_{CSA} = \frac{P_d \cdot \tau_p}{Q_{\max} / \sigma_Q}$$

- Expresses the power cost of achieving SNR and speed
- Can be applied to front ends in any technology
- Corresponds to figure of merit for analog-digital converters:

$$FOM_{ADC} = \frac{P_d}{2^{ENOB} \cdot f_s}$$

Rule-of-thumb estimates

- Use FOM_{CSA} ~ 1pJ, calculate most quantities of interest.
- Given P_{max}, rate r, what is achievable SNR?

$$SNR = \frac{P}{FOM_{CSA} \cdot 10r}$$

  – *e.g.* P *=1mW,* r *=100kHz, SNR ~ 10^3*
- What power needed to get timing accuracy σ_t?

$$\sigma_t \approx \frac{\sigma_V}{dV/dt} \sim \frac{\tau_p}{SNR}; \quad P = \frac{FOM_{CSA}}{\sigma_t}$$

  – *e.g.* σ_t *=2ns,* P *~ 50μW*

Figure of merit for charge amplifiers (FOM_{CSA}) vs. detector capacitance

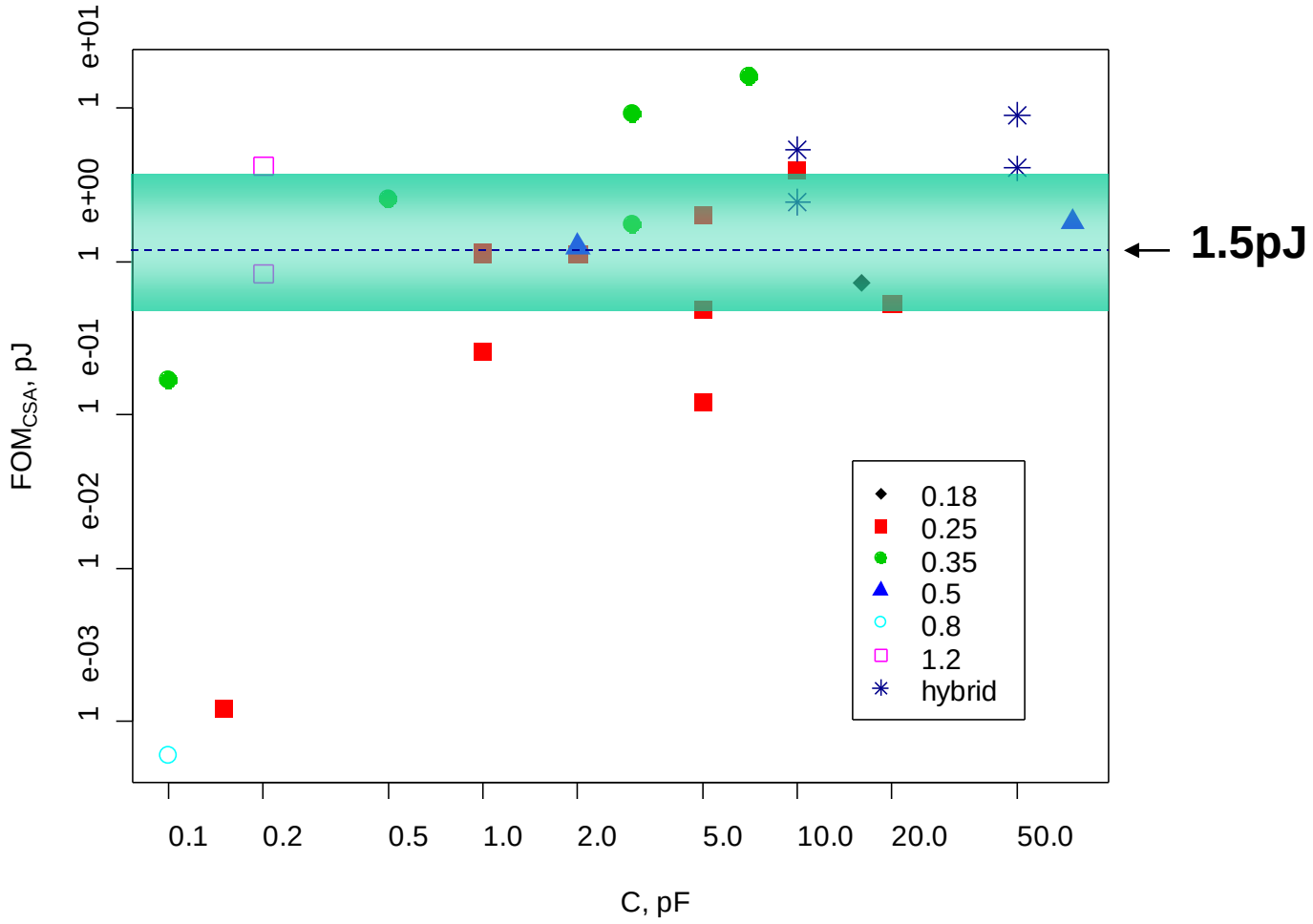
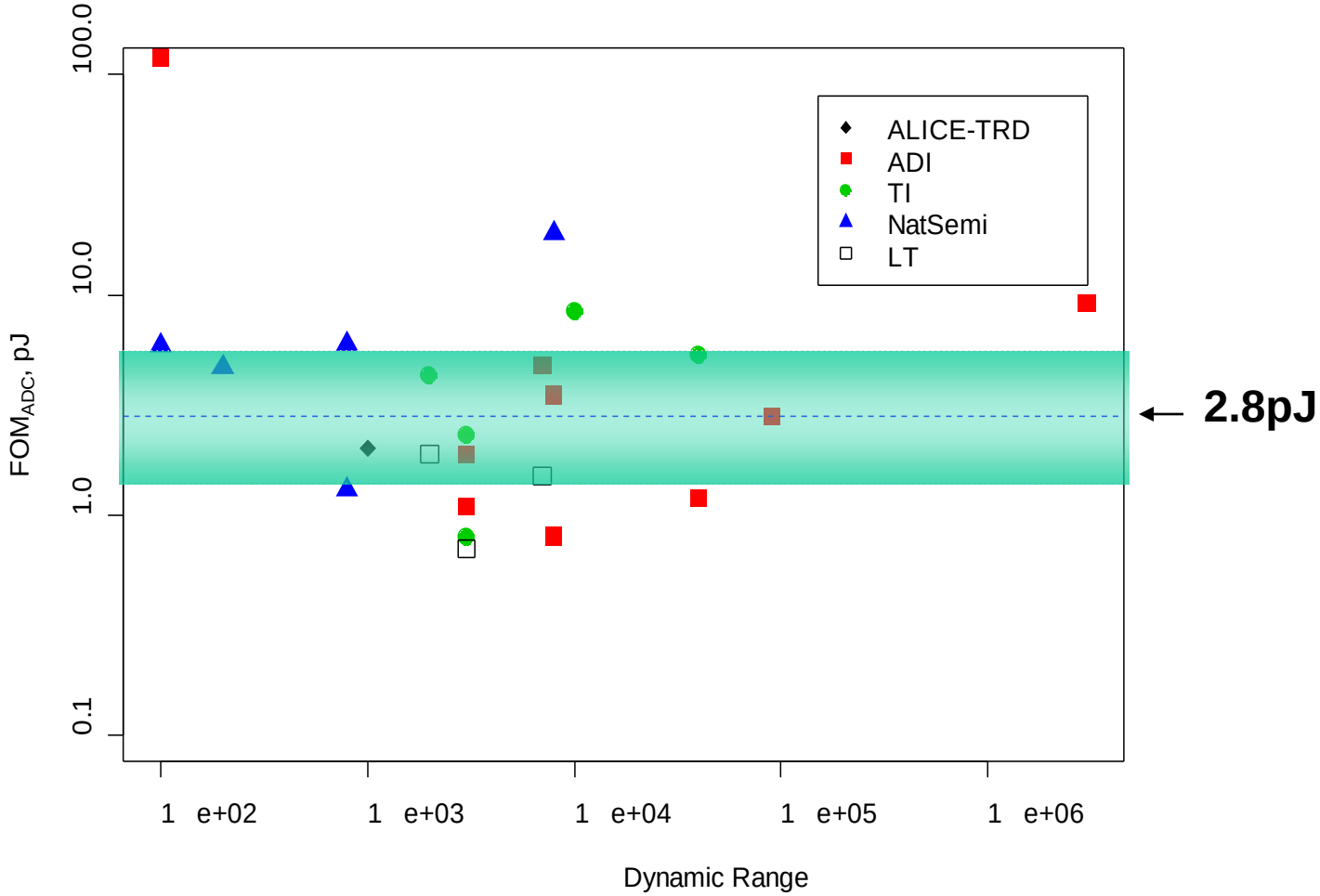


Figure of merit for ADCs (FOM_{ADC}) vs. dynamic range



Architecture choices

- Digital waveform recording of every channel requires ADC to have:
  - *same SNR as charge amplifier*
  - *sampling frequency 2X – 20X higher than analog bandwidth*
- **Guarantees** $P_{ADC} >> P_{CSA}$
- Better architecture: capture and buffer the analog information on the FEE ASIC, then steer samples to the ADC
- Switched capacitors or peak detectors can serve as the sampling cells
- Use analog buffers (memory) with simultaneous READ/WRITE to avoid deadtime

Example: TPC Digitization Power

- N_{pads} 8000
- $N_{timeslices}$ 500
- N_{voxels} 4×10^6
- t_{drift} 7μs
- f_{trig} 2kHz
- Occupancy 2%

- Digitization Energy (12 bit resolution):
  - *10^{-12} J/bit * 2^{12} * N_{voxels} = 16 mJ*
- Power (FADC):
  - *16mJ / 7μs = 2000W (250 mW/chan)*
- Power (buffer and readout at 2 kHz trigger rate):
  - *16mJ / 500μs = 30W (4 mW/chan)*

• Compare with <u>0.75mW/chan</u> for amplifier + <u>0.6mW/chan</u> for PD + TAC.

• With sparsified readout of only occupied channels buffered in PD: P_{ADC} ~ 0.6W (75 μW/chan).

Summary

- Modern IC technologies, optimized for digital performance, are challenging for analog design but offer exceptional integration density, speed, and radiation tolerance.
- Noise is limited by available power, detector properties, event rate, and the 1/f properties of the technology.
- In addition to optimizing the first transistor, choice of shaping function is also important in noise optimization.
- High-order shapers improve the power/noise tradeoff, and also improve pileup and charge collection performance.
- An empirical figure of merit for charge amplifiers, analogous to that for ADCs, can be used to guide design choices.
- Reducing the number of analog-to-digital conversions and minimizing off-chip analog signal transmission (where possible) improves noise by allowing power to be allocated to the front end.

Analog CMOS Circuit Design

Paul O'Connor, BNL

Selected slide captions

Slide 2

Electronic design automation (EDA) tools are essential for even the simplest integrated circuit designs, and EDA has rapidly increased in importance with the continuous scaling of semiconductor technology. Today's software tools are complex chains that take the designer from concept to mask layout. The market is dominated by the needs of digital large-scale chips, where the methodology is focused on formal synthesis techniques that minimize or eliminate the need for the designer to deal with transistor-level operations. Analog design, on the other hand, is less amenable to automation techniques. Design of analog and mixed-signal (analog plus digital) ASICs uses a different, more handcrafted approach and requires a higher level of technology awareness on the part of the designer.

The commercial EDA companies supply comprehensive tool suites addressing both digital and mixed-signal designs. Costs are high but educational institutions are granted generous discounts, and rental arrangements are available. The commercial software is complex and geared for groups having at least one individual dedicated to installation, maintenance, and customization of the tools.

Open-source tools are available and have been used to create designs of up to several hundred thousand transistors. They are best suited to designs in older technologies, as they lack the ability to deal with the complications inherent in deep submicron processes.

Slide 6

Physical design of monolithic analog circuits bears a distant resemblance to the printed circuit layout process. Starting from the schematic representation of the circuit the designer instantiates each component, uses a graphical editor to place the components,

and establishes connectivity using the available routing layers. To aid this process, many tools offer parametric cell generators for transistors and passive components; autorouters are also available in some tool suites. However, many designers prefer to use full-custom layout (draw polygons for each mask layer), at least for the most critical circuit blocks. Layout quality is a function of the designer's familiarity with the technology and a good knowledge of the circuit's sensitivity to parasitics, device mismatch, etc.

In ASIC design layout is always followed by a series of verification checks, since the time scale for correcting a mask error is long. Depending on the methodology used, these checks can include automatic extraction of the components and their connectivity, extraction of parasitics, and checking for design rule violations. It is essential to re-simulate circuit blocks after parasitics have been back-annotated into the netlist. For large designs, full-chip resimulation can consume many CPU-hours or days and requires careful planning.

The ASIC is required to perform in the presence of process, supply voltage, and temperature variations. Process variations have components that include run-to-run, chip-to-chip, chip-level gradients, and local mismatching. The user has to decide how critical it is to set up and run statistical simulations covering all expected variations and combinations. A common practice in digital design is to use "corner" simulations for global process, temperature, and supply variations. Here the combinations are typically selected to produce the fastest/fastest, slowest/slowest, fastest/slowest, and slowest/fastest NMOS/PMOS responses respectively, to reveal timing paths that will fail at the extremes; if all corners meet performance requirements the circuit is judged to be sufficiently robust. For analog design a Monte Carlo approach may be chosen, in which each transistor's parameters are drawn from global and local distributions. Simulation is repeated for many realizations and performance variations measured. This method can provide an estimate of chip parametric yield if the process model is accurate.

Slide 9

The advent of shared multiproject fabrication services in the 1980's served to bring ASIC design to a wider user community. In this model users are provided with process design kits (PDK) from the foundry, generate mask-level designs that pass physical design rule checks, and purchase a share of a manufacturing wafer run. The foundry (or an affiliated broker) aggregates the designs from 10 - 60 users into a single reticle. Users get a limited number of die (which may be packaged) and a guarantee that the process run was within nominal limits, at low cost compared to a dedicated run. Of course, user groups can and do collaborate to create their own multi-project reticles. Turnaround time is typically three months from run closing to packaged, delivered parts.

Multiproject runs (sometimes called shuttle services) are valuable for finding design errors, evaluating or comparing circuit concepts, estimating performance variability, and even for limited quantity production. Since the cost of fabrication is dominated by the mask cost, additional wafers from a MPW run may be purchased at a small fraction of the initial run cost. It can be economical to produce up to 1,000 samples per MPW run.

A useful strategy is to include test structures or circuits with extra diagnostic features in the first iteration of a new design, to speed testing or fine-tune performance.

Slide 19

Many interrelated factors enter in to the design of an MOS charge amplifier. The relevant detector parameters are the capacitance, leakage current, and charge collection time. The experiment dictates the time and amplitude distribution of events. Typically natural sources have Poisson-distributed arrival times characterized by an average rate, while accelerator sources may have a well-defined time structure. The experiment also sets the acceptable limits for noise, linearity, and maximum signal. A very important, but frequently overlooked system constraint is the power budget for the front-end ASIC.

The designer must choose an appropriate MOS technology from the many varieties offered by today’s foundries. The input device characteristics (NMOS/PMOS, gate

dimensions, and bias condition) play the largest role in determining the ENC, and this is where the most careful optimization must take place. The relative allocation of the power budget to the input device and the rest of the circuit is also involved in this decision. As we will see, there are many options for the reset system (low-frequency circuit to discharge the feedback capacitor). Finally the shaper impulse response sets the weighting function for noise and can be tailored to handle the anticipated event rate of the experiment.

Slide 20

Recall that most radiation detectors behave as high-impedance capacitive sources. The ideal integrator is composed of an inverting voltage amplifier and capacitor in feedback. To maintain the input node at virtual ground the output will slew to a voltage $V_0 = -Q_i/C_f$ in response to a current pulse at the input. If the loop gain of the amplifier is sufficiently high the integrator gain V_0/Q_i will be $1/C_f$, independent of detector and amplifier properties.

Slide 22

As shown in the first lecture, the noise sources can be divided into serial (red), parallel (green), and 1/f (blue) components having $t_m^{-1/2}$, t_m^{0}, and $t_m^{1/2}$ dependence on measurement time respectively. If shaping time is a free parameter, there is an optimum where series and parallel noise are equal:

$t_{opt} = C_{det}\sqrt{R_P R_S}$

where R_P and R_S are the equivalent parallel and white series noise resistances,

$R_S = e_n^2/4kT$

$R_P = 4kT/i_n^2$

If power is unconstrained, the equivalent series noise resistance R_S can be reduced by increasing the bias current in the input FET. Parallel noise is not inherent to the amplification process and can be minimized or eliminated in many cases. The ultimate limit to the noise performance of an MOS charge amplifier is the 1/f noise of the technology.

Normally the measurement time is not a free parameter but is constrained by pileup, timing precision requirement, or ballistic deficit due to finite charge collection time.

Slide 24

Considering for the moment only the series white noise component, it is clear that the input MOSFET width has an optimum. This is because both the transconductance and gate capacitance of the FET increase as width is increased. The former leads to a reduction in noise spectral density of the FET, while the latter increases the effective input capacitance of the detector + front end.

Both C_{gs} and g_m depend on the technology (gate oxide thickness), physical gate dimensions (width and length) and the bias conditions (drain current density, degree of inversion). In discrete designs the effective width of the FET is normally changed by introducing one or more devices in parallel, keeping each one at the same drain current. In that case the white series noise is minimized when the combined transistor gate capacitance is equal to the detector capacitance. In custom integrated circuits with power constrained, the drain current budget is fixed and the device width is changed directly. This case leads to an optimum at $C_{gs} = C_{det}/3$ when the device is operated in strong inversion.

The 1/f noise coefficient K_F is more or less independent of bias condition. Therefore the optimum device size for 1/f noise is easily found to be $C_{gs} = C_{det}$.

Slide 25

When we combine the white and 1/f noise components we can't get a clean analytic solution to the optimization. We find the solution numerically by summing in quadrature the white, 1/f, and parallel noise contributions to the ENC. Here is an example
The 1/f match at C_{gs}/C_{det}=1 as always. The white match is at about C_{gs}/C_{det}=0.25, which means the device is just at the weak-strong inversion boundary. The overall optimum is

about 0.7. Note also that the minima are fairly broad. An error by a factor of 2 either way would result in about a 12% increase in noise.

Slide 26

The relationships between device width, drain current, transconductance, capacitance, and noise source spectral density depend on the region of operation. As seen in the second lecture the most advanced CMOS processes favor device operation in the moderate inversion region (low current density). Moderate inversion is even more prevalent in charge amplifier input transistors because they must match (within a factor of ~5) the capacitance of the detector. Detector capacitance is always at least 100 times larger than the capacitance of a minimum-sized transistor in modern processes. The correspondingly large device width together with the low drain current allowed by power dissipation constraints results in a low current density, low inversion coefficient region of operation. Because of this neither the first-order weak nor strong inversion models provide good approximations of device noise behavior.

Slide 27

Analytic expressions for MOSFET behavior in moderate inversion have been lacking until the mid-90's when the "EKV" model was introduced. This new model, which is slowly making its way into engineering textbooks and circuit simulators, has simple expressions that are valid for the entire range of operating conditions from weak to strong inversion. Hence it is particularly useful for analog design in modern submicron processes, where the favored operating point often places the device in moderate inversion. The EKV model makes use of the inversion coefficient i, which is a measure of drain current normalized in such a way that $i \ll 1$, $i \gg 1$ represent weak and strong inversion respectively.

Using the EKV expressions for transconductance, capacitance, and noise spectral density allows the ENC to be optimized without resorting to full analog simulation and without need for a detailed transistor model from the foundry. Since the EKV parameters are

simple and physics-based, it is also possible to predict noise performance for future scaled technologies.

Slide 28

This series of graphs shows the transconductance of NMOS and PMOS devices as a function of gate capacitance. As the device is made wider (higher C_G) at constant drain current it goes from strong to weak inversion. In strong inversion $g_m \sim C_G^{1/2}$, while in weak inversion g_m becomes independent of device size. The weak-strong transition occurs earlier for smaller feature-size technologies, and for lower currents. In strong inversion, the NMOS device has higher g_m/C_G ratio than PMOS due to the higher mobility of electrons compared to holes.

Slide 29

Series white noise has a minimum due to the competing effects of gate capacitance and transconductance as a function of gate width. Higher drain current (more power) and smaller technology feature size lead to lower noise levels. Strong inversion conditions (large I_D/C_G ratio) give rise to a minimum at $C_G \sim C_D/3$, while in moderate and weak inversion the minimum is at smaller values of gate width.

Slide 30

The next 2 slides show some noise and matching trends for the composite series noise. Slide 25 shows the fully optimized noise for 0.5μm gate length NMOS and PMOS transistors as a function of detector capacitance. NMOS results are for a shaper peaking time of 50 ns, while PMOS is optimized for 5 microsecond peaking. Noise (solid lines) and capacitive match (dotted) are shown for three power levels in the input device. When detector capacitance is large and drain current is low, the optimized input device tends to operate in moderate inversion; under these conditions the optimized gate capacitance can be as small as 1% of the detector capacitance.

Slide 31

This figure shows the fully optimized noise as a function of power dissipation for 0.25micron CMOS technology for a 1 pF detector capacitance. Shaper peaking times from 10ns to 3μs are shown.

At short peaking time and low power the series white noise dominates and the corresponding optimum ENC decreases roughly as $P^{-0.4}$. As power (and/or shaping time) increase, the 1/f noise component becomes increasingly important and the slope *dENC/dP* flattens. In this example, an ENC of around 12 e- is the minimum possible for this combination of CMOS technology and detector capacitance.

Slide 32

In the preceding analysis the gate capacitance was modeled as a single, bias-independent value directly proportional to the active gate area. A more accurate model reflects the bias dependence of the intrinsic gate capacitance, and the fact that the gate-source and gate-drain overlap capacitances contribute to the total input capacitance in parallel with C_{det}. C_{GSO} and C_{GDO} depend only on the device width (not area) and are bias-independent. However, these parasitic capacitances do not influence the 1/f noise.

It is found empirically that for some technologies the 1/f noise coefficient K_F increases for the shortest gate lengths, and that the frequency dependence is $f^{-\alpha}$ where α is in the range 0.85 to 1.1. This behavior influences the choice of gate length and the peaking time dependence of the noise. See the reference for details:

G. De Geronimo, P. O'Connor, "MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers", IEEE Trans. Nucl. Sci. 52(6), 3223-3232 (Dec. 2005).

Slide 33

The choice of NMOS/PMOS input device is influenced not only by reaching the minimum ENC, but also by practical concerns of signal swing and voltage headroom, signal return path, and off-chip interfacing. NMOS devices will have lower noise only for operating points far into strong inversion and at short peaking times where the white series noise is strongly dominant over 1/f. For the lowest-noise configurations, e.g. small C_{det}, high power budget, and long shaping time, PMOS will have an advantage over NMOS due to its lower 1/f noise coefficient.

Slide 34

These expressions are same as those given in the first lecture save for numerical constants which depend only on weighting function integrals.

Using these expressions one can crudely determine if the noise will be dominated by the white or 1/f series contribution.

Recall kT/K_F typically ~ 3000 for NMOS, 10,000 – 30,000 for PMOS. When $t_m < 1000\ t_{el}$ the amplifier noise is white series noise limited.

These rules of thumb can also help with the selection of NMOS/PMOS.

Summary – charge amplifier input transistor optimization

From slides 22 - 34 it should be apparent that many interrelated factors influence the design of an optimized charge amplifier input transistor. In particular, recognize that every combination of detector, shaping time, power dissipation limit, and CMOS technology requires re-optimization to achieve the lowest noise. For this reason it is usually the case that ASIC charge amplifiers are custom-designed for every experiment. The quick pace of CMOS technology scaling also means that every few years another technology family becomes obsolete. Since amplifier designs from older technologies are not readily portable to new generations, the initial fabrication run of parts must be sized to cover the lifetime needs for a particular experiment.

Slide 35

R_{eq} expressions can be derived by breaking the long gate finger up into infinitesimal transistors in parallel with their drain currents summed.
It doesn't take into account any time-varying transmission of signal down the gate, which is important for microwave applications.

Slide 36

Applies to any noise source originating in the bulk -- like coupled digital noise. Noise is flat with frequency up to pole from $C_{gate\text{-}channel}*R_{sub}$ (in reality, the bulk resistor and gate-channel capacitor form a distributed RC line). Therefore this noise is superimposed with white channel thermal noise and can masquerade as high gamma. It is more significant at shorter gate length, since it depends on g_{mb}^2 whereas the channel thermal noise depends only on g_m.

Slide 37

It is important during layout of the input device to prevent the introduction of parasitic resistances in the gate polysilicon and from the bulk. One typically computes the maximum allowable gate finger width and the maximum distance from active transistor area to nearest substrate contact. Then the input transistor is subdivided into cells which obey the resistance constraints, tied together in parallel with low-resistance metal wiring. To prevent pickup of induced currents flowing in the substrate, one or multiple guard rings surrounding the input transistor are advisable.

Slide 38

Practical integrators need some method to discharge the feedback capacitor between events. In classical discrete designs a high-value resistor performed this function, giving excellent linearity and low parallel noise contribution. However, another solution must be

found in monolithic circuits where the highest generally-available materials have sheet resistances lower than 200 Ohms/square, making resistors with R>100kOhm impractical. For high-precision circuits the reset system must be linear and low-noise over a wide signal range. It should also be insensitive to process/temperature/supply voltage variation, and should not add parasitic capacitance to the input node.

In addition to resetting the feedback capacitor, it is an important advantage if the reset circuit can supply (or sink) the DC leakage current of the detector, thereby allowing direct coupling of detector to preamp without bulky DC-blocking capacitors.

Slide 39

Physical resistors in a monolithic process are polysilicon or metal meanders and form a distributed RC line with their associated parasitic capacitance to the conductive substrate. Although their DC resistance can be made arbitrarily high by increasing the line length, the noise properties are determined by the real part of the input impedance (frequency-dependent). Hence their parallel noise contribution will be higher than the classical Johnson noise $4kT/R$ whenever the measurement time is less than the RC time constant of the line.

A MOS switch can be used to reset the feedback capacitor in some applications. In the OFF state the switch contributes negligibly to the parallel noise, as leakage currents are usually in the pA region at room temperature. For low event rates the switch may be maintained in the OFF state up to ~ 1millisec. Immediately after discharge, there will be a transient disturbance which must be allowed to settle before the amplifier can be sensitive again. Also, each reset will leave a noise charge kTC on the feedback capacitor, which can be removed by double sampling the output before and after an event arrives.

Slide 40

Many continuous reset circuits that use active elements have been developed. The first circuit shown in this figure relies on the excellent matching of monolithic devices to create a current amplifier by coupling an imperfect integrator stage with a voltage

amplifier having a transfer function that exactly cancels the nonlinearity of the integrator. This circuit is discussed further in slides 42 - 44.

The second solution uses a low-frequency differential amplifier to maintain the output of the integrator at constant potential V_{ref}. A pulse of charge creates a step at the output of the integrator, and the voltage is returned to V_{ref} with a time constant given by the product of the transconductance of the low-frequency stage and C_f. Since a second feedback loop is present the circuit must be carefully stabilized to prevent oscillation. Thermal noise of the transistors in the low-frequency amplifier contributes to the ENC.

Slide 41

R-scaling circuits utilize an attenuating current mirror to create a circuit element that behaves like a resistor of value $R*N$, where R is a physical resistor and N is the attenuation ratio of the mirror. The voltage at the output of the integrator V_{out} is applied to a voltage-to-current converter producing a current V_{ou}/R, which is then sent to the input via a current mirror with ratio $1/N$. The effective resistance $R*N$ must be $>10^6\Omega$ to be effective as an integrator reset; this sometimes requires difficult mirror ratios to be designed.

The slew-rate limited configuration uses a constant current to discharge the feedback capacitor. This produces a linear, rather than exponential return to baseline and can be used with a discriminator to produce a pulse whose width is linearly proportional to the deposited charge.

Slide 42

The diagrams illustrate the similarity of the self-adaptive current-amplifying configuration to the classical pole-zero compensation circuit used in discrete preamplifier designs. In the frequency domain, a zero is created by R_C*C_C that cancels the pole formed by the integrator feedback elements. The monolithic version relies on matching of capacitors and transistors to create the cancellation. Moreover, the transistor's nonlinearities are canceled because their gates and sources are common, and their drains

connect to virtual grounds at the same potential (inputs of A1 and A2). The overall circuit (A1, CF, MF, CC, and MC) injects a current into A2 which is an N-times scaled replica of the input current from the detector.
Note that the PMOS transistors shown (MF, MC) are appropriate for amplifiers which must respond to ***negative*** input charge. If the detector injects positive conventional current into the amplifier, the reset and compensation transistors must be NMOS.

Slide 43

Experimental results confirm that the nonlinear compensation is effective, and that the amplifier self-adapts to leakage current up to 70 nA with negligible change in gain.

Slide 44

A summary of the advantages and disadvantages of the self-adaptive, nonlinear compensated reset system.

Slide 45

In a properly designed charge amplifier the noise is dominated by the input transistor. However, in low-voltage CMOS processes it is difficult to degenerate the current sources which supply the input and cascode branches. Current source noise is minimized by using long-gate devices, but the lower the W/L ratio, the higher the drain-source voltages needed to operate in saturation.

It is also important to model the response of the charge amplifier to large signals. In some experiments, charge in excess of 10^3 the normal signal charge can be generated in the detector. The preamp's recovery from such overload can be extremely slow. If large overloads are expected the preamp must be designed to recover quickly, for instance by re-dimensioning the reset transistor or by providing a fast reset path that is triggered by saturating signals.

Slide 46

As in any amplifier the noise of the second and subsequent stages, when reported to the input, is attenuated by the gain of prior stages.

Slide 48

The shaping amplifier performs analog processing on the signal from the preamp to minimize the measurement error with respect to noise, and at high counting rates to minimize the effects of pulse overlap or pileup.

Shaping amplifiers whose system parameters do not change with time are referred to as time-invariant. Time-invariant systems are described completely by their impulse response. The impulse response function may be unipolar (always positive with respect to the baseline) or bipolar. Unipolar impulse response is characterized by its peaking time (typically from 1% above baseline to peak), width (1% -- 1%), slope at threshold crossing, and first and second moments. The symmetry of the pulse may be characterized by the ratio of rise to fall times, or peaking time to full 1% width. For bipolar functions the time to zero crossing, time to negative peak, and ratio of positive to negative peaks are also important. Bipolar response generated by a linear system always has zero net area.

Slide 49

If the noise spectral density and input signal waveform are completely known, and if count rate is low enough to avoid pileup, then a matched filter can be constructed mathematically that will lead to minimum noise. However, these conditions are rarely met in practice and the ideal matched filter is usually difficult to realize with practical circuits. Selection of the appropriate shaping function is commonly constrained by rate, charge collection time of the detector, and acceptable level of circuit complexity. Some systems perform digital processing on a waveform sampled just after preamplification. This technique is more flexible in realizing an arbitrary shaping function, but must satisfy Nyquist sampling and quantization noise requirements, which often leads to unacceptable levels of power dissipation.

Slide 50

Simple shaper response functions can be realized by cascades of single-order low and high-pass filters. The higher the order of the filter, the more symmetrical the output waveform.

Slide 51

This slide gives expressions for the transfer function, impulse response, and peaking time of the classical semiGaussian ($CR\text{-}RC^n$, $CR2\text{-}RC^n$) filters of Slide 50.

Slide 52

Ohkawa (NIM 1976) gives a formal derivation of the pole-zero constellations giving the closest approximation to a Gaussian pulse. As in the simple $CR\text{-}RC^n$ filters, higher-order filters give more symmetrical response, compared to the $CR\text{-}RC^n$ real-pole filters, the complex-pole shapers derived by this method have a superior symmetry for the same filter order.

Slide 53

The graph compares the impulse response of a 5th-order complex-pole shaper derived by the Ohkawa method with first- and fourth-order $CR\text{-}RC^n$ filters. The filters are compared at equal 1% widths, as appropriate for a pileup-limited signal chain. Since the more symmetric pulse has smaller derivative everywhere, it's series noise weighting function is superior to the others.

Some circuits for realizing two poles per amplifier are shown in the lower part of the figure.

Slide 54

AC-coupled systems are subject to baseline wander with random pulse input, while DC coupling requires careful baseline stabilization against drift caused by detector leakage, temperature, or supply voltage variation. The low-frequency feedback system achieves good baseline stability and can also be used to equalize the baselines of many chips in a system. Note that this is not the same as the LF feedback loop around the preamp in the type of reset system shown in Fig. 40.

Slide 55

Bipolar pulse shaping automatically takes care of baseline wander and rejects low-frequency disturbances, but is noisier.

Slide 57

With a limited power budget, it is critical to expend as large a fraction as possible on the preamplifier and shaper where it can contribute to reducing the noise. In typical applications, the input to the preamp/shaper has low duty cycle, i.e. low channel occupancy in time.

Off-chip analog I/O can be very costly in terms of power if the simplest output drivers, such as source followers, are used. To avoid wasting power the driver should use Class AB stage where the quiescent current can be much smaller than the maximum source or sink current that can be provided to a load.

System architecture choices can have a large effect on the need to drive analog signals over long lines and should be considered at the beginning of the experiment.

Slides 59 – 67

The information of interest to the experimentalist is contained in the analog pulse waveform at the output of the shaping amplifier. Slides 59 – 75 describe circuits which extract the key features of the waveform, typically pulse height and timing. Analog sampling circuits freeze the voltage from the shaper preparatory to analog-to-digital conversion. They fall into two main classes – sample/hold stages and peak detectors, described in slides 62 - 63. In multichannel systems and waveform recorders the analog sampler is followed by an N:1 analog multiplexer, which allows many sampling cells to share the same A-to-D converter.

Slides 69 – 75

These slides discuss discriminators, used to detect threshold crossings of the shaped waveform. They are used as one-bit A-to-D converters (yes/no decision did an event occur) and the time of threshold crossing may also be relevant. In a conventional leading-edge discriminator with fixed threshold the time of discriminator firing relative to the occurrence of the event will vary depending on the pulse amplitude. Time walk refers to the variation of threshold crossing time with pulse amplitude and can be understood geometrically. Another factor plays a role – the propagation delay through a discriminator depends on the "overdrive" or magnitude of the difference between pulse amplitude and threshold voltage. For small overdrive the propagation delay is longer due to the response of the bistable elements in the circuit; the delay approaches infinity as the overdrive goes to zero. Constant-fraction techniques can minimize the effect of time walk, and a walk correction can also be done offline if the pulse amplitude is recorded.

Discriminators also need built-in hysteresis to avoid firing on noise.

Slides 77 – 84

Analog-to-digital conversion circuits are beyond the scope of this course, but these slides introduce the important converter topologies. The commercial market offers converters with extremely good performance and the need to build A-D conversion into a front-end ASIC needs to be carefully evaluated.

Slides 86 – 94

Time-to-digital converters (TDCs) employ a variety of techniques to provide relative timestamps for events, one of which is usually a discriminator firing triggered by a pulse waveform and the other generally derived from a precise external clock. The conversion can be done by first converting time interval to voltage (by charging a capacitor during the interval), then converting the stored voltage to digital with an ADC (Slide 86). Other techniques use digital circuits and can be broadly divided into two classes: those whose time resolution is based on the minimum gate delay in the process technology, and those achieving sub-gate delay resolution. The first category functions by subdividing a precise external clock into sub-intervals in a tapped delay line (Slide 87). Many innovative schemes for achieving finer resolution than a gate delay have been proposed. In one approach, a chain of pulse-shrinking delay elements is used (Slide 93). Other techniques use the difference between delay chains or oscillators in a vernier approach (Slides 88 - 90). A full discussion of the many recent schemes, the best of which have achieved resolutions better than 2ps rms, is beyond the scope of this course.

High precision time detection requires attention to the front end, which has to be optimized for minimum time jitter due to random noise and the effects of time walk. In addition to minimum time resolution and jitter, the many TDC architectures also differ in their robustness to process, voltage, and temperature variation, in their overall dynamic range, and in their linearity.

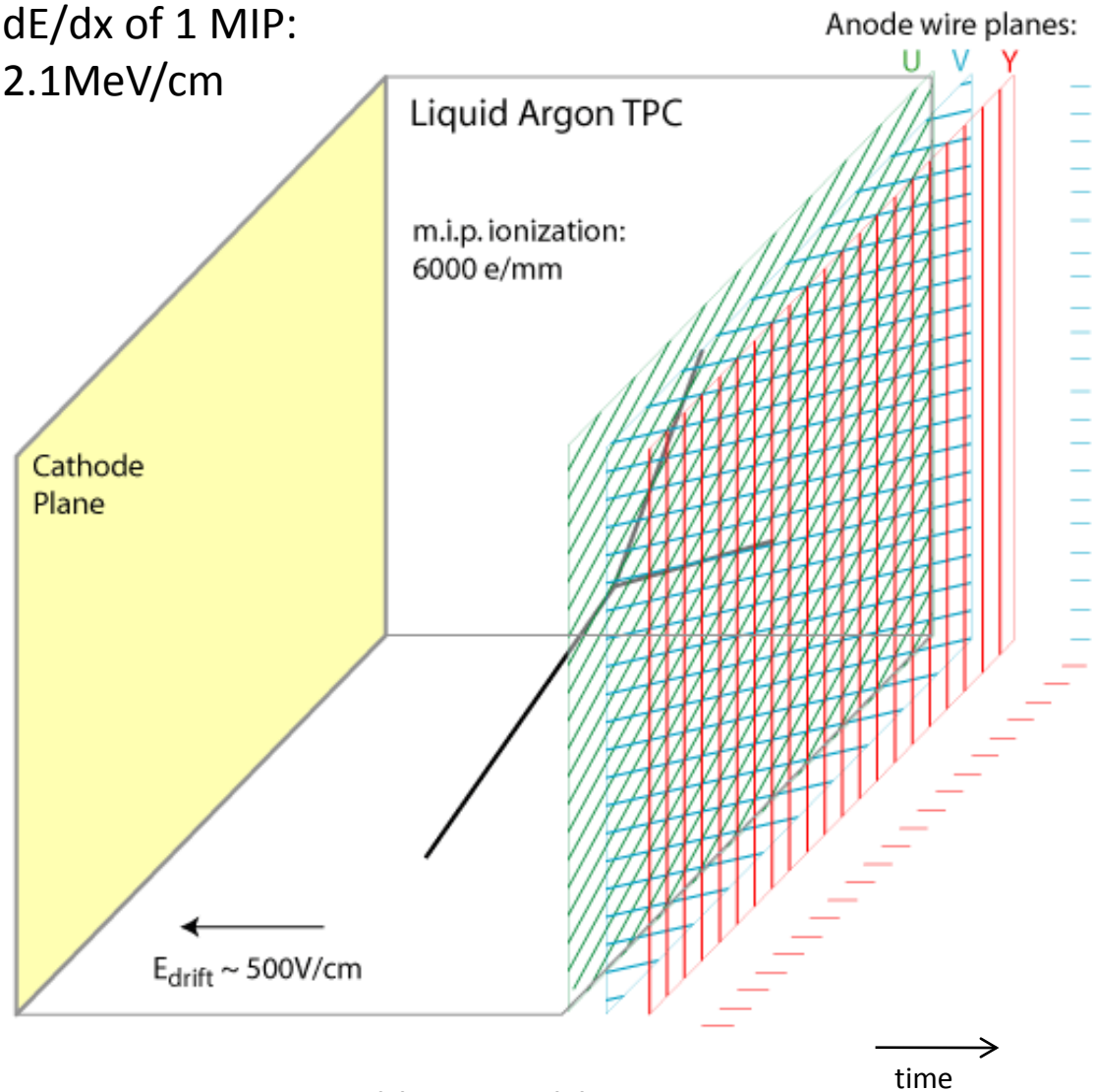
DESIGN EXAMPLES

CMOS at Low Temperature

Veljko Radeka
BNL
radeka@bnl.gov
IEEE NSS
Short Course on Microelectronics, Oct. 27, 2012

How Does a LArTPC Work

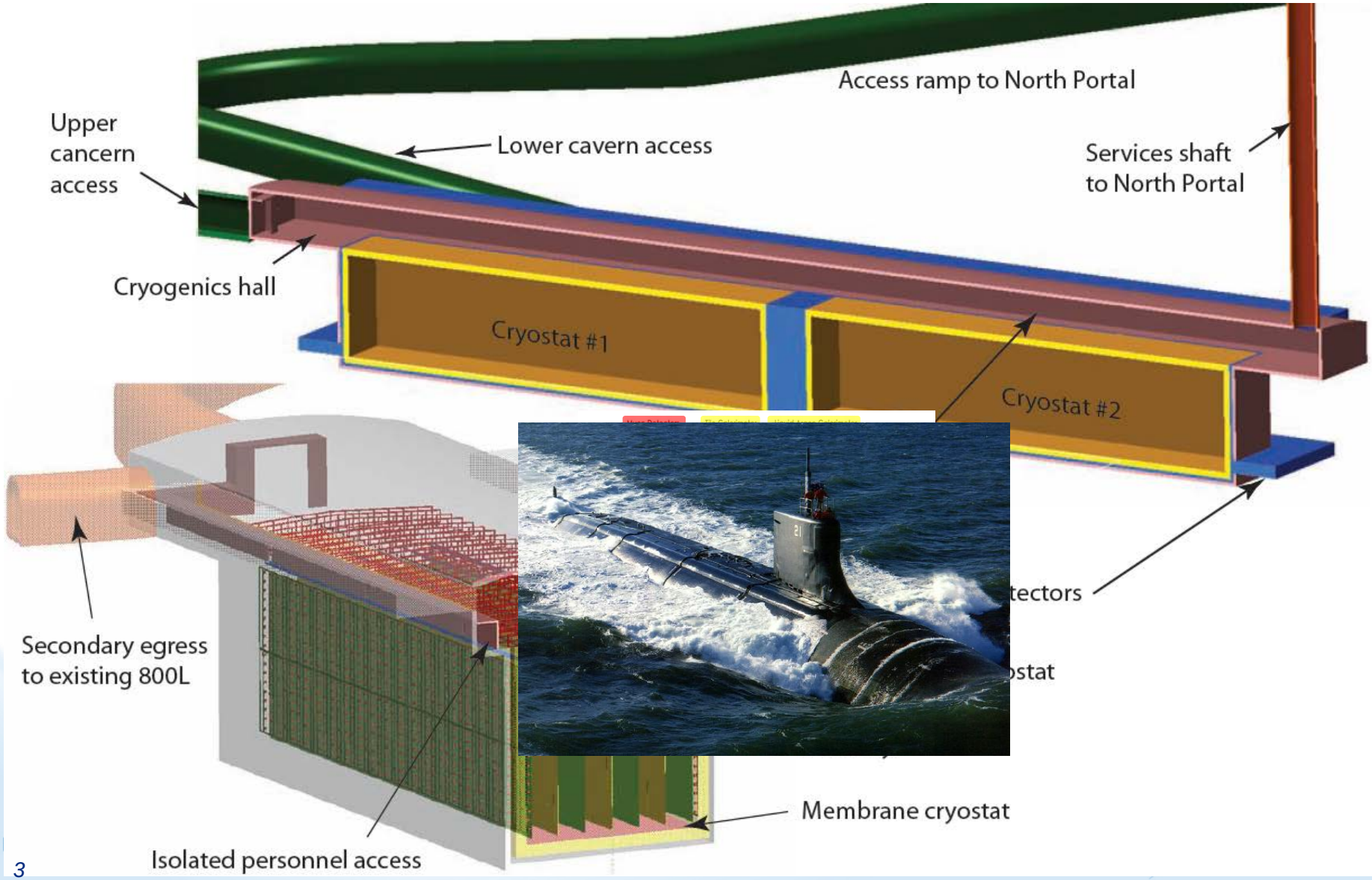
dE/dx of 1 MIP:
2.1MeV/cm



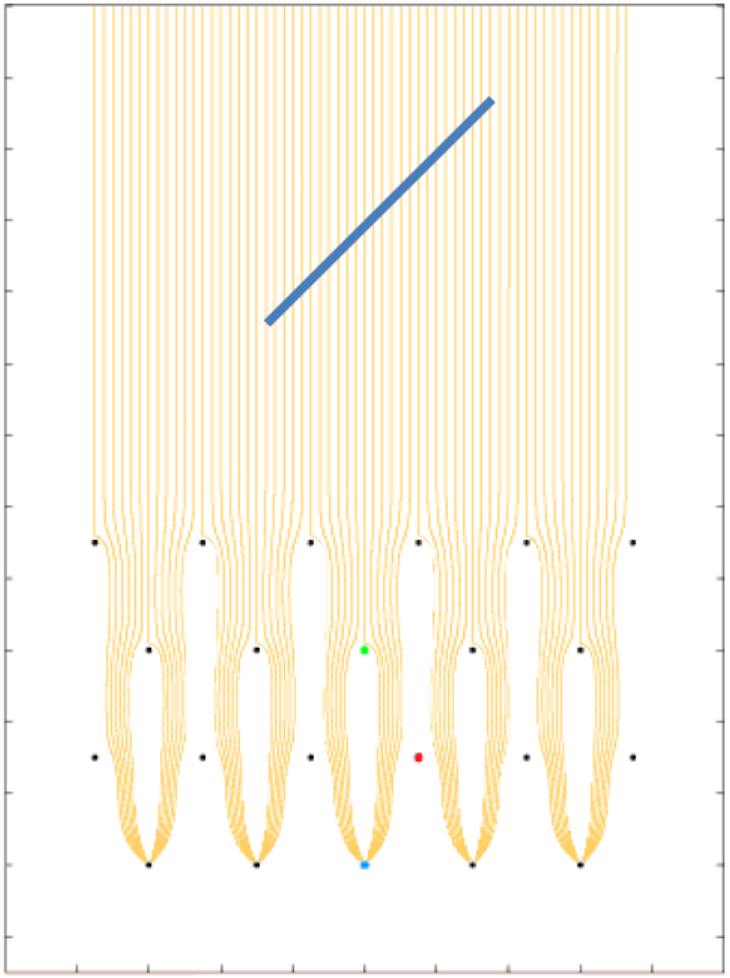
First proposed by C. Rubbia, 1977

- Sense (anode) wires (up to ~ 10m long):
  ~14-**31 kwires/kton**
  - up to **200 pF/wire**
  - collecting (Y)
  - non-collecting (U,V)
- charge sensitivity
  - range ~300 fC
  - ENC < 1,000 e^-
- sample/buffer events
  - ADC 10-12-bit, 1-2 MS/s
  - **3,000 deep buffer**
- **digital multiplexing**
  - **128:1** to1024:1 two-three stages
  - **power constraint**
  - **~ 10 mW** /wire
- operation in LAr
  - **> 30 years**

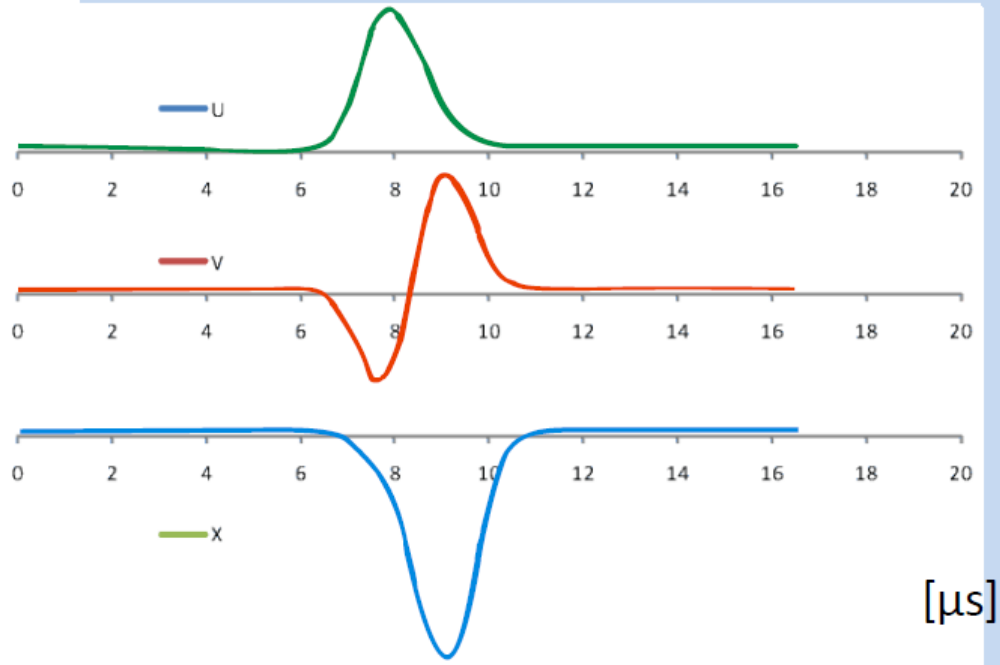
LAr40 Conceptual Design at 800L



Signal Formation on Wire Electrodes in Noble Liquid TPCs: Induced Signals from a Track Segment



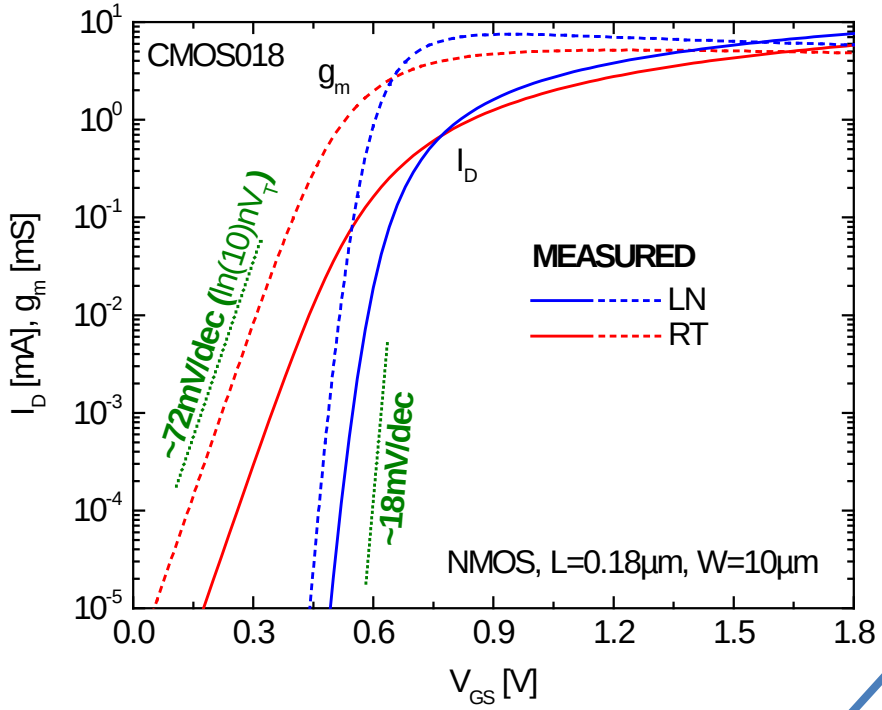
Time scale **is determined by the electron drift velocity and wire plane spacing (3 mm shown)**

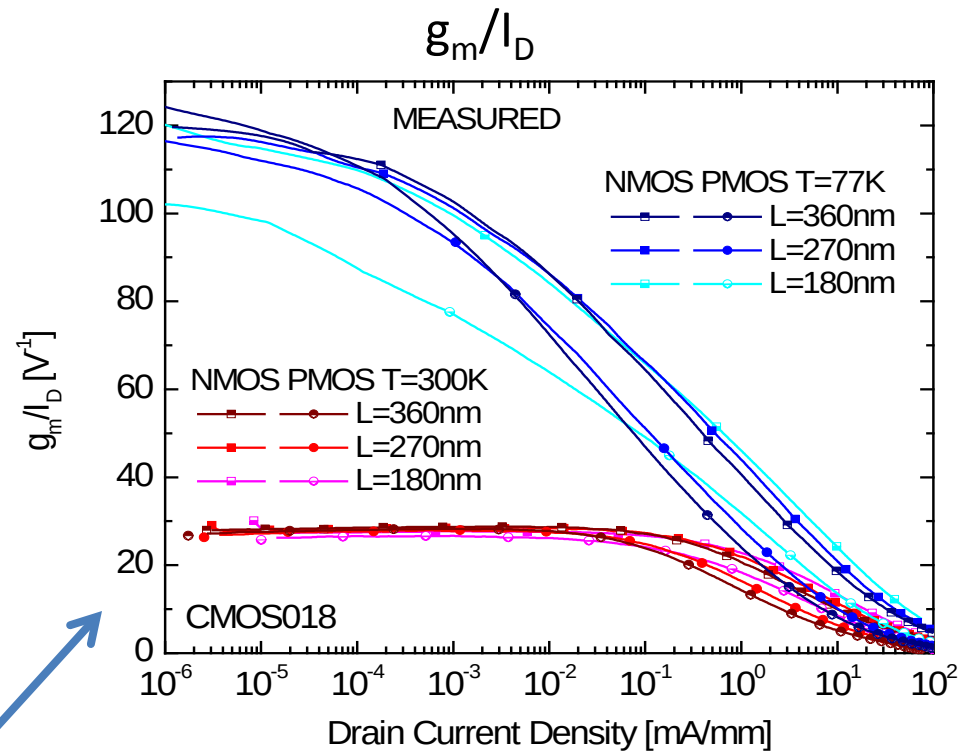


LBNE style wire arrangement: 3 instrumented wire planes + 1 grid plane

Raw current waveforms convolved with a 0.5µs gaussian (~1/2 drift length) to mimic diffusion

CMOS static characteristics vs T

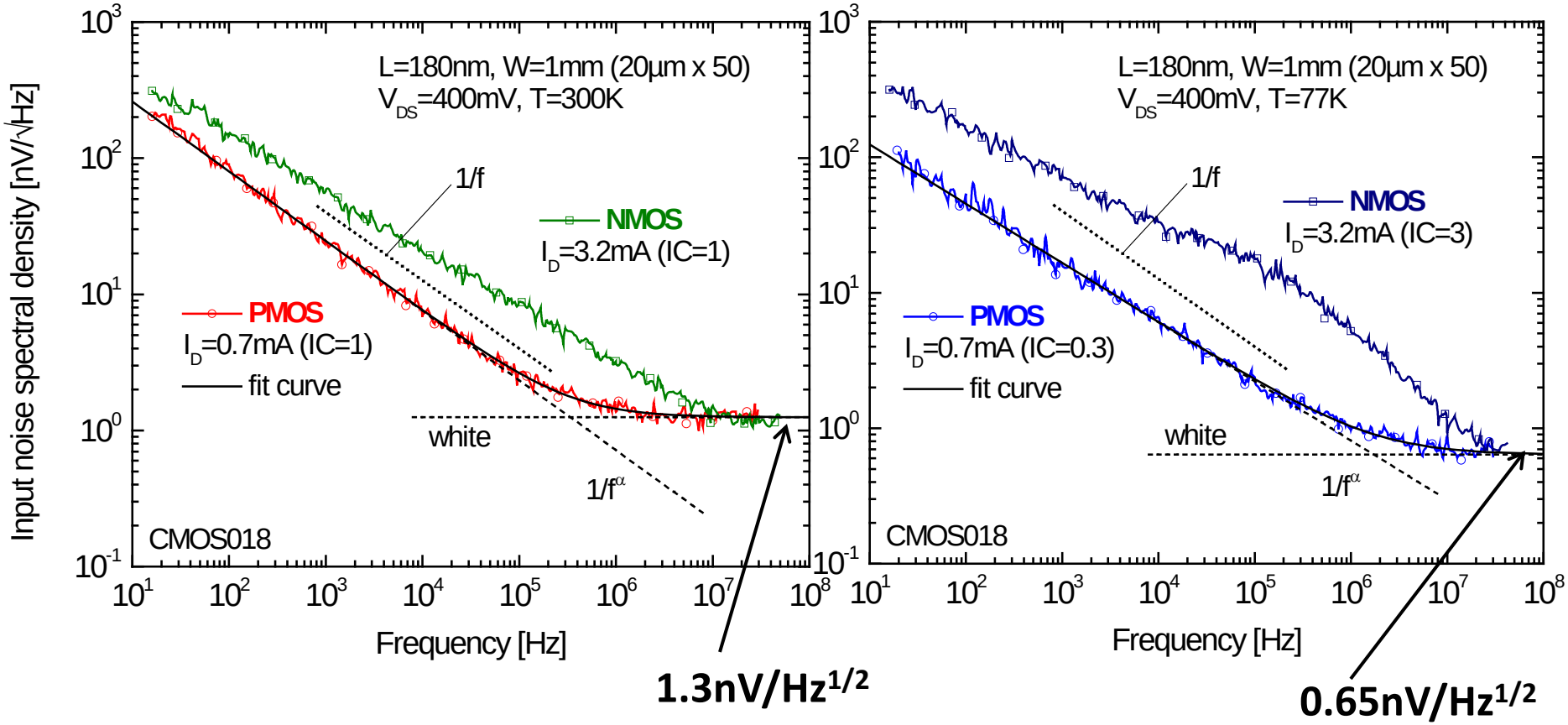




Transconductance/ /drain current ⇒ $\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \;\; at \;\; T = 300K \\ \sim 116 \;\; at \;\; T = 77K \end{cases}$

At 77-89K, charge carrier ***mobility*** in silicon *increases*, ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m ***/I***, ***higher speed*** and ***lower noise***.

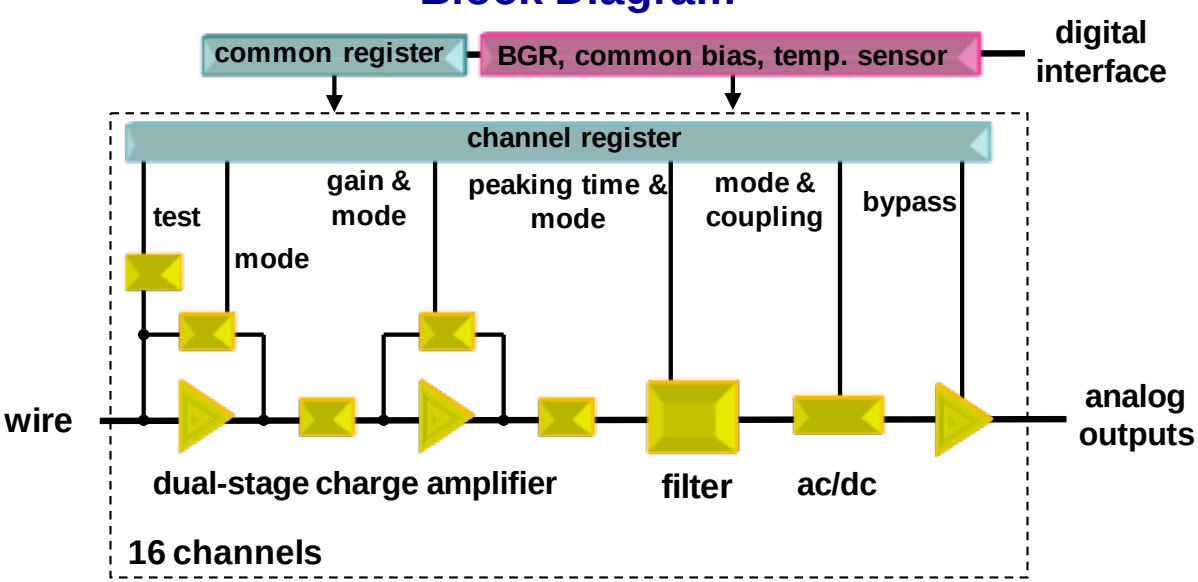
CMOS Noise Spectral Density *vs* T

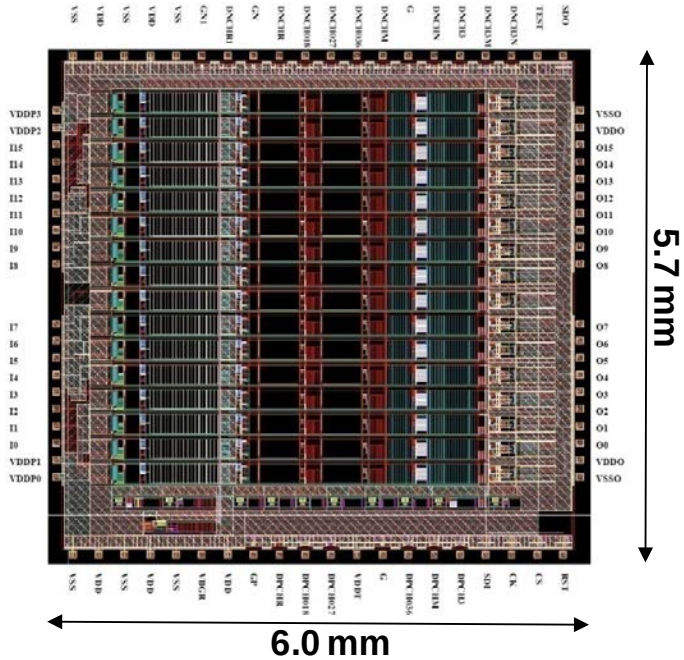


TSMC 180nm: Noise lower by a factor of 2 at 77K across the spectrum for PMOS, only white for NMOS ; (1/f further reduced at longer L)

Analog ASIC

Block Diagram

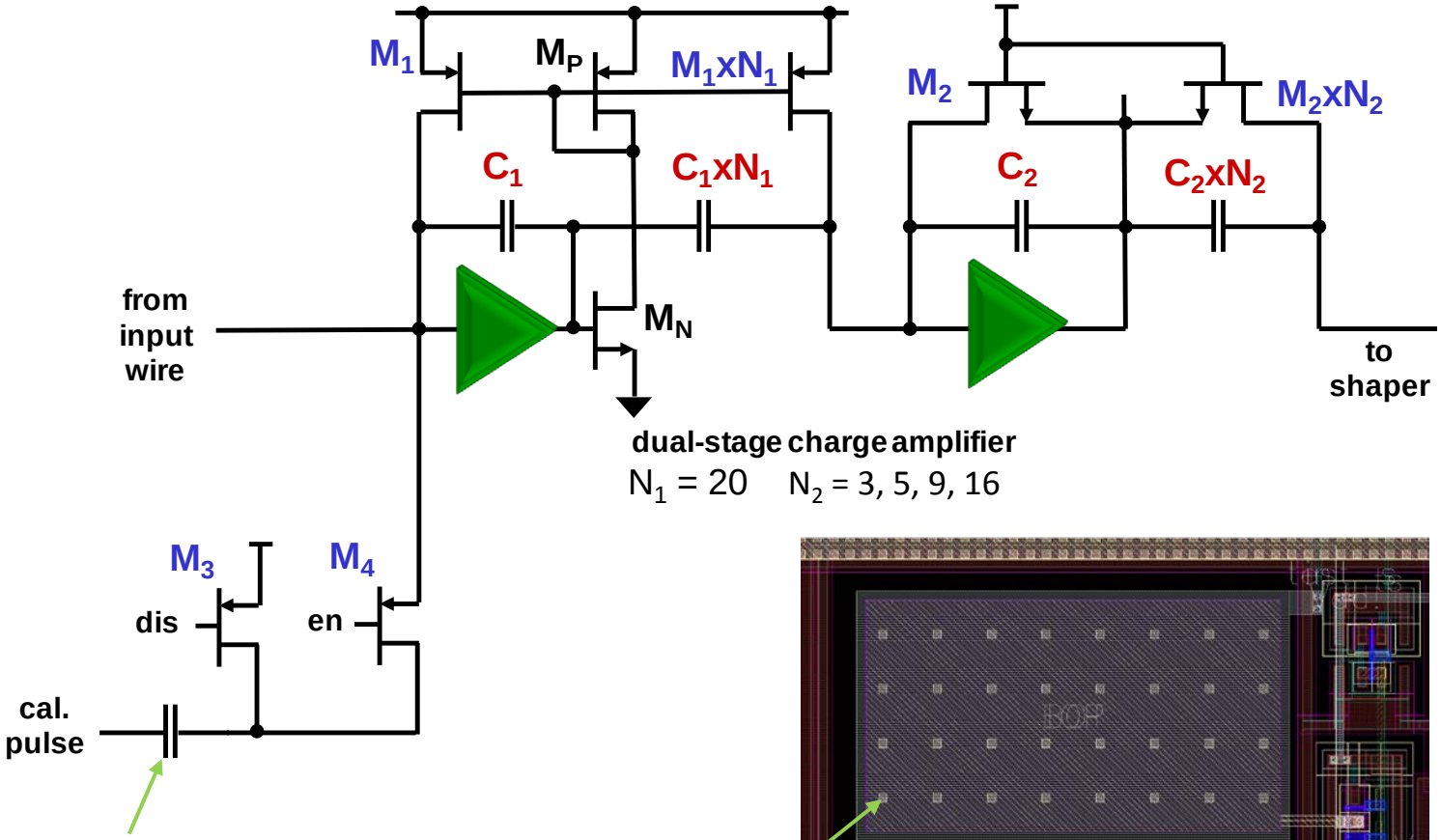




- 16 channels
- charge amplifier, high-order anti-aliasing filter
- programmable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
  programmable filter
  (peaking time 0.5, 1, 2, 3 µs)
- programmable collection/non-collection mode (baseline 200, 800 mV)
- programmable dc/ac coupling (100µs)

- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- **designed for room and cryogenic operation**
- technology CMOS 0.18 µm, 1.8 V

Cold Electronics ASIC - Front-End Detail and Calibration Scheme



$C_{INJ} \approx 180$ fF

Integrated injection capacitance (10 x 18 μm²)

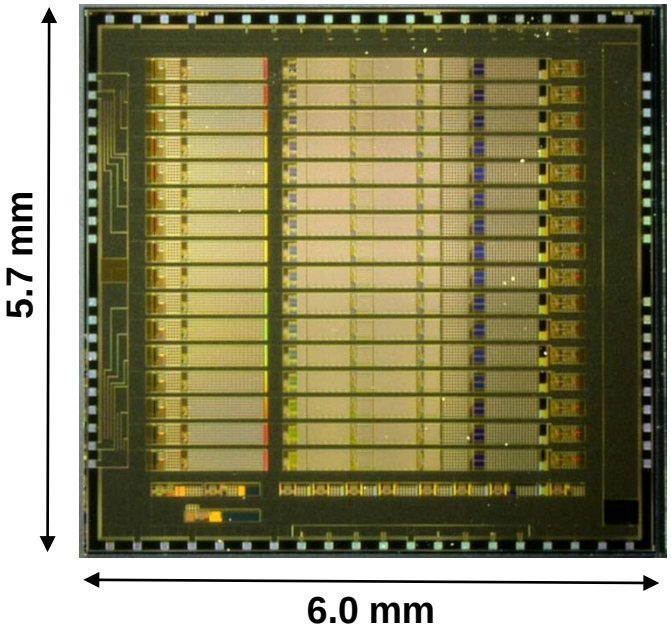
Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184 \ fF \ at \ 300K \\ 183 \ fF \ at \ 77K \end{cases}$$

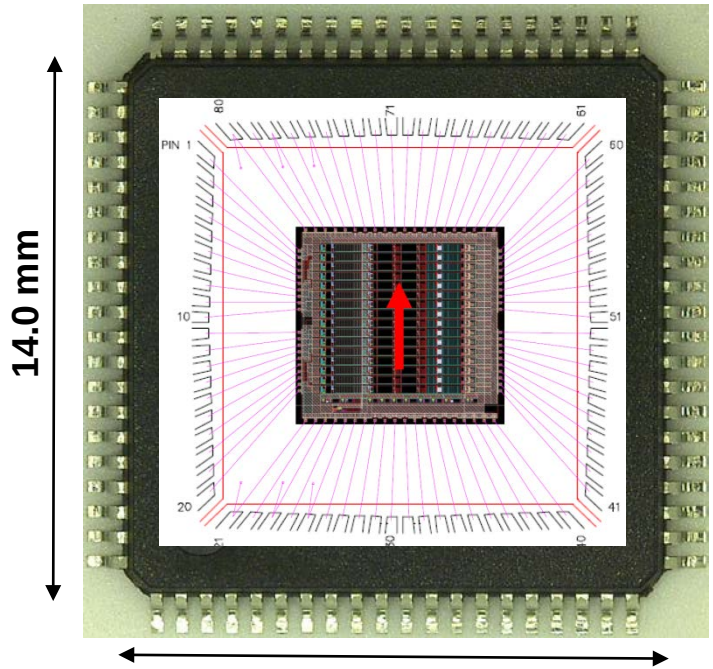
Integrated pulse generators on ASICs ➡ ***Charge sensitivity calibration of entire TPC during assembly, cooling and operation***

Analog ASIC: Die and Packaging, Temperature Cycling

Die Photo

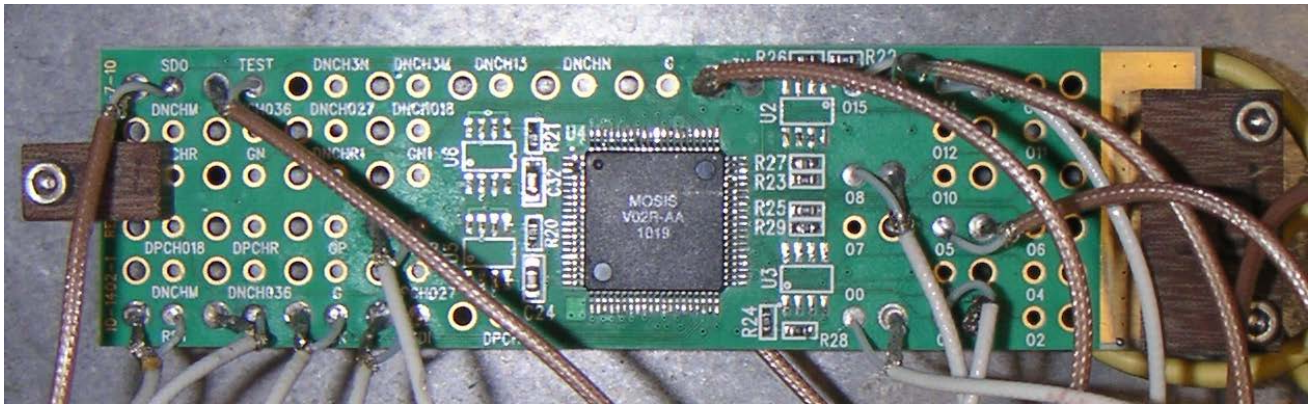


Package Photo



(cavity 10.5 mm)

Test Fixture

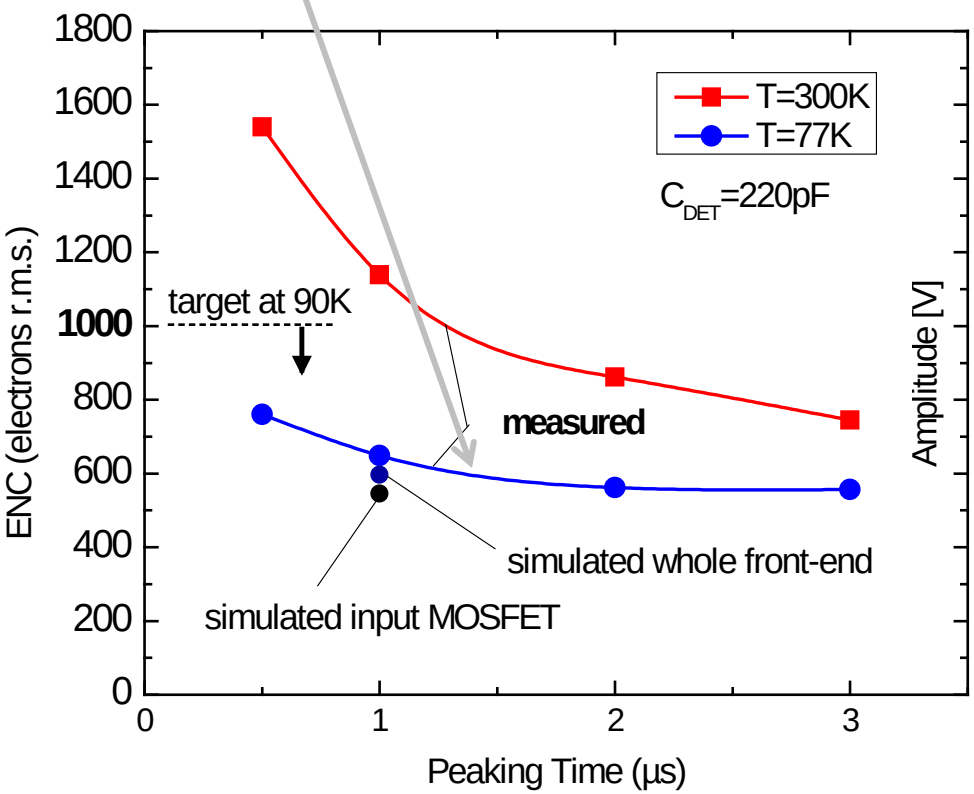


Cycled (abruptly, by pouring LN over the fixture in a dewar) from 300K to 77K more than 30 times

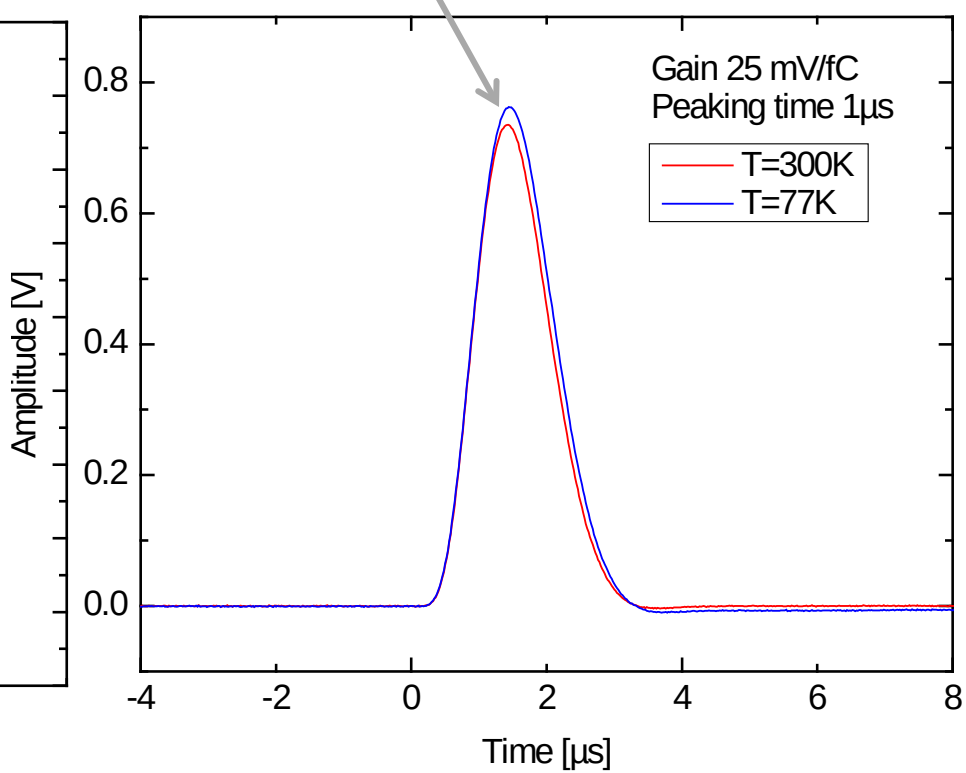
No failure occurred

Cold CMOS: Results from FE ASIC (1st prototype cycle)

Noise gets better at 77K (220pF det. Capacitance):



Signal after preamp+shaper changes little with temperature:



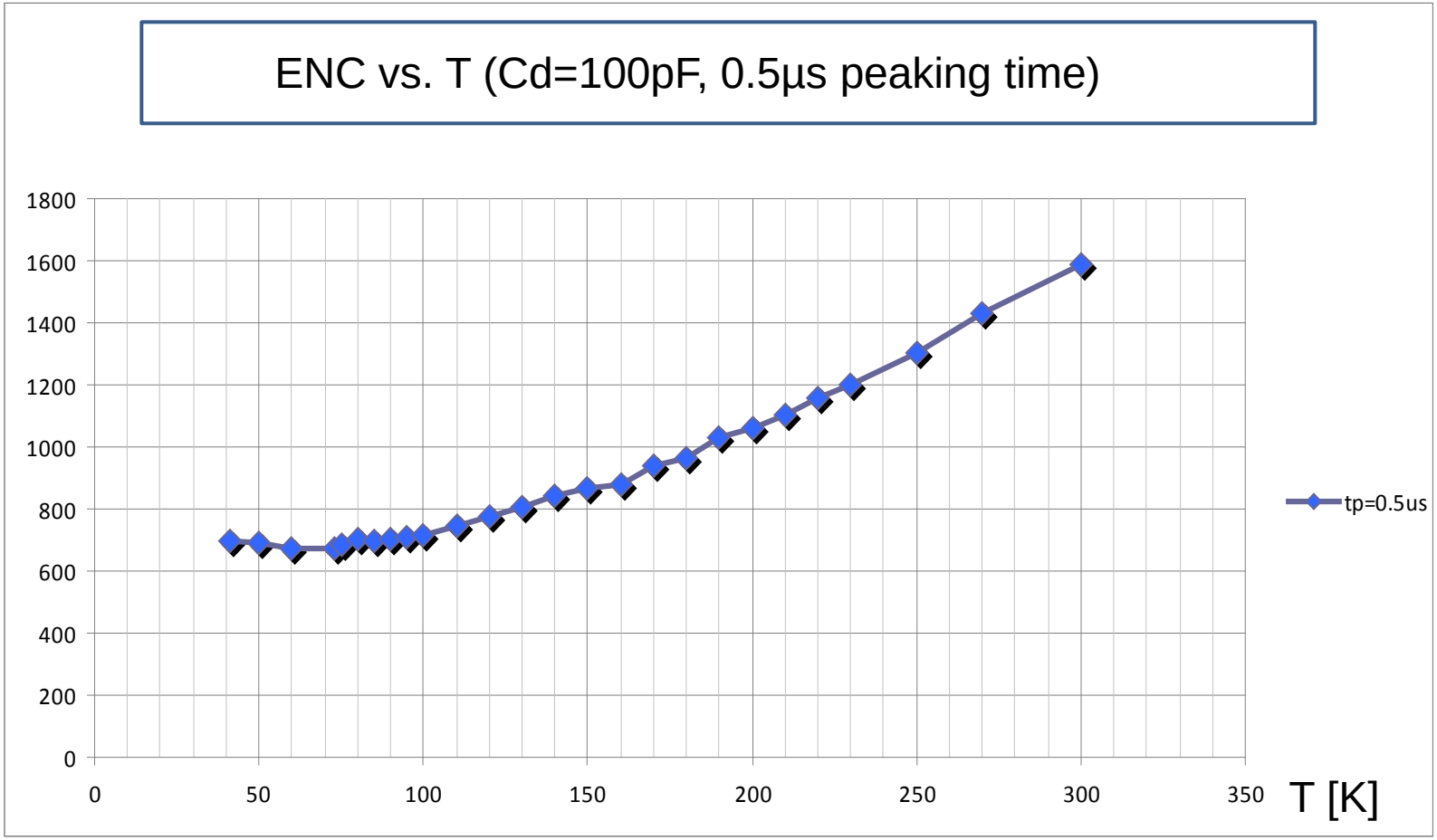
Integrated ***charge calibration*** capacitance
- little change with temperature

Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184\ \text{fF} & \text{at } 300\text{K} \\ 183\ \text{fF} & \text{at } 77\text{K} \end{cases}$$

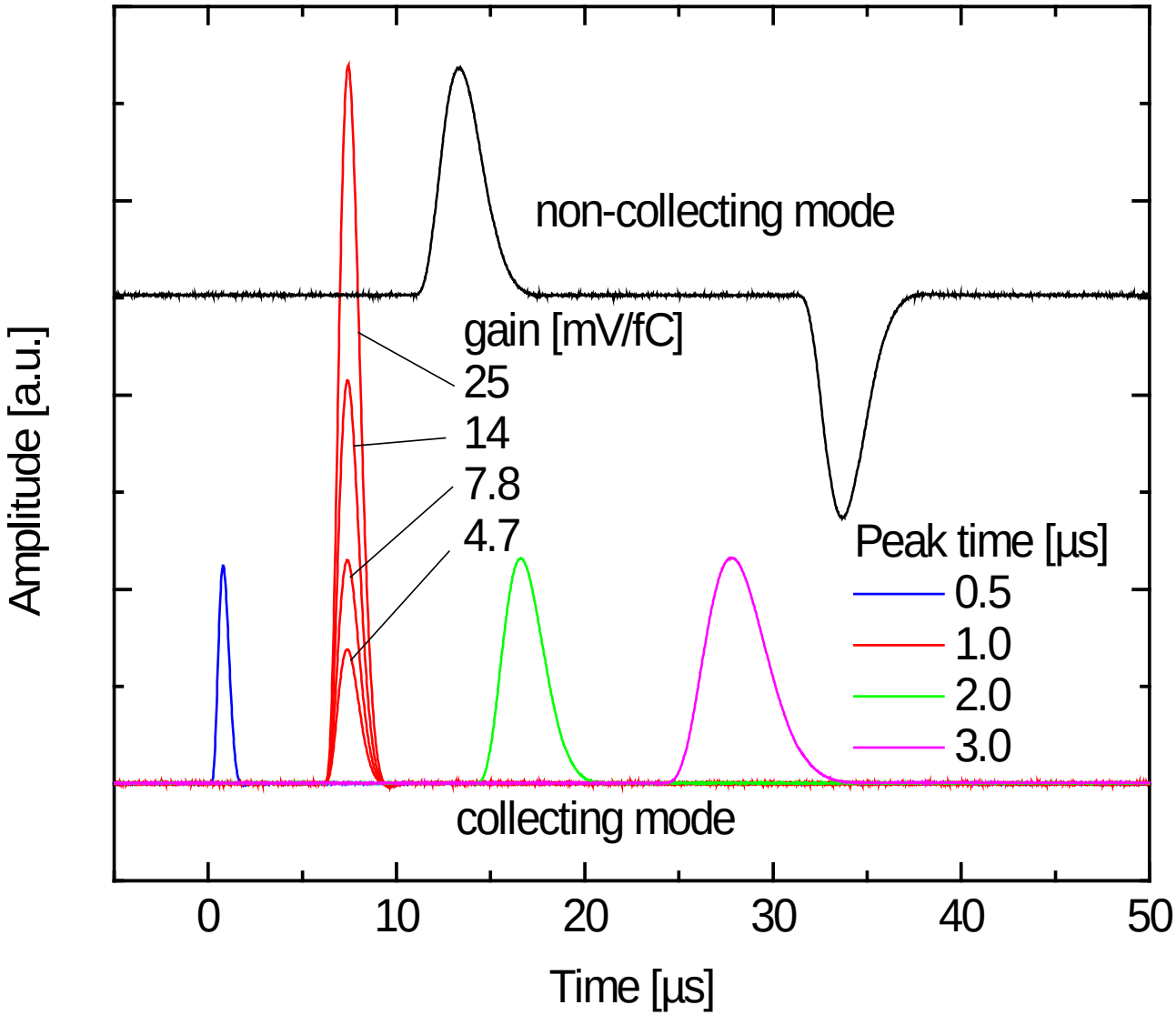
Noise *vs* T in CMOS:

Existing ASIC, 0.25 µm (not designed for Lar)



CMOS in LAr has less than half the (white) noise as that at room temperature, higher mobility and higher transconductance/current ratio

Signal Measurements: programmable gain, peak time and baseline



Bandgap Reference:

$$V_{BGR} \approx \begin{cases} 1.185\ \text{V} & \text{at } 300\ ^\circ\text{K} \\ 1.164\ \text{V} & \text{at } 77\ ^\circ\text{K} \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor:

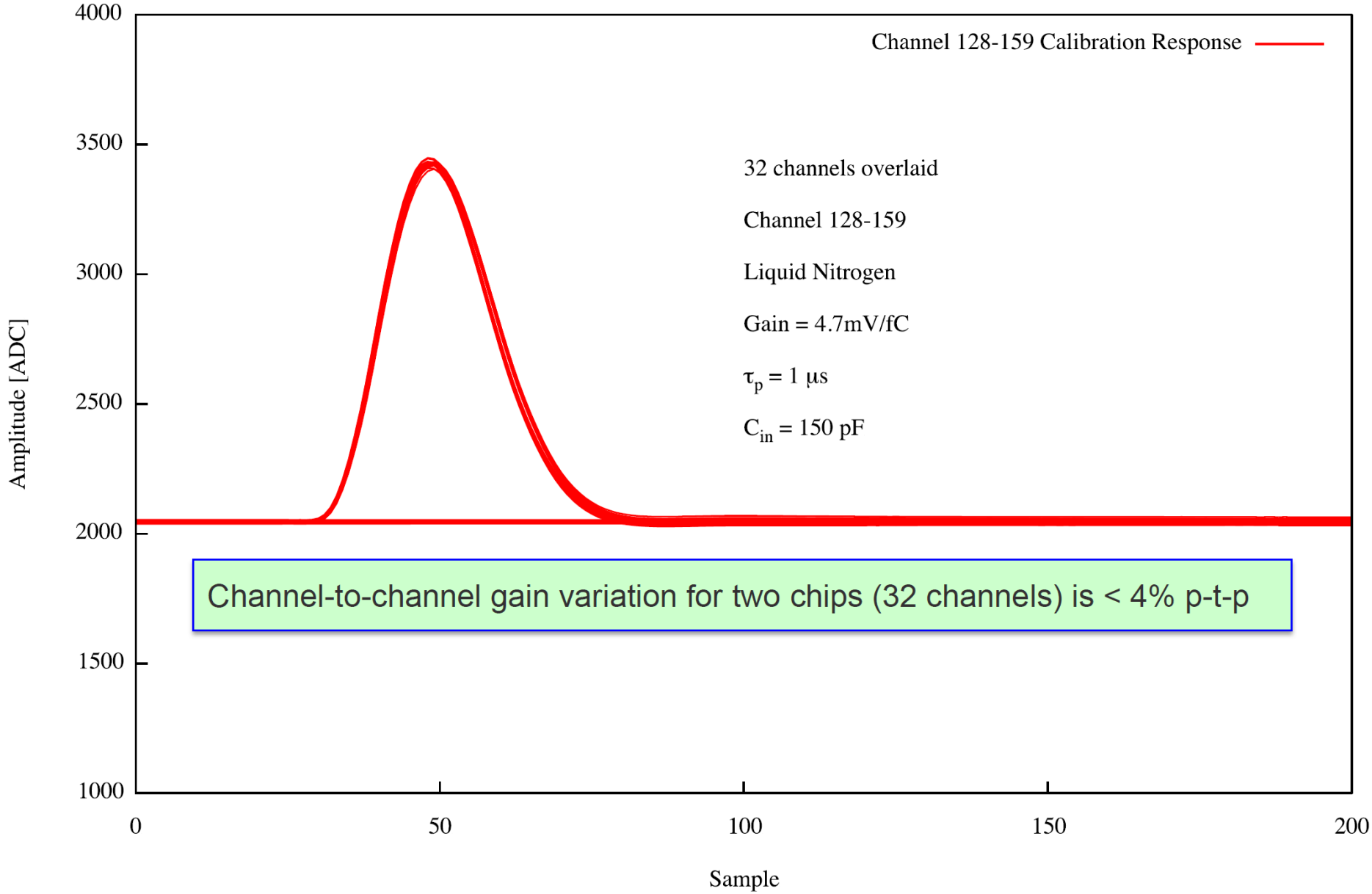
$$V_{TMP} \approx \begin{cases} 867.0\ \text{mV} & \text{at } 300\ ^\circ\text{K} \\ 259.3\ \text{mV} & \text{at } 77\ ^\circ\text{K} \end{cases}$$

~ 2.86 mV / °K

Programmable gain, peaking time and baseline

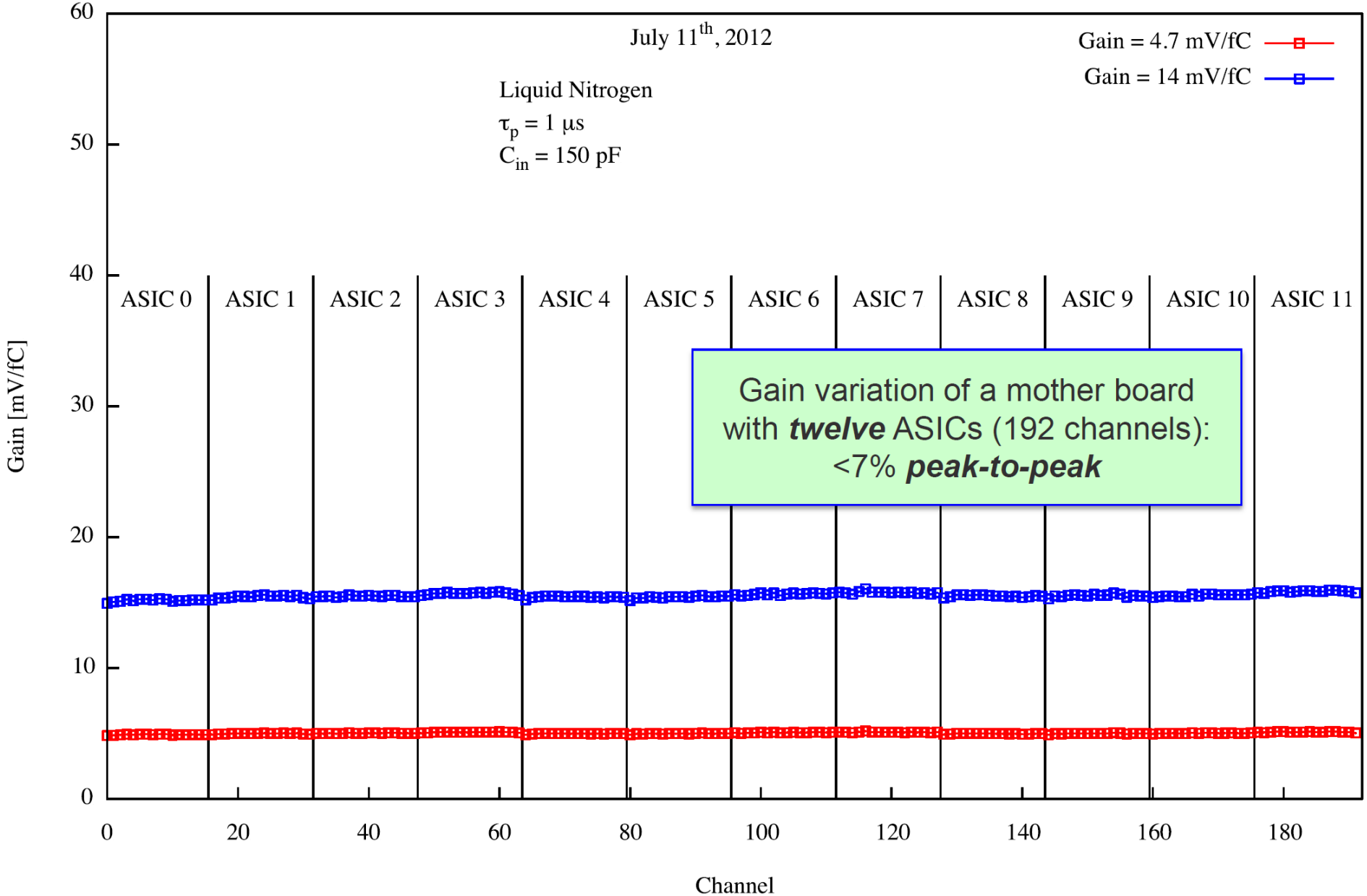
Maximum charge 55, 100, 180, 300 fC

Calibration Response in LN_2

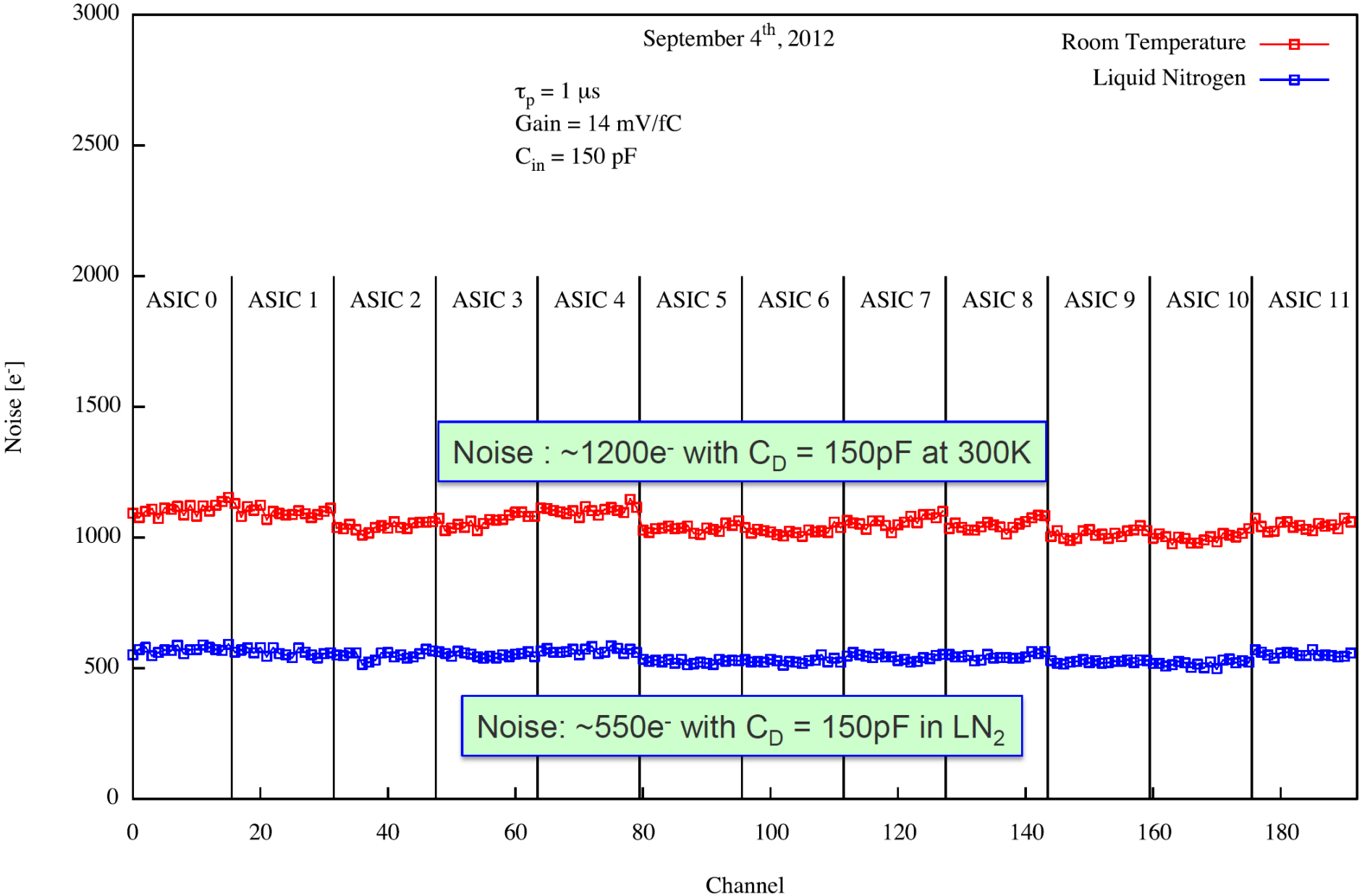


Channel-to-channel gain variation for two chips (32 channels) is < 4% p-t-p

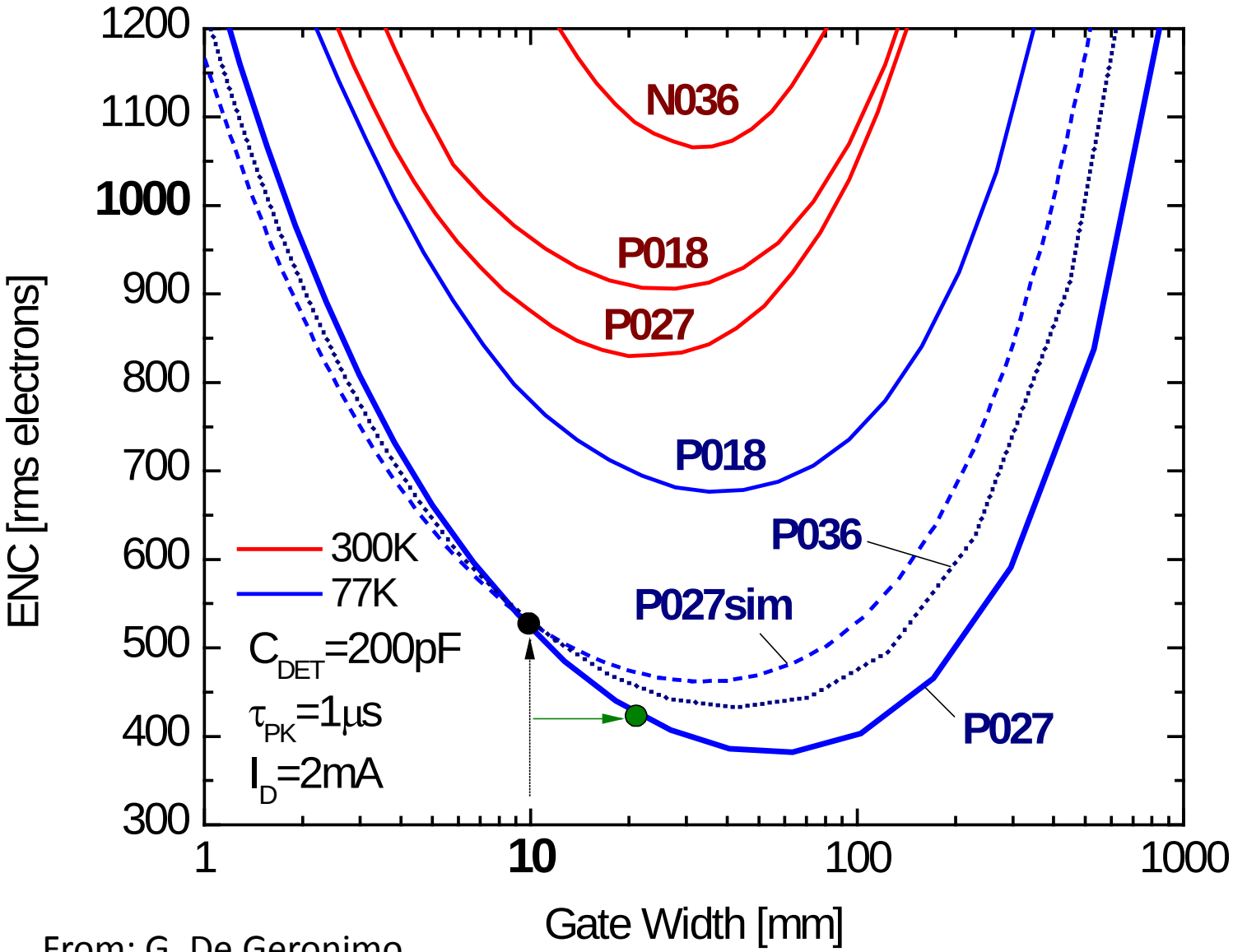
Gain uniformity for 12 ASICs (192 channels)



Noise at 300K and 77K for 12 ASICs (192 channels)

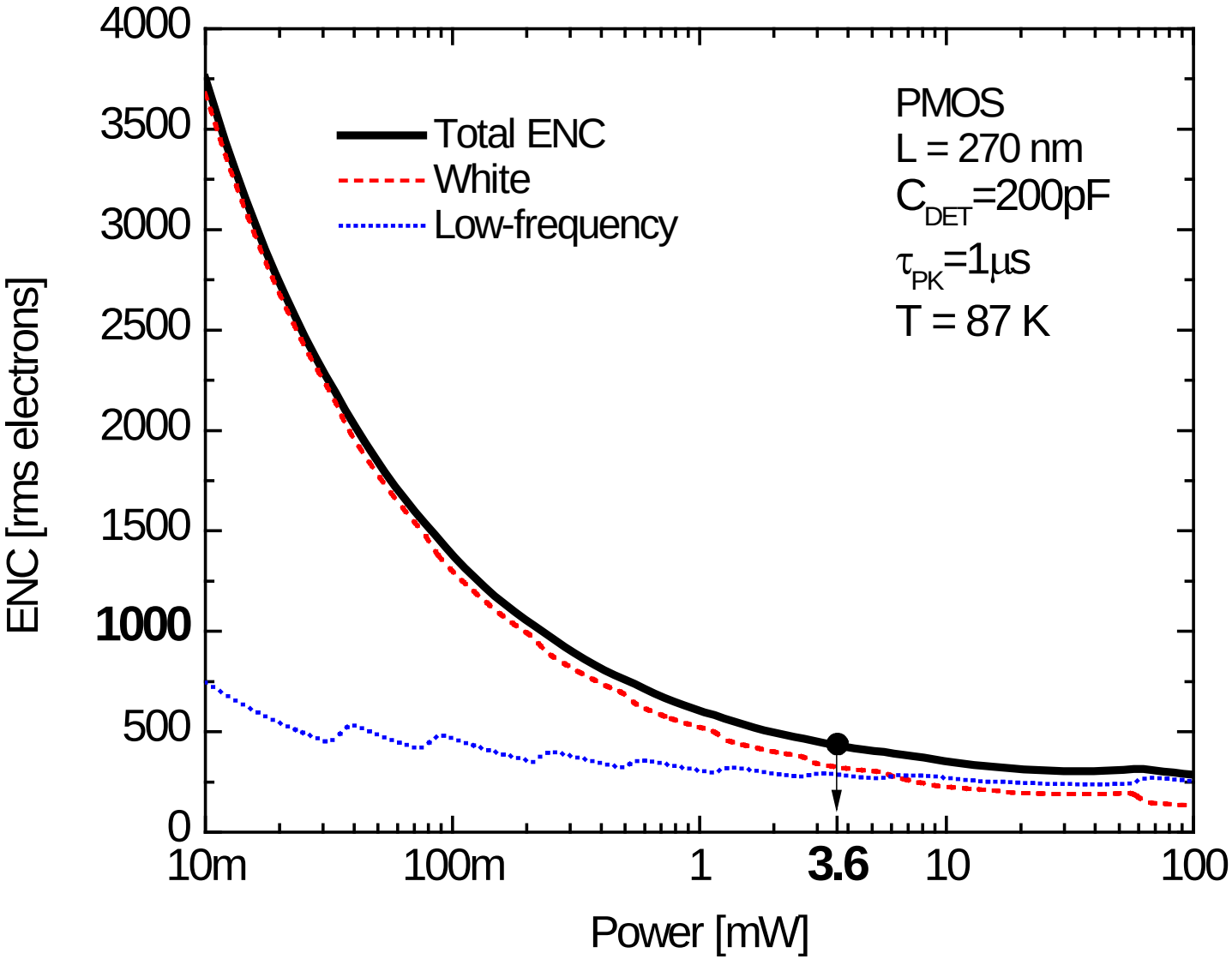


Input transistor ENC optimization



From: G. De Geronimo

ENC vs power in the input cascode



1. Lifetime vs temperature due to aging processes
1.1. CMOS in dc operation: Analog FE ASIC
Introduction (1)

• *Lifetime due to aging*: A limit defined by a chosen level of monotonic degradation in e.g., drain current, transconductance, due to a well understood mechanism. The device "fails" if a chosen parameter gets out of the specified circuit design range. *Such an aging mechanism doe not result in sudden device failure.*

•At high temperatures (300-420K) there are several sudden failure mechanisms strongly temperature dependent
[e.g., electromigration $\propto (IT)^2 \exp(-a/T)$], which become negligible at low temperatures.

•*Physics-of-failure* modeling for CMOS technology in Lar is reduced to study of *hot-electron effects* as the dominant remaining mechanism.

•Thermal expansion/contraction is studied separately.

Principal findings and design guidelines

1.1. A study of hot-electron effects on the device lifetime has been performed for the TSMC NMOS 180nm technology node at 300K and 77K. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (Vds), and a separate measurement of the substrate current (Isub) as a function of 1/Vds. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current , $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of V_{ds} *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and LBNE falls naturally into this domain, where hot-electron effects are negligible.*

1.2. *Lifetime of digital circuits (ac operation) is extended by the inverse duty factor* $4/(f_{clock} t_{rise})$ *compared to dc operation.* This factor is large (>100) for deep submicron technology and clock frequency needed for TPC. As an additional margin, V_{ds} may be reduced by ~10%.

2. Extremely low failure rate (incidence) in ATLAS LAr and NA48/ LKr calorimeters, over a long time scale demonstrates on a large scale that *surface mount circuit board technology withstands very well even multiple abrupt immersions in LN2* applied in board testing, and that the total failure incidence in continuous operation over time, ranging from 6 to13 years so far, is very low.

References

1. C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill, *"Hot-electron-induced MOSFET degradation-model, monitor, and improvement", IEEE Journal of Solid-State Circuits*, vol. sc-20, no. 1, pp. 295-305, Feb. 1985.
2. T. Chen, C. Zhu, L. Najafizadeh, B. Jun, A. Ahmed, R. Diestelhorst, G. Espinel, and J. D. Cressler, "CMOS reliability issues for emerging cryogenic Lunar electronics applications," *Solid-State Electronics*, vol. 50, pp. 959-963, 2006.
3. K. N. Quader, E. R. Minami, W.-J. Huang, P. K. Ko, and C. Hu, "*Hot-Carrier-Reliability Design Guidelines for CMOS Logic Circuits*", *IEEE Journal of Solid-State Circuits*, vol. sc-29, no. 3, pp. 253-262, March 1994.
4. M. White and J.B. Bernstein, "*Microelectronics Reliability: Physics-of -Failure Based Modeling and Lifetime Evaluation"*, JPL Publication 08-5 2/08.
5. G. De Geronimo, A. D'Andragora, S. Li, N. Nambiar, S. Rescia, E. Vernon, H. Chen, F. Lanni, D. Makowiecki, V. Radeka, C. Thorn, and B. Yu, *"Front-End ASIC for a Liquid Argon TPC",* IEEE Trans. Nucl. Sci., Vol. 58, No. 3, June (2011) 1376-1385.

Note: Manuals for each CMOS technology node provided by major foundries are devoted to guidelines how to maximize transistor lifetime. An instructive example is IBM's ~300 page manual for the 90nm node.

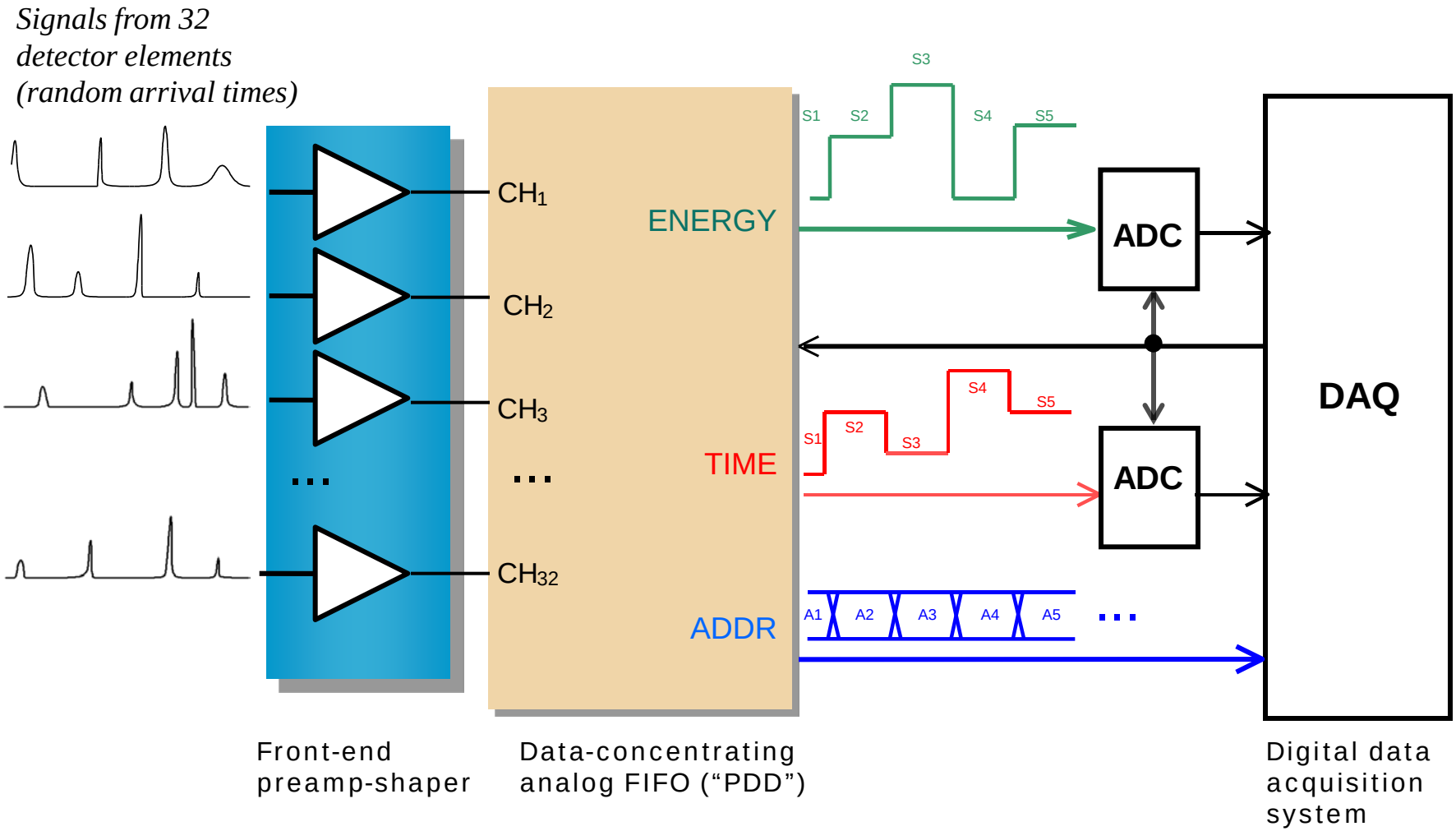
Design Examples:

1. Multichannel pulse measurement with analog data concentration and derandomization

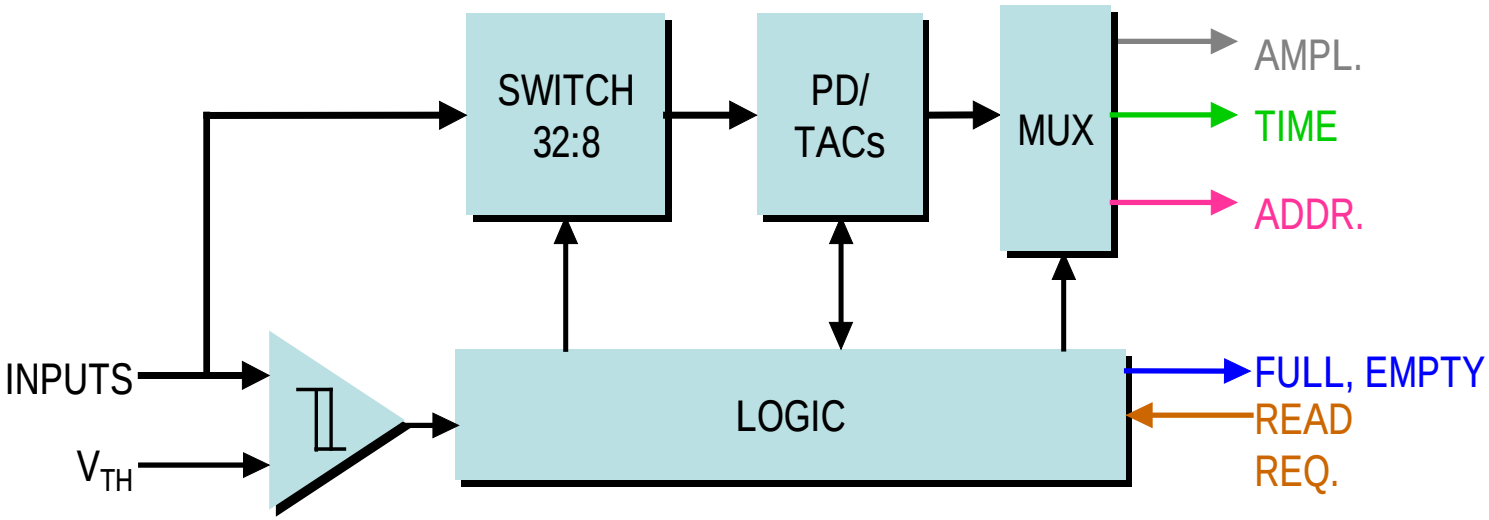
2. ASICs for CCD readout

3. Readout ASIC for miniaturized PET tomograph

1. Multichannel pulse measurement with analog data concentration



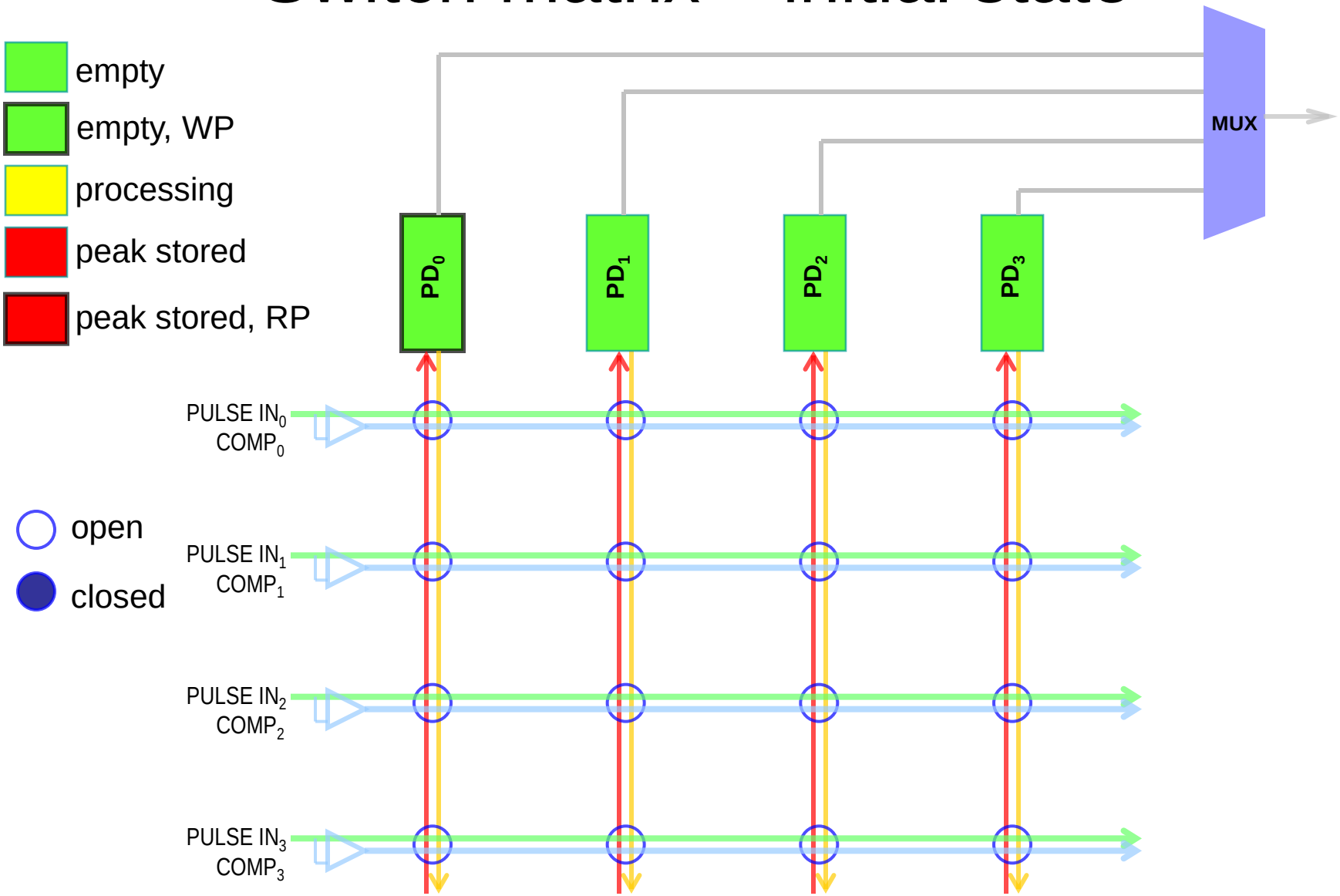
PDD ASIC Block Diagram



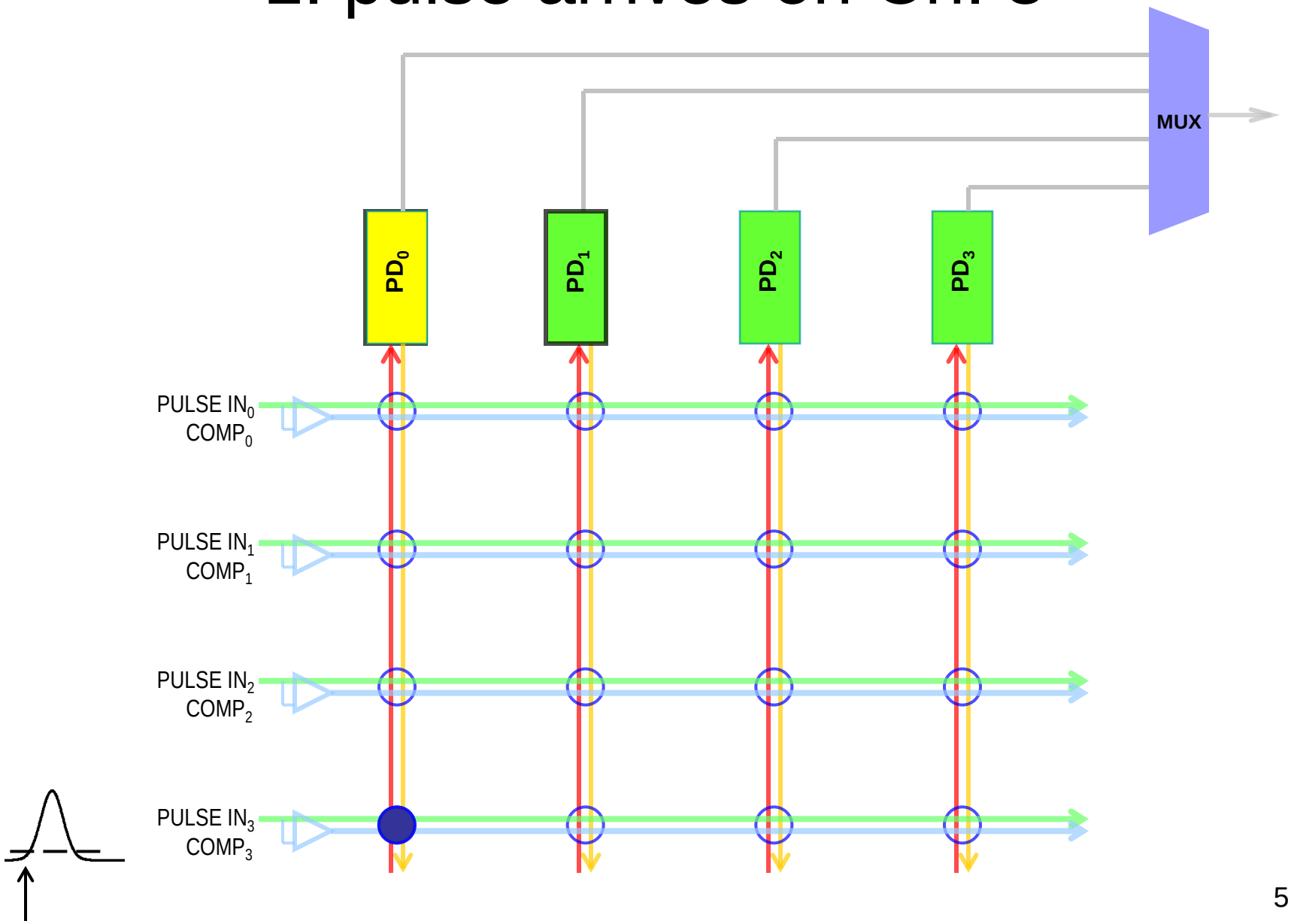
- *Self-triggered and self-sparsifying*
- *Simultaneous amplitude, time, and address measurement for 32 input channels*
- *Set of 8 peak detectors act as derandomizing analog memory*
- *Rate capability improvement over present architectures*
- *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
- *Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel*
- *Low power (3 mW per channel)*

P. O'Connor, G. De Geronimo, A. Kandasamy, *Amplitude and time measurement ASIC with analog derandomization: first results*, IEEE Trans. Nucl. Sci. 50(4), pp. 892-897 (Aug. 2003).

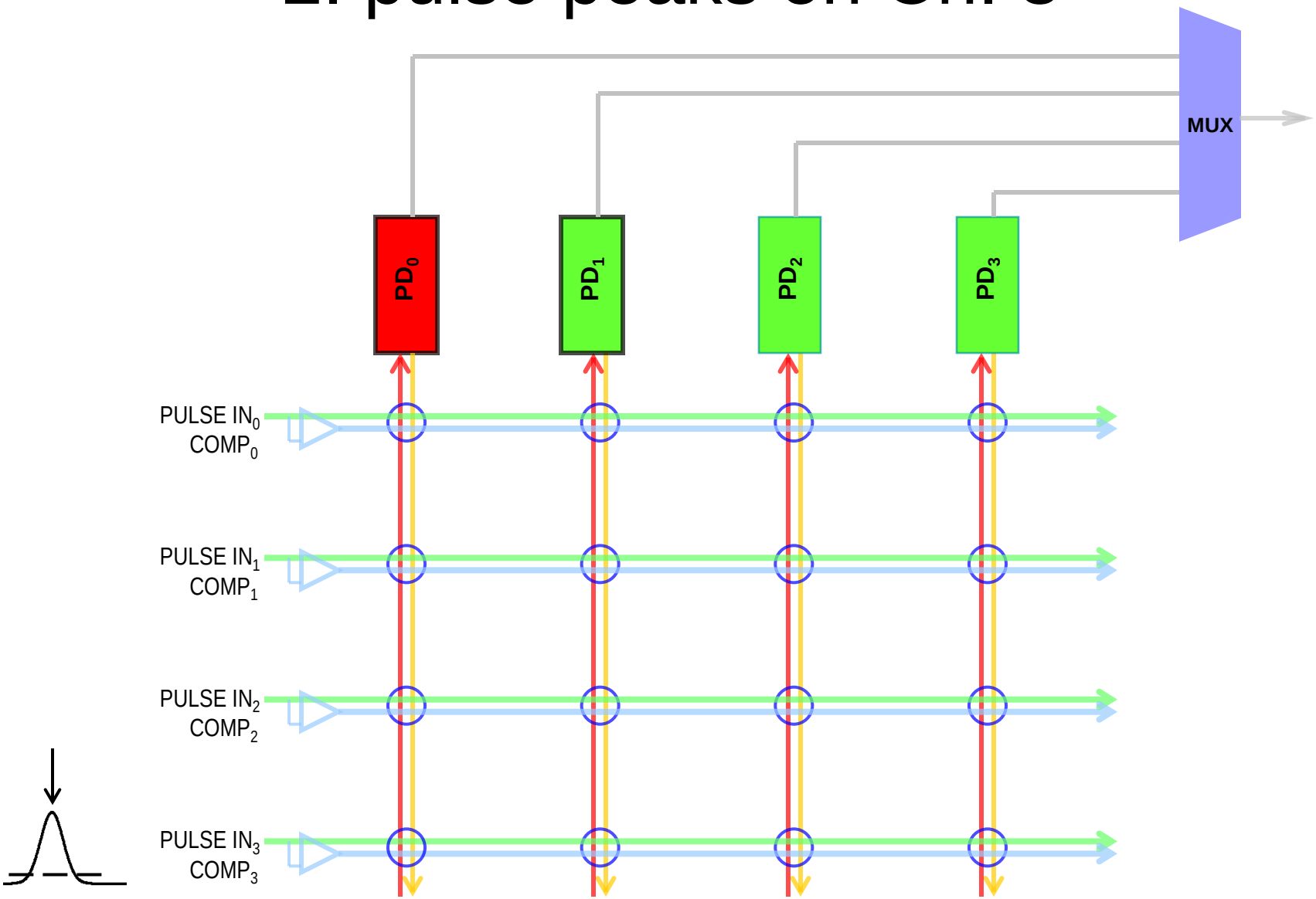
Switch matrix – initial state



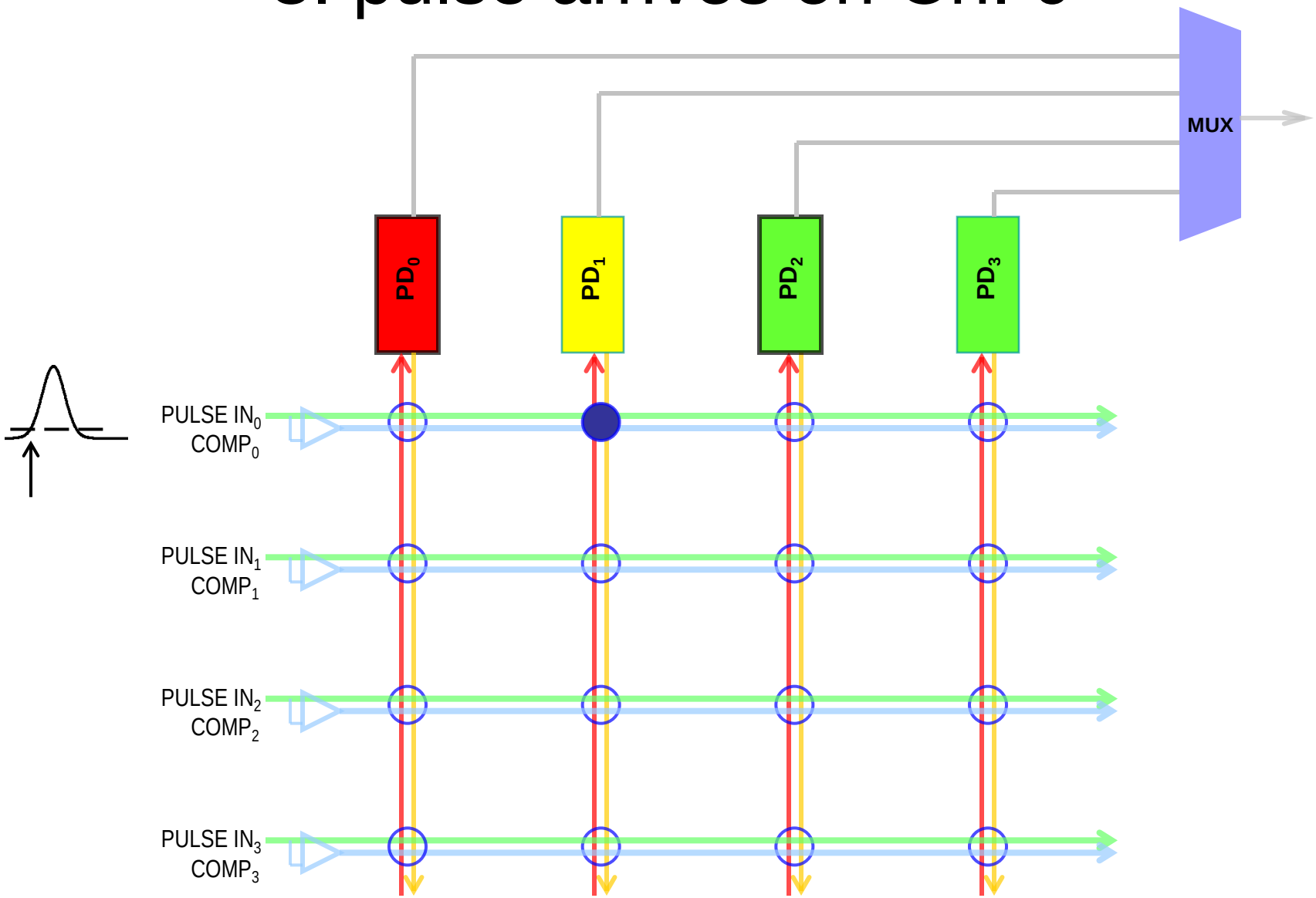
1. pulse arrives on Ch. 3



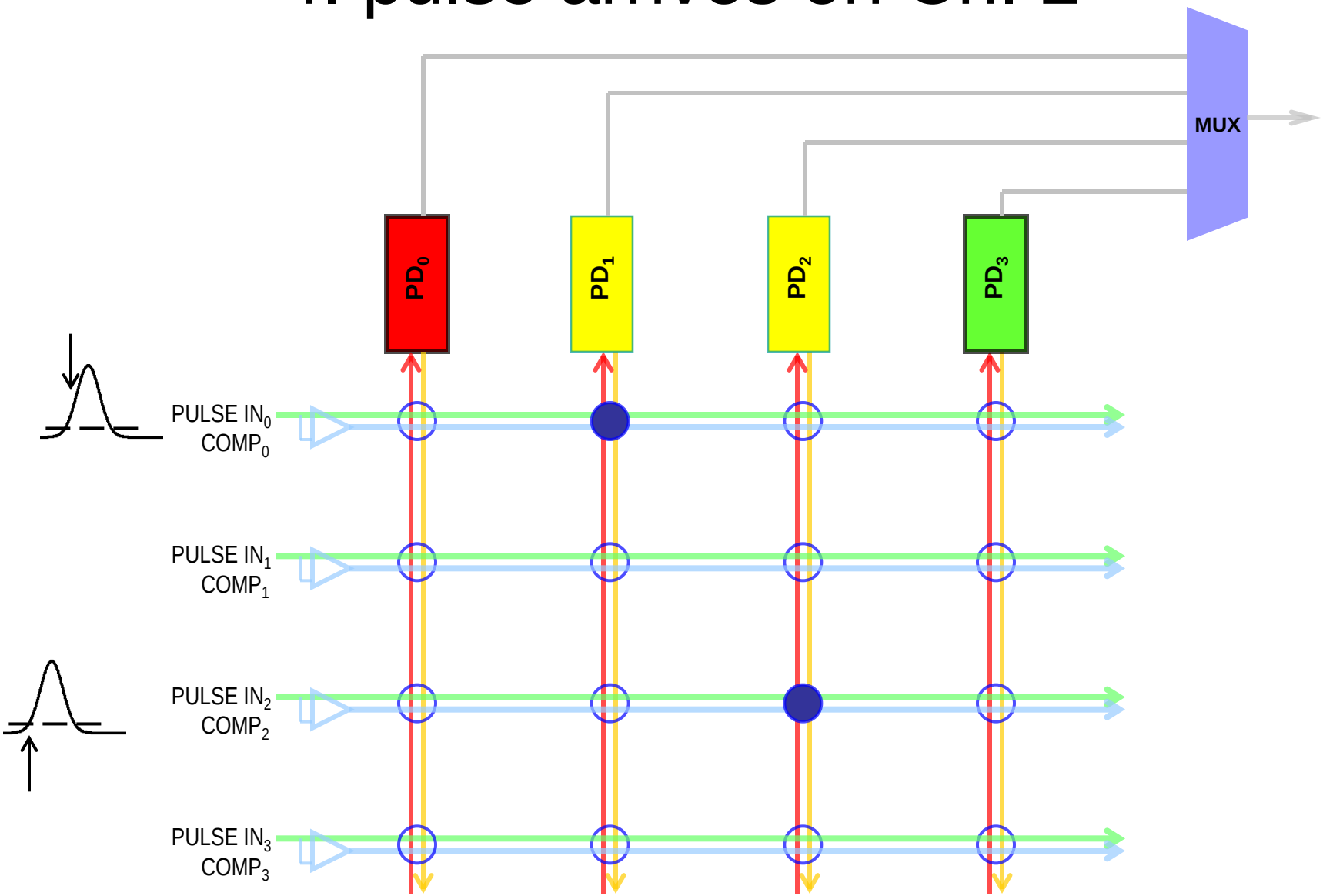
2. pulse peaks on Ch. 3



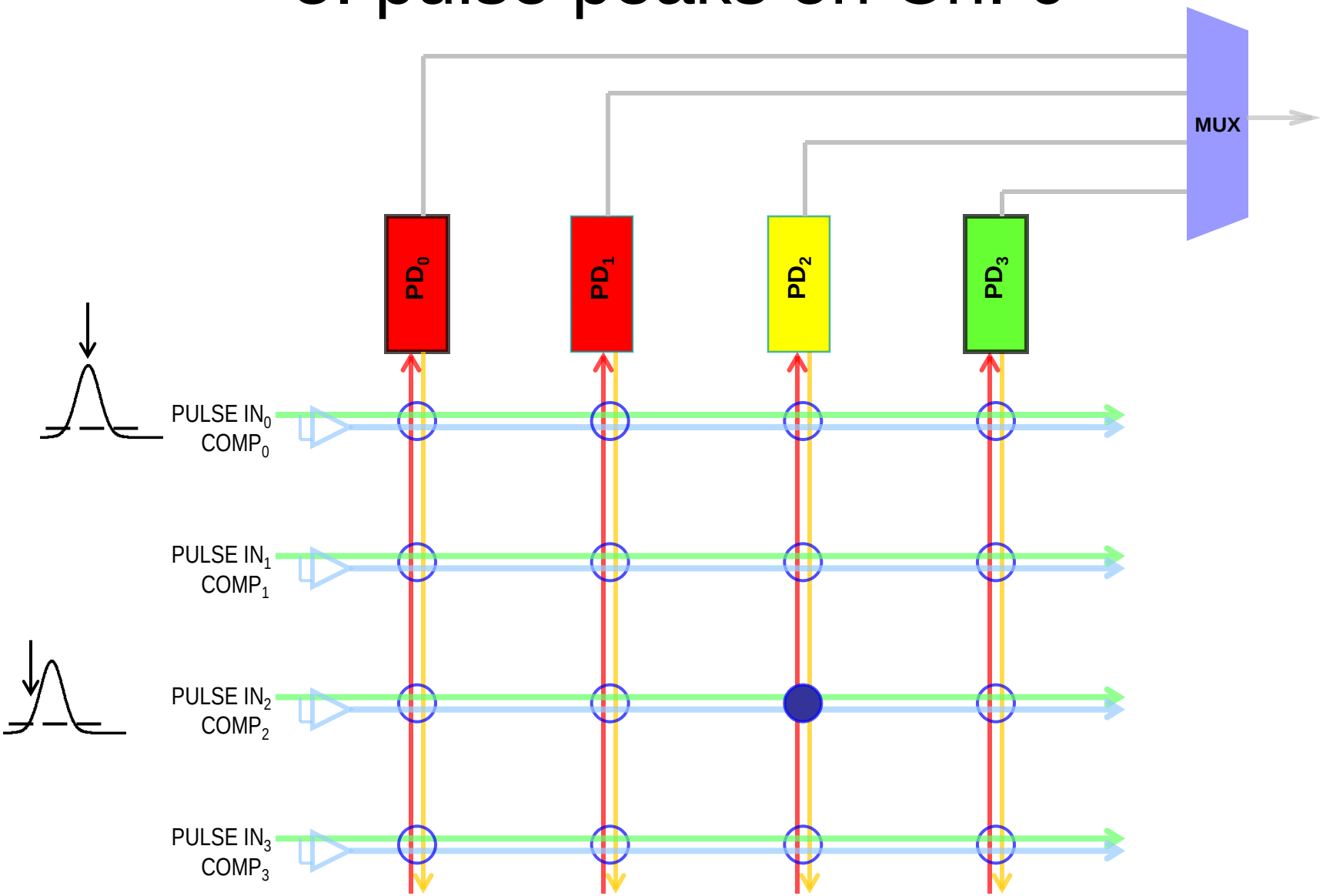
3. pulse arrives on Ch. 0



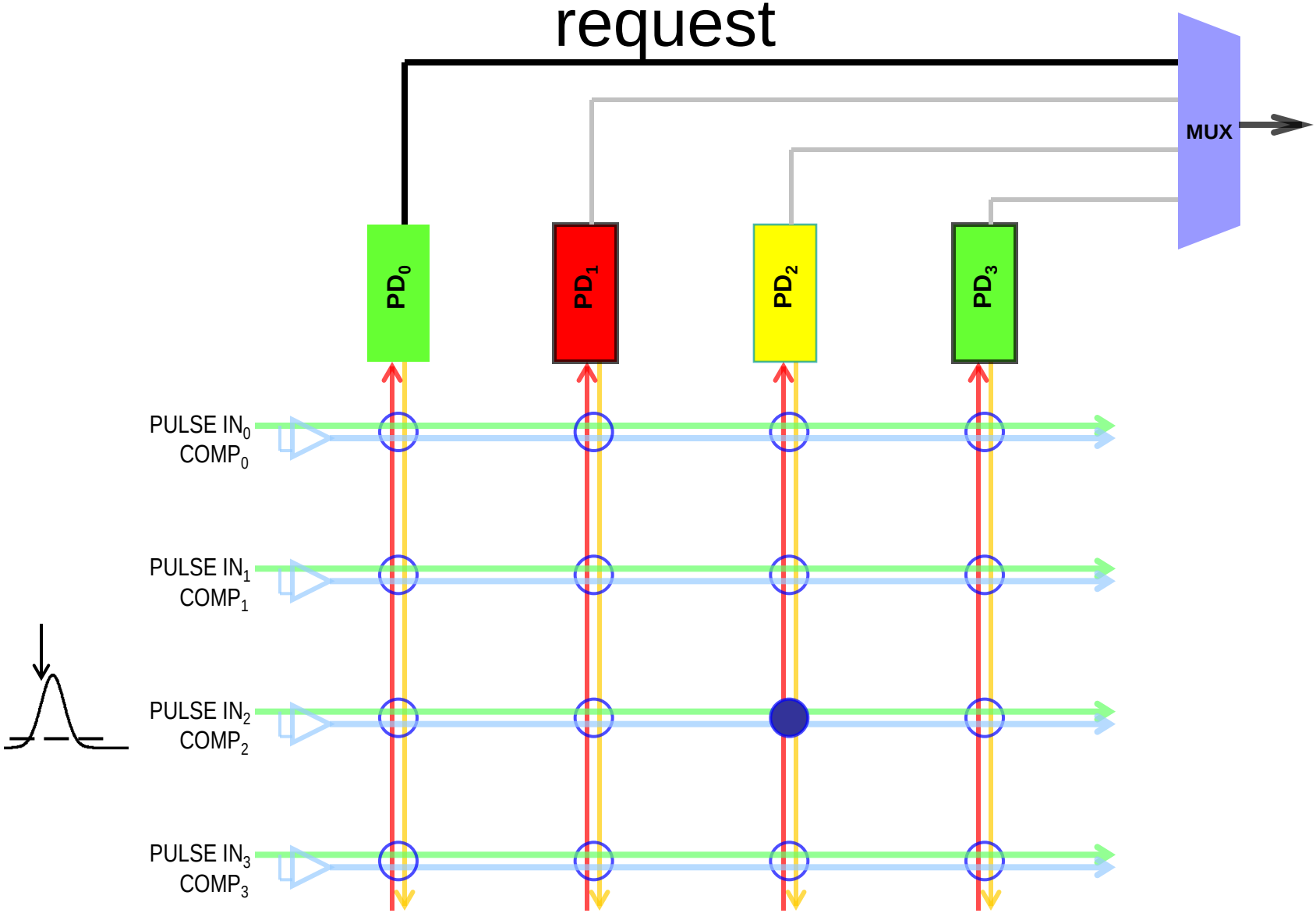
4. pulse arrives on Ch. 2



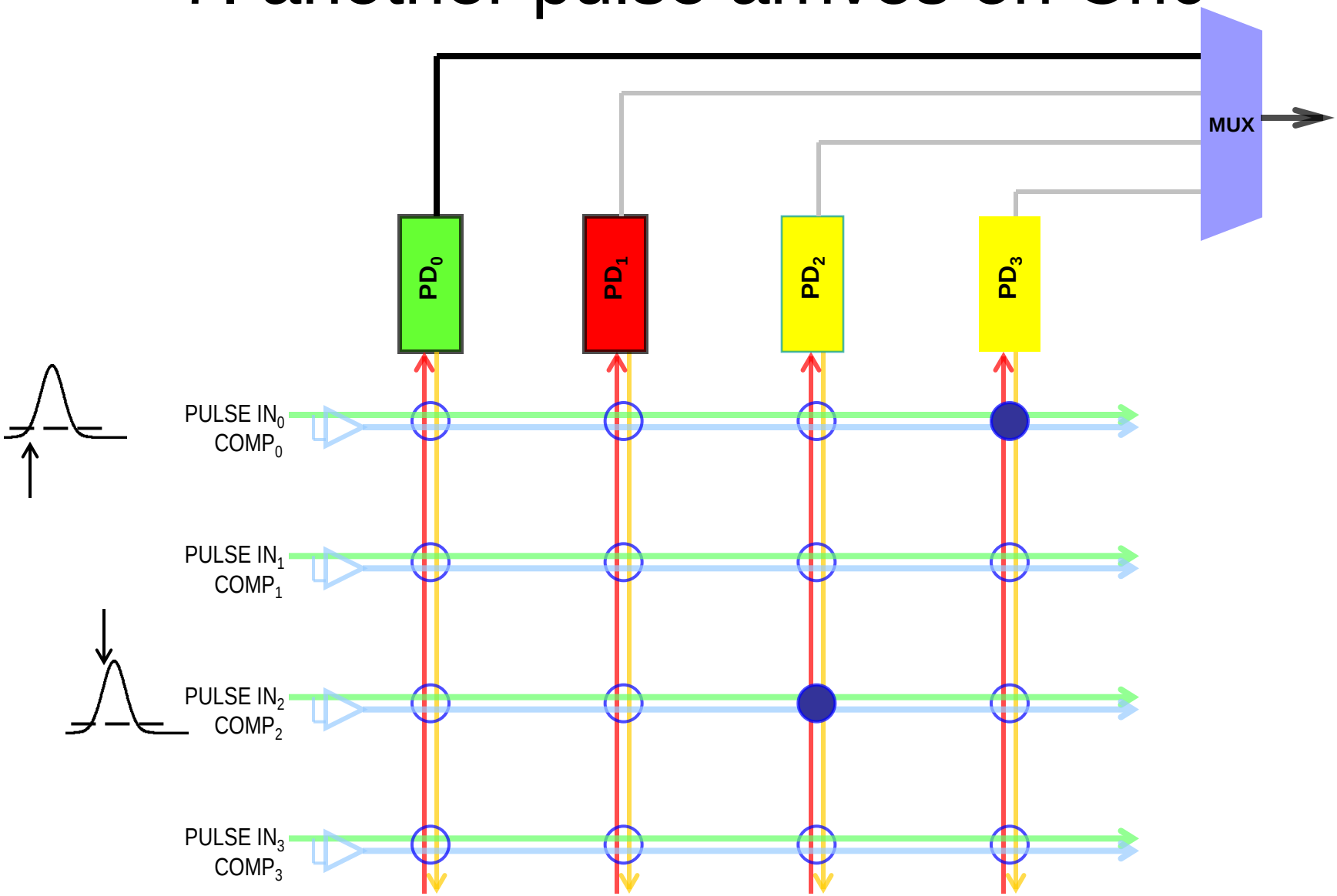
5. pulse peaks on Ch. 0



6. PD_0 read out in response to external read request

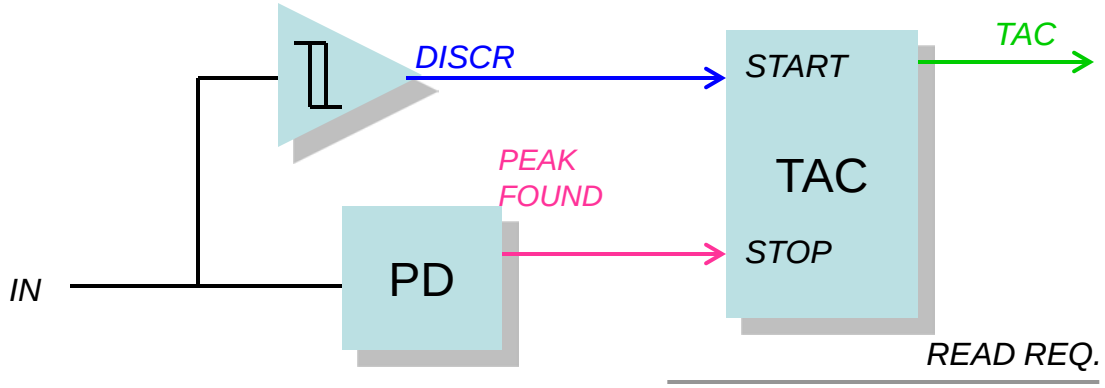


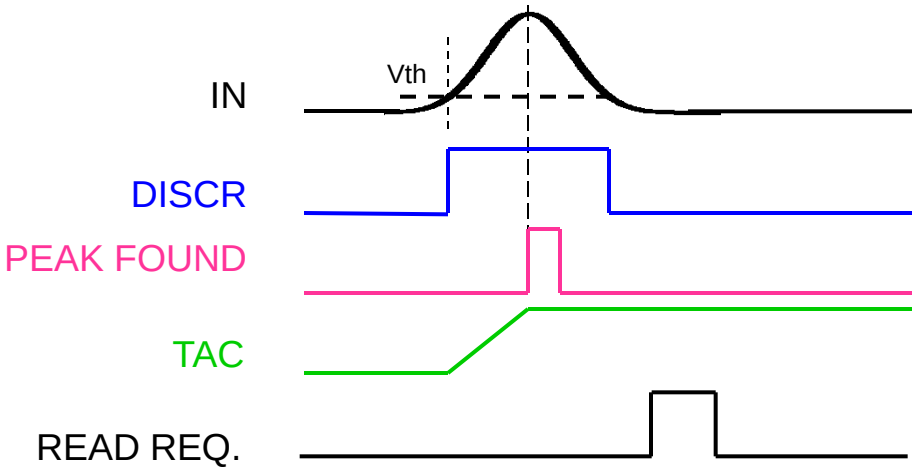
7. another pulse arrives on Ch0



Quad-mode Time-to-Amplitude Converter

MODE 1

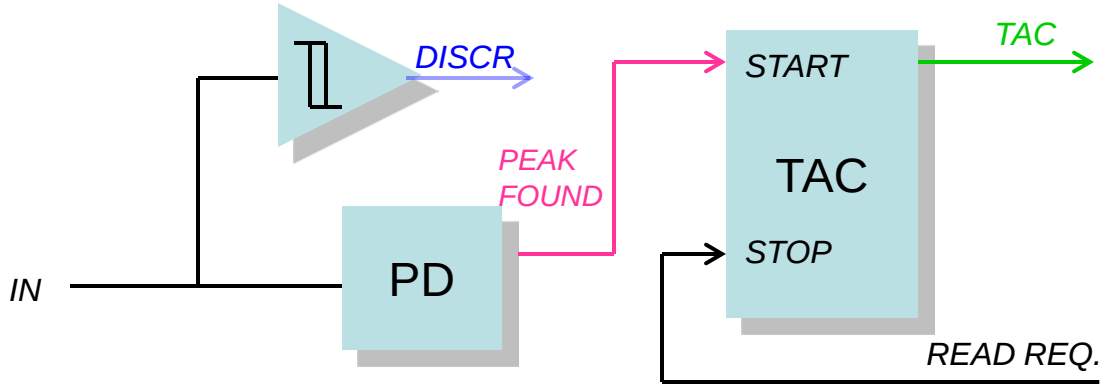


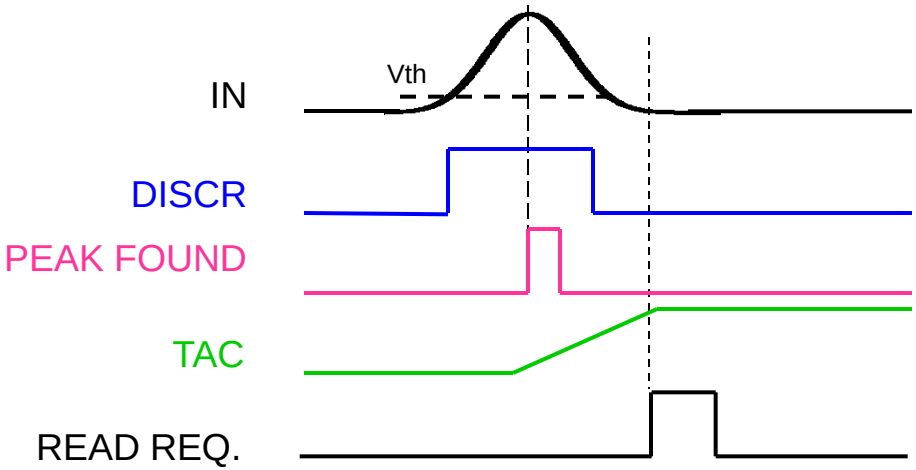


1. risetime
2. peak-RR
3. TOT
4. lead-RR

Quad-mode Time-to-Amplitude Converter

MODE 2

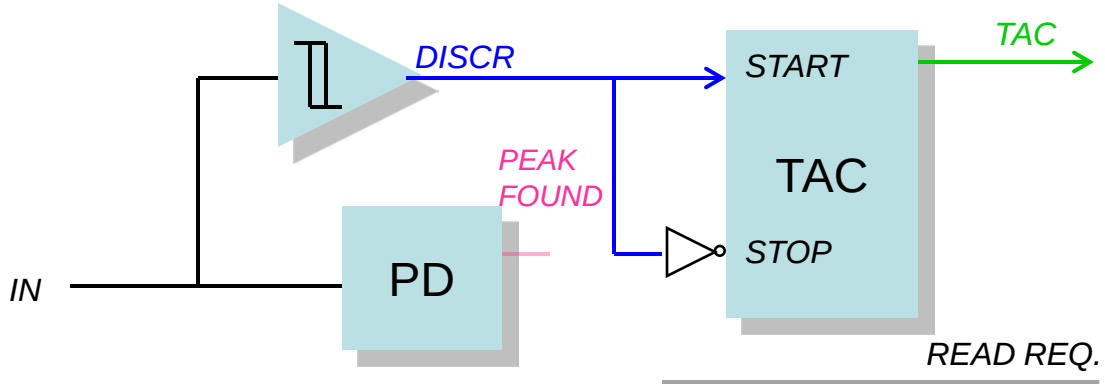


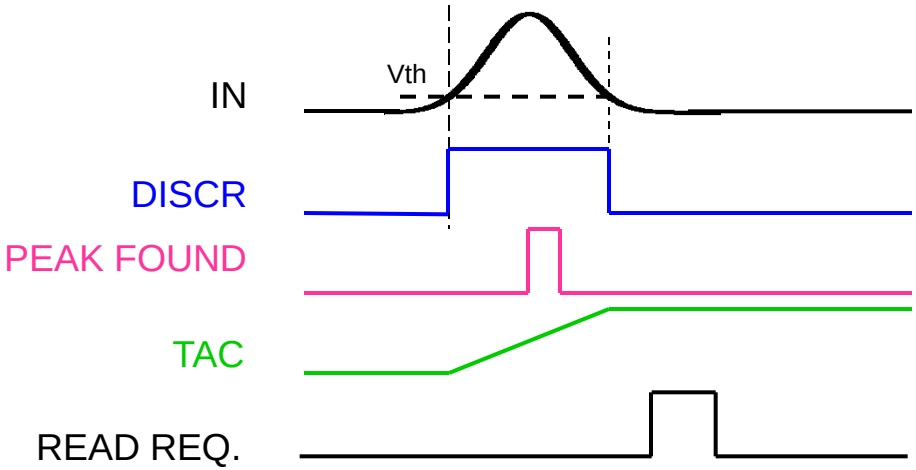


1. risetime
2. peak-RR
3. TOT
4. lead-RR

Quad-mode Time-to-Amplitude Converter

MODE 3

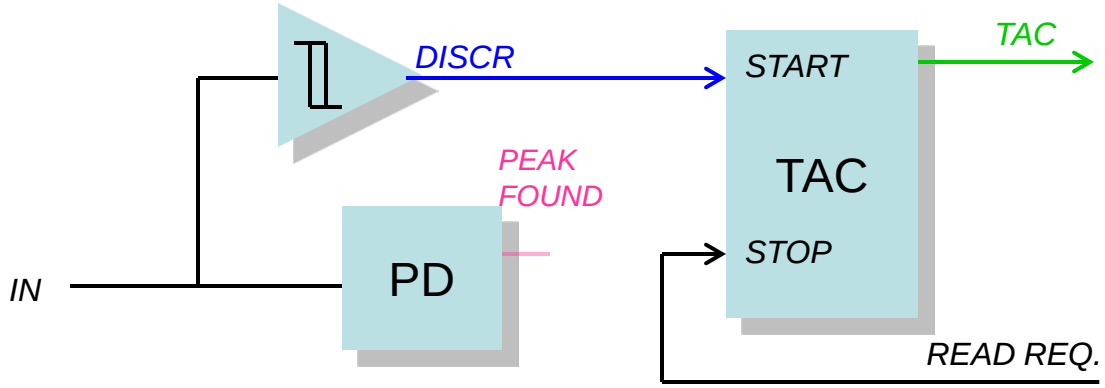


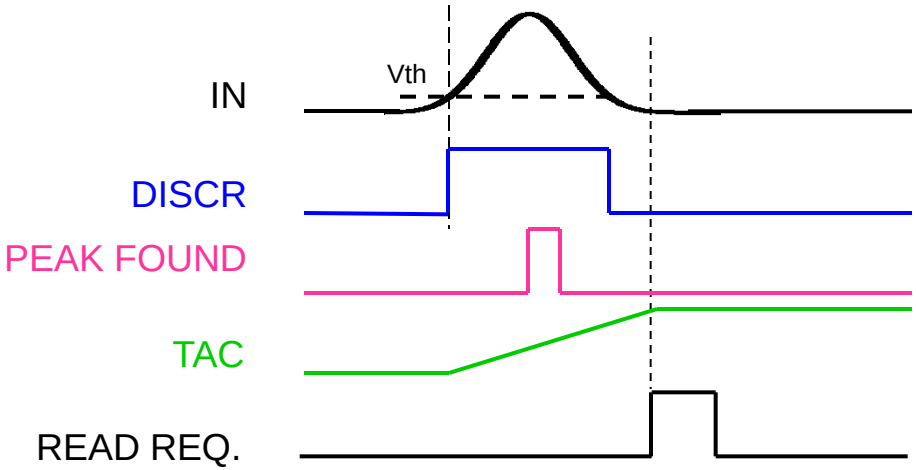


1. risetime
2. peak-RR
3. TOT
4. lead-RR

Quad-mode Time-to-Amplitude Converter

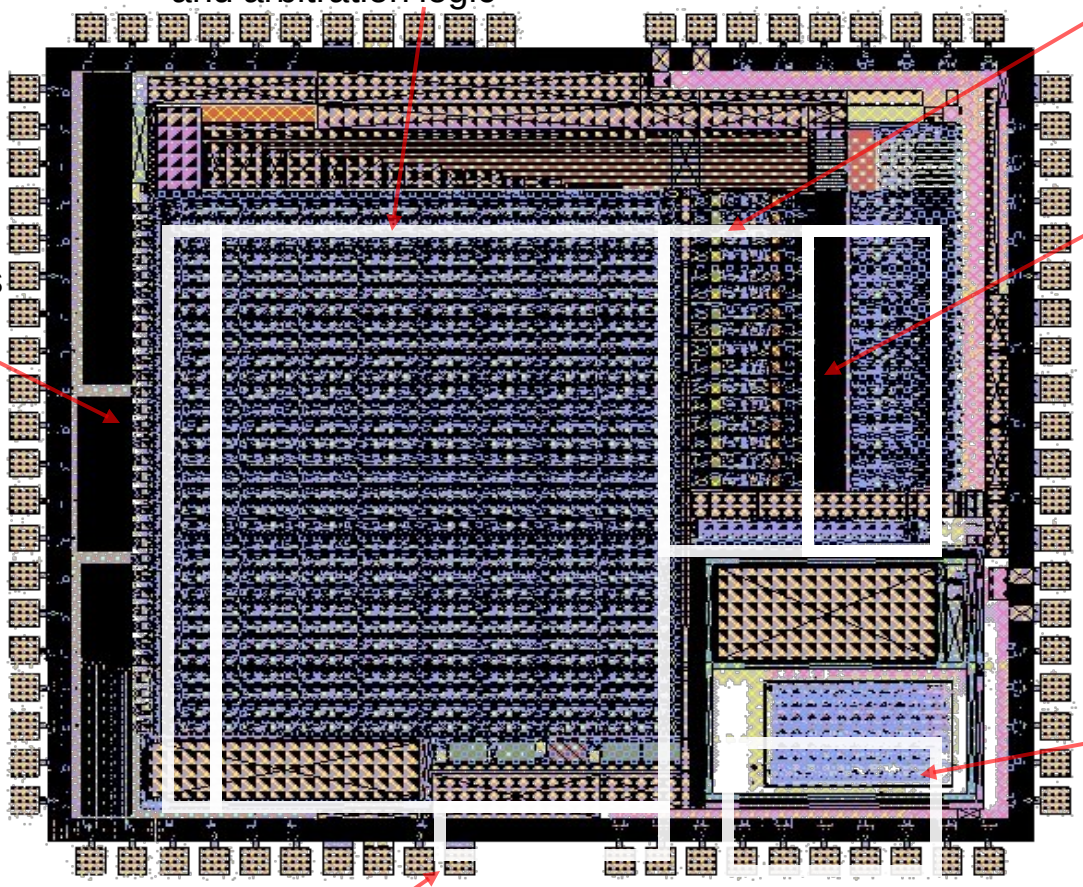
MODE 4





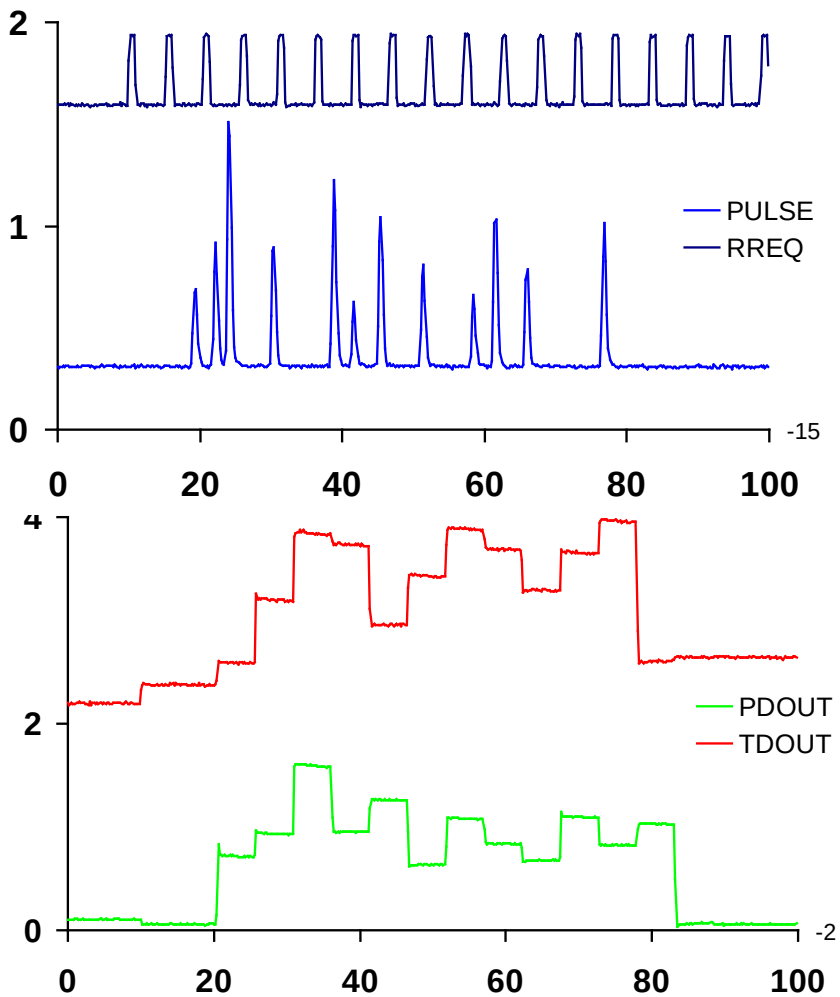
1. risetime
2. peak-RR
3. TOT
4. lead-RR

PDD layout



size : 3.6 x 3.2 mm²
technology: 0.35µm CMOS
DP4M

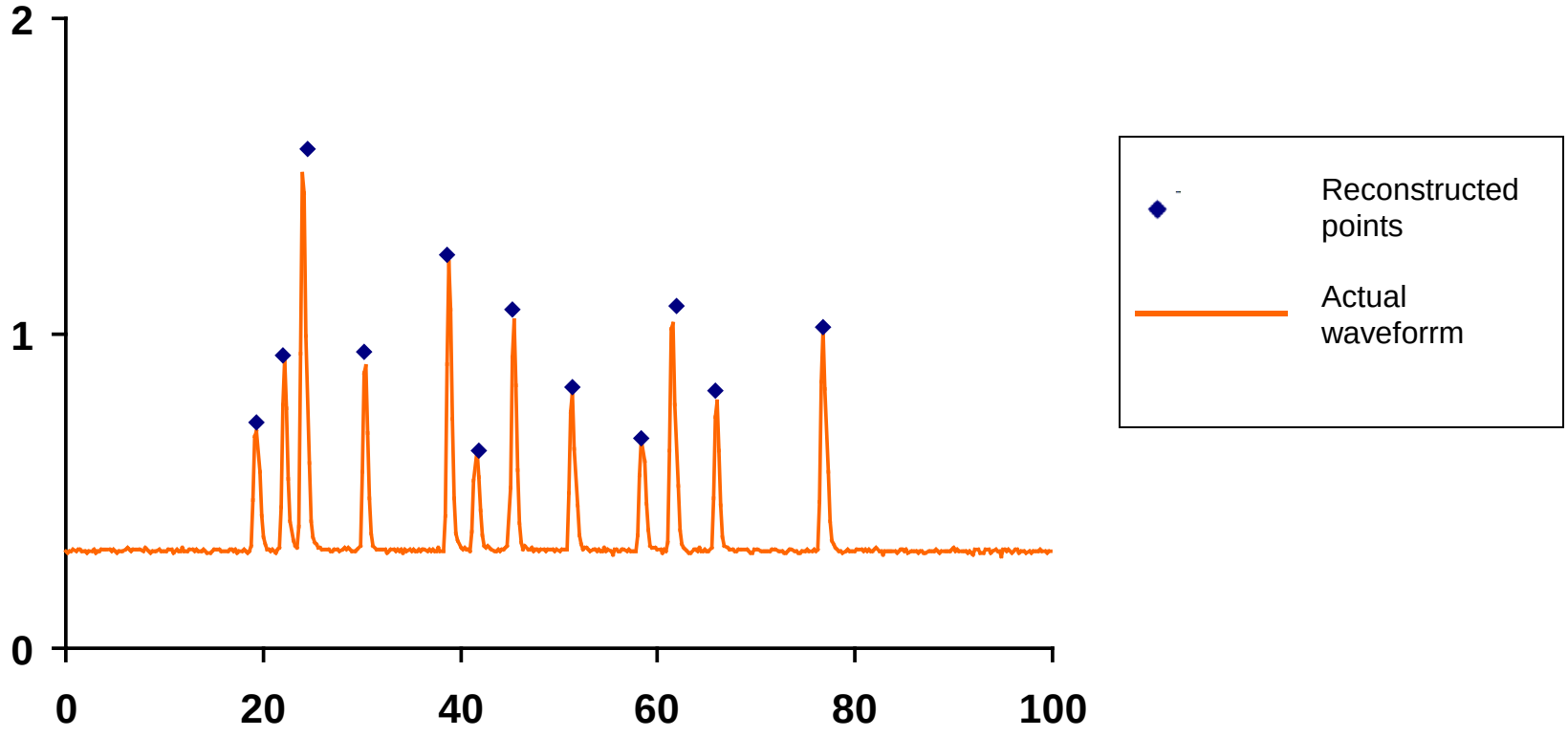
Reconstruction of peak height and time



ASIC Inputs

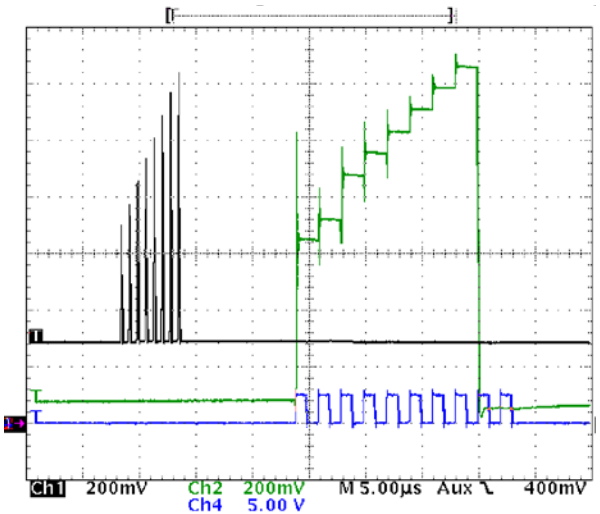
ASIC Outputs

Reconstruction of peak height and time



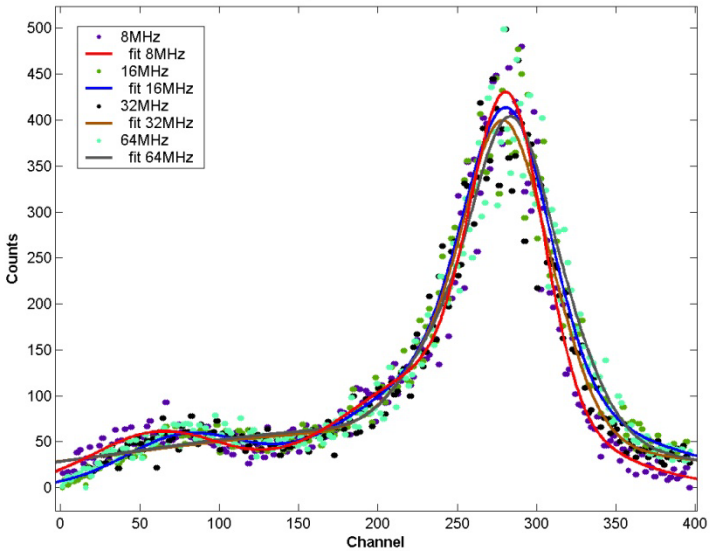
High rate capability

Fast pulses, high rate



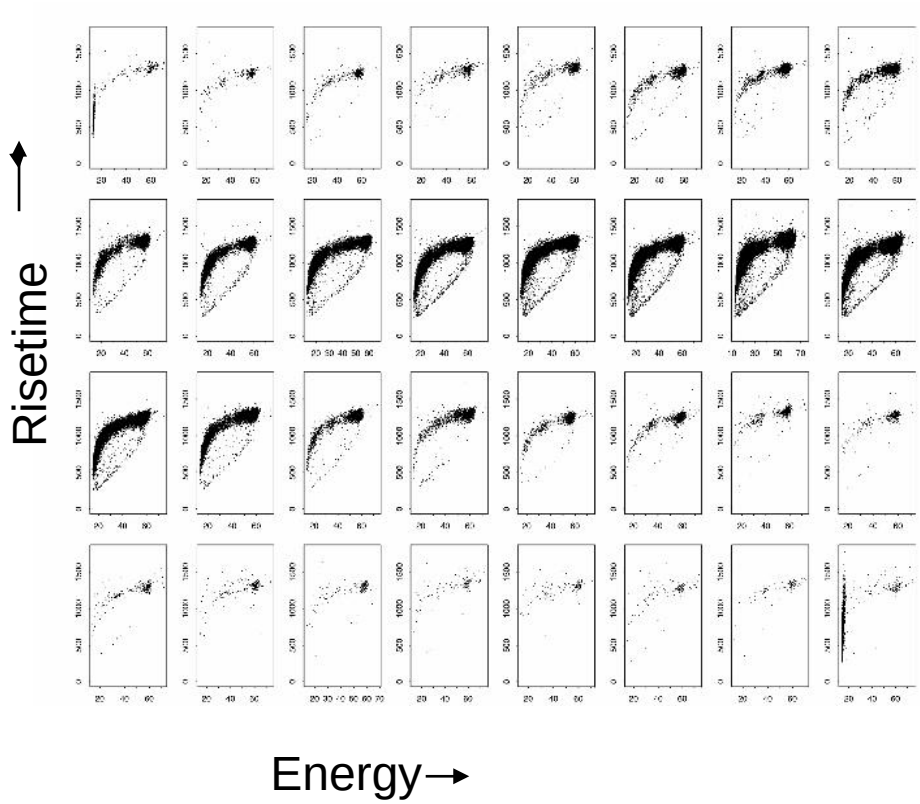
Black – pulse input
Blue – Read Request
Green – PD output

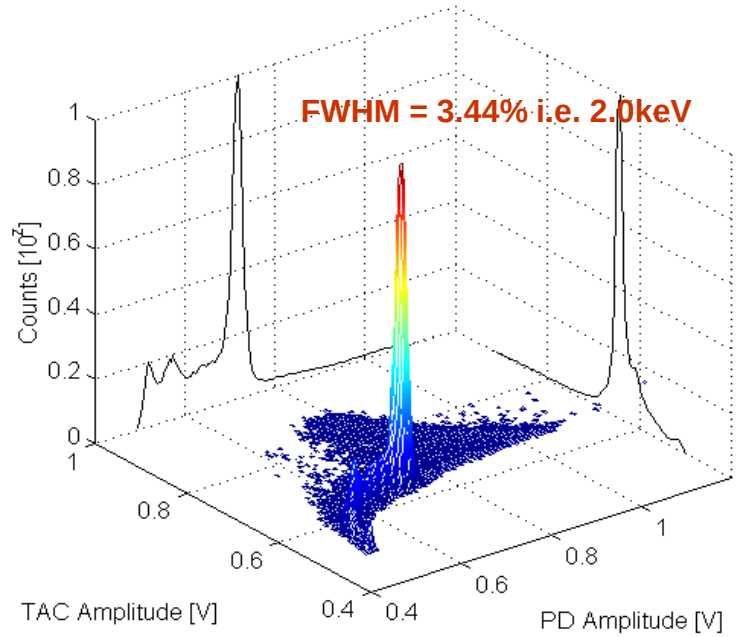
- Input pulses:
  - 30 ns peaking time
  - 1.6 MHz rate
- Readout rate 500 kHz



- 32 CZT sensors, 7x3x7mm^3
- ^{241}Am source, overall rate ~ 8MHz
- Shaper peaking time 600ns
- Rate of read request varied from 8 MHz to 64 MHz
- No peak shift or FWHM degradation seen
- Settling time of output mux ~ 10ns

Biparametric spectra



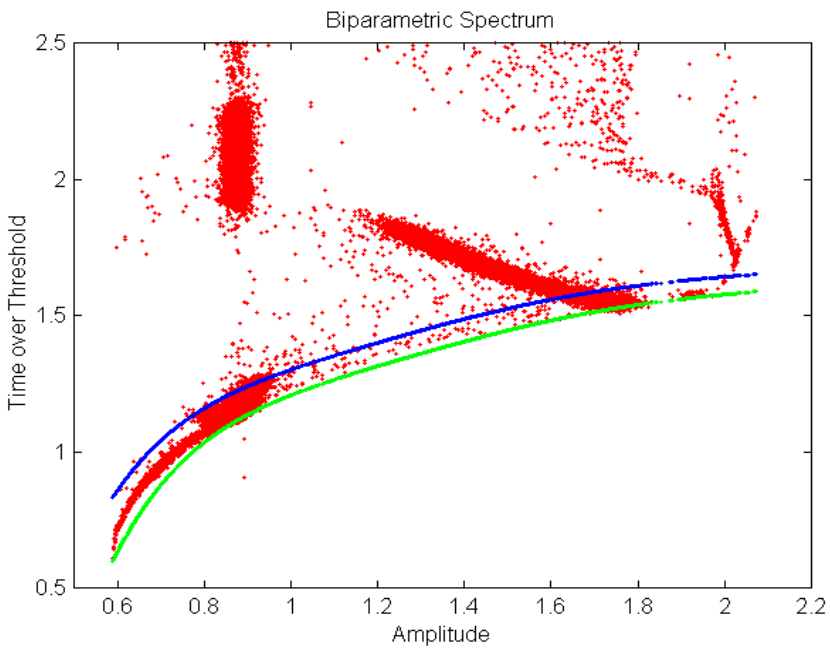


- **Detector: eV Products CZT Pixellated Linear Array of 32 elements 16x3x3 mm^3 biased at 900V**
- **Source: 2 x 8mCi ^{241}Am**
- **FE: t_p = 400ns, gain=200mV/fC**
- **Event Rate: 4.5MCounts/s overall, 210kCounts/s on the single pixel**

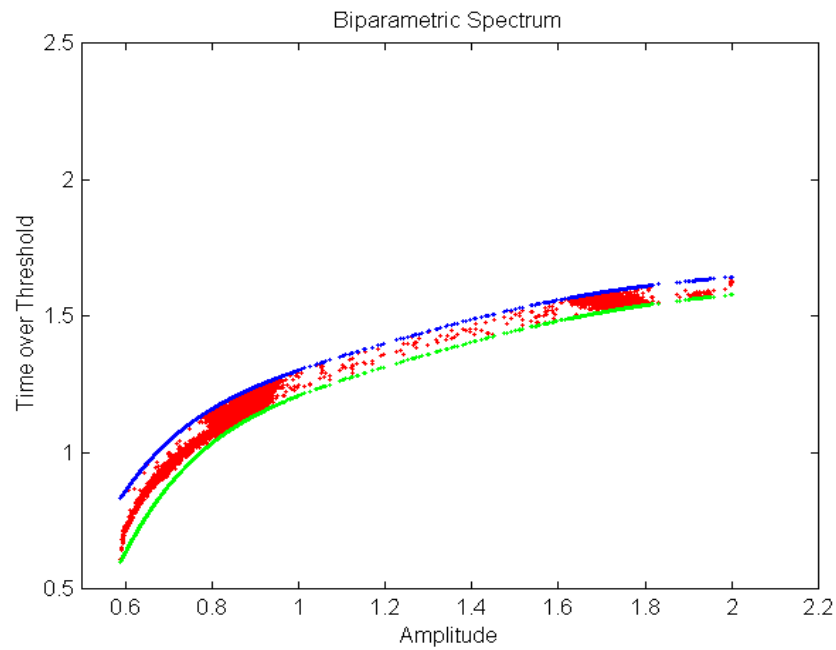
Time-Over-Threshold Measurement for pile-up rejection

Experiment Setup

- Array of 1mm x 1mm silicon diodes, built on a fully-depleted 400um high-resistivity wafer and cooled at ~ -54 ˚C
- 8keV X-ray monochromatic collimated 10umx10um beam from NSLS focused on the center of one pixel
- FE with 2us peaking time

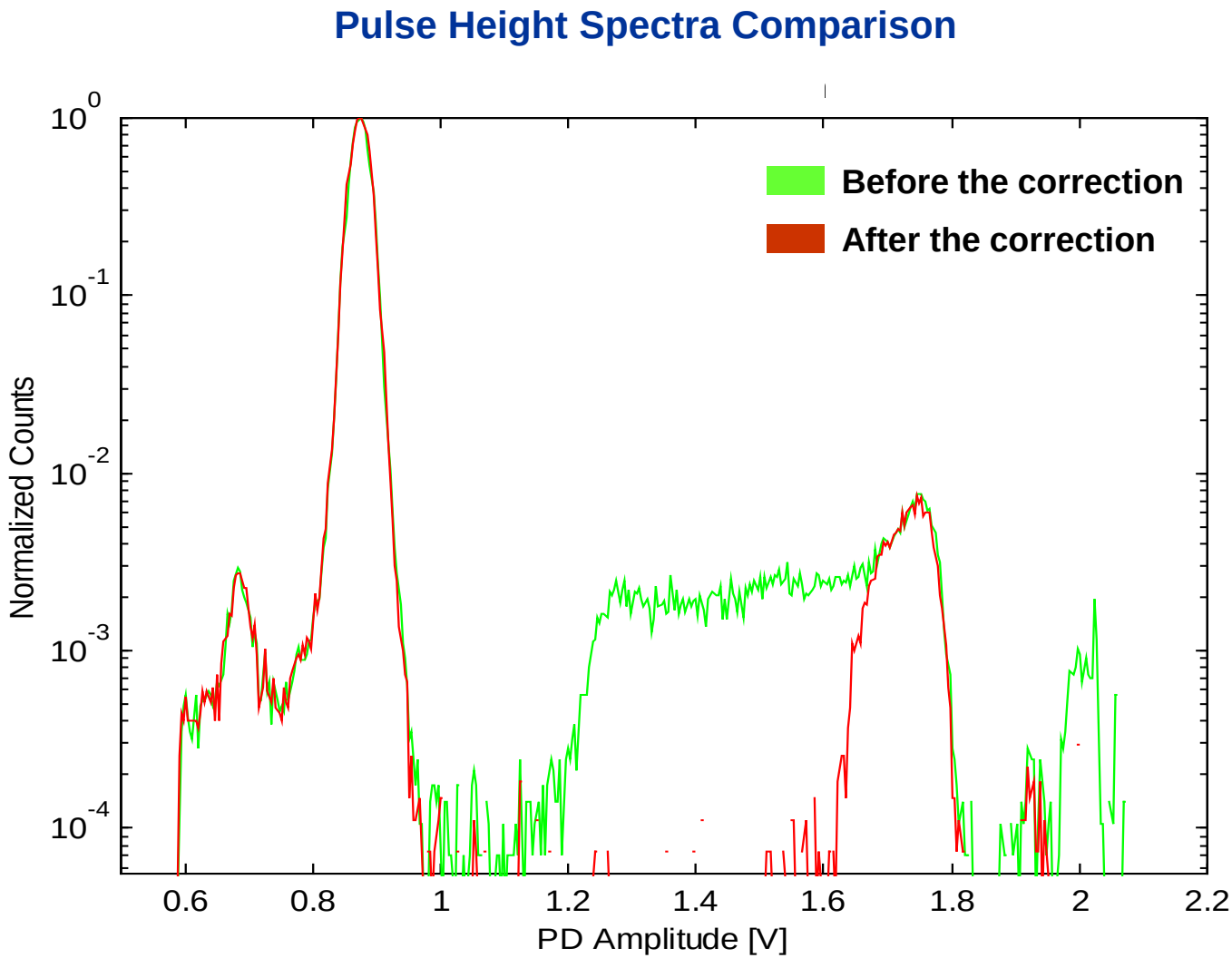


Before The Correction



After The Correction

Time-Over-Threshold Measurement for pile-up rejection

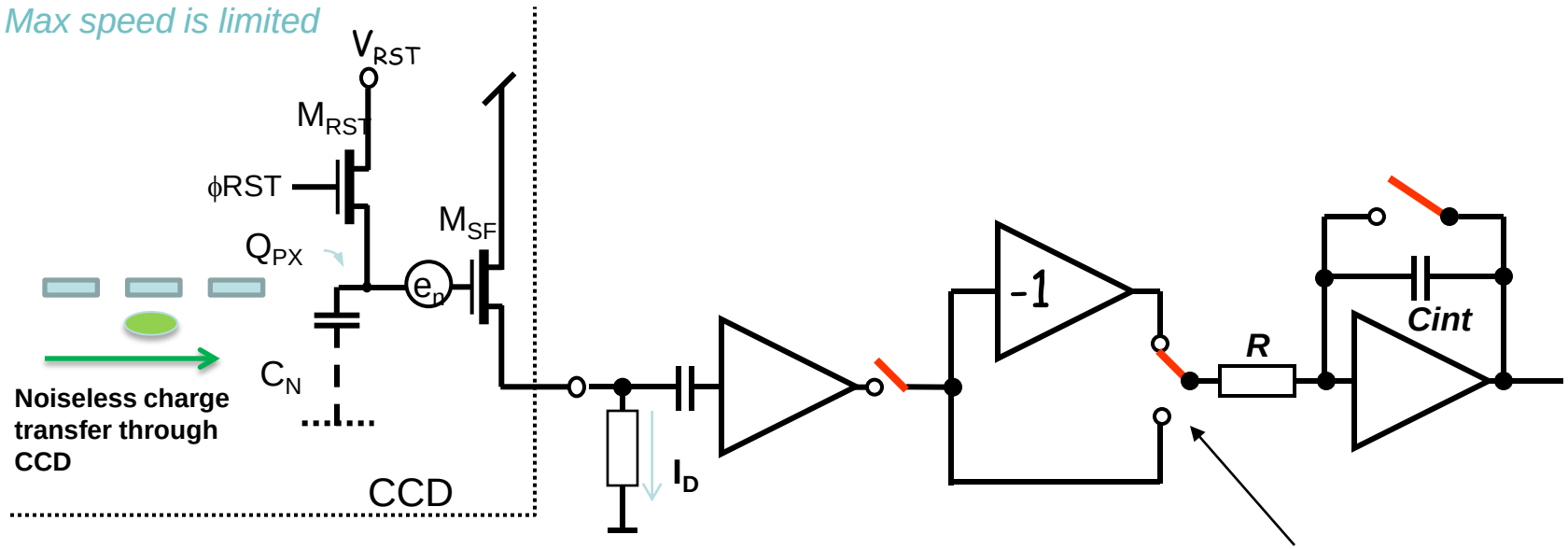


2. Readout of CCDs and Related Detectors

- CCD is characterized by:
  - Random event arrival time
  - Deterministic, noiseless transfer of photocharge to sensing electrode
  - Large dynamic range (few e^- → ~50fC)
  - On-board reset switch and first stage source follower
- In the same family:
  - Controlled Drift Detector
  - Charge-transfer “4-T” active pixel sensor
- Large sensing area with extremely small sense node capacitance
- kTC noise cancellation essential

Analog CDS implementation (1): Dual Slope Integrator

Dual-slope integrator (differential averager) is the matched filter for step waveform with white noise
As long as the pixel frequency is greater than the 1/f noise corner, noise is within 5% of ideal
Max speed is limited



Commutating Switch

C_n	15	fF
e_n	10-20	nV/√Hz
A_{VSF}	0.5	-
I_D	2 - 3	mA
f_c	150	kHz
Pixel time	1.8	μs
ENBW	~2	MHz
ENC	~5	e^-

$$\left|H_{DSI}(f)\right|^2 = \frac{4\sin^2(\pi f T_S)\sin^2(\pi f(T_S+T_G))}{(\pi f T_S)^2}$$

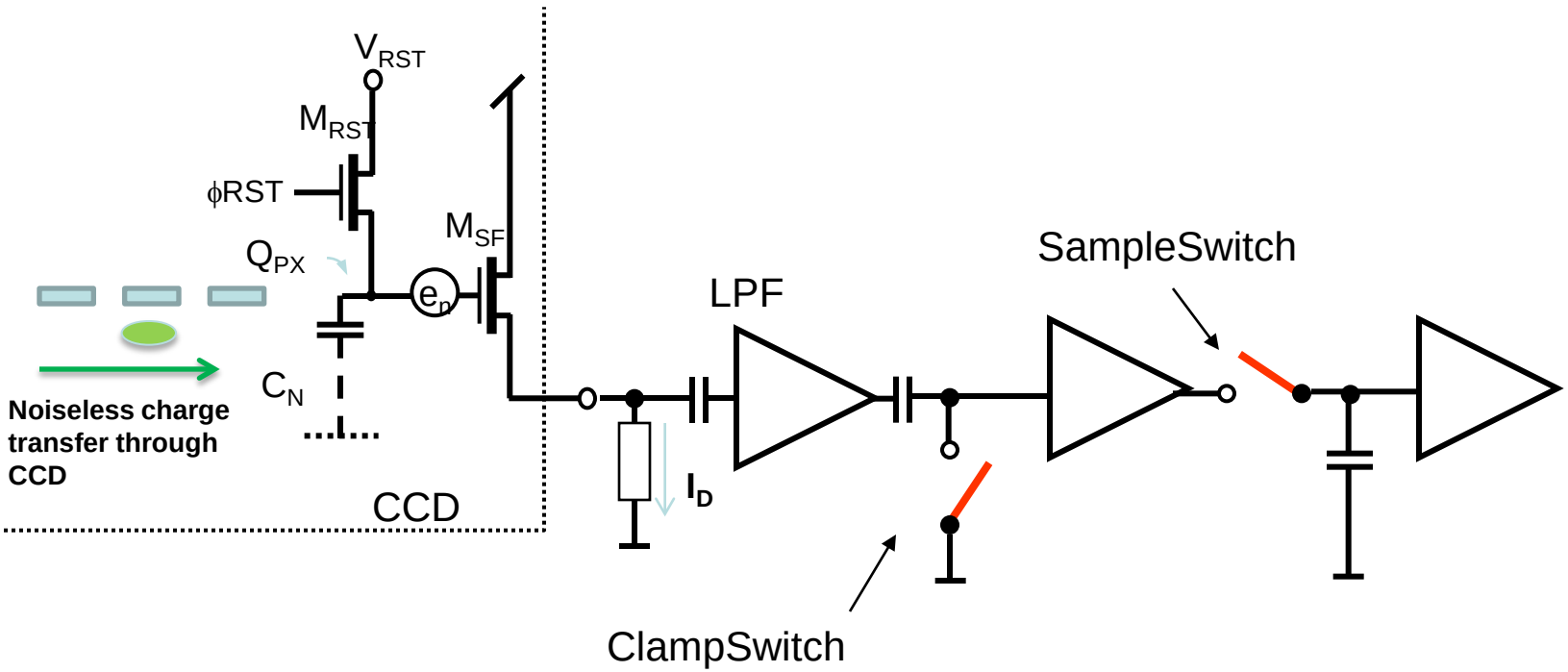
T_S = integration window (typically 25 – 40% of pixel period)
T_G = gap between end of reset and start of signal integration window

Neglecting 1/f noise,
$ENC \sim e_n \cdot \sqrt{ENBW} \cdot C_N/A_{VSF}$

D. Hegyi, A. Burrows, Astron. J. 85(10), 1421(1980)

Analog CDS implementation (2): Clamp-and-Sample

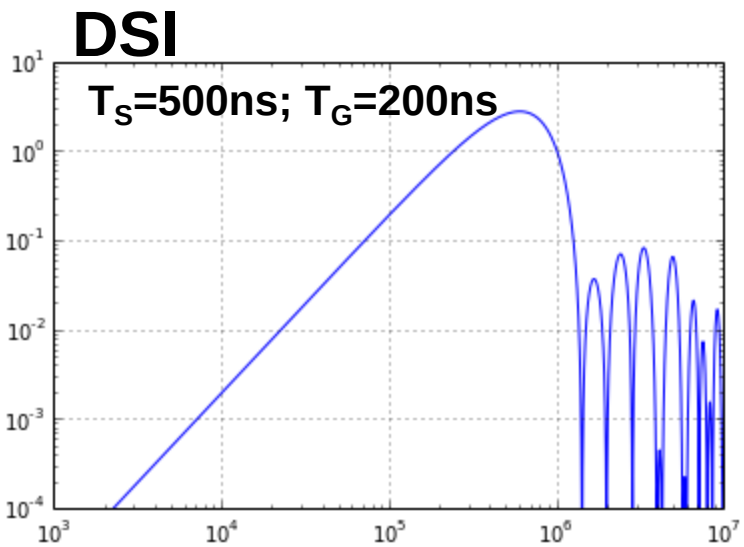
Prefilter bandpass must be set optimally; too high → excess noise; too low → image lag

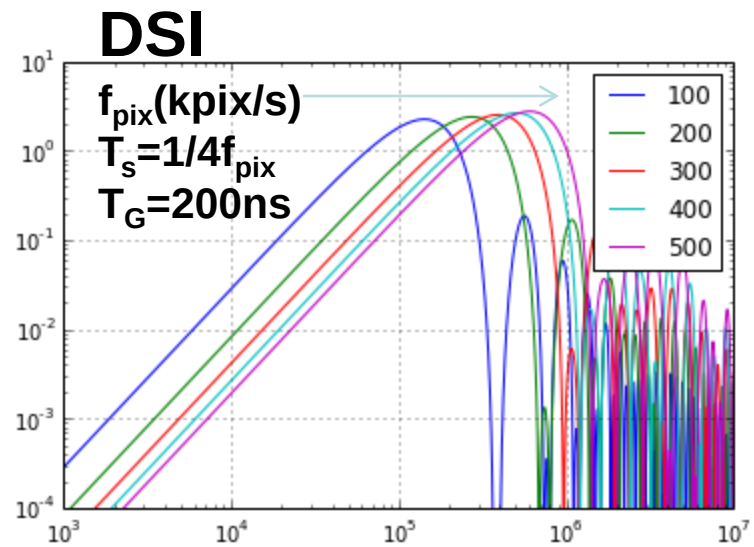


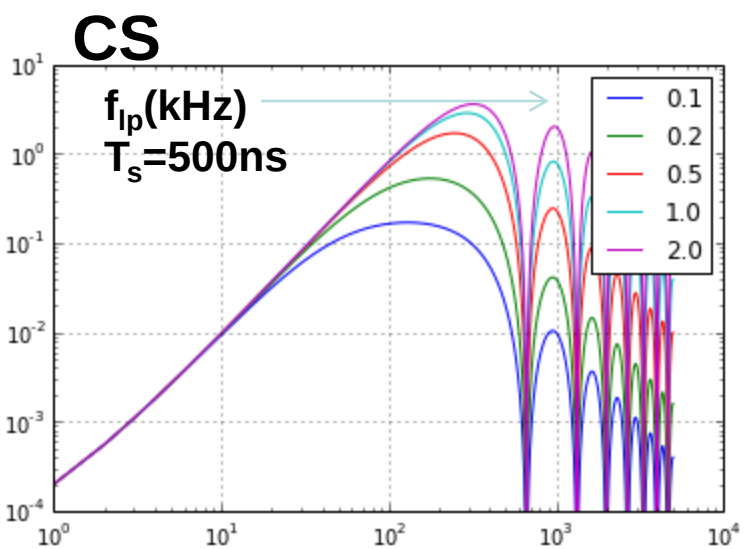
$$\left|H_{CS}(f)\right|^2 = \frac{4\sin^2(\pi f T_S)}{1+\left(\frac{f}{f_{LP}}\right)^2}$$

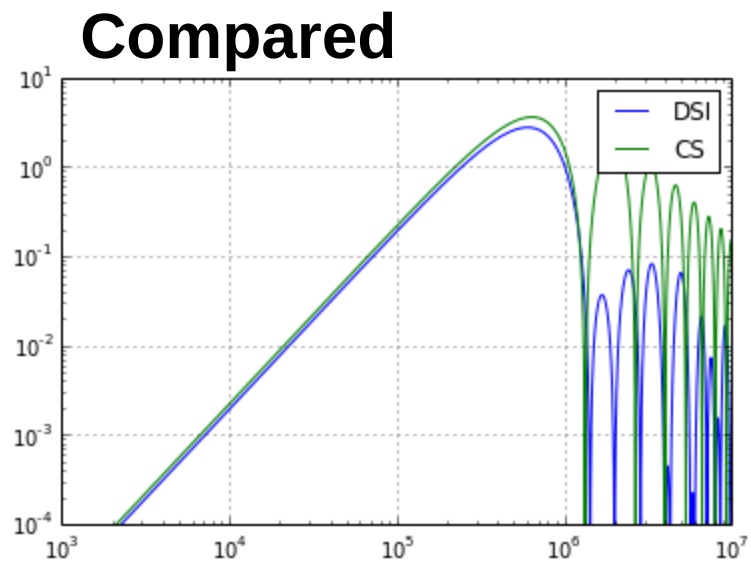
T_S = integration window (typically 25 – 40% of pixel period)
f_{LP}= prefilter bandwidth (single-pole)

DSI and CS transfer functions



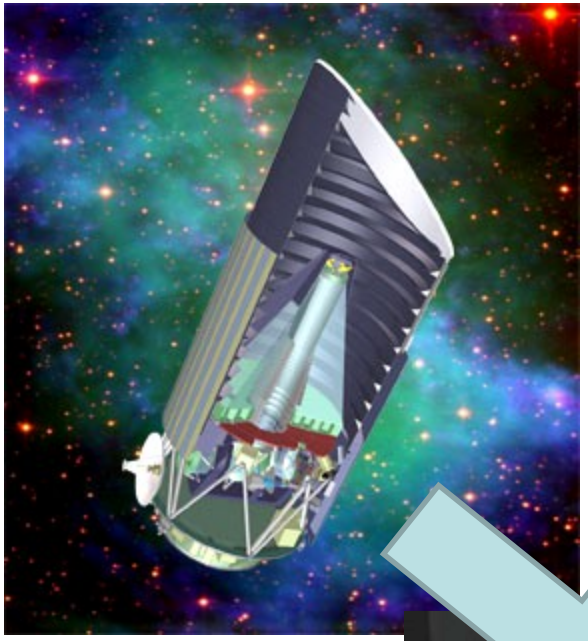


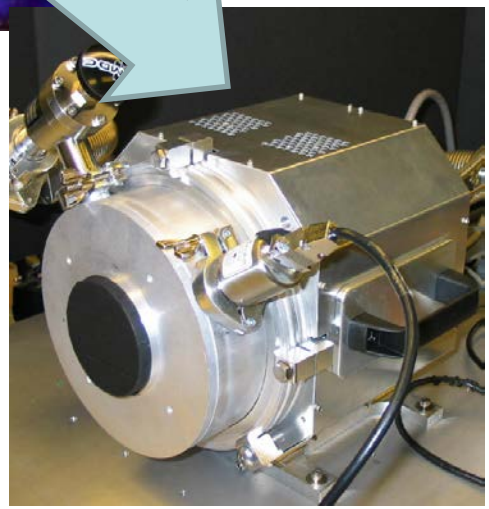




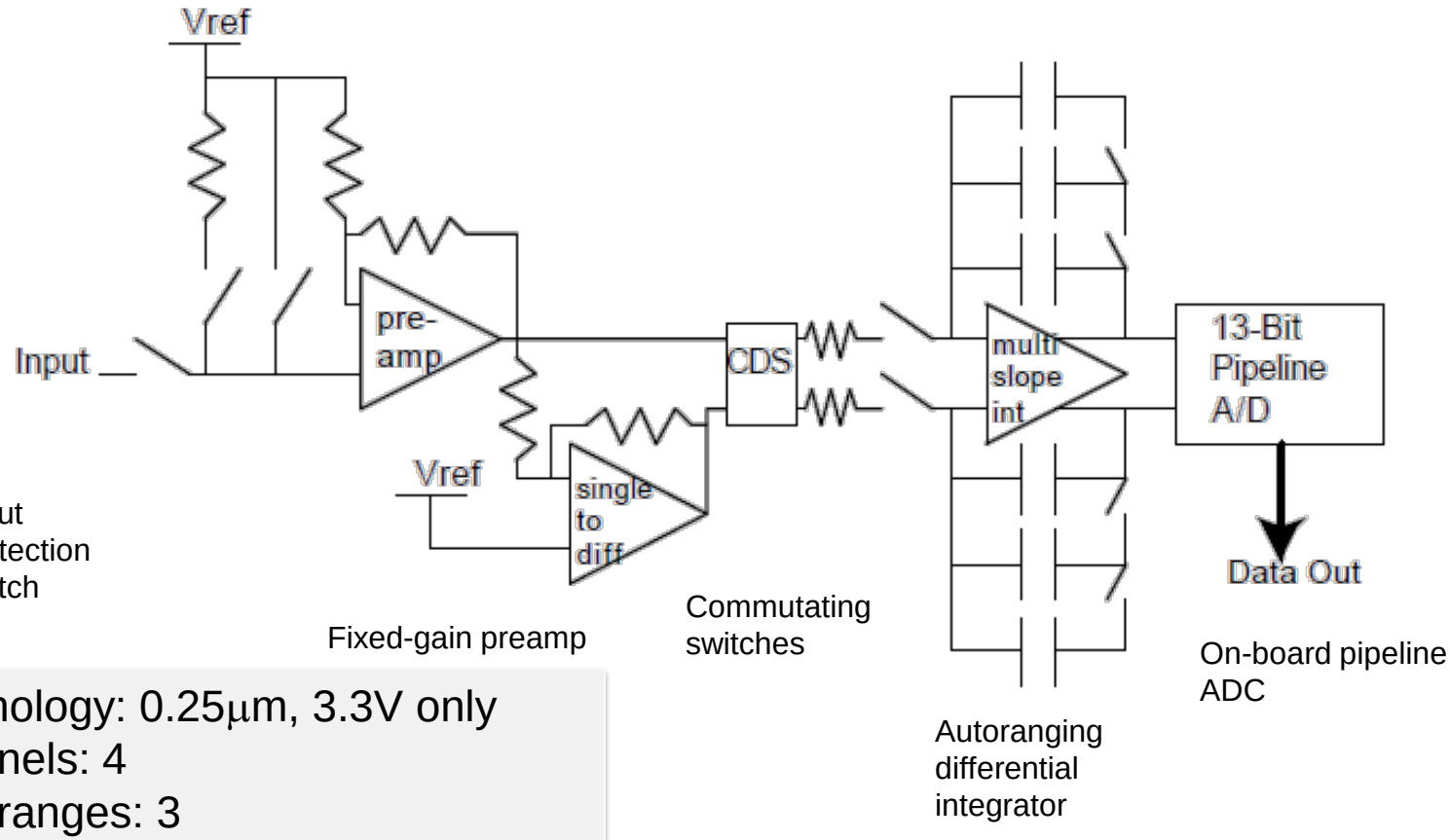
CRIC readout ASIC for SNAP

- Application: highly-integrated readout for high dynamic range space-based astro camera
- Key performance requirements:
  - 16b linearity
  - Auto-ranging front end
  - On-board ADC
  - Radiation tolerance > 10krad
  - Low temperature operation (140K)
  - 100kpix/s readout rate
  - Noise < 2.0e- input referred
  - <20mW/channel
  - High reliability





CRIC readout ASIC for SNAP

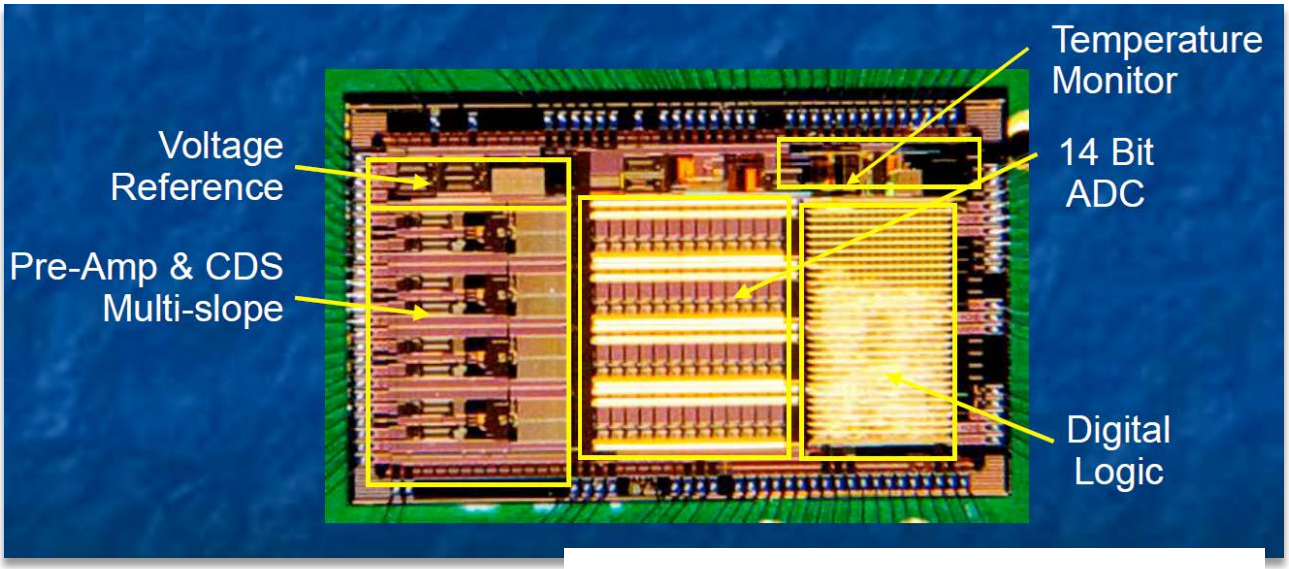


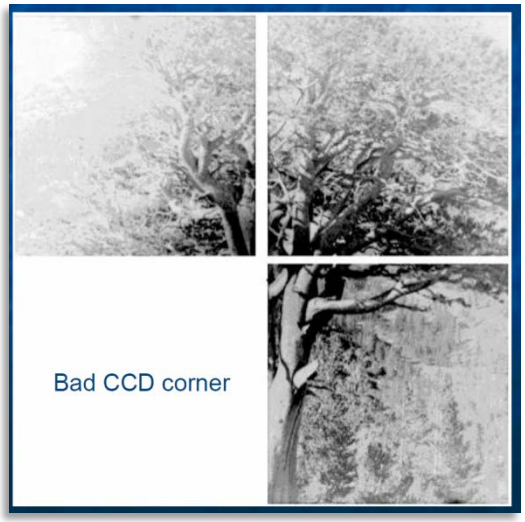
Technology: 0.25μm, 3.3V only
Channels: 4
Gain ranges: 3
ADC DNL: < 1LSB
Equivalent input noise at 100kpix/s:
- high gain: 7μV
- mid gain: 44μV
- low gain: 100μV

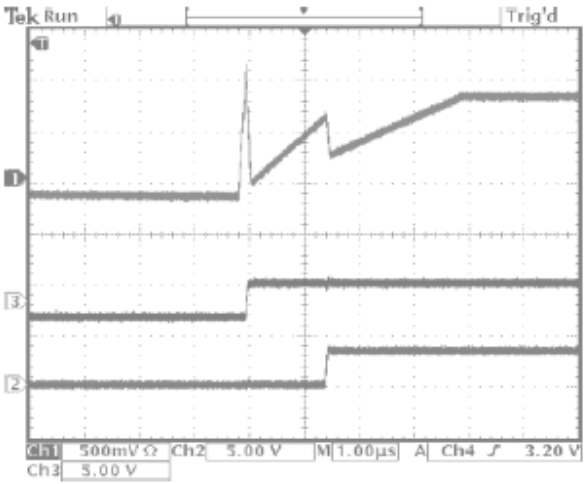
Power dissipation: 17mW/channel

Karcher, Armin, et al. "Integrating Signal Processing and A/D CONVERSION in One Focal Plane Mounted ASIC." Scientific detectors for astronomy 2005. Springer Netherlands, 2006. 691-698.

CRIC performance





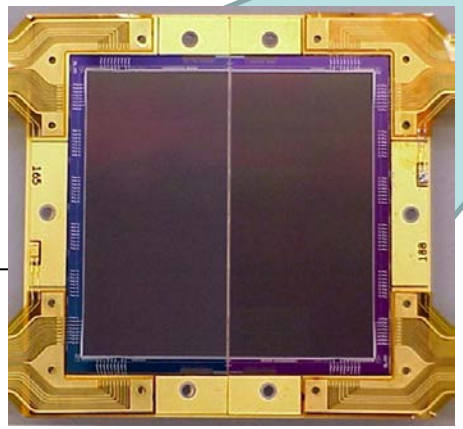


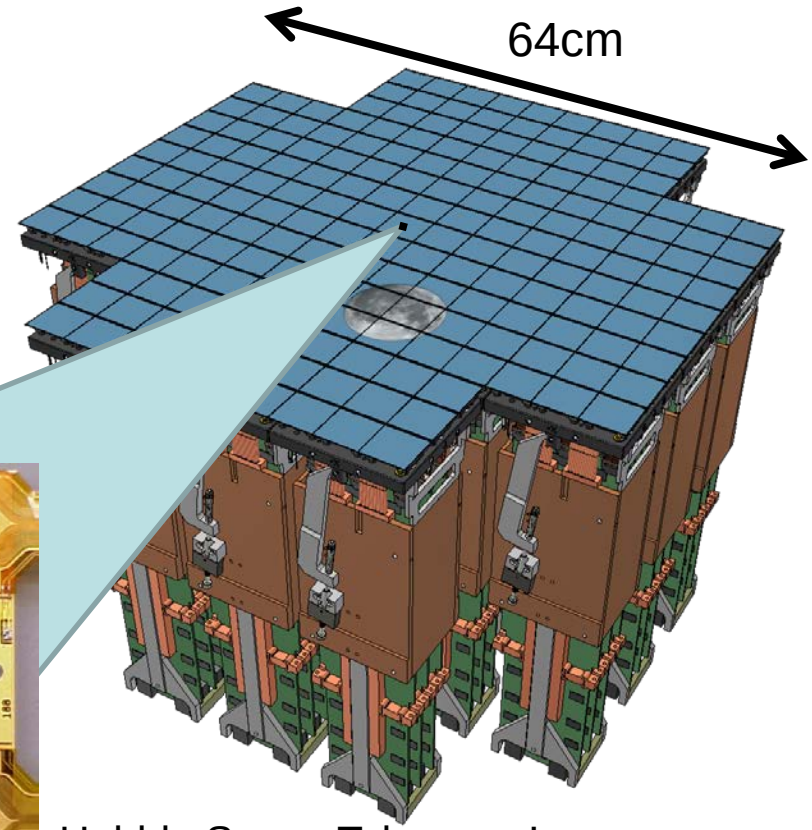
Integrator output for large signal

Range bits

ASPIC readout ASIC for LSST

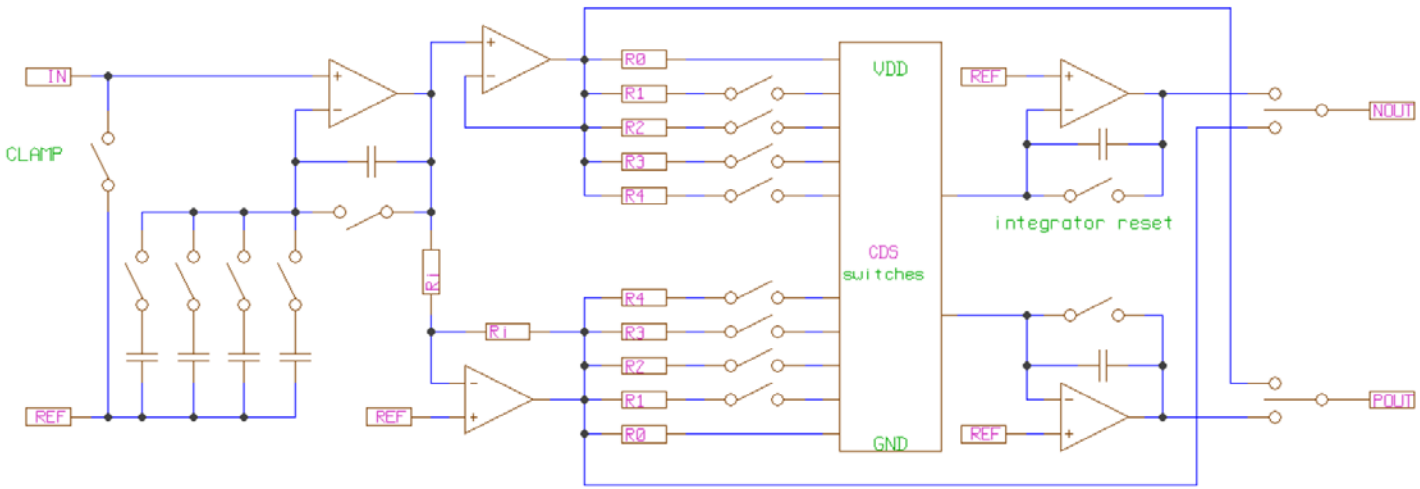
- Application: low-power front end for 3.2Gpix wide-field astro camera
- 201 CCDs (3024 channels) in vacuum cryostat
- Key performance requirements:
  - 550kpix/s readout rate
  - Noise < 2.7e- input referred
  - Crosstalk < 0.04%
  - <30mW/channel
  - High reliability





Hubble Space Telescope's Wide Field Camera

ASPIC architecture



Clamp for DC decoupling

Inverting and non-inverting stages

Commutating switches

Integrator bypass (“transparent mode”)

Programmable-gain preamp

Programmable integrator time constant

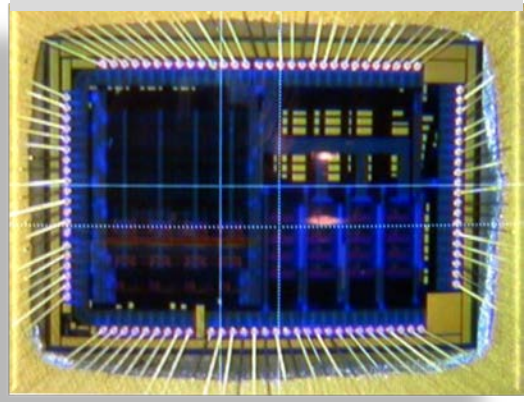
Differential integrator/line driver

Technology: 0.35μm AMS
Channels: 8
Preamp gains: 1 – 6.5, 17 steps
Integrator time constants: 0.25 – 4μs, 16 steps
Equivalent input noise at 500kpix/s, low gain: 12μV
Crosstalk: -74dB
Power dissipation: 25mW/channel

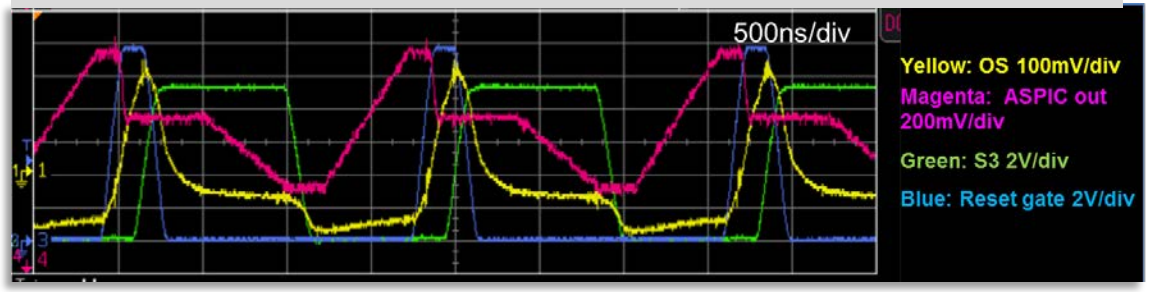
C. Juramy et al., SPIE Proc. 91541P-1, (2014)

ASPIC reading out LSST CCD

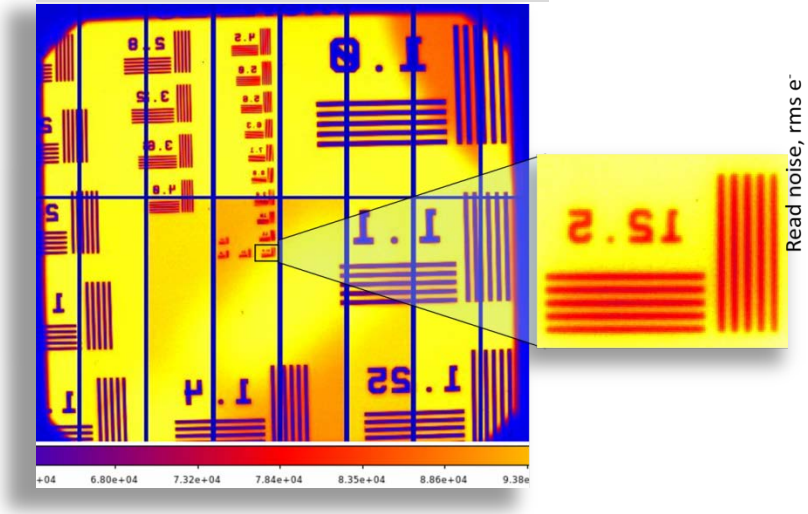
Die Photo



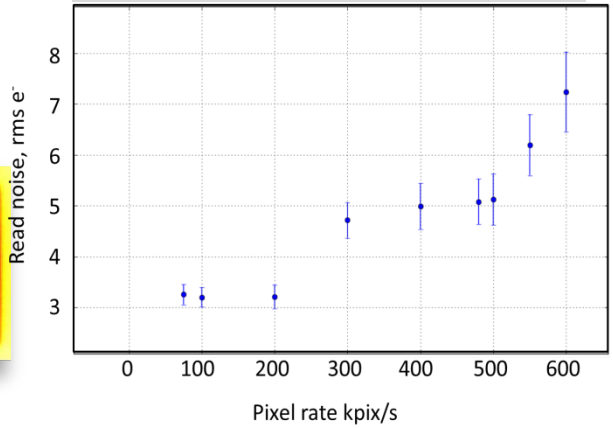
CCD and ASIC waveforms



Target image

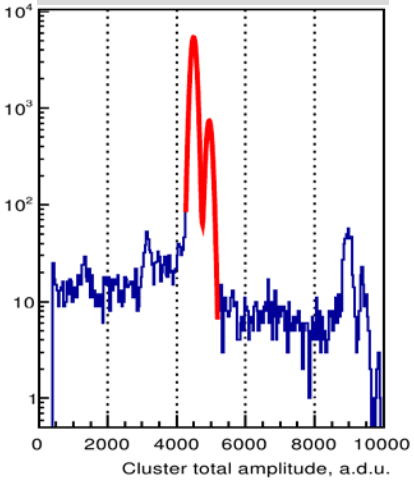


Read noise vs. pixel rate

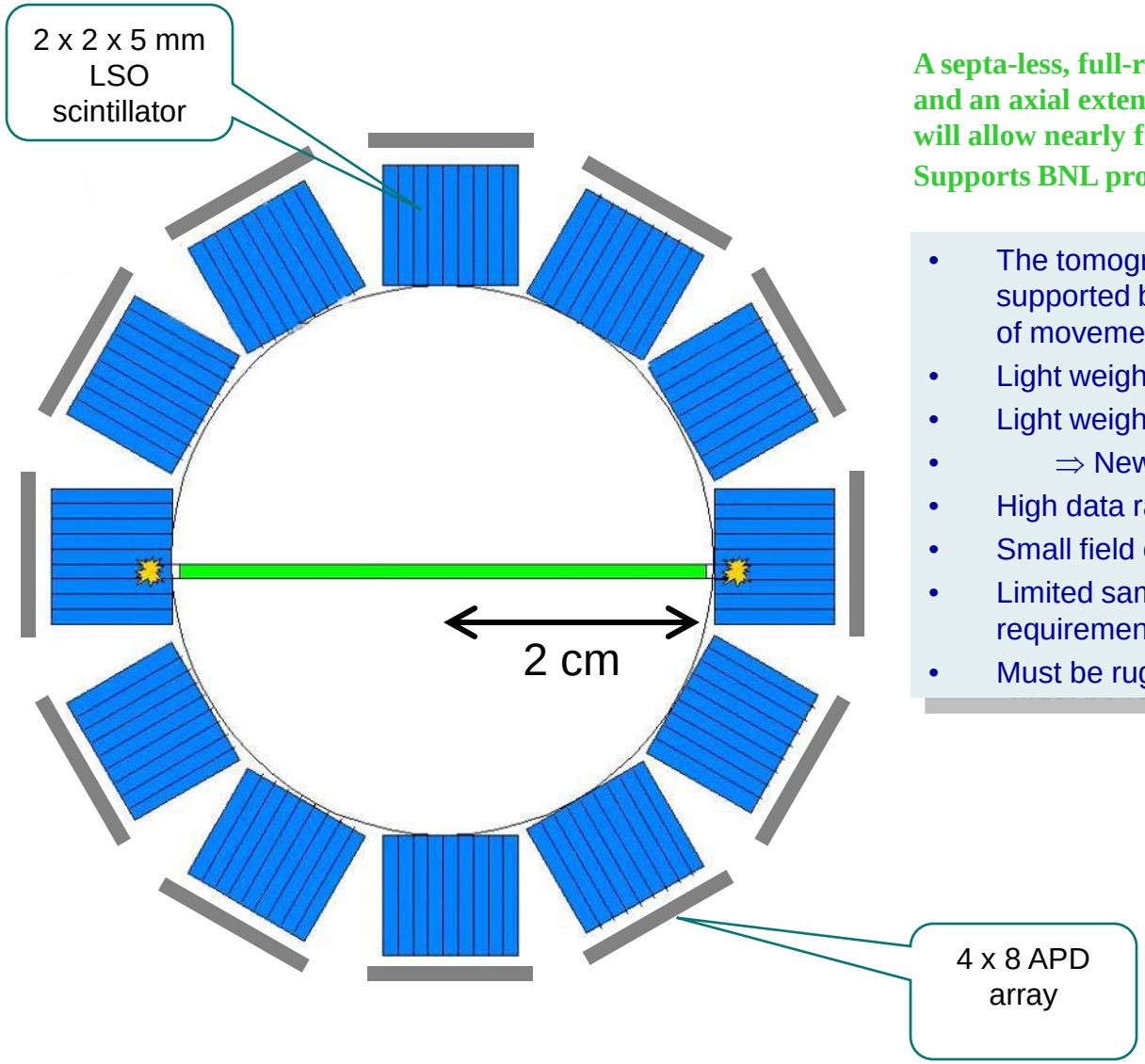


6.2 ±0.5 e⁻ noise @ 550kpix/s

^{55}Fe spectrum

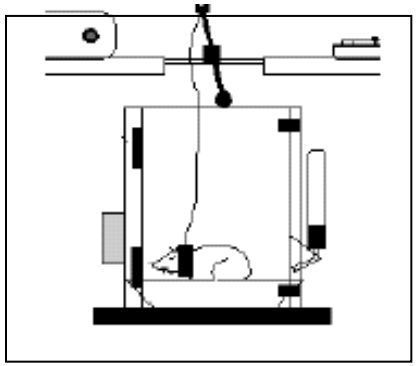


3. RatCAP – Rat Conscious Animal PET

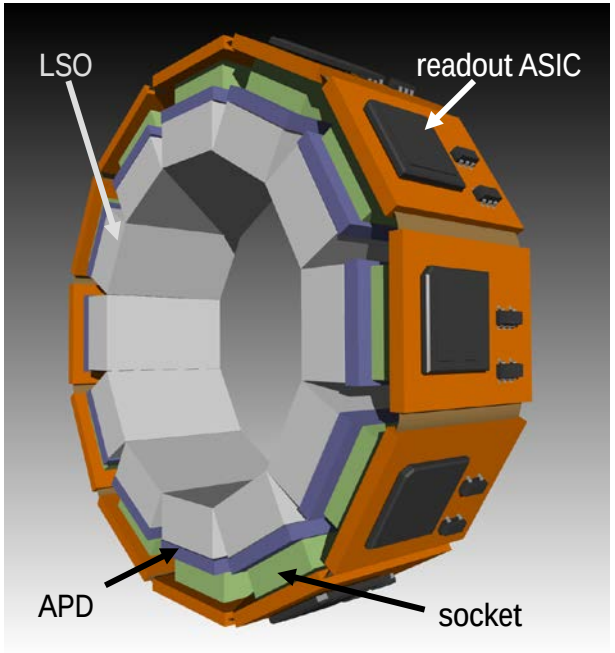


A septa-less, full-ring tomograph with a diameter of 4 cm and an axial extent of 2 cm, suspended by a tether, which will allow nearly free movement of the awake animal. Supports BNL program in addiction research.

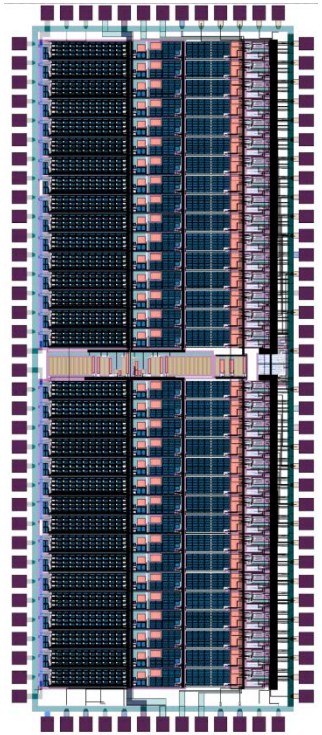
- The tomograph ring must be light enough to be supported by the rat and allow reasonable freedom of movement
- Light weight detectors (~ 150 g total weight)
- Light weight electronics with low power dissipation
- ⇒ New custom ASIC
- High data rates and large singles background
- Small field of view and large parallax effects
- Limited sampling due to space and weight requirements
- Must be rugged enough withstand activity of the rat



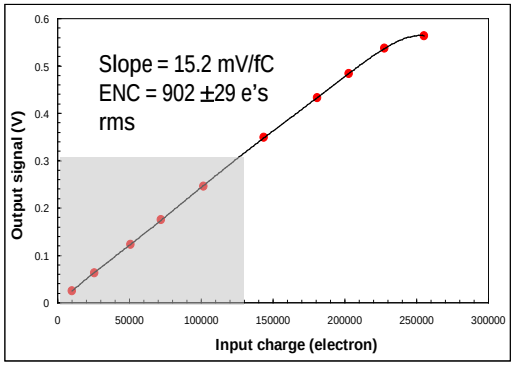
Electronics for a mobile, miniature animal PET tomograph



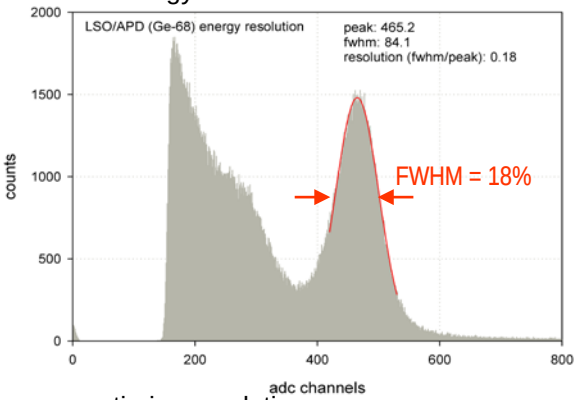
- 0.18 μm CMOS
- 1.5 mW/channel
- 32 channel ASIC
- Preamplifier + shaper + timing discriminator
- address encoding
- serialized output



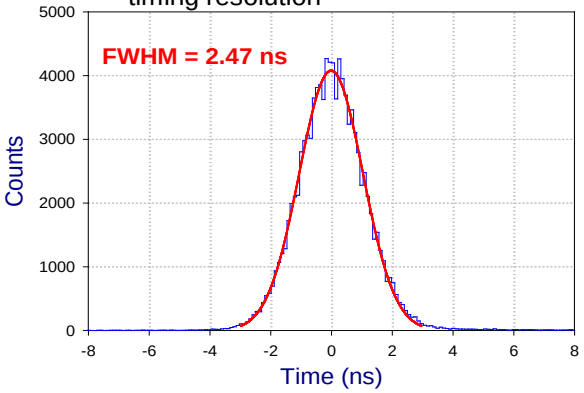
linearity



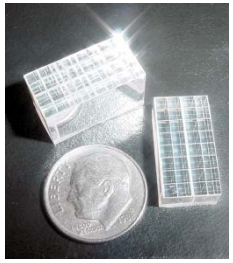
energy resolution



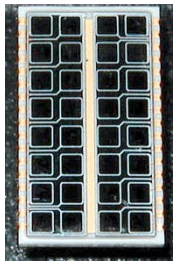
timing resolution



Mockup of the portable ring on the head of a rat



LSO scintillator

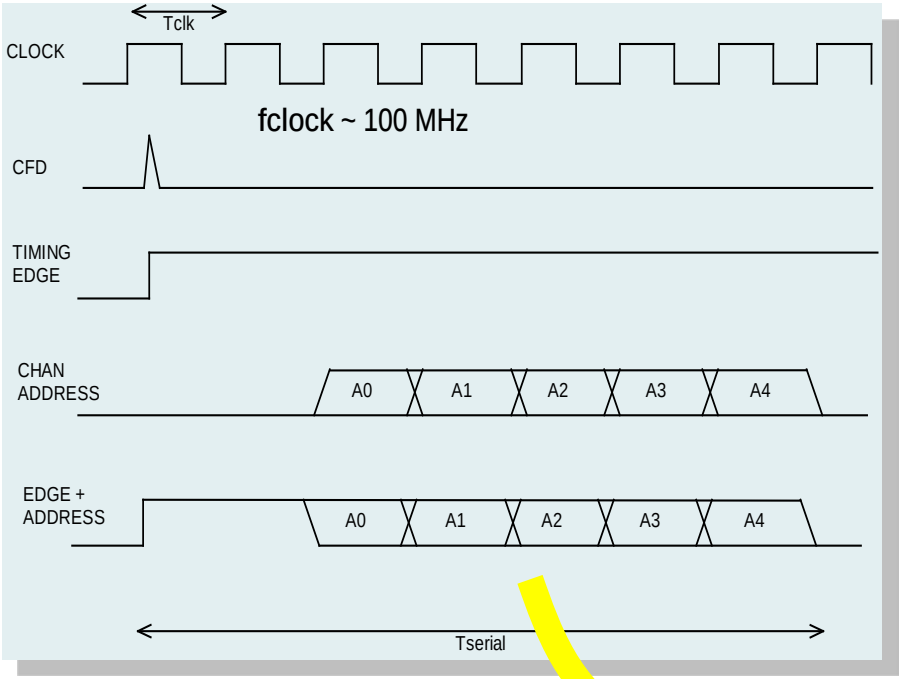


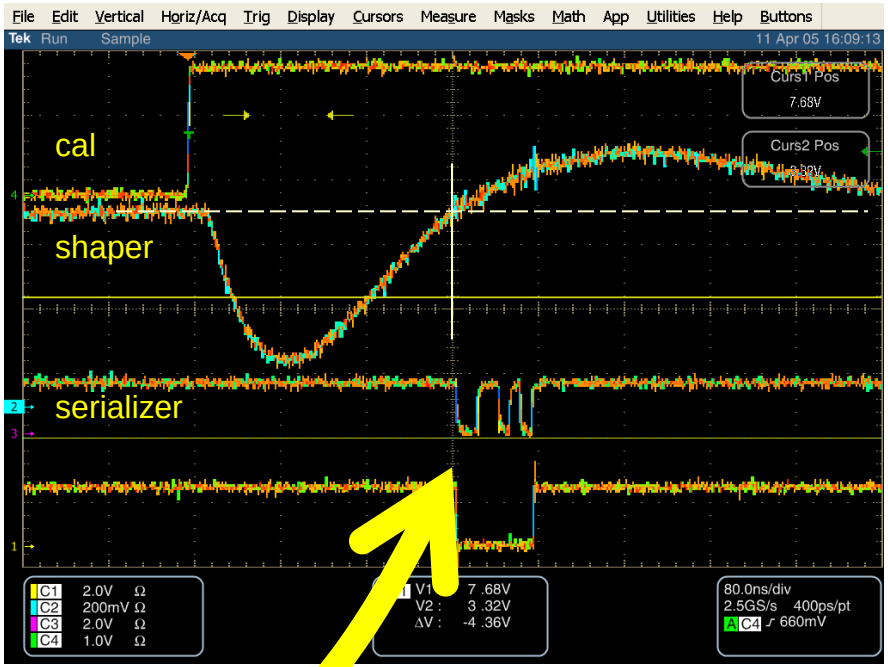
APD array

ASIC preamplifier with CFD vs. BaF_2/PMT

RatCAP ASIC address serializer

- 384 channels on ring make it impossible to bring all signals off detector.
- Analog pulse height information is not saved, lower level discriminator only.
- Discriminator pulse is encoded to give 5 bit address
- Leading edge of encoded serial pulse train gives time information

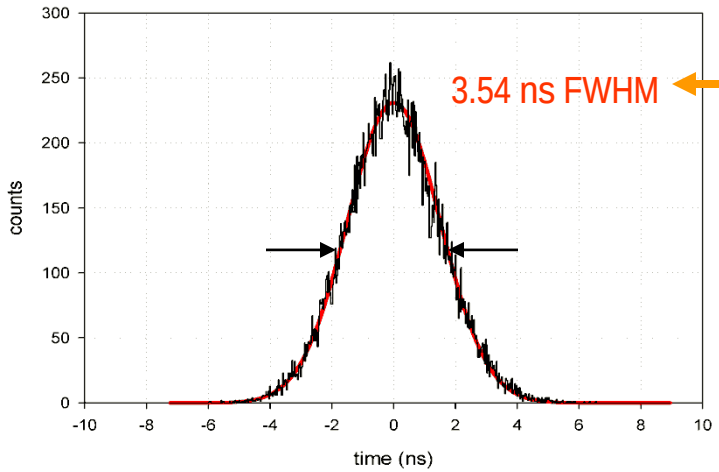




J.-F. Pratte et al., *Front End Electronics for the RatCAP mobile animal PET scanner*, IEEE Trans. Nucl. Sci. 51(4), pp. 1318-1323 (Aug. 2004).

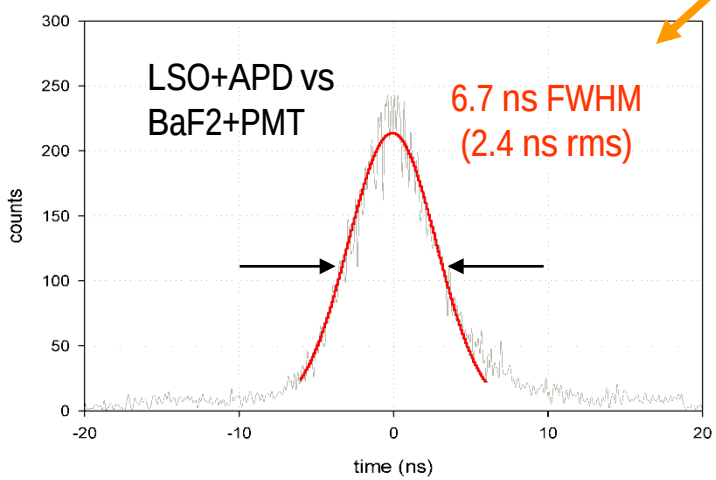
ASIC Performance - Timing Resolution

Preamp/Shaper + ZCD

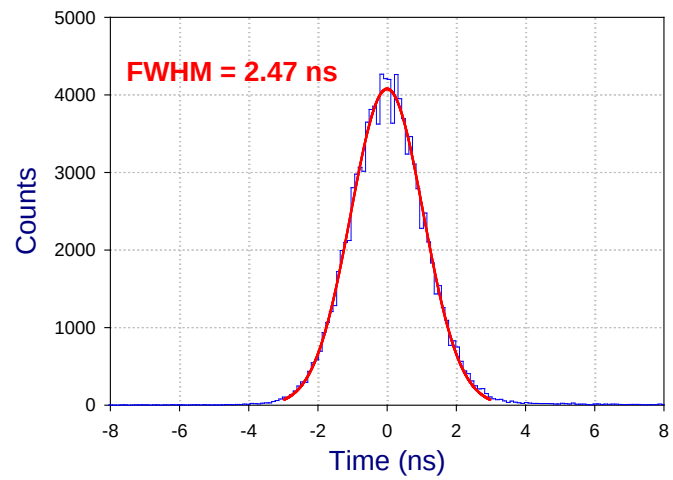


Electronic Timing Resolution at 511 keV equivalent energy

Coupled to LSO/APD with 511 keV γ's timed against a BaF_2 scintillator w/PMT

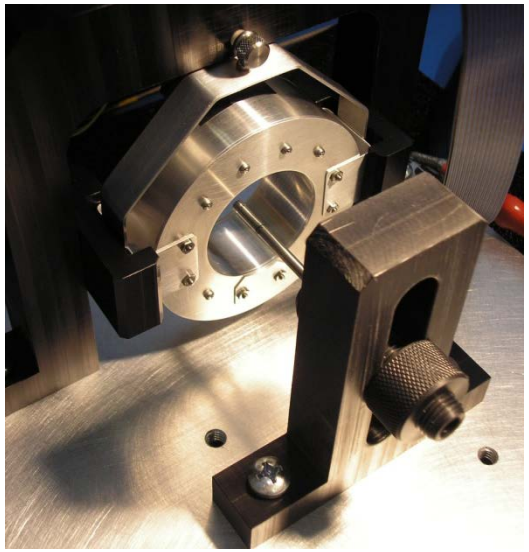


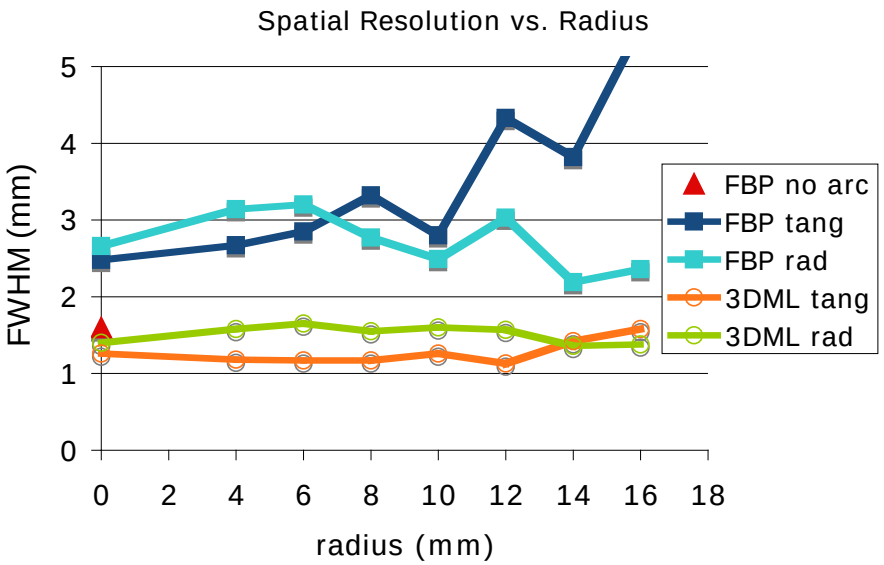
Same with CFD



Spatial Resolution

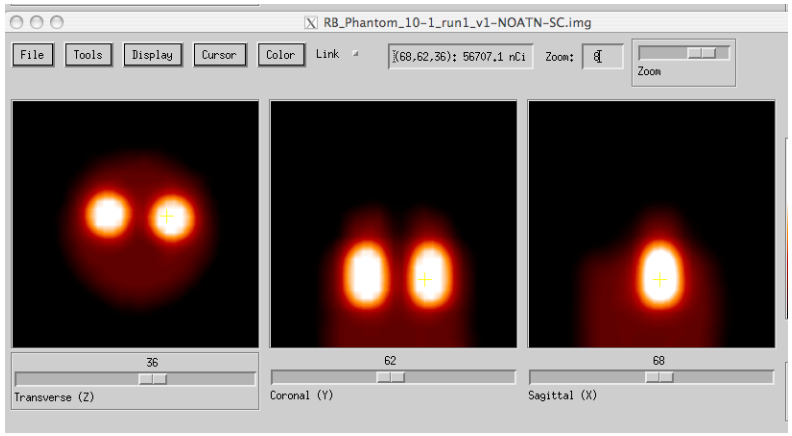
- ^{68}Ge point source
  - ~1 mm dia.
  - r = 0-16 mm
- 2D FBP
  - sinogram arc correction by linear resampling
  - ramp filter
- 3D Monte Carlo MLEM
  - 50 iterations
- Note:
  - arc correction parameters to be optimized
  - point source size NOT deconvolved

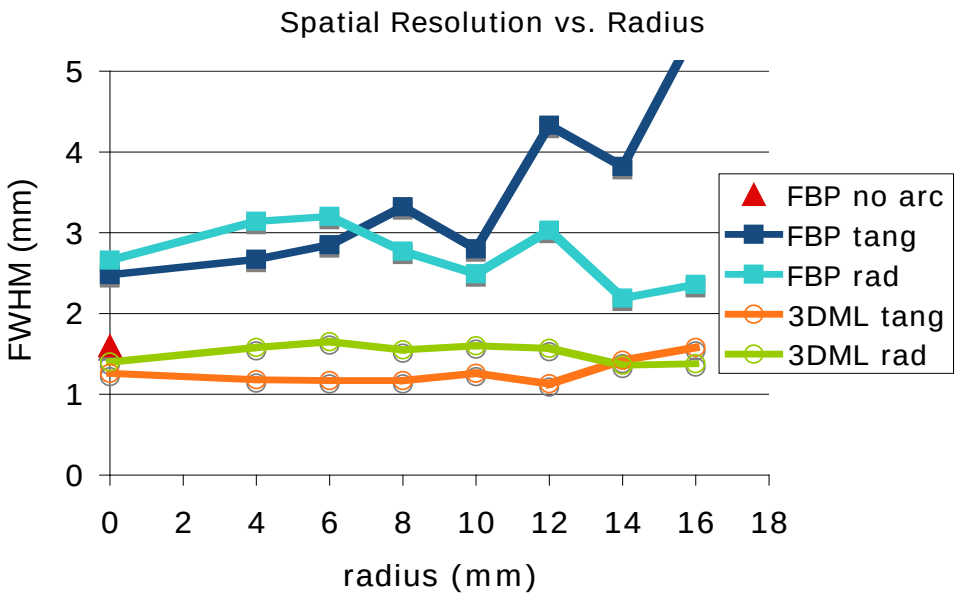




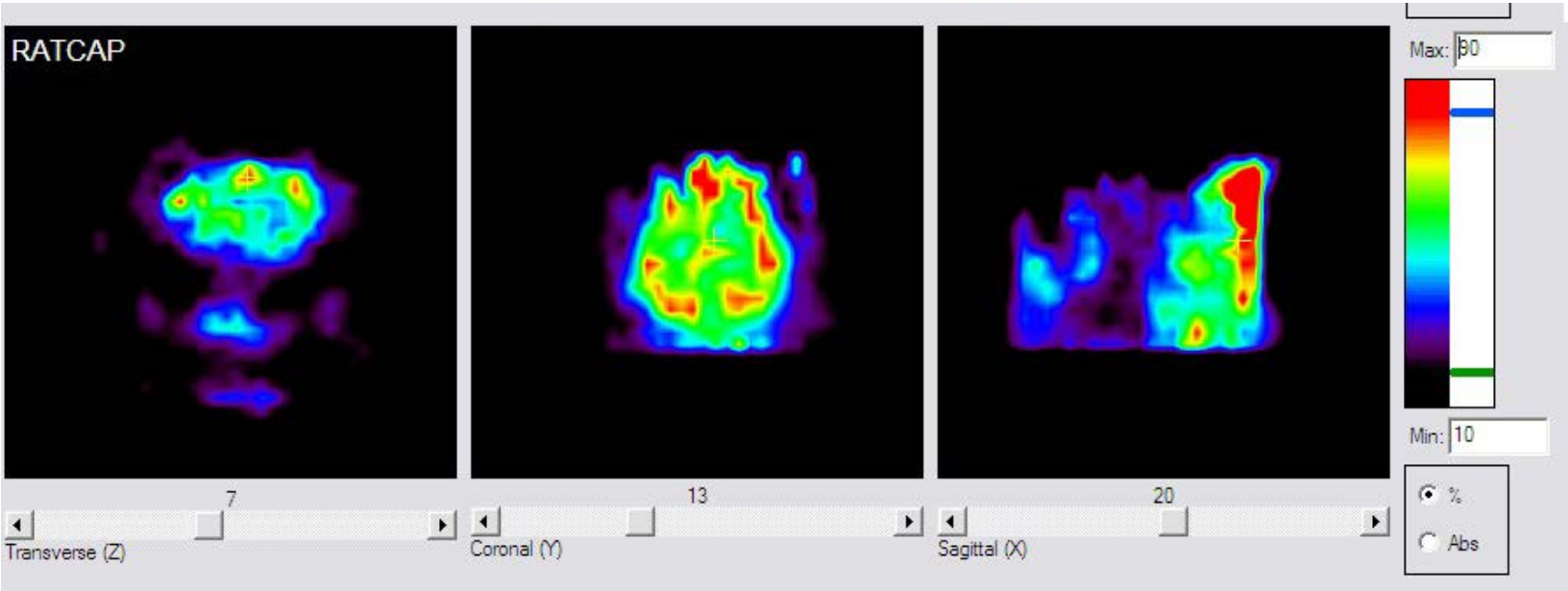
First Phantom Data

- Rat striatum phantom
  - 3.4:1 ratio
  - RatCAP
    - MLEM
    - 25 iterations
    - post-smoothing with 2 mm FWHM Gaussian

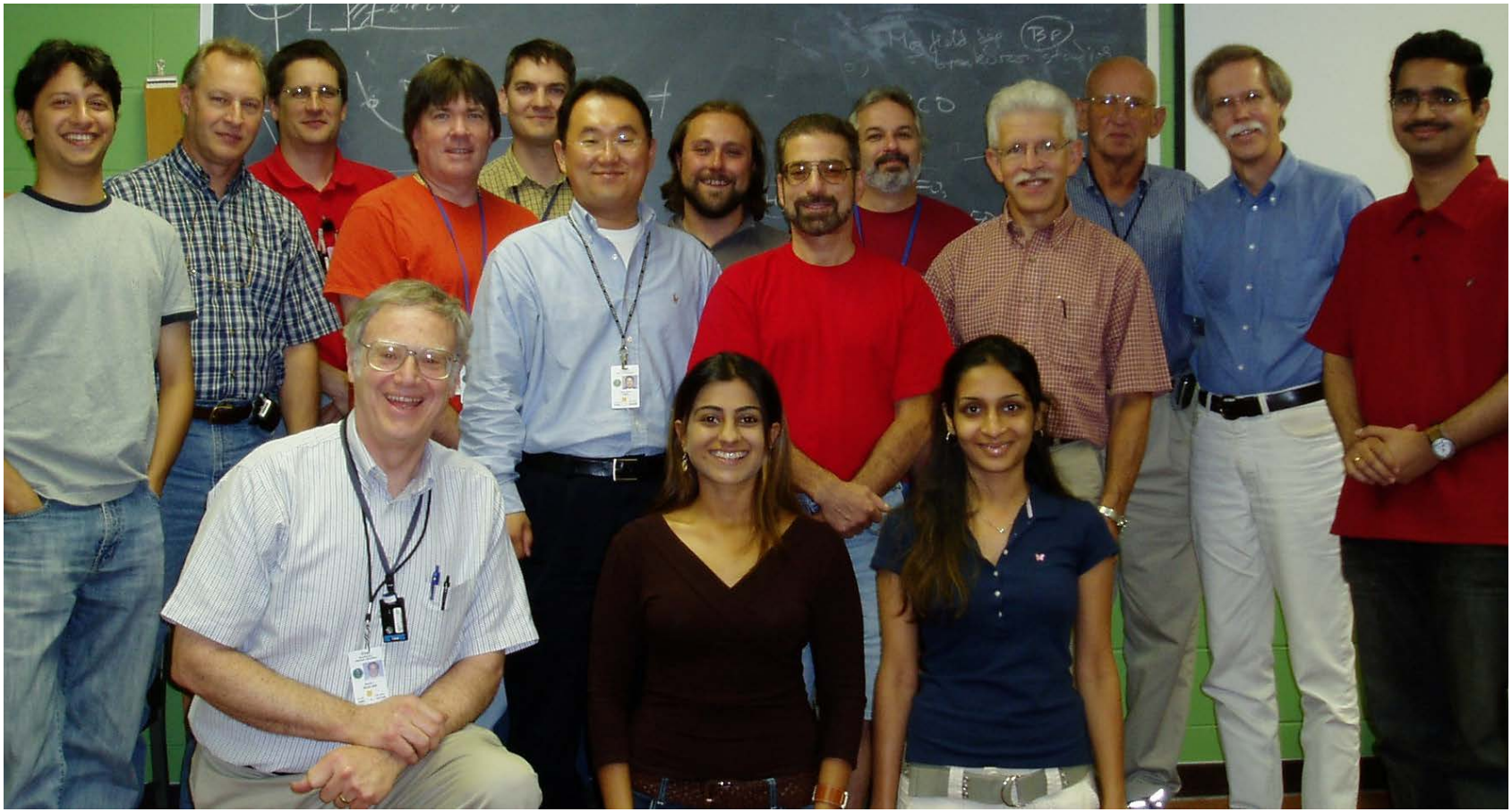




First conscious rat brain image



Thanks!



BNL RatCAP team