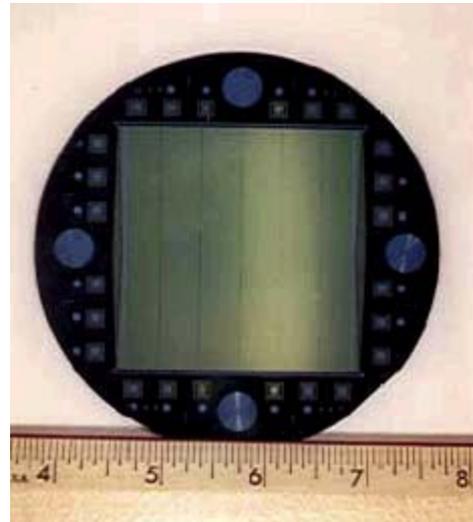
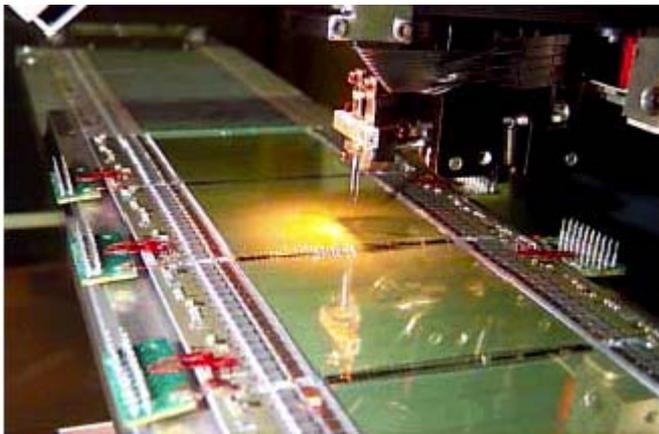


Electronics in High Energy Physics

BNL Instrumentation Division

- 20 scientists/professionals, 25 tech/admin
- Detector research and Electronics design for
 - High energy physics
 - Nuclear physics
 - Synchrotron radiation research
 - Medical instruments
- Major facilities
 - Gas detector lab
 - Silicon detector clean room
 - Printed circuit shop
 - Irradiation test facility

Detectors



HEP applications

- Modern detector $10^7 - 10^9$ channels
- Cost of detector \$500M
- Cost of electronics about 1/3
- Cost per channel $< \$10$
- Requires
 - High level of integration
 - Custom integrated circuits

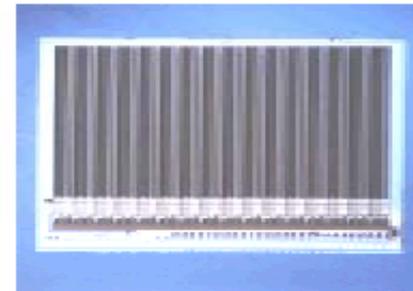
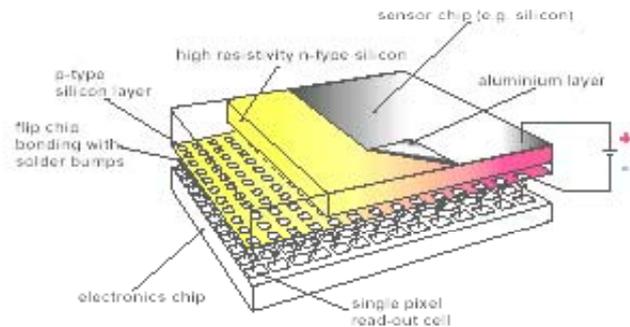
Electronics categories

- Front ends
 - Trackers
 - Fast, dense, binary decision, high radiation
 - Calorimeters
 - Large energy range
 - Muon
 - Large area
- Data links
- Data acquisition
- Trigger
- Timing
- DCS

Front end

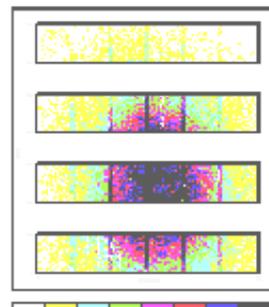
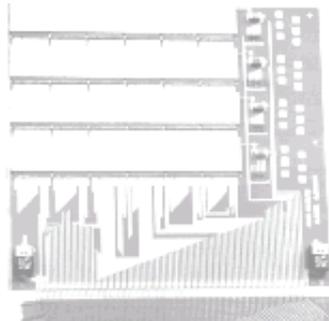
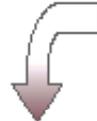
- Charge amplifier
- Threshold detection
- Time of arrival
- Analog sampling and storage
- Analog-to-digital conversion

Example : Hybrid Pixel Detectors (CERN RD-19 E. Heijne et al.)

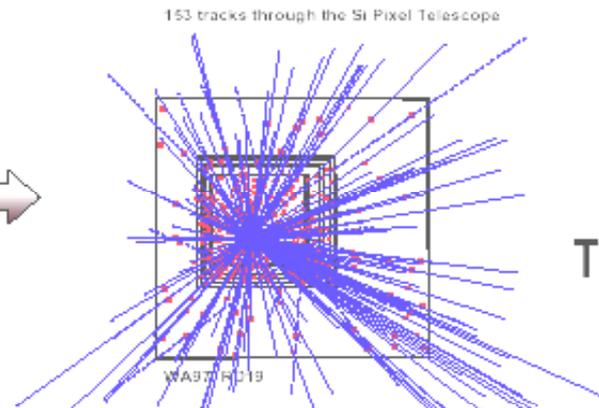


**LHC1 : 2000 CMOS
readout channels**

**Pixel Ladders
(6 chips)**



Half plane ~ 50 000 sensing elements

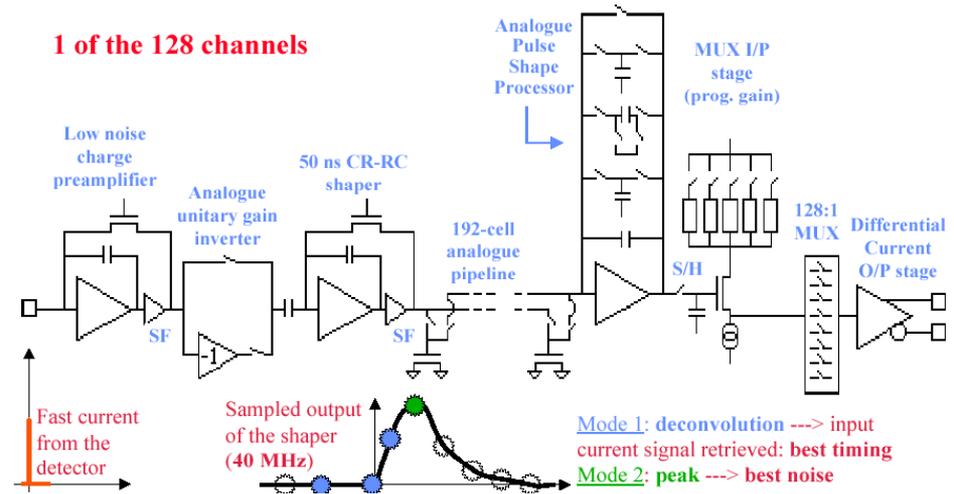


**153
Tracks !**

**WA97 NA57 Experiment
1.2 M channels**

CMS silicon strip readout

Prototype of layer 3 in the Inner Tracker



230 m² Si

12 million pixels

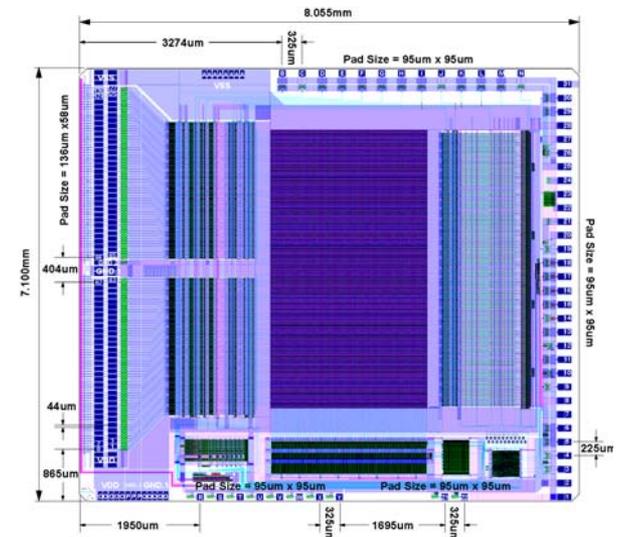
92,000 APV-25 chips

APV-25: 0.25 μ m CMOS

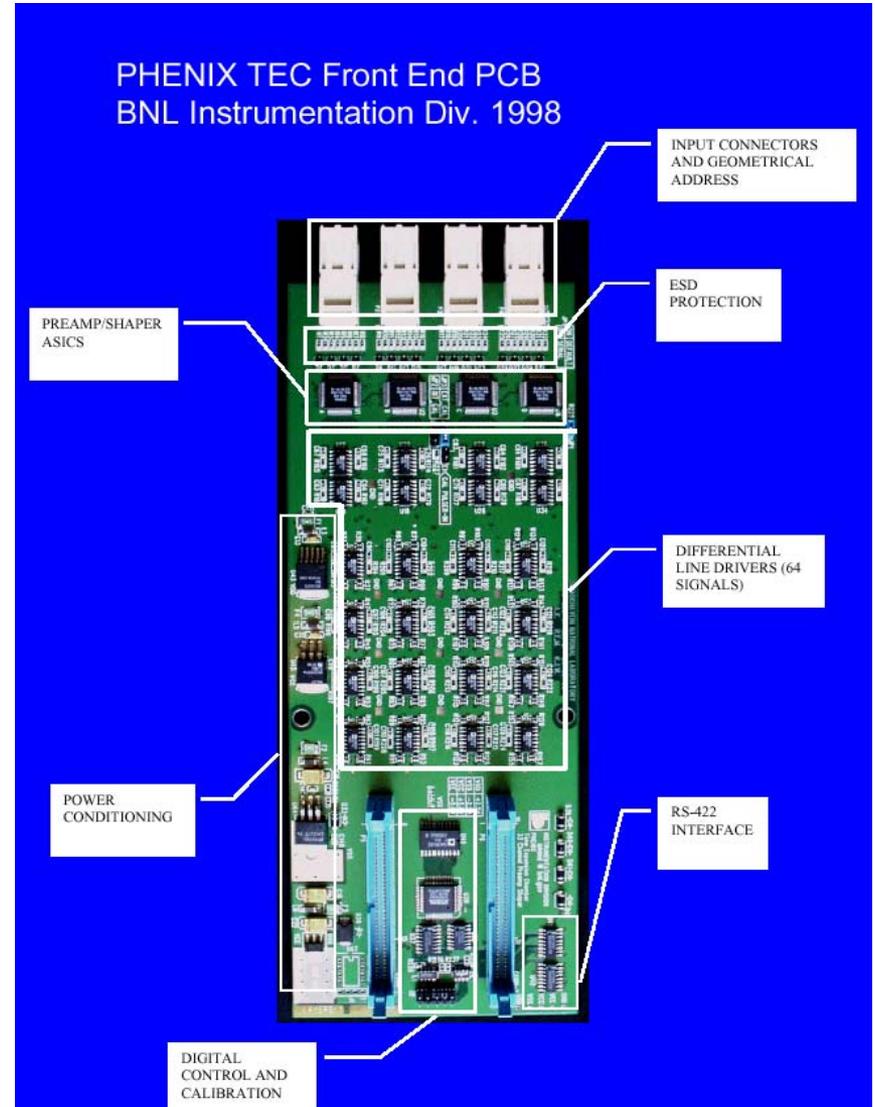
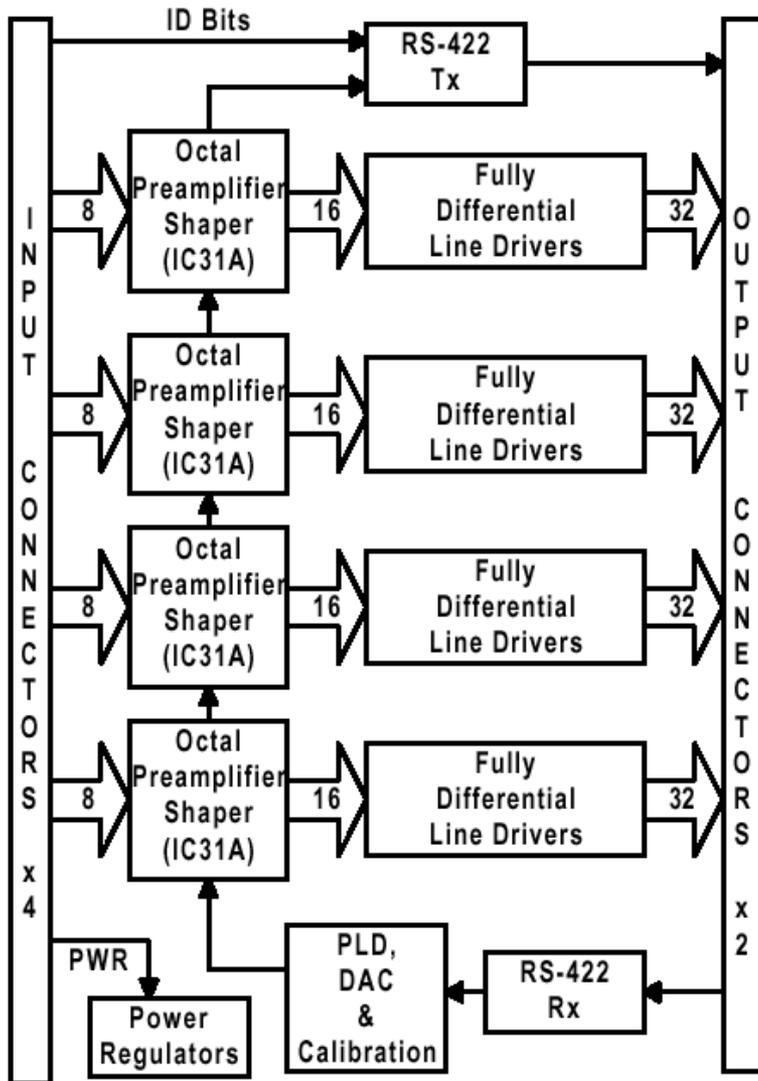
128 chan X 192 bucket P/S, SCA, mux

246 + 36.3 e/pf, 2.3mW/chan, 2% nonlinearity to 5 MIP

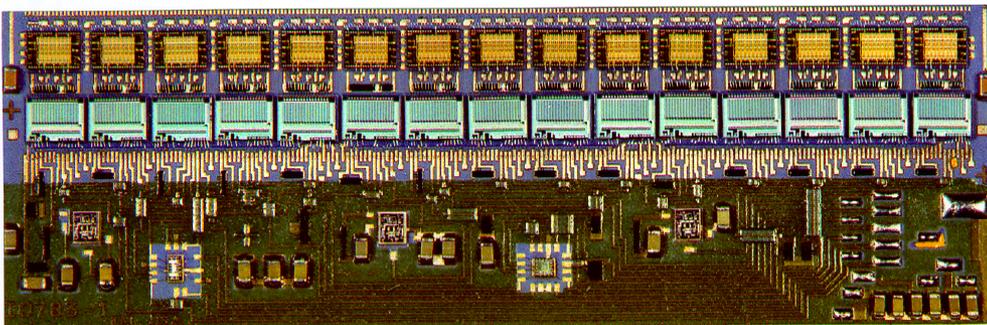
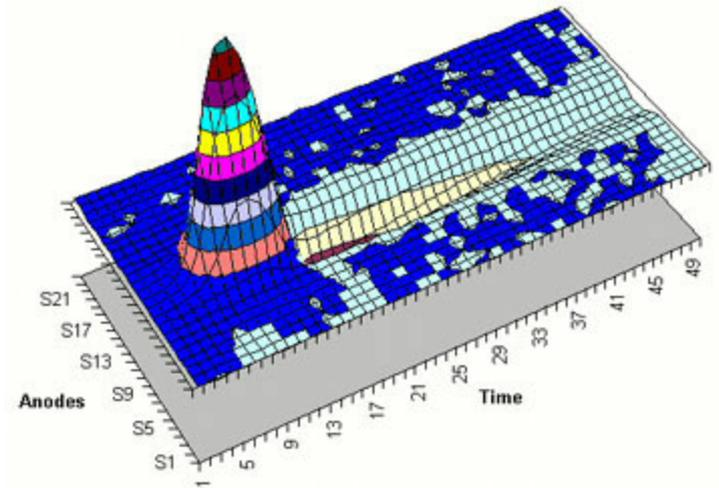
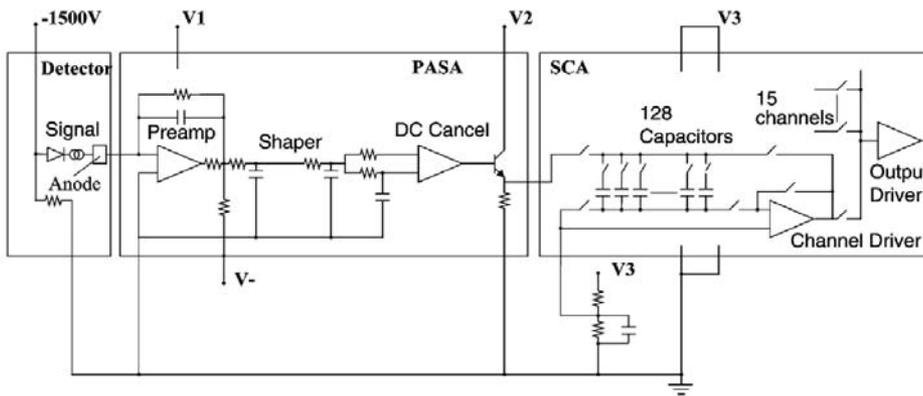
7.2 X 6.5 mm, 85% yield



TEC Front-End Card



SVT 240-channel Multi-Chip Module



D. Lynn et al., "A 240 channel thick film multi-chip module for readout of silicon drift detectors", NIM A439 (2000), 418 - 426

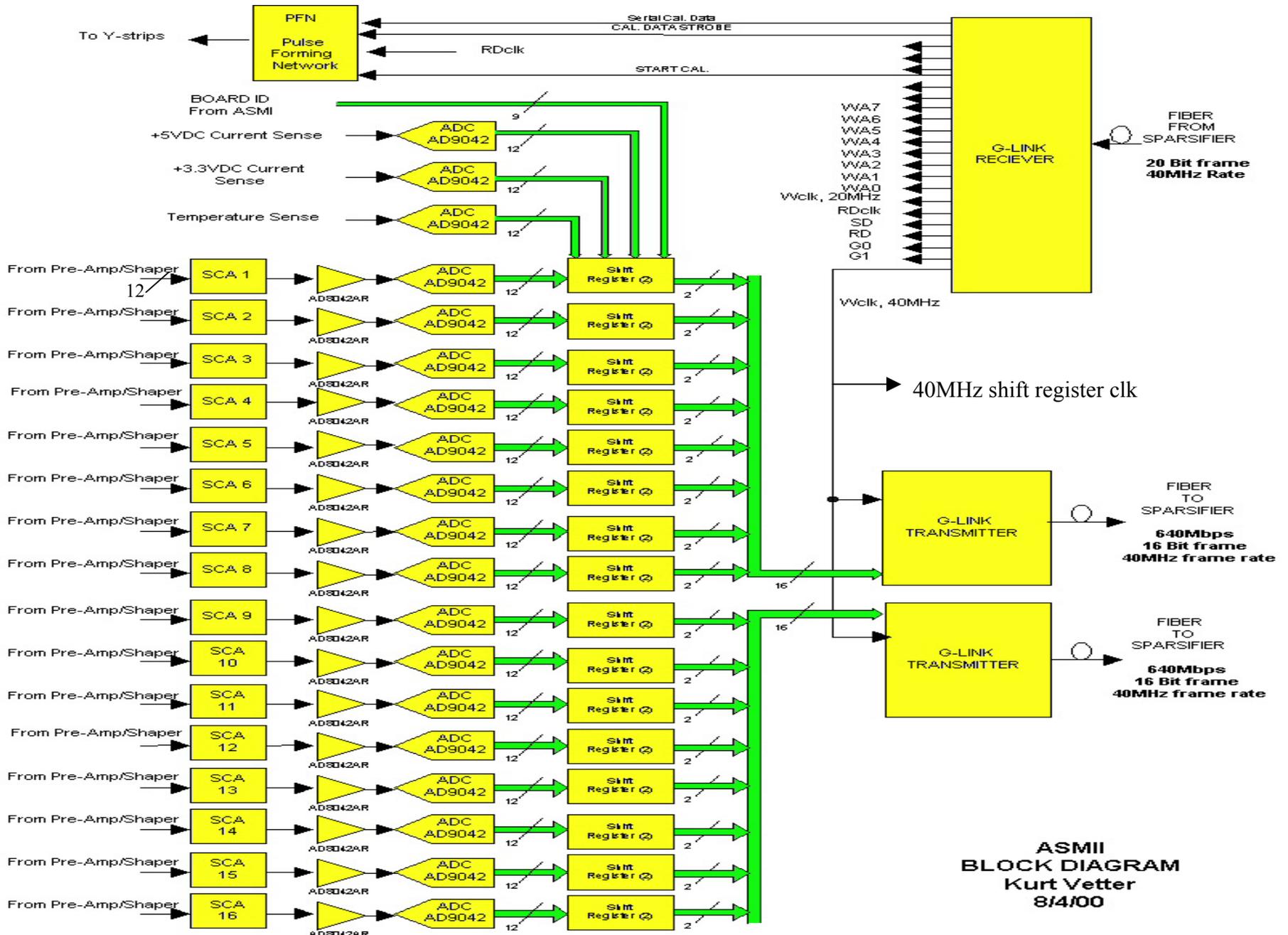
Data link

- Can be analog or digital
- Optical links preferred
- Up to 1.4 Gbits/s
- Many thousand links per detector

Data acquisition

- Receive data from front end
- Digitize
- Zero suppression
- Feature extraction
- Formatting
- Transmit to central DAQ

ASMI Block Diagram



Trigger

- Examine prompt data from a subset of detector
- Decide if event is of interest
- Issue trigger decision yes/no
- Important to minimize time to decision
- Distribute trigger to all sections of detector

Timing system

- All segments of detector have to be synchronized
- Fundamental frequency (clock) linked to accelerator frequency

Detector control system (DCS)

- Monitor environmental conditions at detector
 - Temperature
 - Magnetic field
 - Alignment
 - High voltage
 - Gas properties
 - Cooling system

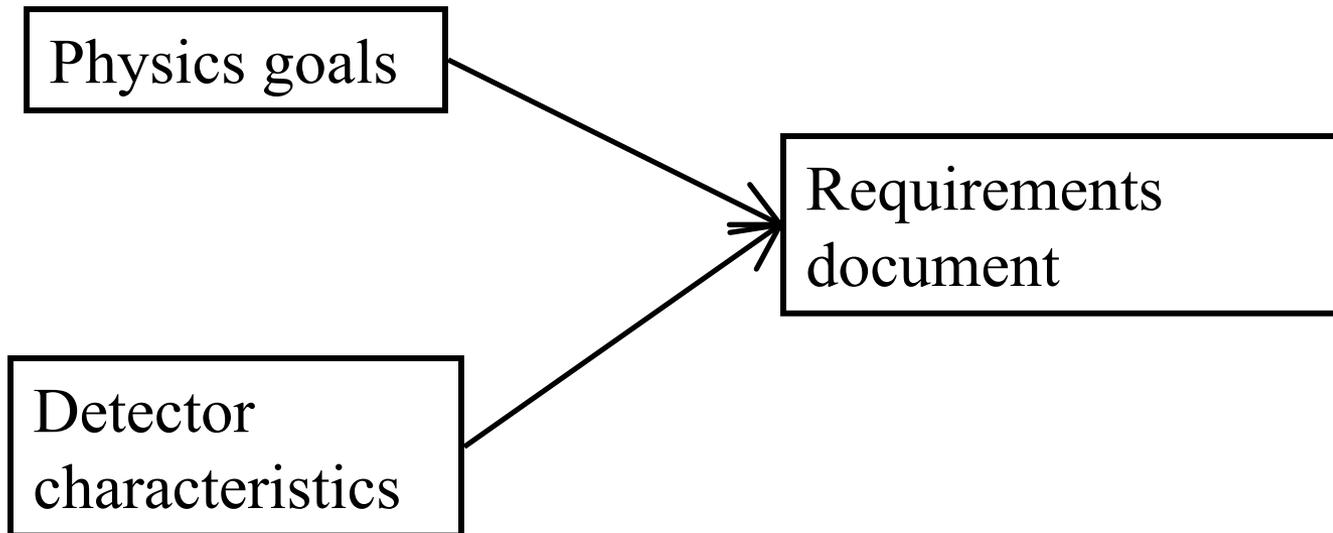
Infrastructure

- High voltage power
- Low voltage power
 - Many kA
 - Hard to transmit over long distances
- Cabling
- Cooling

Integrated circuit design

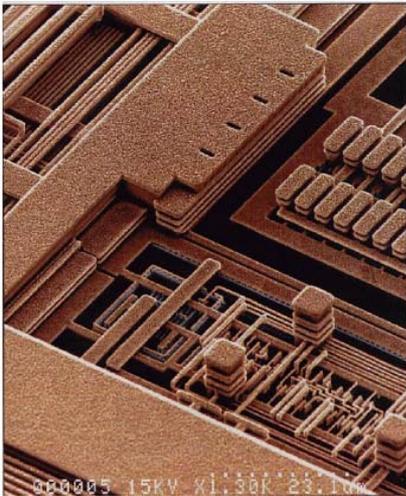
- Design process
 - Choose foundry
 - Get models, design rules
 - Schematic capture
 - Simulation
 - Layout
 - Verification
 - Physical
 - Logical
 - Transmit design to foundry
 - Receive processed chips

What do we need to build?

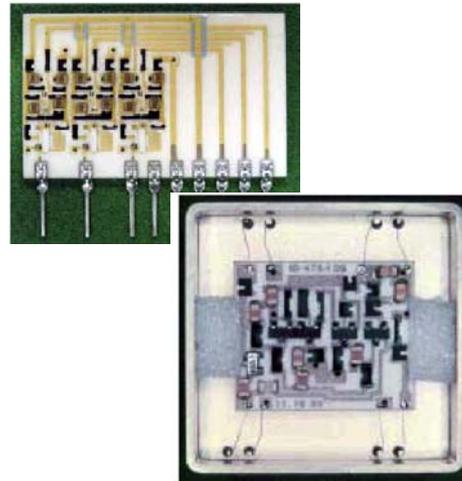


What technology to use?

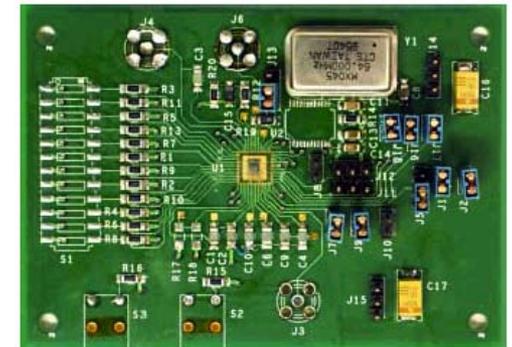
Submicron CMOS



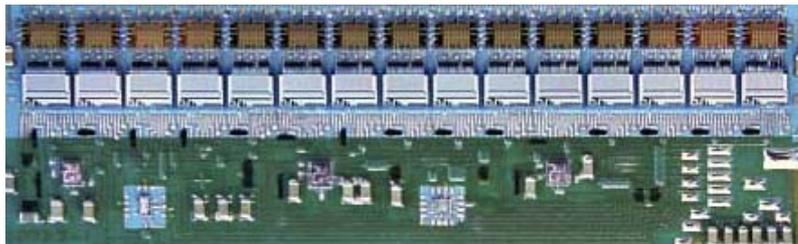
Ceramic Hybrid



Chip-on-board



Multichip module

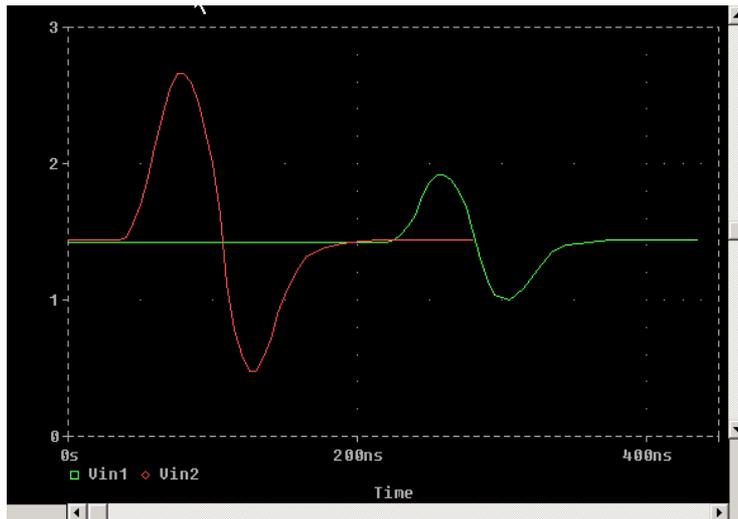


Surface-mount PCB

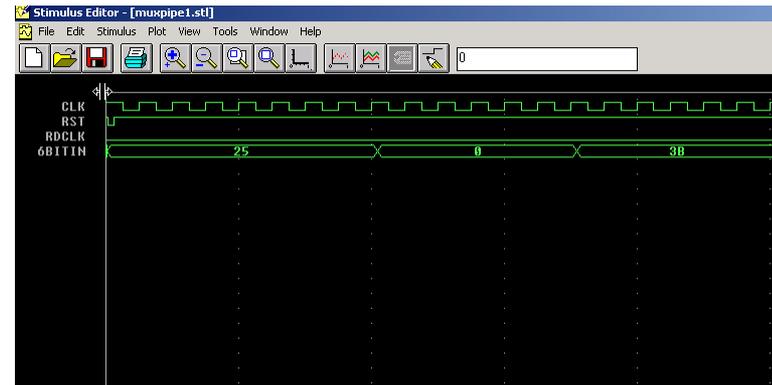


What input signals will the circuit receive?

Analog stimulus waveform

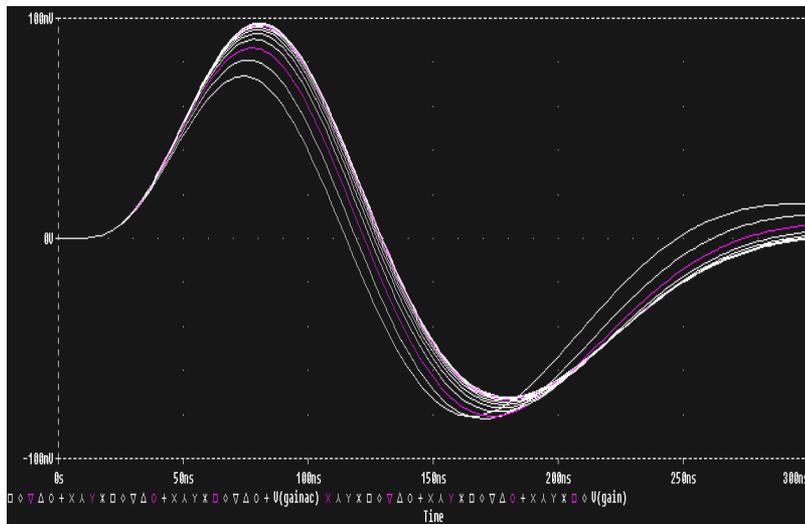


Digital test vector

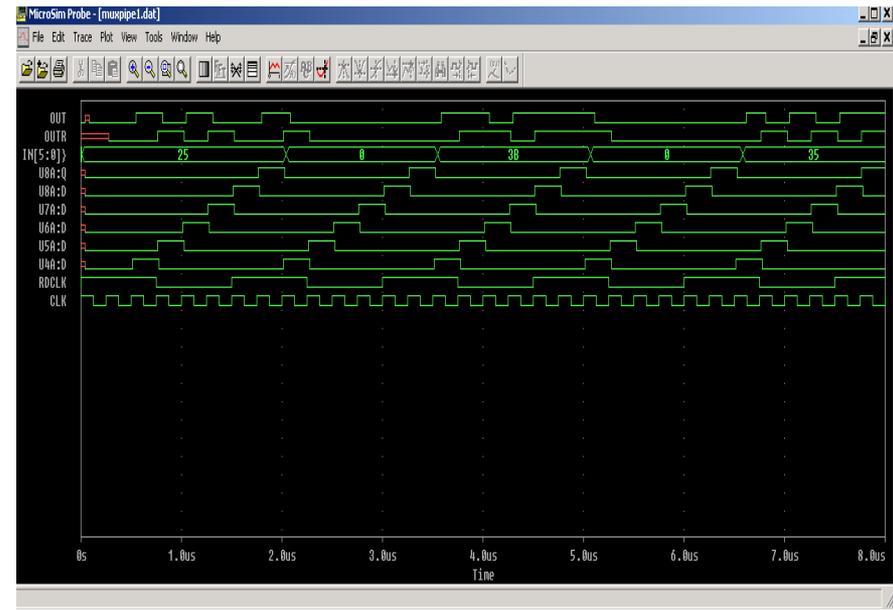


How will the circuit respond to inputs?

Analog simulation

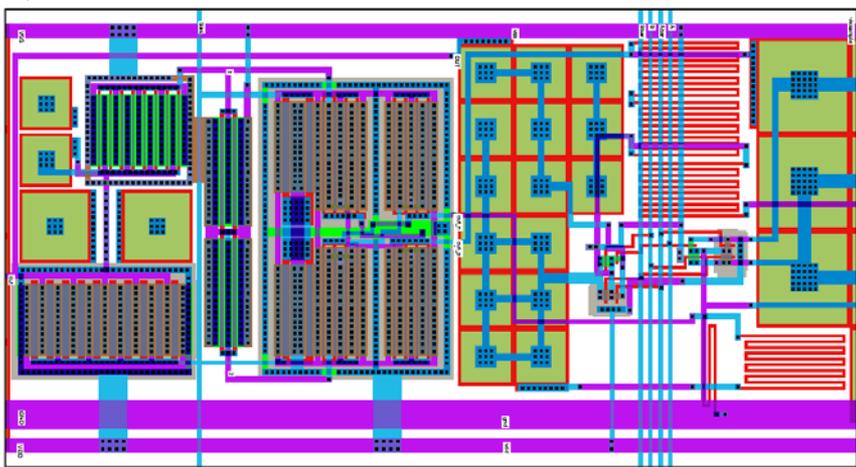


Digital timing simulation

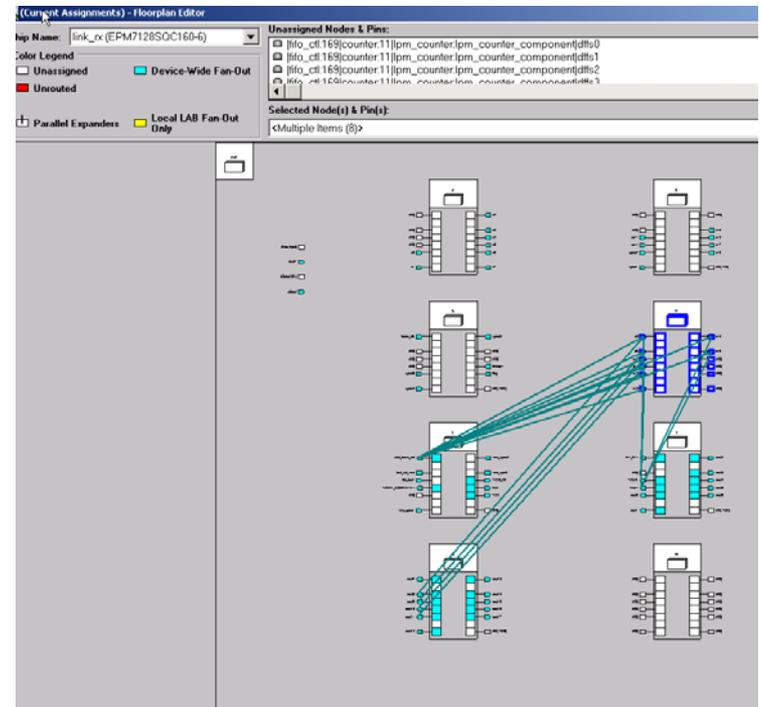


How physically will our circuit be constructed?

Analog CMOS layout

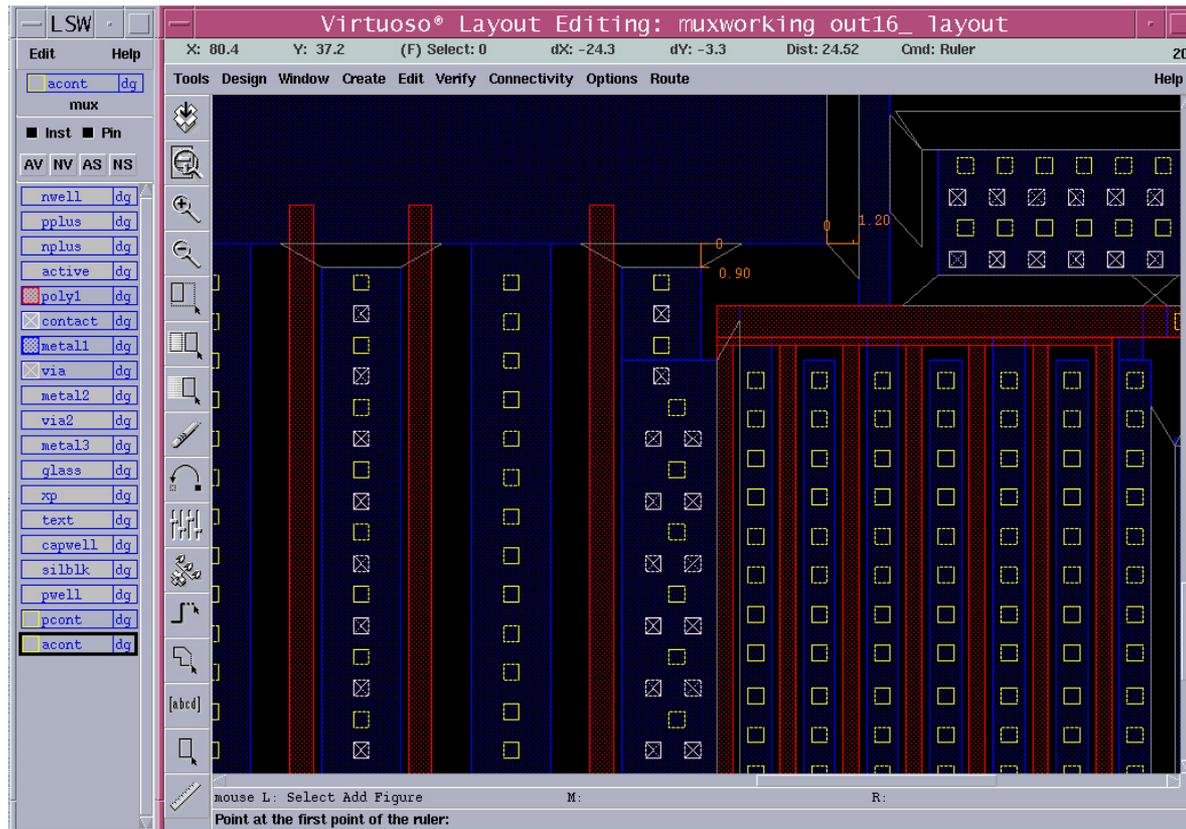


Digital: FPGA floorplan



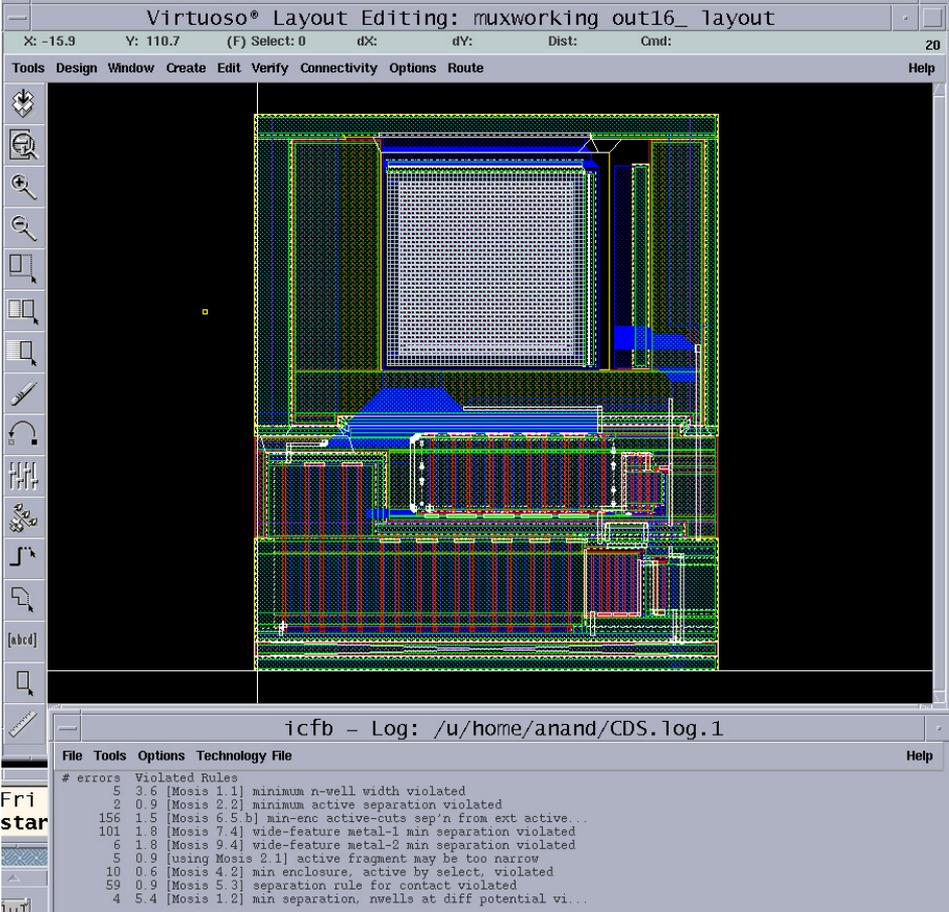
Does our design conform to the rules of the fab?

Design rule checker



Does our physical design correspond to our schematic?

Layout-vs.-
Schematic
comparison

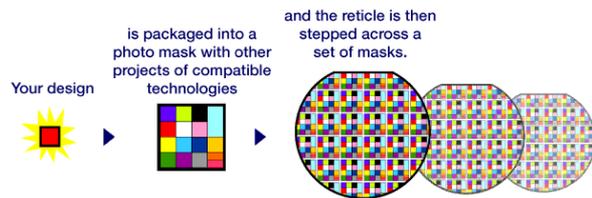


The screenshot shows the Virtuoso Layout Editor interface. The main window displays a physical design layout with a schematic overlay. The layout is a complex circuit board design with various components and connections. The schematic overlay is a grid of lines representing the circuit connections. The error log at the bottom lists the following violations:

# errors	Violated Rules
5	3 6 [Mosis 1.1] minimum n-well width violated
2	0 9 [Mosis 2.2] minimum active separation violated
156	1 5 [Mosis 6.5 b] min-enc active-cuts sep'n from ext active...
101	1 8 [Mosis 7.4] wide-feature metal-1 min separation violated
6	1 8 [Mosis 9.4] wide-feature metal-2 min separation violated
5	0 9 [using Mosis 2.1] active fragment may be too narrow
10	0 6 [Mosis 4.2] min enclosure, active by select, violated
59	0 9 [Mosis 5.3] separation rule for contact violated
4	5 4 [Mosis 1.2] min separation, n-wells at diff potential vi...

Making the circuit

Multiproject wafer fabrication



PCB shop



Board assembly

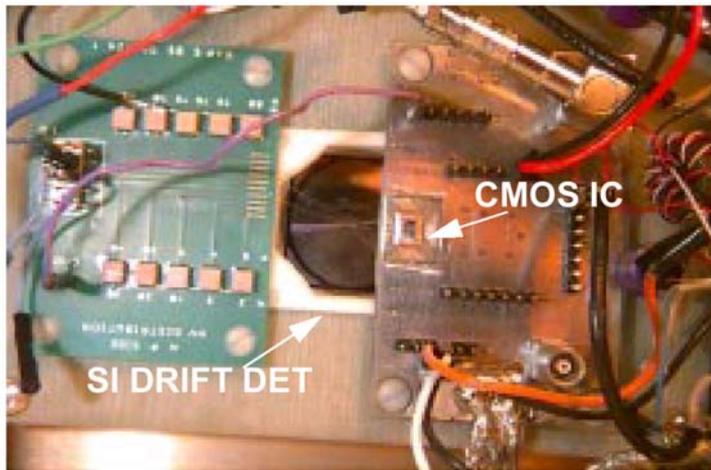


Burning the FPGA

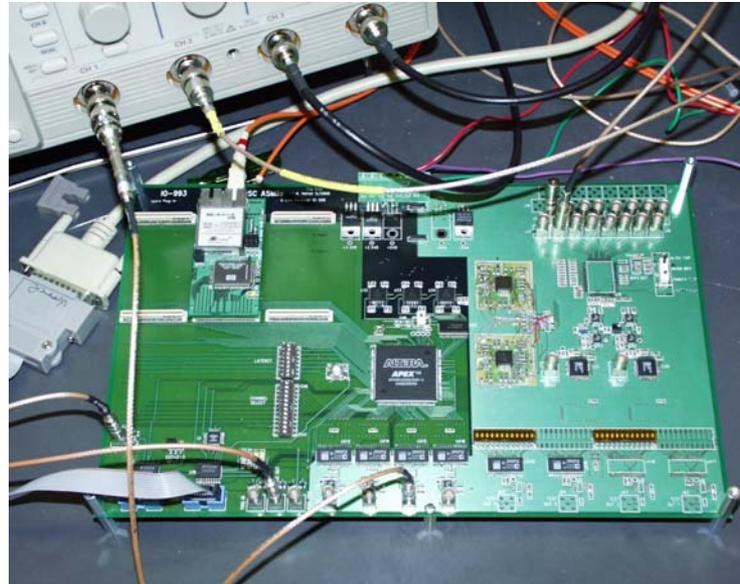


Testing

Bare die with detector



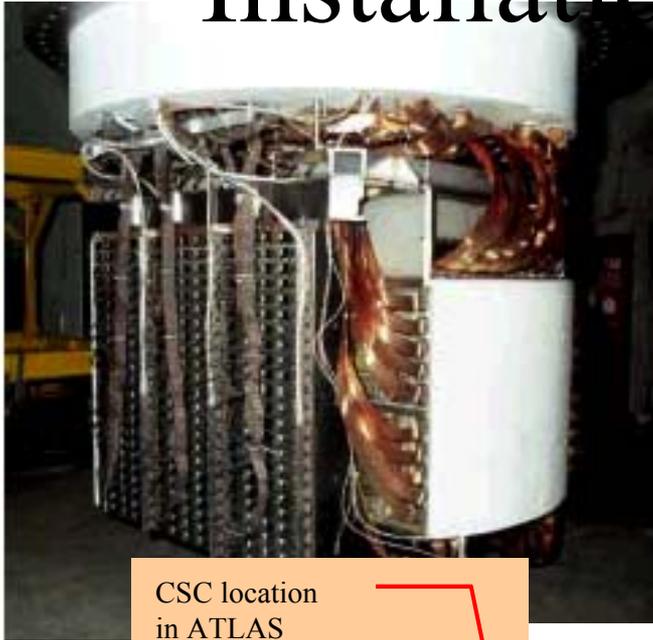
Board under test



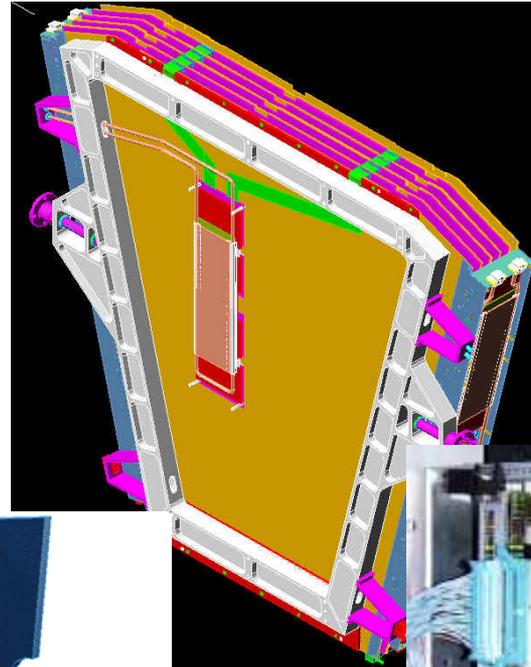
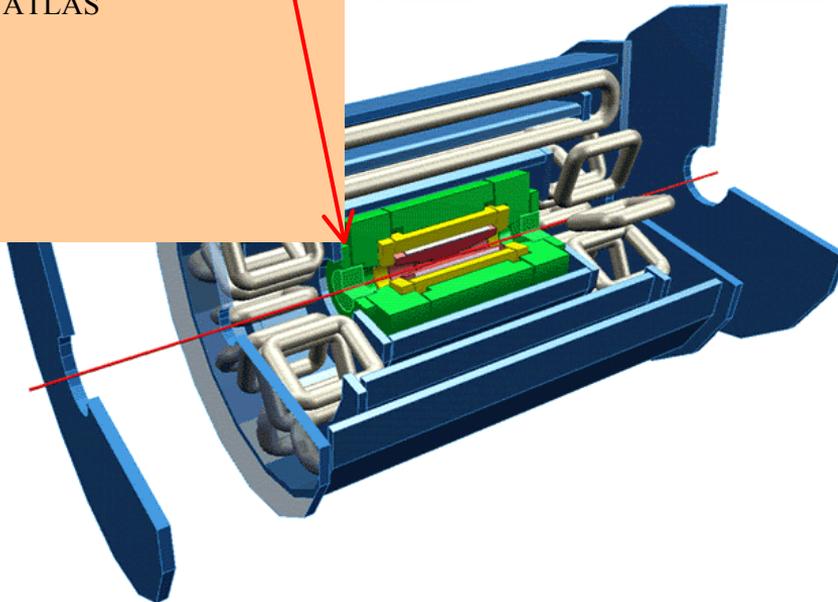
Production



Installation in the Experiment



CSC location
in ATLAS



Multiproject services

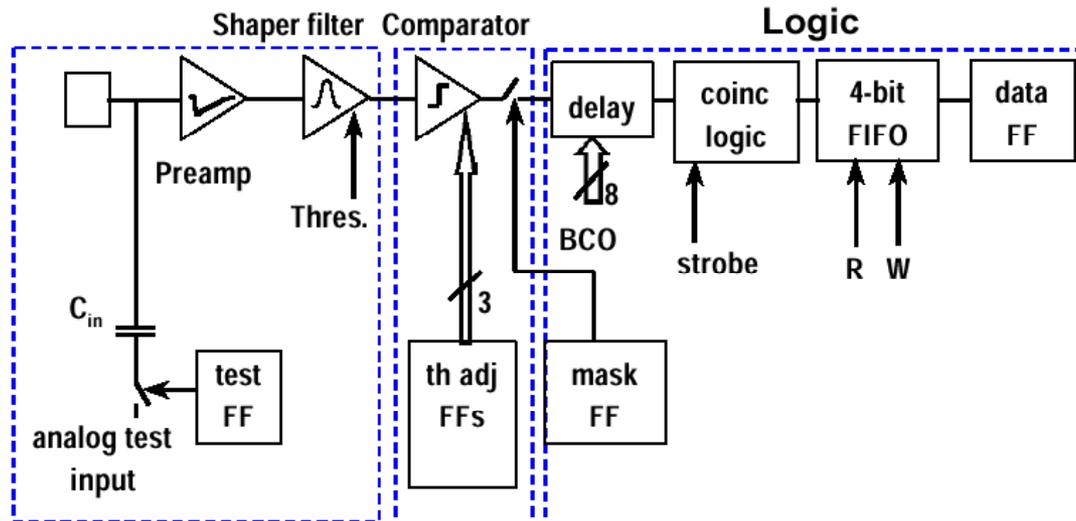
- Combine designs from many institutions on one maskset
- Arrange for regular runs with a variety of popular foundries
- Design support
 - Models
 - Design rules
 - Process monitoring
- Amortize cost of run over all users

Examples

- Inner detector
 - Si pixels for LHC
 - Si strips for LHC
- Muon detector
 - Cathode strip chamber for LHC/ATLAS
- Gas tracking detectors
 - TEC for RHIC/PHENIX
- Si Drift Detectors

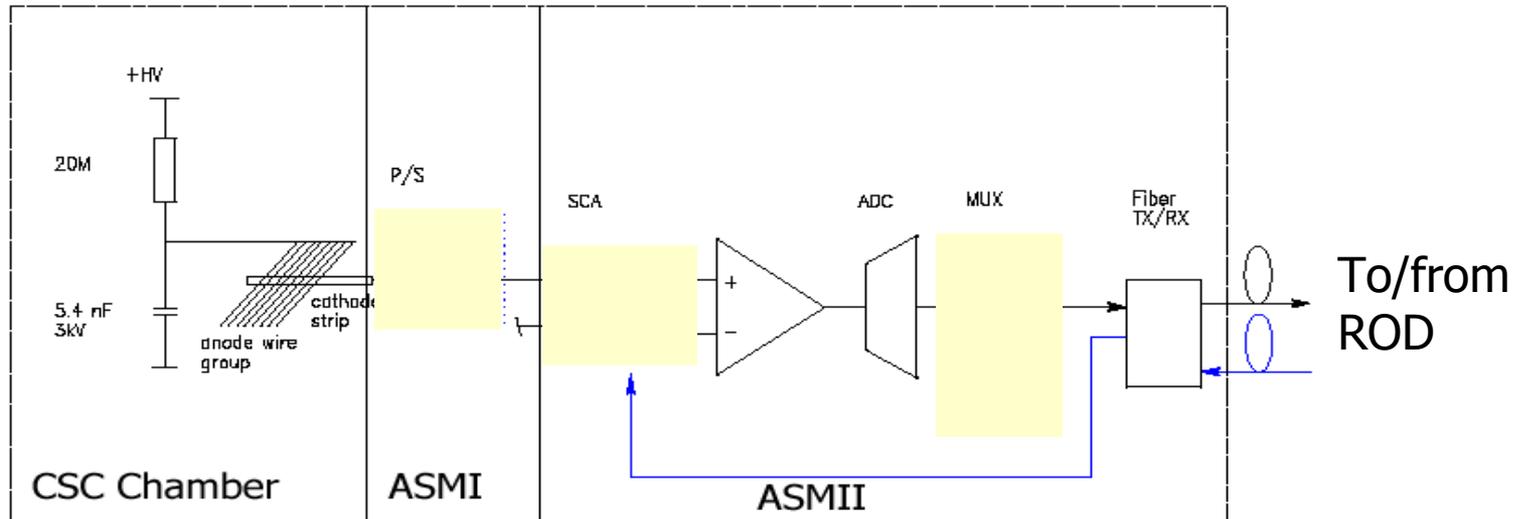
Si pixel readout

- Binary readout



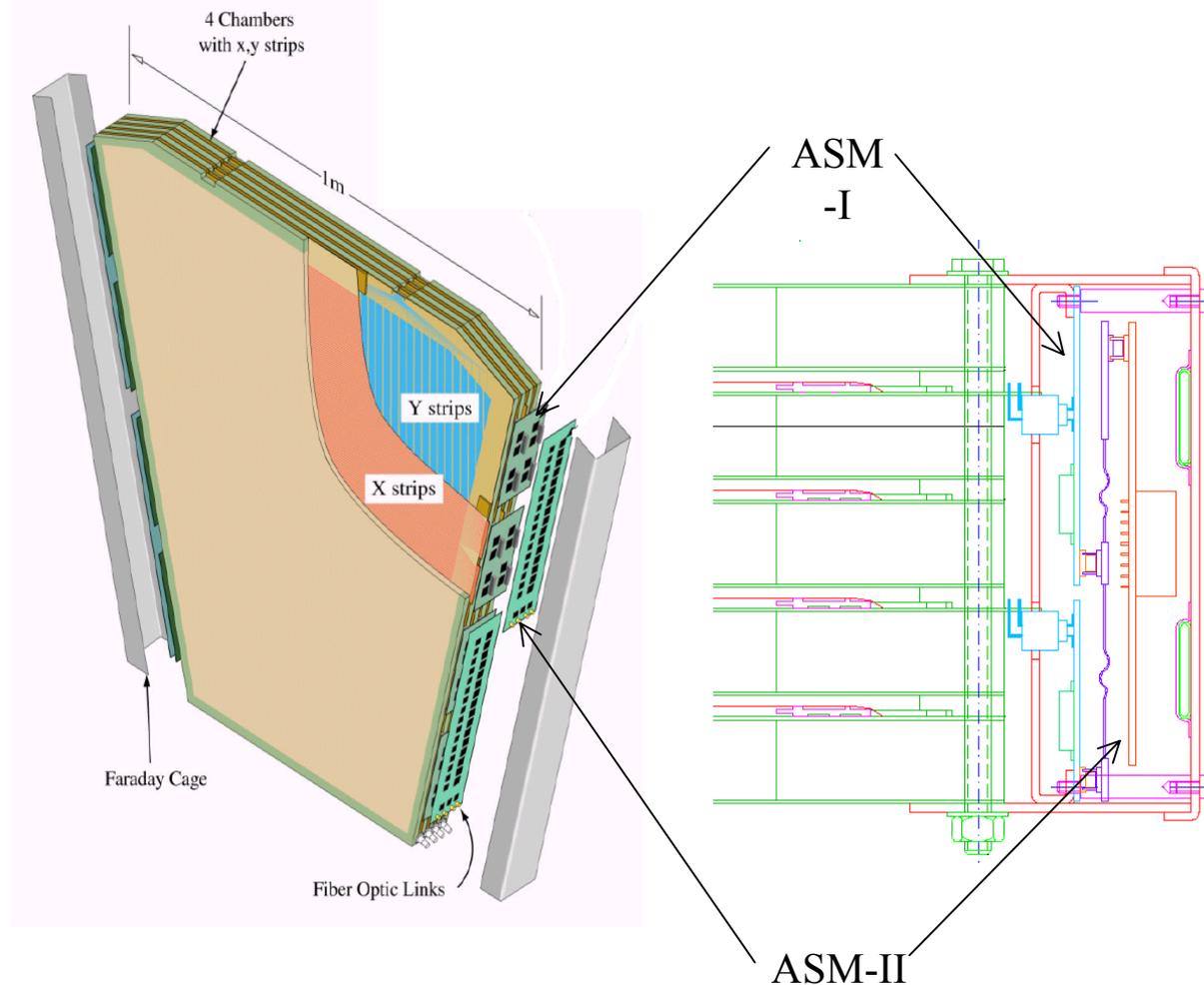
Pixel needs to tell whether particle passed or not in a 25 ns time slot
it does NOT need to tell how much charge was collected over a certain time

CSC On-chamber Electronics Chain



- **A**mplification, **S**ampling, digitization, and **M**ultiplexing into optical fiber performed on detector.
- 70 ns shaping
- 10 bit dynamic range
- 3 custom, radiation-tolerant ASICs

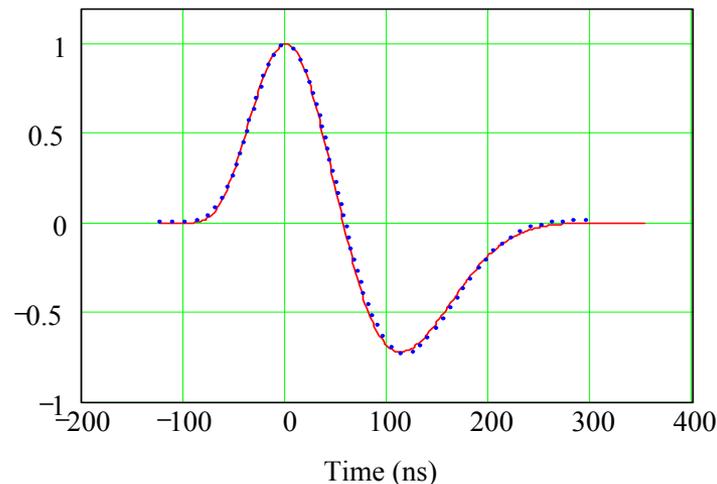
Electronics Location in Faraday Cage



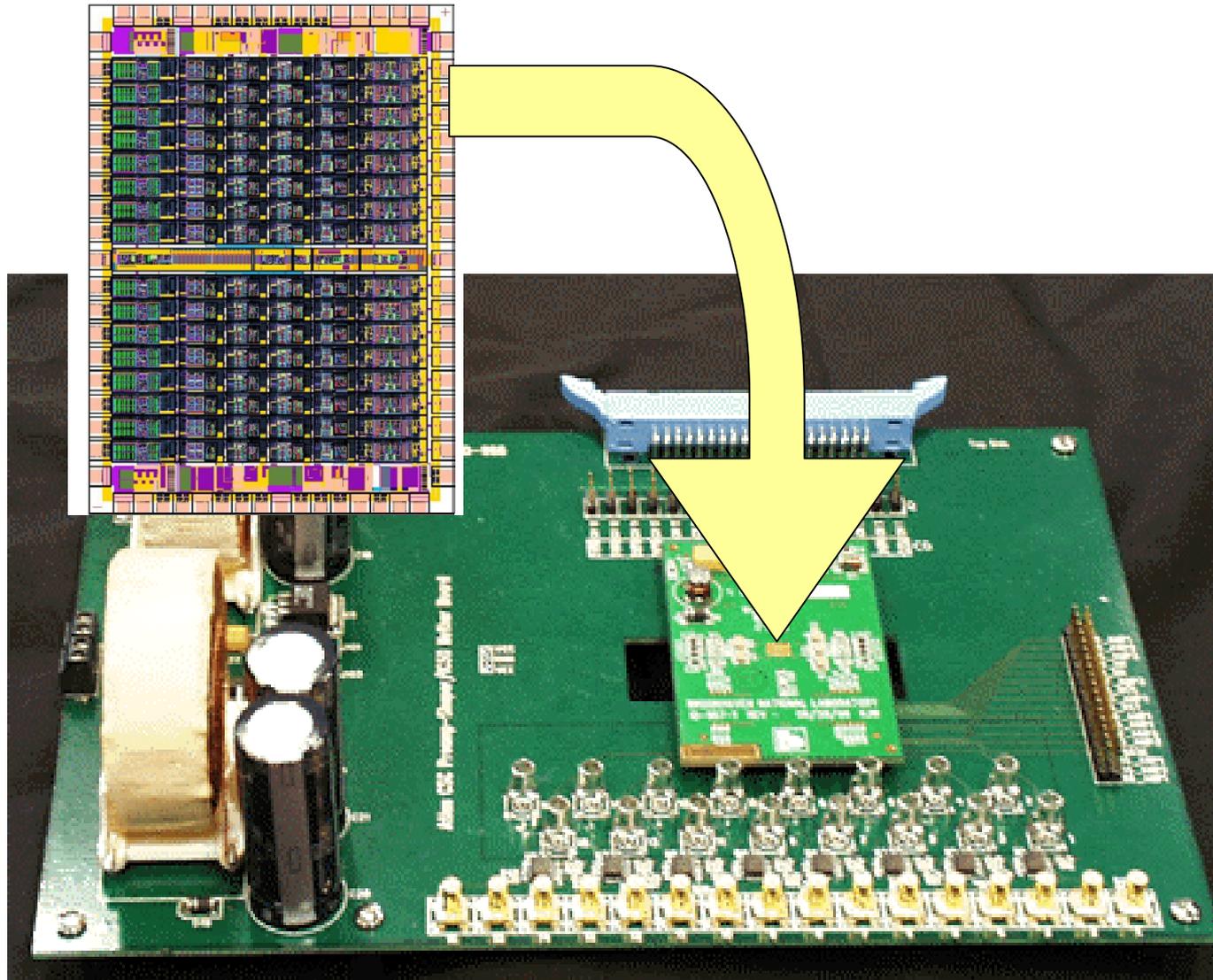
Pre-Amp Shaper

- Optimal pulse shaping is a compromise between noise, which degrades position resolution, and pileup which contributes to inefficiency.
- Bipolar pulse preferred in high-rate environment.
- From Monte Carlo study, peaking time should be ~ 100 ns and $FW1\%M < 430$ ns
- Bipolar 7th-order shaper using complex poles gives same return to baseline as 12th-order CR²-RCⁿ configuration

- Pulse Waveform



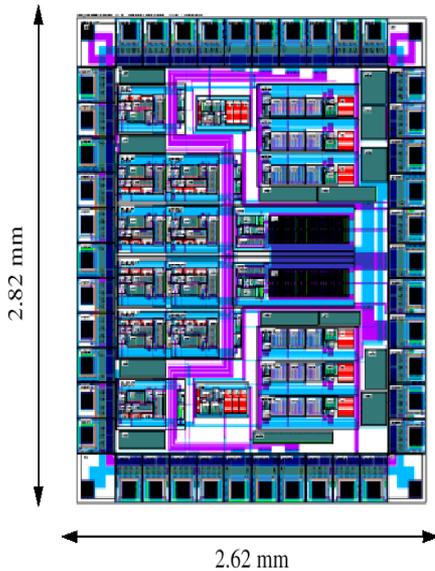
ASM 1 Prototype with P/S chip



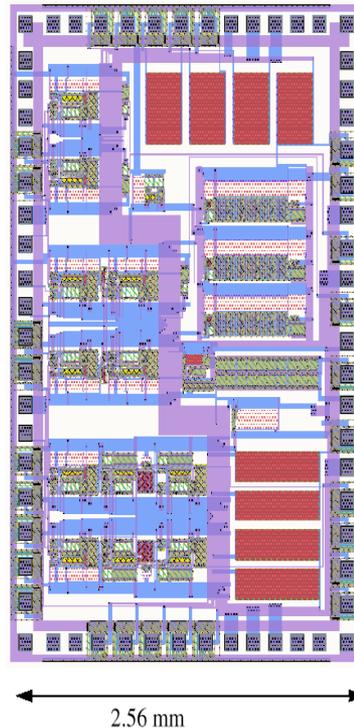
Drift Detector Preamplifier

- Used with ultra-low capacitance silicon drift detector, $C_{\text{det}} < 0.3 \text{ pF}$
- Preamp only, used with external shaper
- Purpose: explore lowest noise possible with CMOS
- Reset system: MOS transistor with special bias circuit to achieve stable, $>$

HP 1.2um version



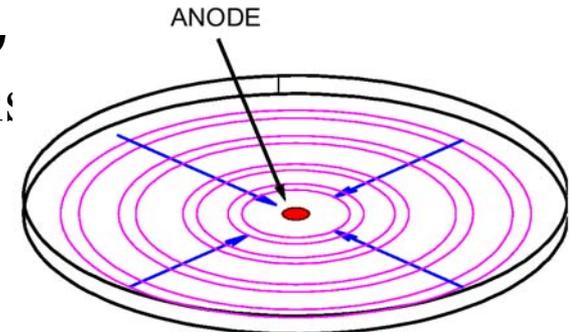
AMS 1.2um version



Requirements for 100 eV resolution with a 0.2 pF detector at 1 - 5 μs shaping time:

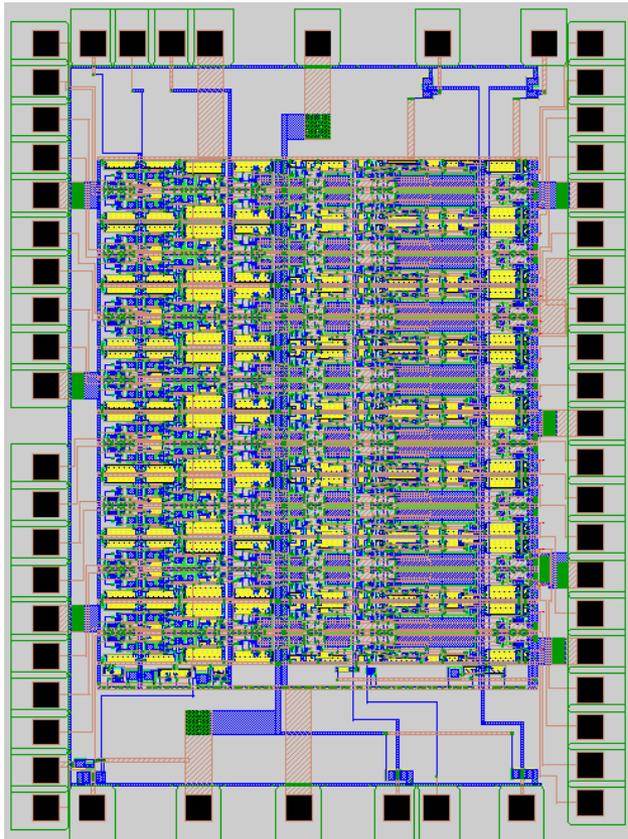
- $I_{\text{leak}} < 10 \text{ pA}$
- $R_{\text{F}} > 3 \text{ G}\Omega$
- $g_{\text{m}} > 0.4 \text{ mS}$
- $K_{\text{F}} < 1.8 \times 10^{-25} \text{ J}$

Detector
100
resis



SVT Preamp/Shaper

Die Layout



Output Waveform

