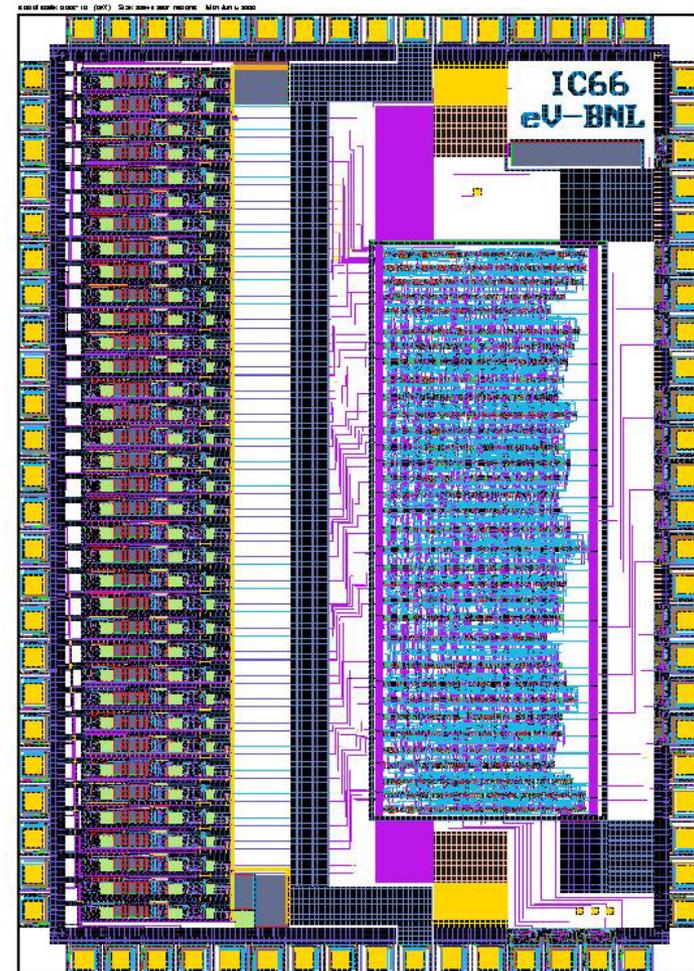


# Microelectronics Developments, 1991 – 2001

Paul O'Connor  
BNL

# Microelectronics Developments, 1991 – 2001

- Technology
- Scaling
- Pitfalls
- Monolithic active pixel sensor



# Custom Monolithics – technology options

- **Bipolar**
  - Workhorse of “old” analog
  - Available from a handful of vendors
  - Speed/power advantage over CMOS (diminishing)
  - Low integration density
- **Standard CMOS**
  - Suitable for most analog designs
  - Best for combining analog and digital
  - Highest integration density
  - Widely available
  - Short life cycle (3 years/generation)
- **BiCMOS**
  - Complex process, viability uncertain
- **Silicon on insulator (SOI)**
  - Modest speed advantage for digital
  - Drawbacks for analog
- **SiGe**
  - Exotic
  - Interesting for high frequency work
- **GaAs**
  - Unsuitable for wideband analog

## Access to custom CMOS is easy

- Design tools available at low cost to universities
- Multiproject services (MOSIS, Europractice, ...) provide low cost access to foundries for prototyping

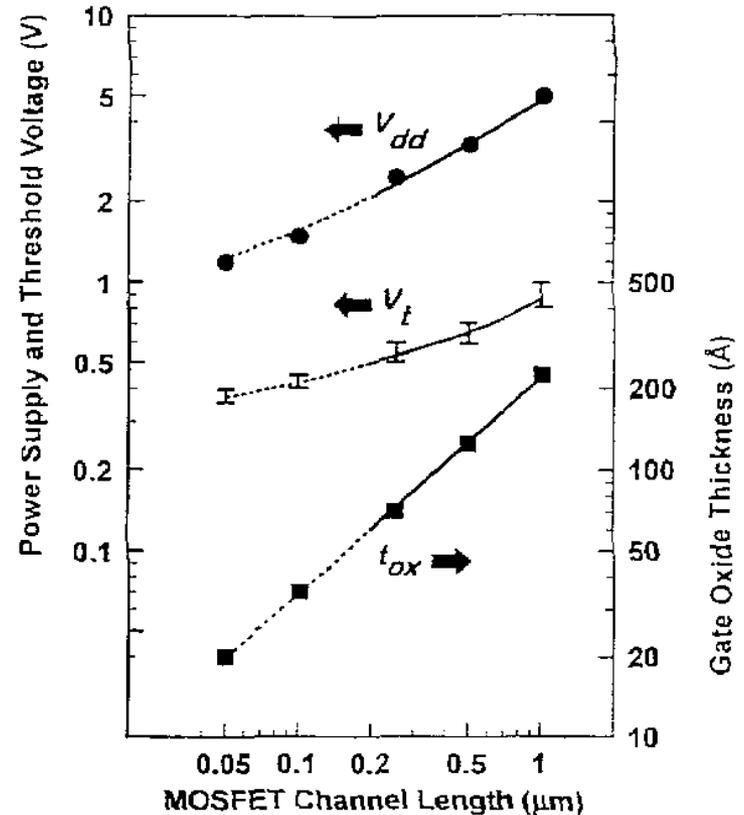
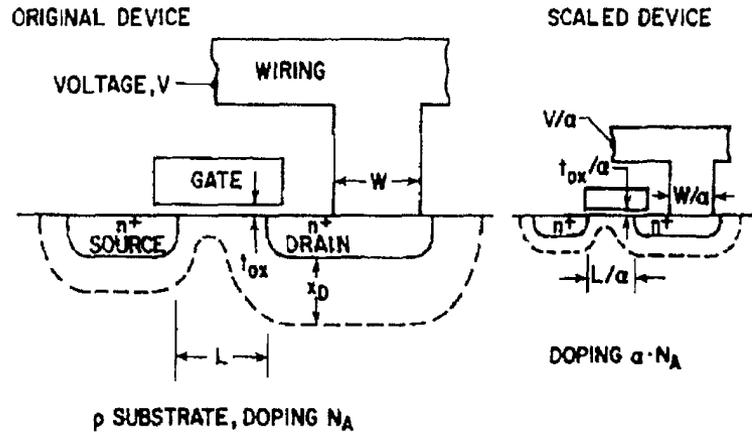
# CMOS Economics

Each ASIC may need

– 1.5 engineer-years	\$300K
– 2 prototype runs	30K
– 1 minimum production run	150K
<hr/>	
TOTAL	\$480K

Incremental cost per chip ~ \$10 – 20 / cm<sup>2</sup>

# CMOS Scaling



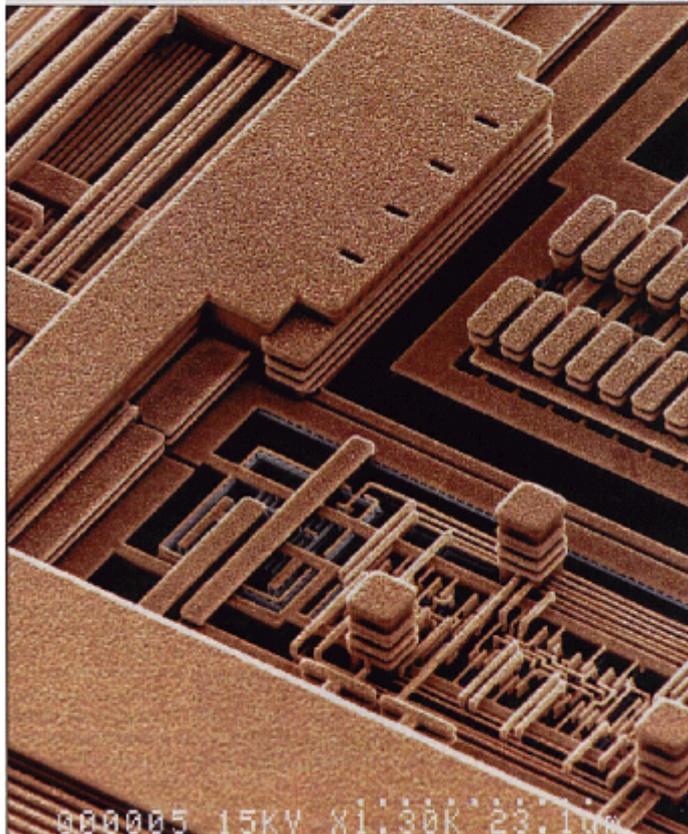
- Driven by digital VLSI circuit needs
- Goals: in each generation:
  - 2X increase in density
  - 1.5X increase in speed
  - Control short-channel effects, threshold fluctuation
  - < 1 failure in  $10^7$  hours

# CMOS Technology Roadmap

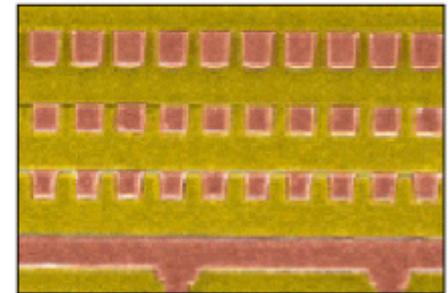
Year	85	88	91	94	97	00	02	04	07	10	13
Min. feature size [ $\mu\text{m}$ ]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.10	0.07
Gate oxide [nm]	44	33	22	16	11	7.7	5.5	4.0	2.9	2.2	1.6
Power supply [V]	5	5	5	5	5/3.3	3.3	2.5	1.8	1.2	1	.7
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5	0.45	0.4	0.3	0.3	0.3



# IBM Cu-11 Process (Blue Logic)



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12  $\mu\text{m}$ . It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].



Section showing Cu-11 copper and low-k dielectric process.

- $L_{\text{eff}} = 0.08 \mu\text{m}$ ,  $L_{\text{drawn}} = 0.11 \mu\text{m}$
- Up to 40 million wireable gates
- Trench capacitor embedded DRAM with up to 16 Mb per macro
- Dense high-performance, compact SRAMs
- Power supply: 1.2 V with 1.5 V option
- I/O power supply: 3.3 V (dual oxide option) / 2.5 V (dual oxide option) / 1.8 V / 1.5 V
- Power dissipation of 0.009  $\mu\text{W}/\text{MHz}/\text{gate}$
- Gate delays of 27 picoseconds (2-input NAND gate)
- Seven levels of copper for global routing
- Low-k dielectric for high performance and reduced power and noise
- HyperBGA (flip chip): 2577 total leads

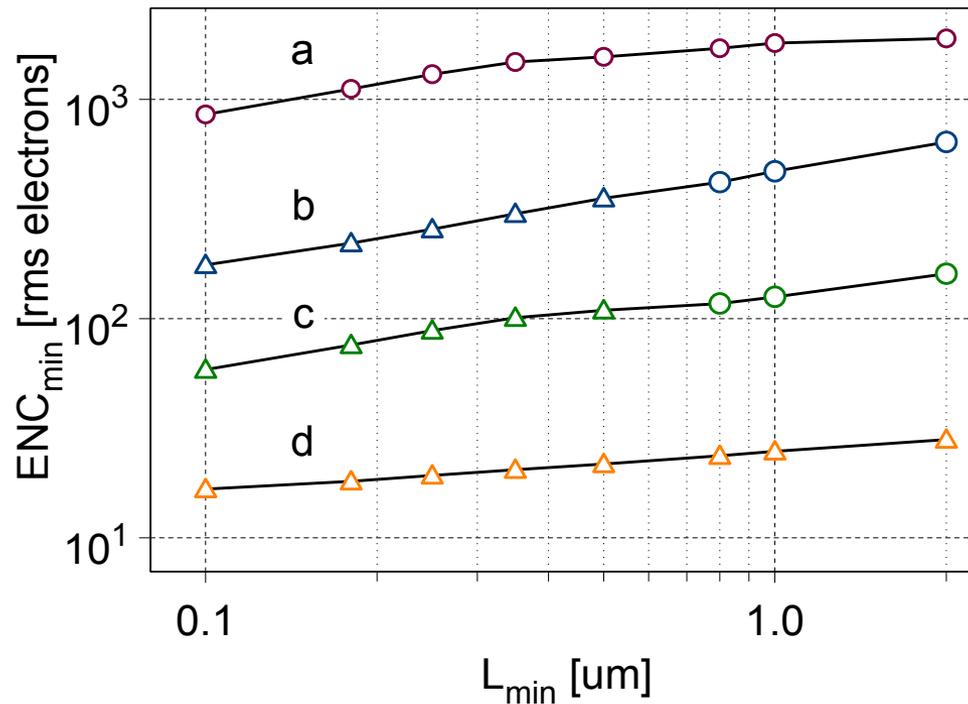
# CMOS scaling and charge amplifier performance

- Fundamental noise mechanisms
  - so far, no dramatic changes with scaling
- Noise
  - slight improvement with scaling
  - higher device  $f_T$  reduces series thermal noise
- Weak- and moderate inversion operation more common
  - need different matching to detector capacitance.
- Reduced supply voltage
  - difficult to get high dynamic range
- Many difficulties with “end of the roadmap” devices

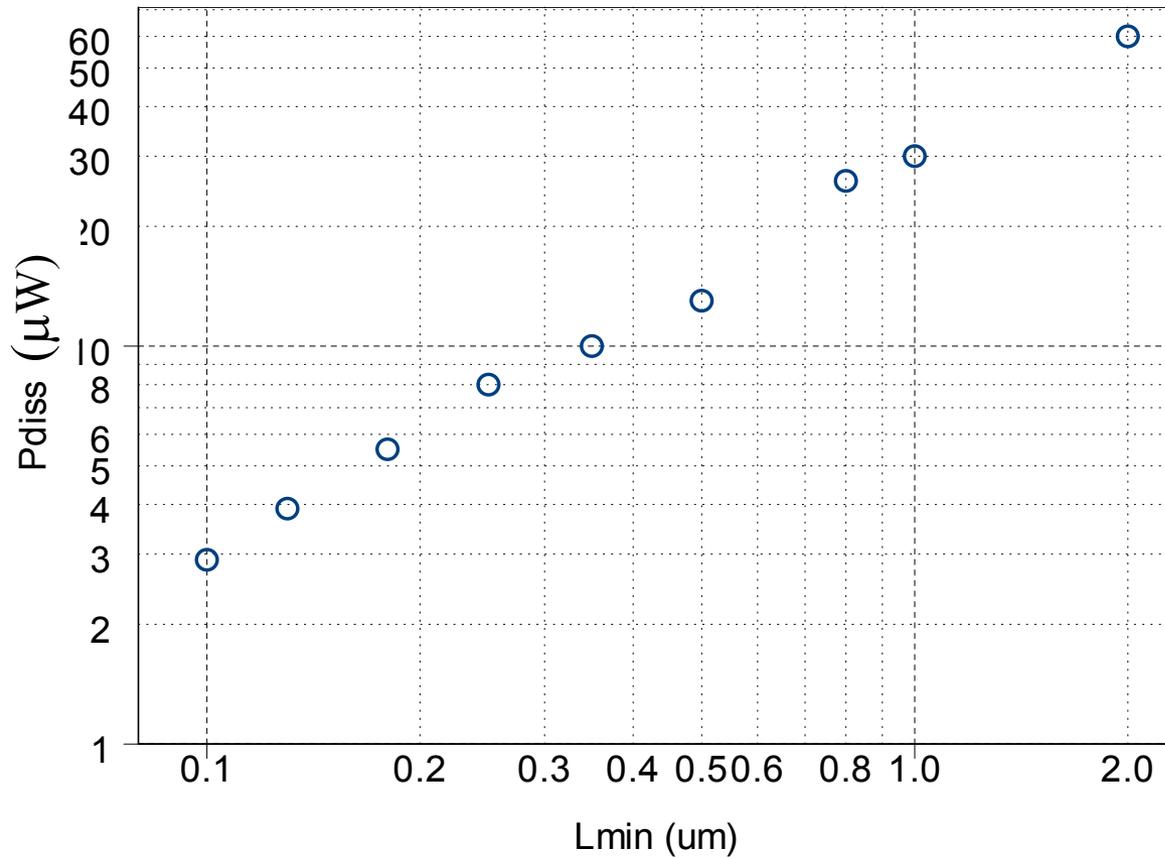
# Charge preamplifier noise vs. scaling

System	$C_{det}$	$t_{sc}$	P	$I_{leak}$	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

\* For this system, the shaping time was varied at each  $L_{min}$  to optimize the overall noise (i.e., to make the white series noise and parallel noise equal).



# Charge amplifier power vs. scaling



$$C_d = 0.3 \text{ pF}$$

$$t_s = 100 \text{ ns}$$

$$ENC = 100 e^-$$

# Commercial microelectronic components, what's changed since 1991?

- Renewed development of analog catalog parts
  - Data converters
  - Computer components -- disk drive readout, phone/network interface, displays
  - Wireless communication
  - Handheld and consumer devices
- CMOS supplanting bipolar as the technology of choice for analog applications
- Advances in packaging, PCB, assembly technology
  - Thin- and fine-pitch leaded SMT components; BGAs; chip-scale packages; packages with low thermal resistance
  - Flip-chip and chip-on-board assembly
  - Microvias, thin-core laminates, flex for high density integration (HDI)
  - Passive component miniaturization, arrays

# Cellular telephone handset trends

- 1991 cell phone

- ¾ pound
- 12V battery
- 700 components
- 8 hrs assembly time
- \$600

- 2001 cell phone

- 2 oz.
- 3V battery
- 4 –5 modular components + passives integrated in substrate
- 15 minute assembly time
- < \$150 or free

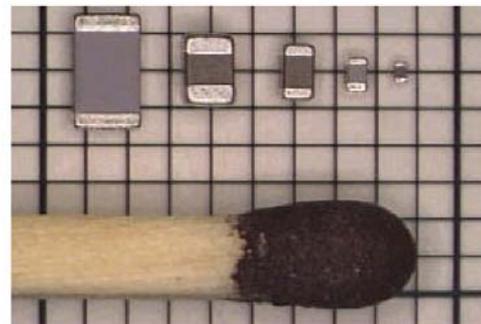
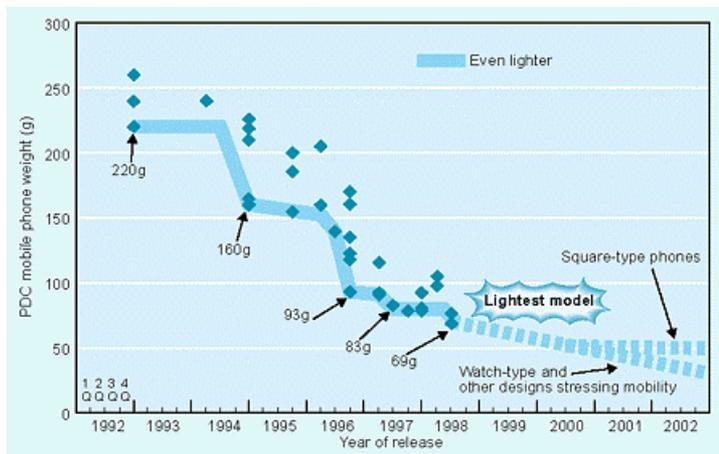


Figure 4 - Capacitors Ranging from 1206, 0805, 0603, 0402 and 0201



This is the world's first WRIST CAMERA. It features 1 MB of memory to hold up to 100 images.

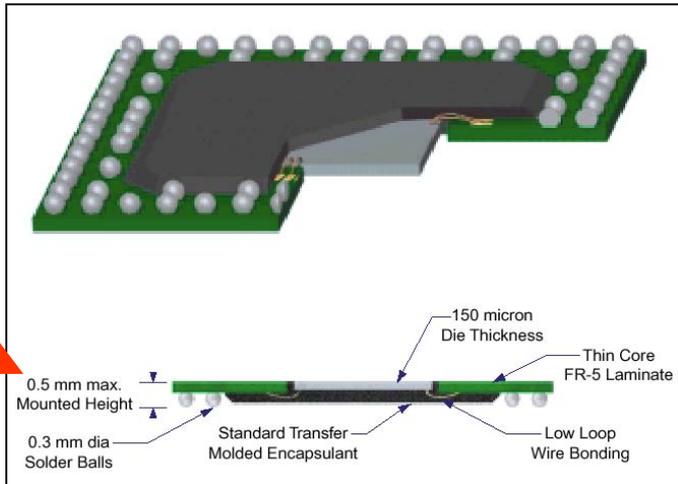
# Standard packages of 2001



National microSMD

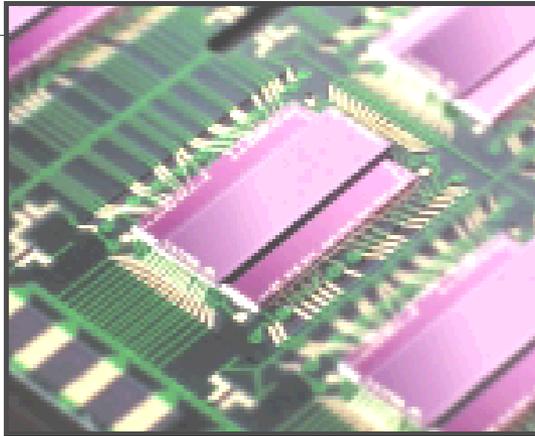
1.41 x 1.67 x 0.85mm body size (8L)

“Silicon Dust”

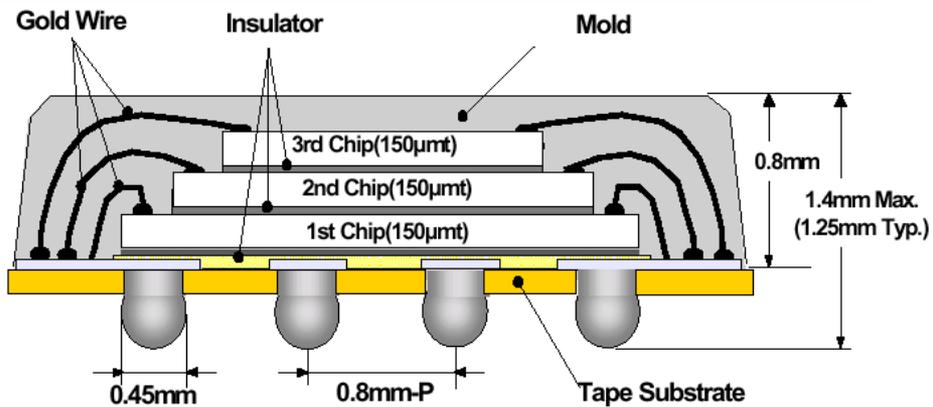


Amkor thin BGA

# Stacked Chip Scale Package



Double-decker  
(in production now)



Triple

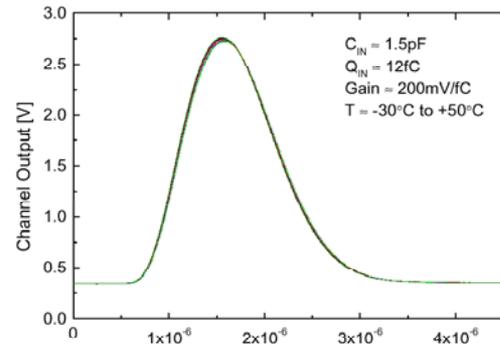
# Monolithic front ends – what can go wrong

- Frequently overlooked problems in design
  - Good electrical model of detector
  - Statistical nature of signals
  - Unusual signal conditions:
    - turn-on
    - calibration
    - response to background events
  - Detector-preamp interface
  - Board-level issues:
    - power conditioning,
    - bias decoupling,
    - calibration,
    - input protection,
    - interface components,
    - cooling

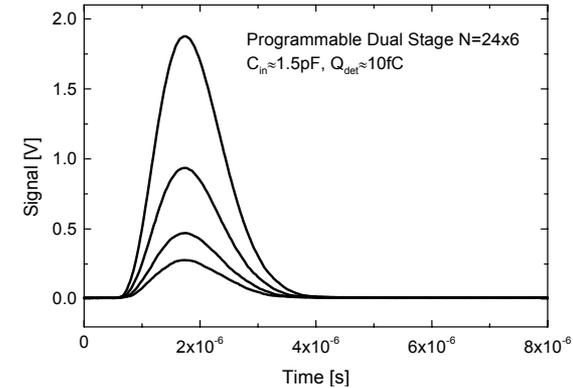
# Monolithic amplifier design: practical considerations

- Preamplifier reset
- High order filters
- Programmable pulse parameters
- Self-biasing
- Low-swing, differential I/O
- Circuits tolerant to variations in
  - temperature
  - process
  - power supply
  - DC leakage current
  - input & output loading

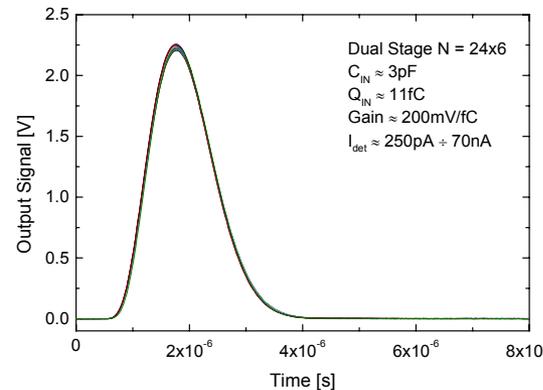
**Pulse vs. Temperature**



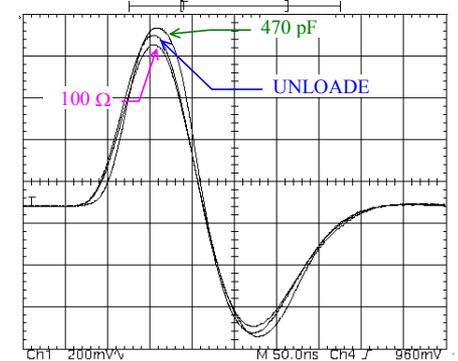
**Gain variation**



**Pulse vs.  $I_{leak}$**



**Loading**



	$I_{leak}$	Supply	Temperature	Rate (to 5/tp)	Cin	Zload
Gain	< 0.1%/nA	<.001%/V	-0.04%/°C	< 0.1%	<0.1%/pF	No slew-rate limit
Baseline	< 0.3mV/nA	<30 $\mu\text{V/V}$	75 $\mu\text{V}/^\circ\text{C}$	< 8 mV	-	Zout ~ 150 $\Omega$

# Monolithic front ends – what can go wrong

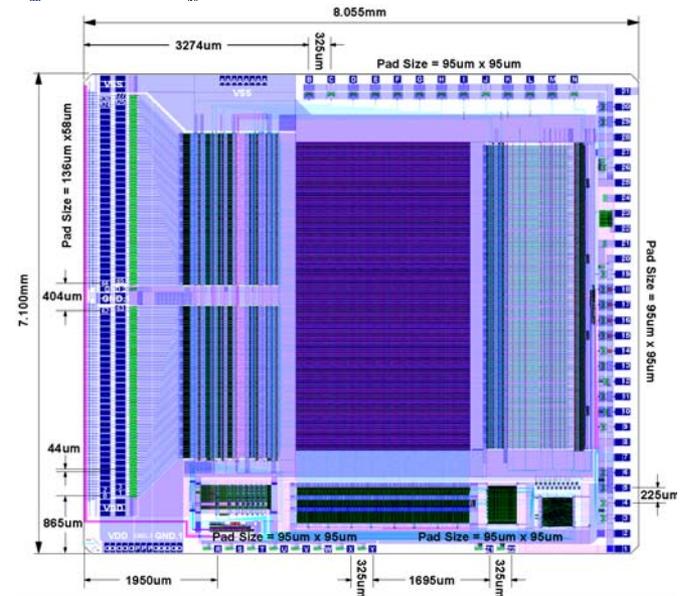
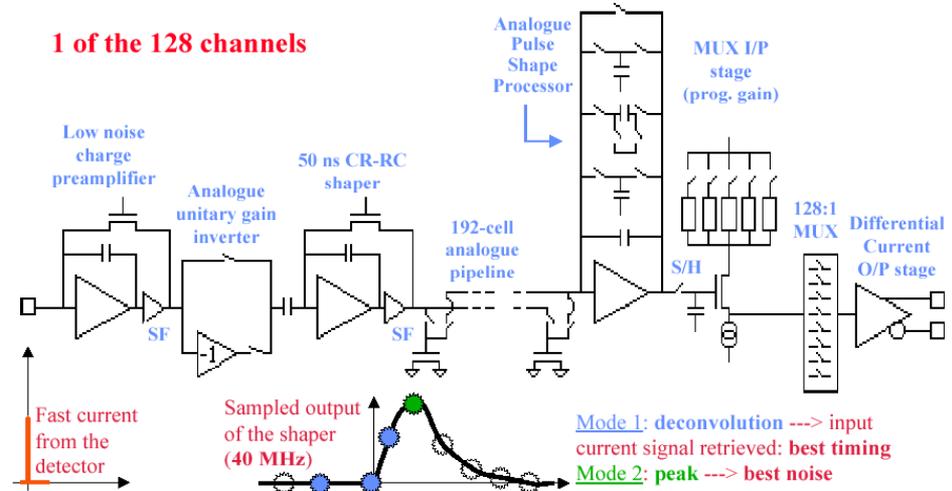
- Management issues
  - Isolation of chip designer, board designer, detector specialist
  - Managers not knowledgeable of chip design process:
    - CAD tools
    - Foundry capabilities
    - Documentation and review procedures
    - Timelines, iterations
  - Progress episodic rather than incremental
    - Harder to track progress

## Commonly heard phrases

- “We prototyped all the functional blocks, now all we have to do is put them together on the same chip and wire them up.”
- “All the chips work let’s go to production”
- “The chip works fine in simulation”
- “We already have a chip that does that, all we have to do is...”

# CMS silicon strip readout

Prototype of layer 3 in the Inner Tracker



230 m<sup>2</sup> Si

12 million strips

92,000 APV-25 chips

APV-25: 0.25 um CMOS

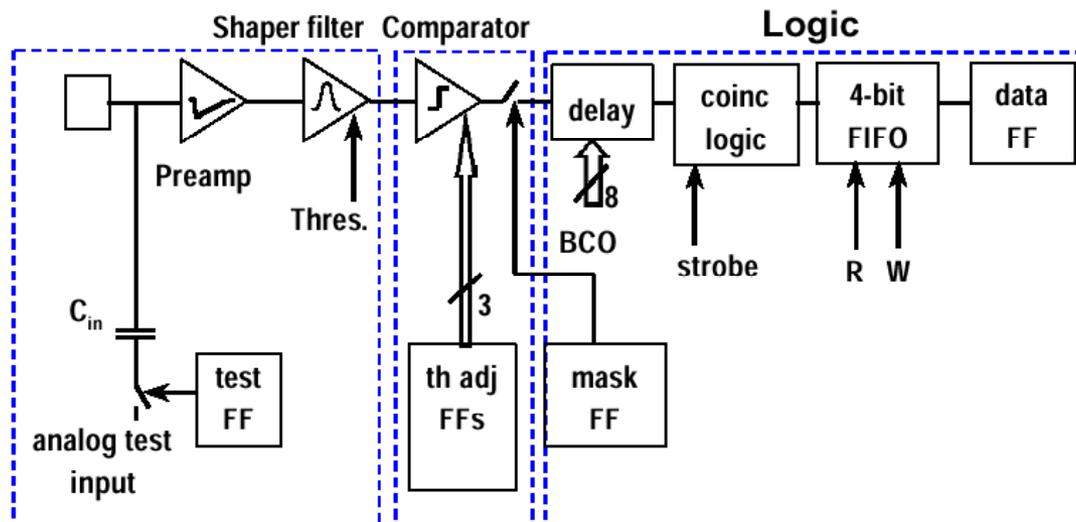
128 chan X 192 bucket P/S, SCA, mux

246 + 36.3 e/pf, 2.3mW/chan, 2% nonlinearity to 5 MIP

7.2 X 6.5 mm, 85% yield

# Si pixel readout

- Binary readout

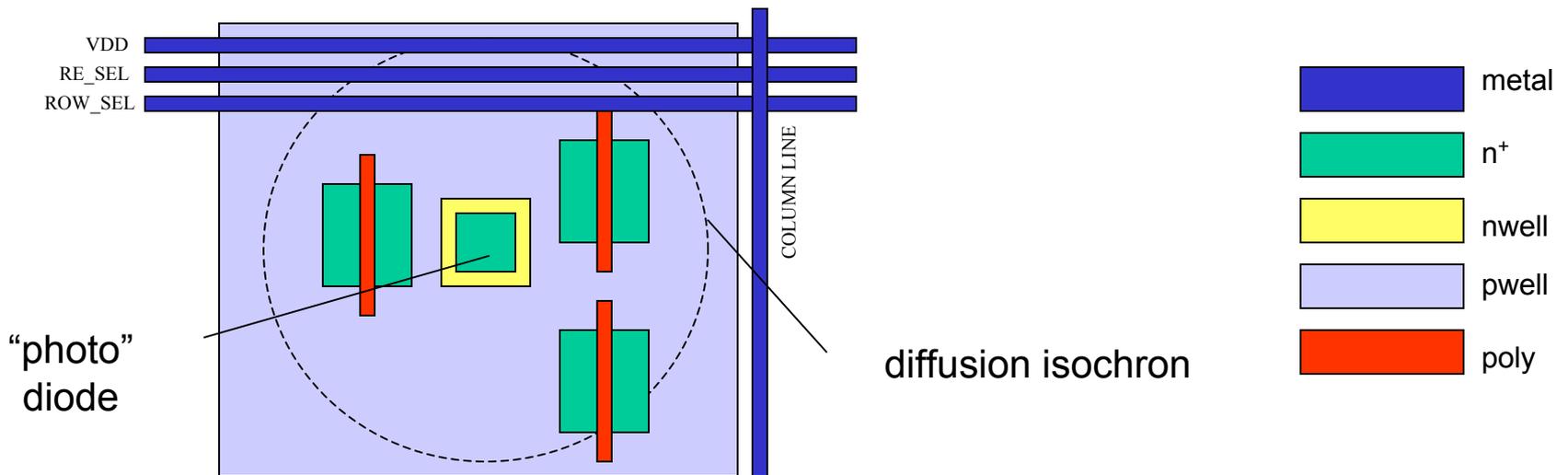
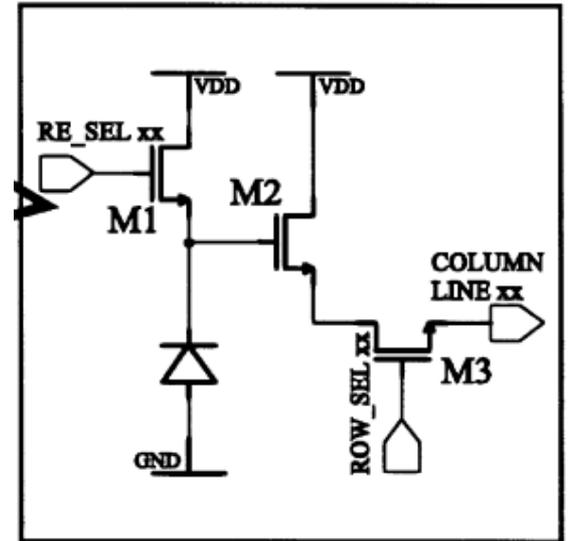
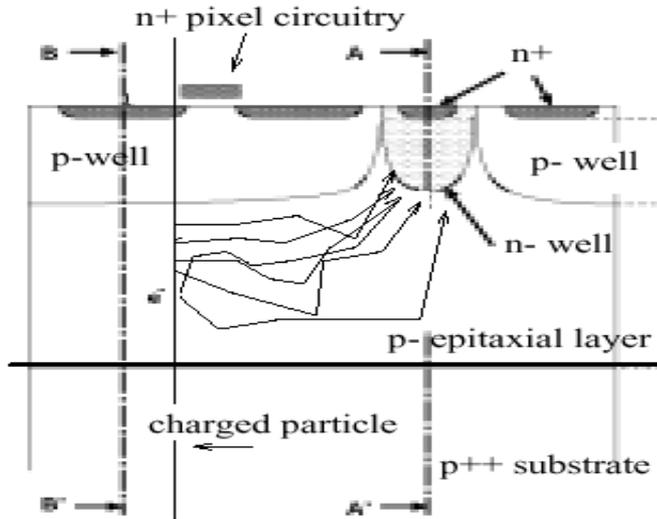


Pixel needs to tell whether particle passed or not in a 25 ns time slot  
it does NOT need to tell how much charge was collected over a certain time

# CMOS APS for particle detection/tracking

- ✓ Monolithic –special assembly technology not required
- ✓ Low cost
- ✓ Low multiple scattering
- ✓ Good spatial resolution (few  $\mu\text{m}$ )
- ✓ Random access
- ✓ Integration of control and DSP
- ✓ Radiation tolerance (?)
  
- ⊘ Special process
- ⊘ Collection time scales with pixel size
- ⊘ Circuit architecture embryonic

# Simple monolithic active pixel

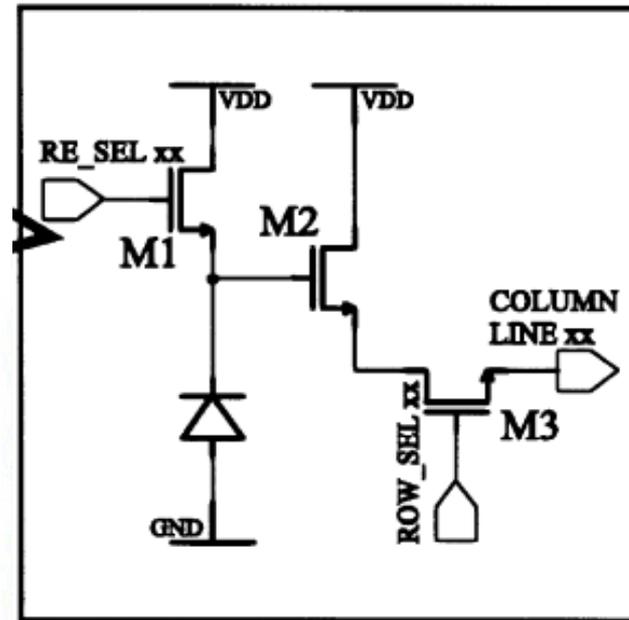
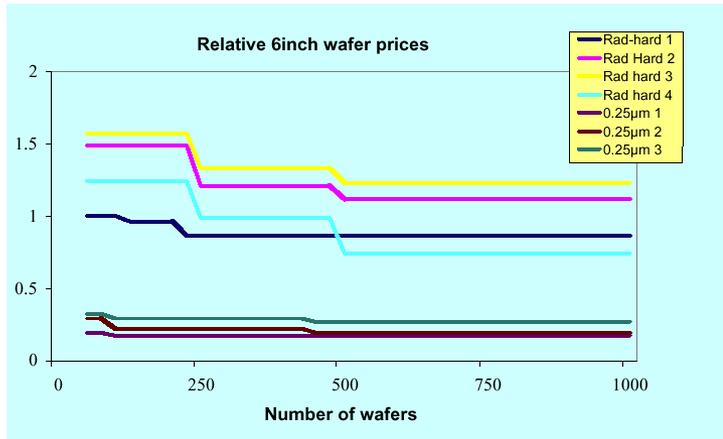


# Comparison of bump-bonded and active pixel sensors for tracking

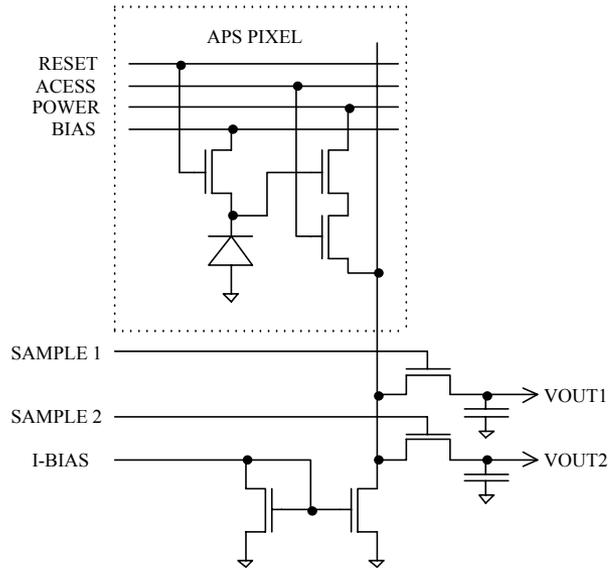
	Bump-bonded sensor	Active pixel	
Technology	hybrid	monolithic	
MIP signal charge	< 24000	800	e-
ENC noise charge	100 – 300	20 – 50	e- rms
Pixel area	20,000	< 400	$\mu\text{m}^2$
Sensor capacitance	200	< 10	fF
Detector bias	100	1	V
Charge collection time	< 20	depends on pixel area	ns

# Summary

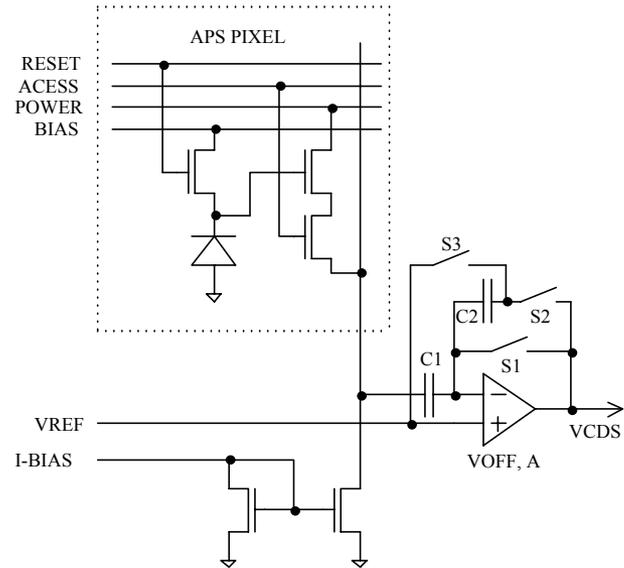
- PHENIX upgrade program can take advantage of a decade of progress in microelectronics.
- A study of the monolithic active pixel sensor as a vertex detector is warranted.
- By avoiding known pitfalls in the ASIC development process, cost and performance goals should be met.



BASIC APS READOUT WITH  
CORRELATED DOUBLE  
SAMPLING.

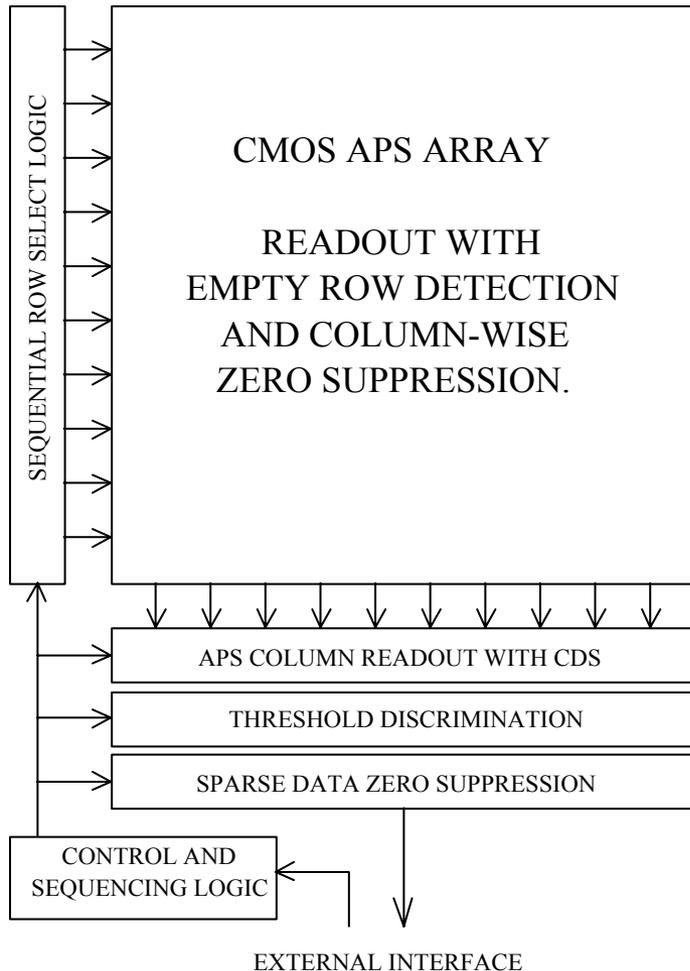


APS READOUT, CDS WITH  
SUBTRACTION AND OP-AMP  
OFFSET CANCELLATION.



$$VCDS = (C1/C2)VSIG + (1 + C1/C2)(VOFF/(1 + A))$$

# APS Readout with Zero Suppression



- Readout of each row followed by threshold discrimination and zero suppression in columns.
- No additional logic in pixels.
- Minimal periphery in one dimension allows close abutting.
- Achieves substantial reduction in readout time compared to non-sparse readout, but with much less overhead than full pixel-level zero suppression.

# Video chip

Stuart Kleinfelder, SukHwan Lim, Xinqiao Liu, Abbas El Gamal

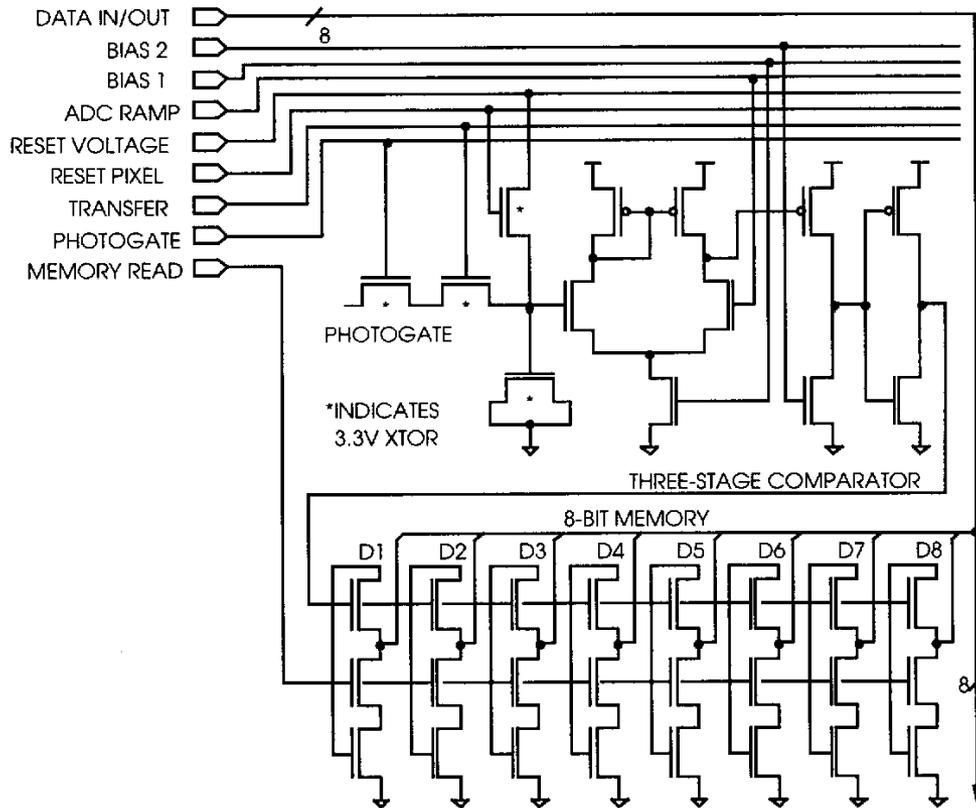


Figure 3: Pixel schematic.

Stuart Kleinfelder, SukHwan Lim, Xinqiao Liu, Abbas El Gamal

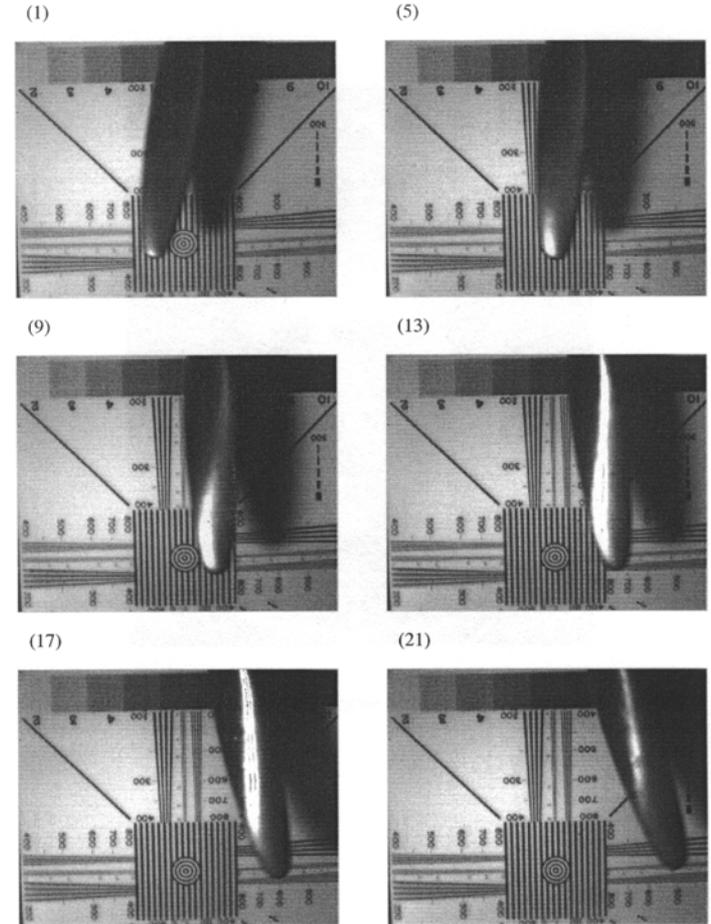
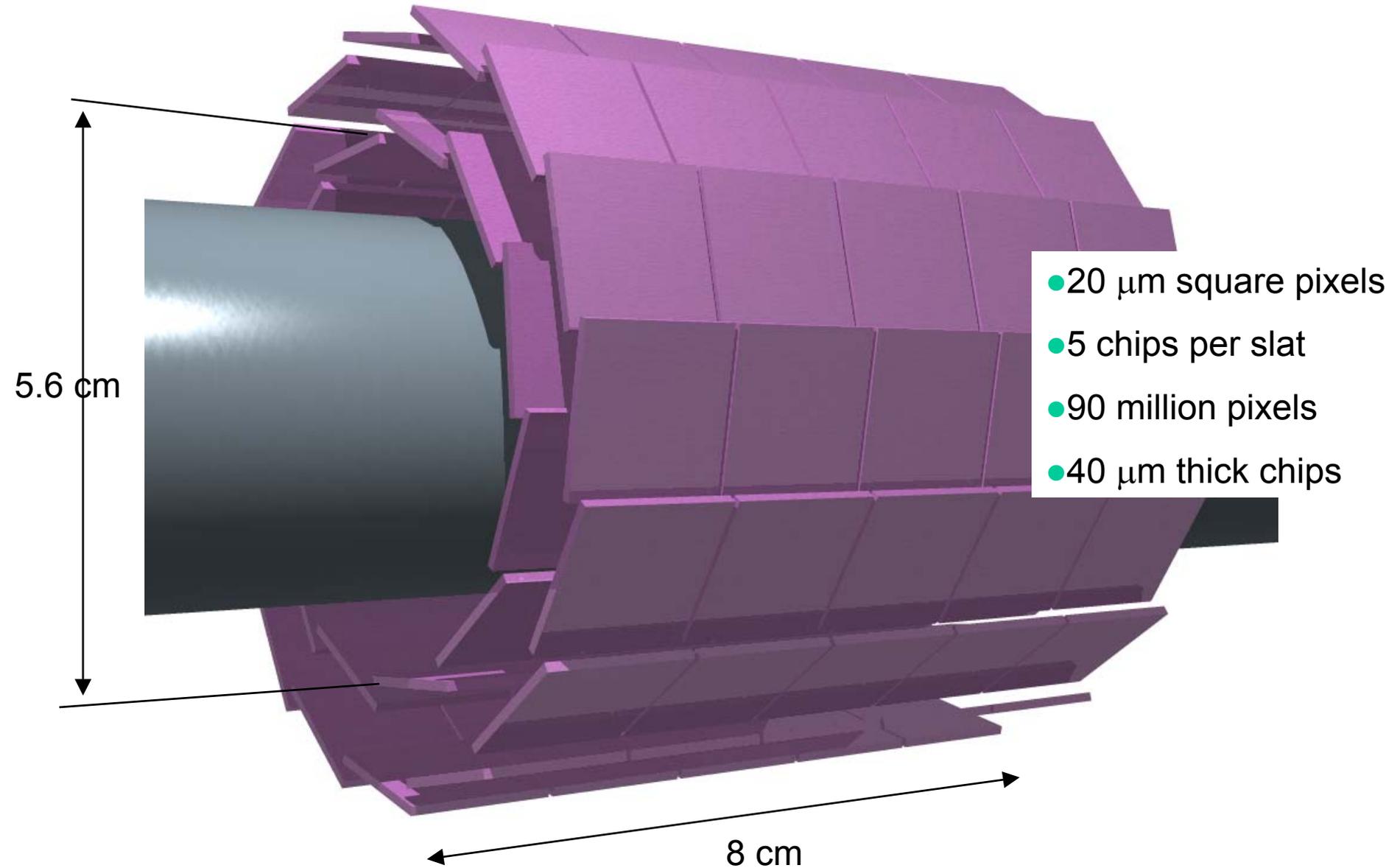
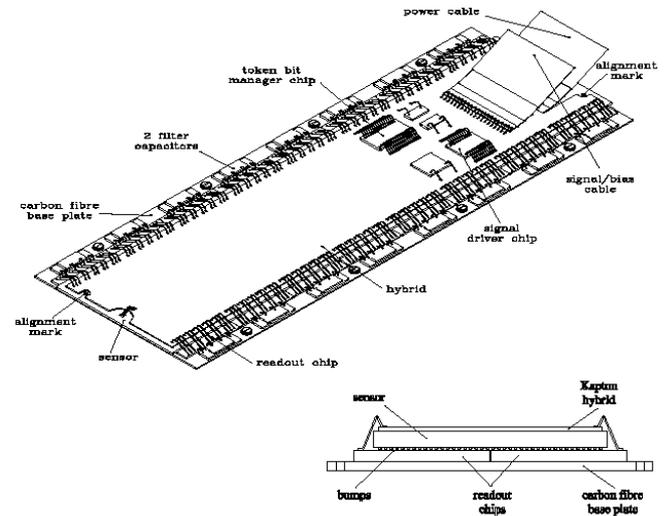
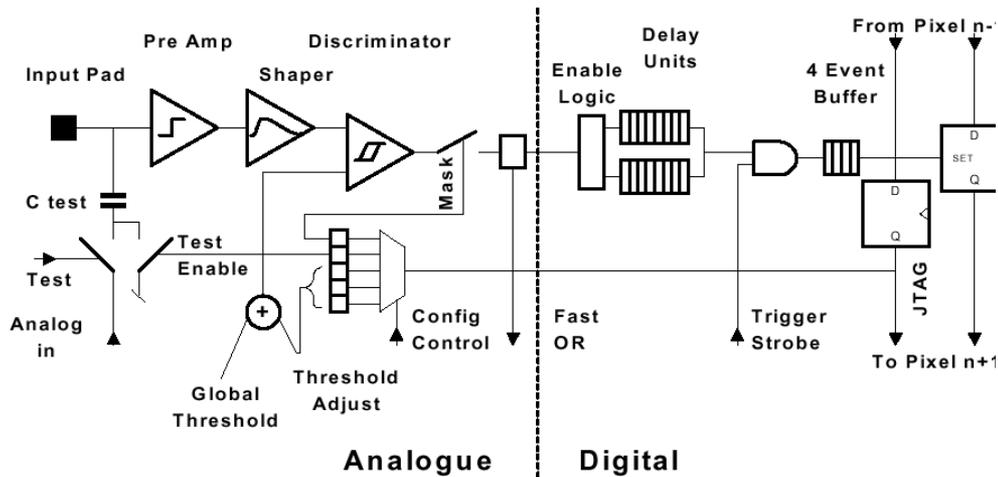


Figure 6: Non-enhanced 10,000 fps image sequence (every 4th frame, no CDS).

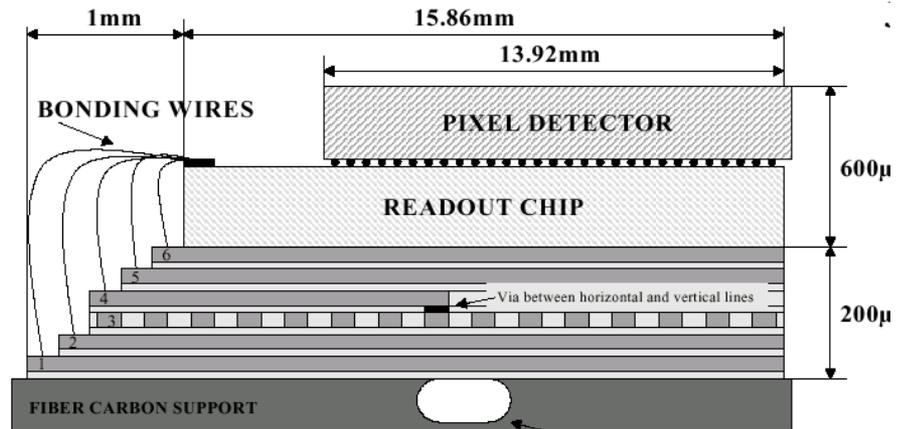
10,000 fps, every 4<sup>th</sup> frame displayed  
propeller speed ~ 2000 rpm

# Active Pixel Sensor (APS)





Note: the drawing is not to scale

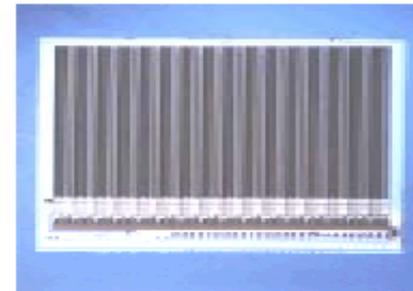
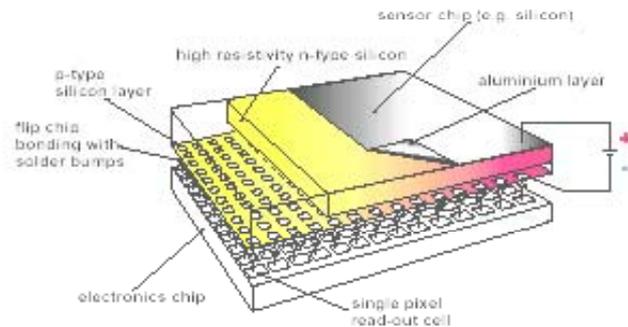


- 6 ANALOG\_GND 25μ
- 5 ANALOG\_POWER 25μ
- 4 VERTICAL LINES 5μ
- 3 HORIZONTAL LINES 10μ
- 2 DIGITAL\_POWER 25μ
- 1 DIGITAL\_GND 25μ

COOLING TUBE

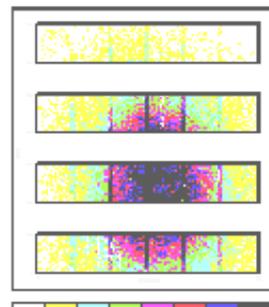
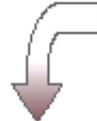
- Aluminium
- Polyimide

# Example : Hybrid Pixel Detectors (CERN RD-19 E. Heijne et al.)

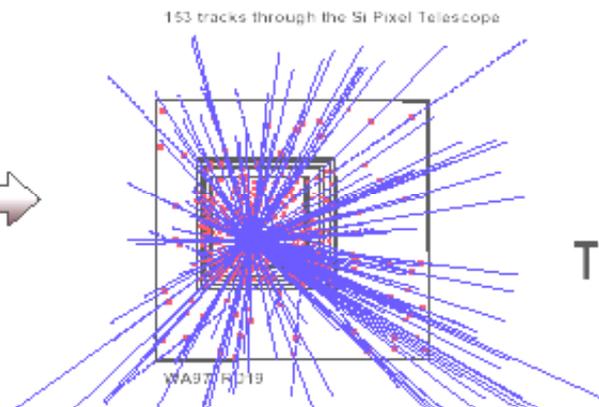


**LHC1 : 2000 CMOS  
readout channels**

**Pixel Ladders  
(6 chips)**

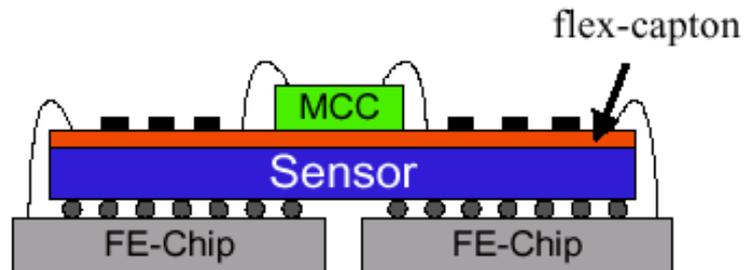


**Half plane ~ 50 000 sensing elements**



**153  
Tracks !**

**WA97 NA57 Experiment  
1.2 M channels**



- *Sensor and FE-chips are directly connected with bumpbonds*
- *Signals are routed in a (flex-) capton layer on the sensor*
- *MCC and passive components are mounted on the flex*
- *Wirebonds connect FE-chips and MCC with the flex*

