A Generation of CMOS Readout ASICs for CZT Detectors[1]

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Abstract

As a result of a cooperation between Brookhaven National Laboratory and eV Products a generation of high performance readout ASICs was developed. The ASICs, realized in CMOS 0.5μm technology, are available in several different versions, single or multi-channel and with unipolar or bipolar shaper, in view of their use in research, spectroscopy, medical, safeguard and industrial applications. Four innovative circuit solutions are implemented in the ASICs: (i) a high linearity compensated continuous reset system which self-adapts to a wide range of detector leakage currents with minimum noise contribution; (ii) a high order shaper realized by using the follow-the-leader feedback (FLF) approach; (iii) a class AB rail-to-rail output stage with high driving capability; (iv) a baseline holder (BLH) for the baseline stabilization. The basic structure of the ASICs, a description of the circuit solutions and the preliminary experimental results are reported.

I. INTRODUCTION

The inherent advantages and rapid improvement of $Cd_xZn_{1-x}Te$ (CZT) detectors led to an increase in the number of their applications [1-4]. Several motivations (see subsection A) suggest that most of these applications can benefit from the use of ASIC readouts in place of discrete solutions.

The purpose of the collaboration between Brookhaven National Laboratory and eV Products is the development of high performance ASIC readout prototypes to be used in place of discrete solutions in most of CZT applications. In order to be a valuable alternative, the ASICs must satisfy stringent requirements (see subsection B). In particular they must offer equal or even better performance and increased commercial potential. Due to the limited performance of their analog front-ends, both the ASICs currently reported in the literature and the commercially available readout ICs don't satisfy all these requirements [5-20]. As a consequence they represent a good alternative to discrete solutions only in a limited number of applications, in particular where large number of channels and very low power are required.

A. Motivations

In the following, some of the motivations which led to the investigation on ASICs as alternative to discrete readouts are reported.

Cost: ≈ \$35/ch for multi-project and ≈ \$1/ch for large numbers, to be compared to ≈ \$75/ch in the discrete case; an initial R&D cost for the migration from discrete to ASIC must be also considered.

Size: ≈ 1 mm^2/ch, to be compared to ≈ 700 mm^2/ch; consequent opening to new applications.

Power: ≈ 18 mW/ch, to be compared to ≈ 300 mW/ch; consequent reduction, in some cases, of detector temperature; opening to battery operation.

Manufacture: reduced interconnects, board simplification and reduced number of process steps.

Reliability: it is expected to increase due to reduced external interconnects and reduced circuit exposure to environment.

Performance: reduced parasitics, high order shaping and additional signal processing easily available.

B. Requirements

With the purpose of a readout electronics with overall performance comparable to or better than discrete solutions, stringent requirements were imposed to the ASICs. Together with low noise, high linearity, good driving capability, low dependence on temperature, low power and programmability, the ASIC had to exhibit:

- *detector dc coupling capability:* ASIC front-end capable of handling, with high linearity and minimum noise contribution, detector leakage currents over the wide range typical of CZT detectors.
- *high order shaper:* implementation of a high order shaper, characterized by a longer peaking time (lower curvature of the peak) at equal duration, thus reducing the ballistic deficit [21] typical of CZT detectors [22].
- *high baseline stability:* with the aim of using unipolar shaping, characterized by lower curvature of the peak when compared to bipolar shaping, the ASIC must exhibit high output baseline stability over the whole dynamic range, also at high rates.

In Section II the basic structure of the ASIC channel, details on the circuit solutions and corresponding experimental results are presented. Sections III gives details on the production and available prototypes. In Sections IV the ASICs' performance and more general preliminary experimental results are reported.

II. STRUCTURE OF THE ASICS

Fig. 1 shows the basic structure of the ASIC channel, composed of a charge preamplifier with a fully compensated continuous reset, a high order shaper, a class AB output stage and a feedback loop which provides the baseline stabilization. The arrangement is slightly different in the case of bipolar shaping. In the following subsections a description of each stage is reported. For some of the stages, a much more detailed description can be found on dedicated papers.

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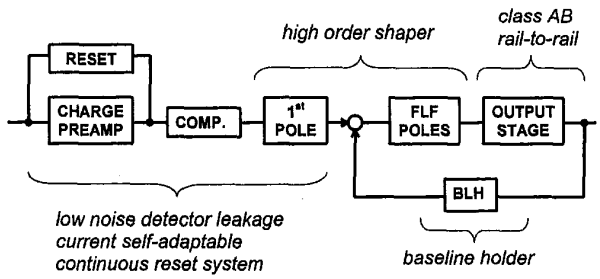

Figure 1: Basic structure of the ASIC channel.

A. Preamplifier and Continuous Reset System

The preamplifier input transistor is a nominal 200μm×0.5μm n-channel MOSFET biased at Id ≈ 600μA and Vds ≈ 300mV and optimized for a 2pF input (detector plus parasitic) capacitance and 1μs peaking time [23]. The open loop amplifier is based on a cascode plus follower configuration and is characterized by a dc gain ≈ 75dB, a GBWP ≈ 300MHz and an equivalent input noise voltage spectrum ≈ $5\times10^{-12}/f + (1.5\text{nV})^2$. The power dissipated by the preamplifier is close to 3mW. The compensated continuous reset system is schematized in Fig. 2. A brief description and some of the results are reported here. A theoretical analysis and simulation results are discussed in [24]. Additional analysis and most of the experimental results are reported in [25].

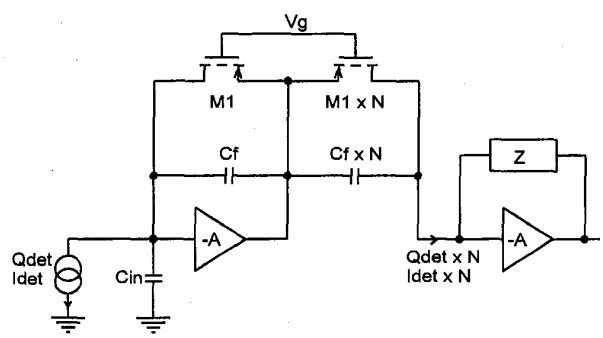

Figure 2: Schematic of the compensated continuous reset system.

The reset system is based on the use of a p-channel MOSFET M1 in parallel to the feedback capacitance with source connected to the output and drain connected to the input of the amplifier. The gate geometry and gate bias voltage are chosen to set the device operating point above threshold and in saturation at the minimum expected value of detector leakage current (typically ≈ 1nA for CZT). An N times parallel replica of the feedback stage is used to couple the charge preamplifier output to the input of the following stage. The ratio between the drain currents (both static and dynamic) of the two MOSFETs equals N and any non-linearity and finite transist time introduced by the feedback is recovered by its N times replica [24]. The quadratic relationship between the gate-to-source voltage of the MOSFETs and its dc drain current (which equals the detector leakage current I_{DET}) prevents the saturation of the preamplifier output over a wide range of I_{DET}. As a consequence the system self-adapts to detector leakage currents up to several tens of nA always acting as a high linearity current amplifier with gain N, and always contributing with a noise lower than the shot noise of the detector [24,25]. An additional non-stationary noise contribution, related to the reset phase, must be also considered. A simplified expression of this additional contribution is given by [22]:

$$\delta ENC^2 \approx 0.17[\text{Coulomb}]\cdot Q_{DET} \qquad (1)$$

where Q_{DET} is the charge released by the detector. Experimental results in agreement with Eq.(1) were found [25].

The matching between M1 and its N-times replica plays a determinant role in the accuracy of the compensation. In order to achieve large values of gain N a cascade of two stages was implemented, the first based on p-channel MOSFETs with N1 = 24 and the second based on n-channel MOSFETs with N2 = 6. A total gain N = N1×N2 = 144 was thus achieved for this dual-stage system.

A compensated continuous reset system exhibits a dependence of the gain on the value of the charge preamplifier feedback resistor. The mechanism of this dependence is described in detail in [25]. In the implemented reset system, where the feedback resistor is replaced by a MOSFET, the effective value of the feedback resistance depends on the value of the detector leakage current. A change in gain ≈0.23% was measured for a change in I_{DET} from 1nA to 2nA and ≈0.97% from 1nA to 10nA [25]. In Fig. 3 the pulses measured at the output of the ASIC channel for different values of detector leakage current I_{DET} are reported.

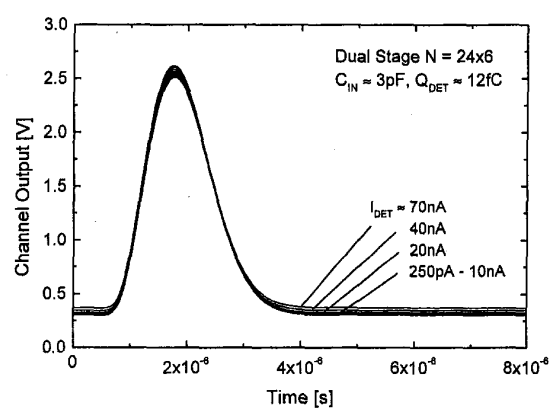

Figure 3: Pulses measured at the output of the ASIC channel for different values of detector leakage current I_{DET}.

From the baseline return of pulses shown in fig Fig. 3 it can be observed the effectiveness of the compensation over a wide range of leakage currents. The same figure shows the dependence of the gain and of the baseline on I_{DET}.

Related to the dependence of the gain on the value of the charge preamplifier feedback resistor is an increase in integral linearity error [25]. When $Q_{DET}/C_F > |V_{T1}|$ and the operating point of M1 is in weak inversion region, the increase in integral linearity error can become non-negligible. The analysis of this effect is not straightforward and only the experimental

results will be reported. For Q_{DET}/C_F > 800mV, an increase ε in the integral linearity error < 0.1% for $I_{DET} \geq$ 1nA and < 1% at $I_{DET} \approx$ 100pA (M1 operating in weak inversion) were measured [25].

The analysis reported in [25] suggests three additional design criteria for the compensated reset system: (i) M1 should operate above threshold at the minimum expected value of I_{DET} [22] (in most cases it means that M1 should have long and narrow channel); (ii) C_F should be chosen to satisfy the condition $C_F \geq Q_{DET}/V_{T1}$ at the maximum expected value of Q_{DET} and (iii) the GBWP of A should be maximized. Corresponding criteria apply to the second stage in case a dual-stage compensated reset system is implemented.

As previously discussed, the second of the dual-stage provides a current gain equal to N2, where N2 is the ratio between the coupling impedance to following stage and the feedback impedance. In order to provide gain programmability, switches were introduced for the modification of the ratio N2. The switches were introduced in series to each one of the N2 coupling impedances as well as in series to the feedback impedance, thus providing full compensation of switches parasitic effects (capacitance, on-resistance r_{ON}, non-linearity, etc.). The switches were connected to the virtual ground in order to minimize the dependence of r_{ON} on the detector leakage current. When introducing these switches, attention was paid to the additional time constant generated by r_{ON} along the feedback, which could lead to instability. In Fig. 4 it is shown the measured response to $Q_{DET} \approx$ 9fC while setting the gain to ≈ 30, 50, 100 and 200mV/fC.

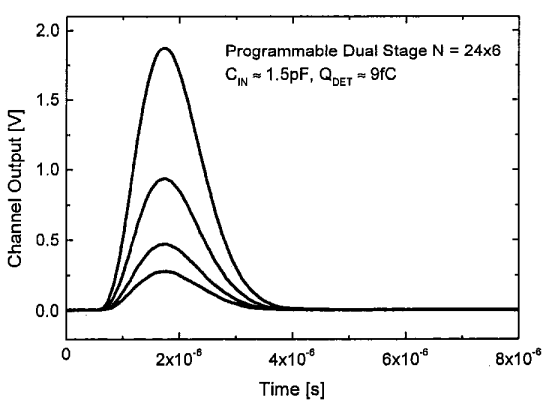

Figure 4: Measured output pulses corresponding to $Q_{DET} \approx$9fC for different gain settings.

In a comparison to a non-programmable version, no increase in the integral linearity error was measured.

B. Shaper Amplifier

The shaping is a classical 5th order complex semigaussian, implemented in most of commercial nuclear amplifiers and based on one real pole plus two pairs of complex conjugate poles [26].

The reason for this choice can be clarified by observing Fig. 5, where the implemented shaping is compared, at equal 1% width, to a 5th order non-complex semigaussian shaping and to a 2nd order shaping. It can be observed that the peaking time of the implemented shaper is longer. Since CZT detectors suffer from long hole collection time and charge trapping effects [22], they can benefit from the lower curvature of the peak while operating at equal rate [21,27].

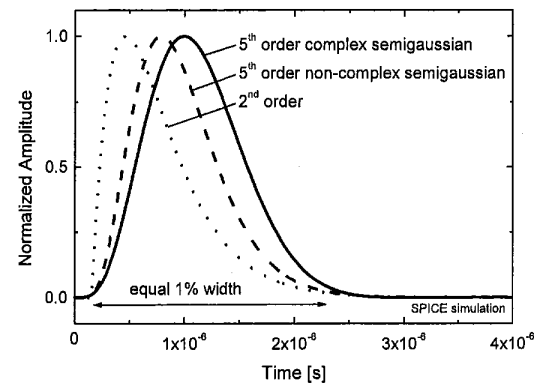

Figure 5: Simulated comparison, at equal 1% width, of the implemented 5th order complex semigaussian shaping, a 5th order non-complex semigaussian shaping and a 2nd order shaping.

The ENC can be expressed as [28,29]:

$$ENC^2 = C_{in}^2\left(\frac{A_{1W}}{\tau_W}S_{vw} + A_{2W}\pi A_{vf}\right) + A_{3W}\tau_W S_{iw} + A_{4W}\tau_W^2\pi A_{if} \quad (2)$$

where A_{1W}, A_{2W}, A_{3W} and A_{4W} are coefficients related to the shaping, C_{in} is the input capacitance, S_{vw} and S_{iw} are respectively the (bilateral) white series and white parallel noise spectral densities, A_{vf}/f and A_{if}/f are respectively the (unilateral) $1/f$ series and $1/f$ parallel noise spectral densities and τ_W is the 1% pulse width.

In Table 1 the values of the coefficients for the evaluation of the ENC are reported for the three shaping cases of Fig. 5. The corresponding values for the 1%-100% pulse peaking time τ_P and for the 99% peak width τ_{PW} (i.e., a measure of the peak curvature), normalized to τ_W, are also reported.

Table 1
Coefficients for the shapings of Figure 5

	5th cpx	5th	2nd
A_{1W}	5.48	6.78	14.43
A_{2W}	1.048	1.046	1.181
A_{3W}	0.32	0.27	0.24
A_{4W}	4.36	3.27	2.68
τ_P/τ_W	0.42	0.27	0.13
τ_{PW}/τ_W	0.052	0.043	0.037

From Table 1 it can be observed a gain in series noise coefficients A_{1W} and A_{2W} and a loss in parallel noise coefficients A_{3W} and A_{4W}. In most practical cases the overall difference between the two high order shapings, when taking into account series and parallel noise sources, is contained within a few percent. On the other hand the peak curvature is reduced more than 20% (and more than 40% with respect to 2nd order).

A simplified schematic of the shaper amplifier is shown in Fig. 6. The four complex conjugate poles were implemented by using the follow-the-leader feedback (FLF) approach, a multi-feedback technique which offers a lower sensitivity to changes in circuit parameters when compared to other solutions [30].

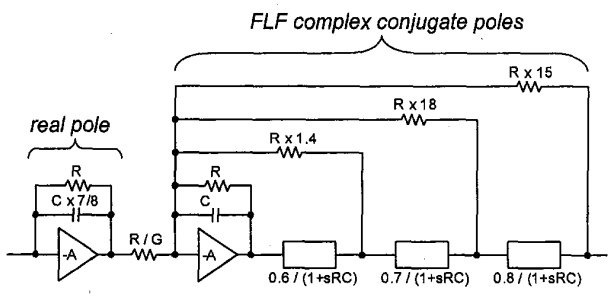

Figure 6: Simplified schematic of the shaper amplifier.

The coefficients reported in Fig. 6 were chosen to give, for a given input signal, the same maximum signal amplitude at the output of each internal stage of the FLF. Later in this subsection it will be shown that the minimization of the shaper noise contribution requires the use of large values for R. In order to emulate the very large resistors used in the multiple feedback, current mirrors and cascode stages were used, as shown in Fig. 7.

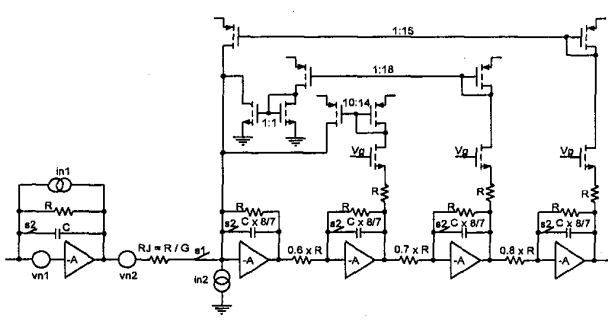

Figure 7: More detailed schematic of the shaper amplifier.

Once the values of R and C are defined, the gain of the shaper can be set through the ratio G between the value of R and the value of the injection resistor RJ. The programmability of the shaping time can be obtained by changing the value of C. It can be easily verified that, in order to keep the gain constant while changing the shaping time, the ratio RC/G must be kept constant. Thus, every change in the value of C requires a change in the value of the injection resistor RJ.

In Fig. 7 the series RJ-s1 represents a parallel connection of switchable resistors and the series C-s2 represents a parallel connection of switchable capacitors. The switches can be connected to the virtual grounds, as indicated in the same figure. Assuming that the MOS switch, when closed, operates always in strong inversion and triode region, the non linear dependence of the drain to source voltage can be approximated by [31]:

$$v_{ds} \approx \left(V_{gs} - V_{th}\right)\left[\frac{1}{2}\frac{i_d}{i_{dsat}} + \frac{1}{8}\left(\frac{i_d}{i_{dsat}}\right)^2\right] \tag{3}$$

where i_d is the drain current, i_{dsat} the saturation current, V_{gs} is the gate to source (i.e., V_{dd} to V_{in}) voltage and V_{th} is the threshold voltage. From this equation the following conditions for the minimum channel width W1 and W2 of the MOS switches s1 and s2 can be derived:

$$\begin{aligned} W1 &\geq \frac{L \cdot G}{R\mu C_{ox}} \frac{\sqrt{\frac{1}{2\varepsilon}\frac{V_{max}}{V_{gs} - V_{th}} - 1}}{V_{gs} - V_{th}} \\ W2 &\geq \frac{L \cdot C}{\mu C_{ox}} \frac{\sqrt{2\pi GBWP \frac{1}{2\varepsilon}\frac{V_{max}}{R C_i}}}{\left(V_{gs} - V_{th}\right)^{3/2}} \end{aligned} \tag{4}$$

where L is the channel length, V_{max} is the maximum voltage swing ε is the maximum tolerable integral linearity error, GBWP is the gain-bandwidth product of the amplifier and C_i the total capacitance at the input of each amplifier. The values of W1 and W2 necessary to satisfy a total error $\varepsilon < 0.1\%$ were found of the order of few tens of μm. It can be shown that, if the value of W1 is large enough, the switch s1 can also be used to trim the gain within ≈ 10% through its gate voltage without appreciable impact on the linearity.

As shown in subsection A, the gain of the channel can be reduced by reducing the gain N2 of the second of the dual-stage. For large values of charge released by the detector, the gain must be lowered in the dual-stage, rather than through G, in order to avoid the saturation of following stages.

When low values of $N = N1 \times N2$ are used, the noise contribution of the shaper can become non-negligible. In Fig. 7 the major noise sources of the shaper are shown: (i) v_{n1} is the equivalent series noise of the first amplifier, (ii) i_{n1} is the thermal noise of the first feedback resistor, (iii) v_{n2} is the equivalent series noise of the remaining part of the shaper (i.e., ≈ thermal noise of RJ) and (iv) i_{n2} is the equivalent parallel noise of the remaining part of the shaper (i.e., ≈ noise of the current mirrors).

Each contribution can be represented at the input of the channel as an additional equivalent parallel noise source δi_{neq}. It can be easily verified that δi_{neq} is given by:

$$\begin{aligned} \overline{\delta i_{neq}^2} = &\left(\frac{1}{N}\right)^2 \overline{i_{n1}^2} + \left(\frac{1}{NR}\right)^2 \overline{v_{n2}^2} + \left(\frac{1}{NG}\right)^2 \overline{i_{n2}^2} + \\ &+ \omega^2 \left[C_f^2 \overline{v_{n1}^2} + \left(\frac{C}{N}\right)^2 \overline{v_{n2}^2} + \left(\frac{RC}{NG}\right)^2 \overline{i_{n2}^2}\right] \end{aligned} \tag{5}$$

From Eq.(5) and taking into account that RC/G must be kept constant as the shaping time (i.e., C) changes, it follows for the additional contribution to the ENC:

$$\delta ENC^2 = \\ = \frac{A_1}{\tau}\left[C_f^2 S_{v1w} + \left(\frac{C}{N}\right)^2 S_{v2w} + \left(1+\frac{A_3}{A_1}\right)\left(\frac{RC}{NG}\right)^2 S_{i2w}\right] + \\ + A_2\pi\left[C_f^2 A_{v1f} + \left(\frac{C}{N}\right)^2 A_{v2f} + \left(1+\frac{A_3}{A_2}\right)\left(\frac{RC}{NG}\right)^2 A_{i2f}\right] + \\ + A_3\tau\left[\left(\frac{1}{NR}\right)^2 S_{v2w} + \frac{S_{i1w}}{N^2}\right] + A_4\pi\tau^2\frac{A_{i1f}}{N^2} \tag{6}$$

where A_1, A_2, A_3 and A_4 are coefficients related to the shaping, S_{vw}, S_{iw} are the bilateral white noise spectral densities and A_{vf}, A_{if} are the $1/f$ noise coefficients. It is worth noting that, as consequence of the condition on RC/G, the contribution of i_{n2} turns out to be inversely proportional to the shaping time τ.

C. Output Stage

One of the innovative circuit solutions implemented in the ASICs is a class AB rail-to-rail output stage. The development of this stage was due to the relatively low 3.3V bias voltage of the ASIC imposed by the technology [32]. The output stage has a gain ≈ -2 and dissipates a power ≈ 4mW. It can drive up to rail capacitive loads of hundreds of pF.

In Fig. 8 the simplified schematic of the output stage is shown. The core of this stage is the left (loaded) inverter, composed of MN and of two resistors, and characterized by a gain ≈ -2. The quiescent current of MN is set by MP.

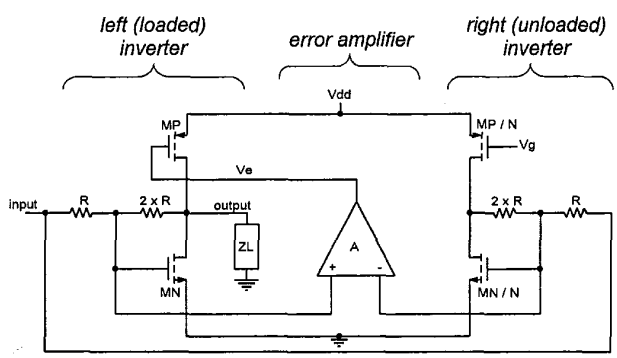

Figure 8: Simplified schematic of the output stage.

The right (unloaded) inverter is an N time scaled down replica of the loaded inverter. The resistors are not scaled down, but the mismatch has relatively low impact on the overall performance of the stage. The two inverters share the same input, but only the left one is loaded (i.e., it is the output of the stage).

When the impedance of the load $Z_L = R_L // C_L$ is high the two inverters exhibit almost the same voltage at their two virtual grounds. The error amplifier A consequently keeps its output voltage Ve equal to Vg. When Z_L is low the error amplifier A drives Ve to provide the necessary current to minimize the error, thus reducing the sensitivity of the gain to the load. The correction is effective from dc to a frequency set by the bandwidth of the error amplifier.

The stability criterion is straightforward, the loop gain G_{loop} being given by:

$$G_{loop} \approx A(s)\frac{g_{mP}Z_L(s)}{3+g_{mN}Z_L(s)} \tag{7}$$

where A(s) is the transfer function of the error amplifier A and g_{mN} and g_{mP} are respectively the transconductance of MN and of MP. The linearity is essentially determined by the right inverter, and the quiescent current can be accurately set through Vg and can be relatively small, thus classifying this stage as a class AB. As other classic low-power stages based on common source configurations, this stage is capable of operating within few tens of mV from the two rails [33-36].

In the output stage currently implemented in the ASICs a very simple configuration was used for the error amplifier. Simulations have shown that an improved design of the error amplifier can lead to non-negligible improvements with respect to the results reported here.

In Fig. 9 the frequency response of the output stage, measured with a load Z_L = 1MΩ // 100pF is shown.

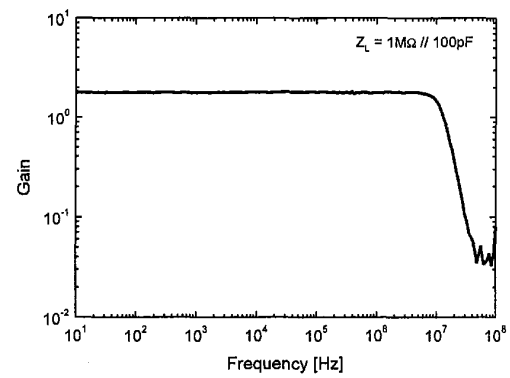

Figure 9: Measured frequency response of the output stage.

The presence of three poles can be observed. Two poles are related to the configuration, the third is due to the capacitive load and the ≈150Ω output resistance.

In Fig. 10 the driver response to a negative square pulse of amplitude -1V and rise time 1ns for different capacitive loads is shown. A rise time below 15ns is achieved with C_L = 10pF while for larger loads the limit is imposed only by the ≈150Ω output resistance and no slew rate limit occurs even operating close to the rail.

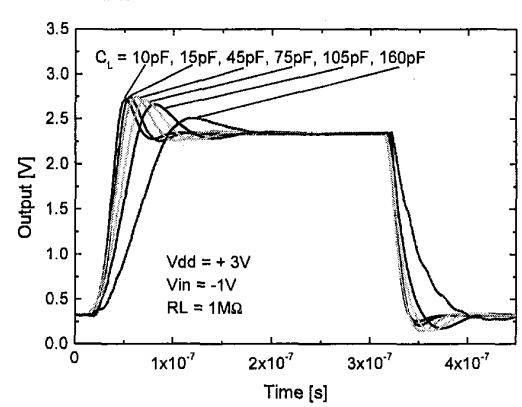

Figure 10: Measured output stage response to a negative square pulse of amplitude -1V for different capacitive loads.

In Fig. 11 the response of the ASIC channel to injected charges from 0.7fC to 15.3fC (non equal increments of charge) is shown. Its driving capability up to a few tens of mV from the +3V rail can be observed. The peaking time is 400ns and the overall integral linearity error is < 0.3% at 13fC.

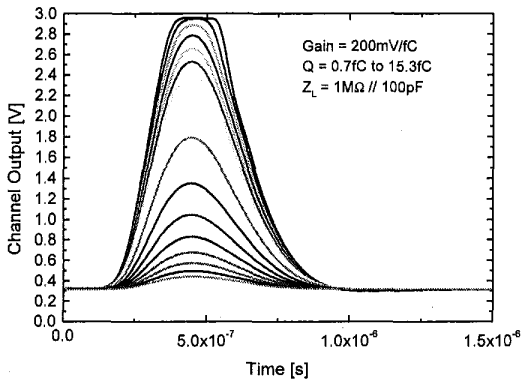

Figure 11: Measured channel response to different values of injected charge (not equal increment of charge).

D. Baseline Holder (BLH)

As shown in subsections A and B, CZT detectors can benefit from the use of dc-coupling and unipolar shaping. On the other hand these solutions expose the internal nodes and the output baseline to a strong dependence on the detector leakage current. In order to provide the ASIC channel with a stable output baseline both at dc, at low frequency and at high rate operations, the baseline holder (BLH) was developed. In addition, the channel implements a switch which enables direct reading of the output of the first pole stage thus providing a way to measure the value of the detector leakage current.

The BLH is composed of three stages: a differential amplifier, a non-linear dynamic buffer and a low-pass filter. The low-pass filter provides the dominant pole necessary for the stability of the loop. The non-linear buffer dynamically reduces the gain of the feedback loop only in presence of large and fast signals. Due to the presence of the low-pass filter, the BLH is characterized by a very low bandwidth (has essentially zero response to each pulse) and, for this reason, conceptually differs from the feedback baseline restorer (BLR) which, in order to provide a quick baseline restoration before the arrival of following pulse, it requires a large bandwidth (it must respond to each pulse) [37-40]. The BLH was used for the first time (and for the only time at our knowledge) by L. V. East [41] in 1970. Our approach consists of the realization of the non-linear buffer through a one-directional slew-rate-limited stage. A brief description and some relevant results on the BLH are reported here. A more detailed description, the theoretical analysis and most of the experimental results are reported in [42].

In Fig. 12 a simplified schematic of the BLH is shown. The non-linear buffer is composed of the p-channel MOSFET MP in follower configuration and of the capacitance C_1. The bias current I_{dP} of MP is set by a p-channel MOSFET through the bias voltage Vg1. If I_{dP} is set to a low value and C_1 is set to a large enough value, the response of the follower to large and fast pulses is slew-rate limited to I_{dP}/C_1.

The low-pass filter is composed of the n-channel MOSFET MN in follower configuration, of the capacitance C_2 and of an output n-channel MOSFET Mo in the common source configuration for the voltage-to-current conversion. The bias current I_{dN} of MN is set by a n-channel MOSFET through the bias voltage Vg2. If I_{dN} is set to a very low value and C_2 is set to a very high value, the frequency response of the follower exhibit a pole at very low frequency (i.e., the dominant pole of the loop gain). For small and slow signals no slew-rate limit occurs and the high loop gain keeps $V_{OUT} \approx V_{BL}$. For large and fast signals the strong reduction in gain due to the one-directional slew-rate limited stage lets the main signal flow through the forward stages almost unaffected by the feedback. The design criteria for stability and additional circuitry to prevent effects from swings of sign opposite with respect to the main pulses are also discussed in [42].

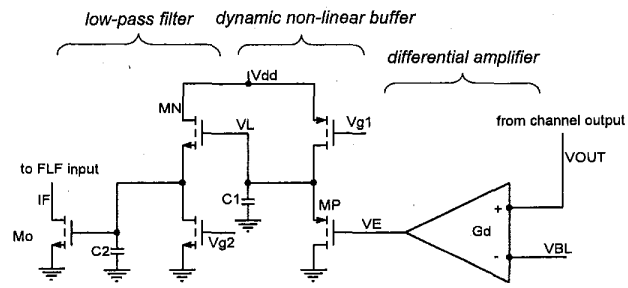

Figure 12: Simplified schematic of the baseline holder (BLH).

The BLH introduces an approximated high-pass filter in the main transfer function V_{OUT}/I_{IN} [42]. A major consequence of the reduction of channel dc gain is that the sensitivity of the output baseline to the detector leakage current I_{DET} is strongly reduced. An increase in baseline ≈ 0.4mV was measured for an increase in I_{DET} from 1nA to 2nA and ≈ 0.7mV from 1nA to 10nA.

It is well known that, when an ac-coupling (i.e., high-pass filter) is present along the channel with unipolar shaping, the output baseline exhibit a shift as the rate of pulses increases. This shift is originated by the zero-area requirement due to the ac coupling. In a similar way, due to the presence of the approximated high-pass filter generated by the BLH a dependence of the baseline on the rate must be expected. In order to minimize this effect the one-directional slew-rate limited stage was introduced. The dynamic non-linearity introduced by the slew-rate limit affects only fast signals, without limiting the gain of the BLH when slow movements of the baseline occur.

In [42] it is shown that there exists a ratio I_{dP}/C_1 below which the baseline shift is minimized. The shift depends on the gain G_d of the differential amplifier, on the peaking time τ_P and on the rate Rt.

In the case of periodic arrival of pulses the asymptotic shift of the baseline it is given by [42]:

$$\delta V_{BLO} \approx -2\tau_P \, Rt \frac{0.04}{G_d}, \qquad (8)$$

and experimental results in agreement with Eq.(8) were found.

In the case of random arrival of the pulses at average rate Rt, the relative standard deviation is given by [42]:

$$\frac{N}{S} \approx \sqrt{\frac{Rt(2\tau_P)^2}{2\tau_{HP}}\left(\frac{2\cdot 0.04}{G_d \cdot V_P}\right)^2} \qquad (9)$$

where V_P is the output peaking voltage and τ_{HP} is the approximated high-pass time constant. A resolution higher than 12 bit was found for $\tau_P \times Rt < 0.1$ and V_P=2V.

In Fig. 13 the ASIC channel response to $Q_{DET} \approx 12$fC with rate increasing from 20kHz to 500kHz is compared to the ac-coupling. The negligible movement of the baseline while the rate changes of more than one order of magnitude, can be observed.

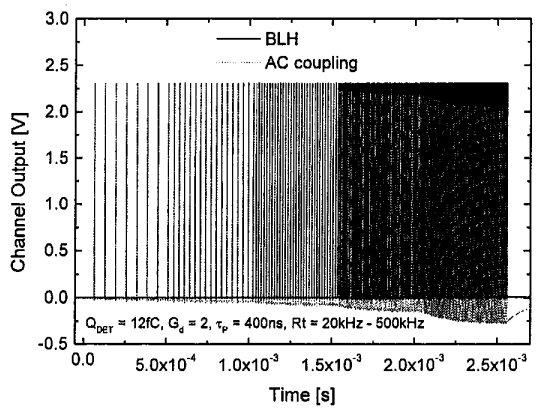

Figure 13: Experimental comparison for Q_{DET}=12fC and increasing rate Rt=20kHz - 500kHz between ASIC channel output and case with BLH disabled and ac-coupling with same time constant of the approximated high-pass filter.

III. PROTOTYPES

Several prototypes were designed, produced and tested, all giving results in agreement with the predictions. In Table 2 the list of the currently available prototypes is reported.

Table 2
Currently available prototypes

	application	channels	shaping	gain [mV/fC]	pk time [μs]
IC45	B,D,E	2	unip.	200	0.4
IC46	B,D,E	2	unip.	200	0.4
IC48	B	2	bip.	260	0.2
IC49	B,D,E	4	unip.	200	0.4
IC54	A	16	unip.	30-200	0.9 - 1.2
IC55	C	8	unip.	26-180	2.25 - 3.0
IC56	B	4	bip.	260	0.2
IC59	D,E	4	unip.	200	0.4
IC60	A	16	unip.	30-200	0.6 - 4.0

Each prototype was designed to be used in some specific applications ranging from general purpose (A) to medical (B: bone densitometry; C: intra-operative probe), security (D: baggage scanning) and industrial (E: down-hole logging).

In Fig. 14 the measured response of a bipolar shaping prototype and of a unipolar shaping prototype are shown. All prototypes of Table 2 were produced in the CMOS HP 0.5μm technology with linear capacitor and non silicided resistor options available through the MOSIS service [43].

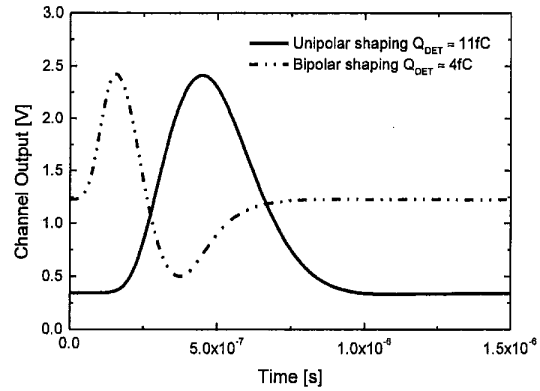

Figure 14: Measured channel response of a bipolar shaping prototype and of a unipolar shaping prototype.

IV. OTHER EXPERIMENTAL RESULTS

In this section some other typical experimental results and the first test results with CZT detectors are reported.

A. Linearity and Dependence on Temperature

In Fig. 15 the typical integral linearity error is shown. These results are currently affected by the limits in the measurement system used (8 bit resolution oscilloscope operating in averaging mode) and can be improved by using a good quality PHA. Simulations have shown that the linearity is limited by the output stage.

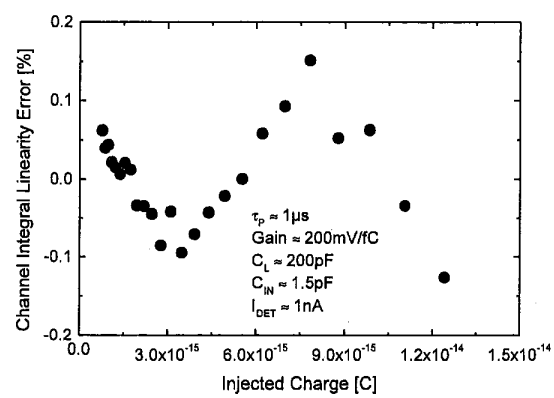

Figure 15: Measured channel integral linearity error.

Fig. 16 shows the dependence of channel response on the temperature ranging –30 °C to +50 °C. The charge was injected through the internal calibration capacitor (≈ 100fF). The dependence of the value of this capacitor on the temperature (≈ 30ppm/°C) was neglected when compared to the observed dependence of gain (≈ -400ppm/°C). A dependence of the baseline on the temperature ≈ 75μV/°C and of the peaking time ≈ 65ppm/°C were also measured. The measured tem-

perature coefficient for the non-silicided poly resistors available with the technology [43] was ≈ 372ppm/°C.

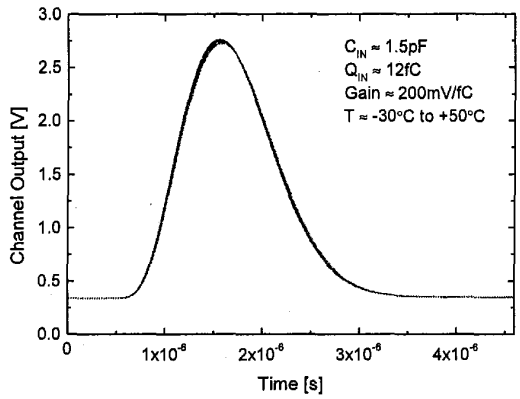

Figure 16: Measured channel response to Q_{DET}≈12fC for different values of temperature T.

B. Parasitics and Cross Talk

A parasitic effect which can limit the performance of the ASIC is due to the parasitic feedback capacitance C_{IO} between the output and the input of the channel. This capacitance, largely due to the bonds, lies in the range of few hundreds of attofarad and is responsible for the small distortion of the output pulse shown in Fig. 17. A small piece of grounded copper tape located over part of the ASIC ceramic cover provided enough shielding to reduce this effect down to a negligible level.

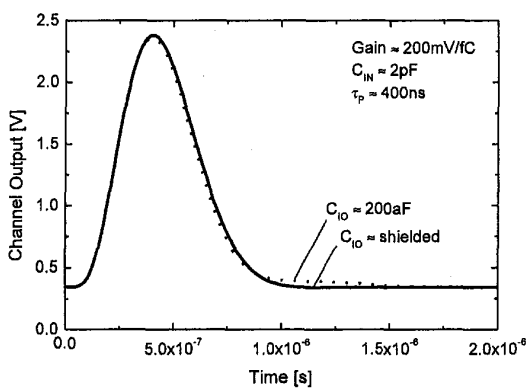

Figure 17: Distortion generated by the parasitic feedback capacitance C_{IO} between the output and the input of the channel.

Through measurements and simulations it was possible to locate the main sources of cross talk and to evaluate the contribution of each. Most of the cross-talk was due to parasitics external to the ASIC. The main contributions are shown in the simulation of Fig. 18. The cross-talk is here expressed as percent ratio between maximum amplitude in secondary channel and maximum amplitude in main channel.

An important source of cross-talk was the previously discussed parasitic capacitance C_{IO} between inputs and outputs. With an inverted bipolar shape (see Fig. 18) this contribution at τ_P ≈ 400ns was around ≈ 0.25% per 10aF of C_{IO}. The shield was effective in reducing this contribution down to negligible values.

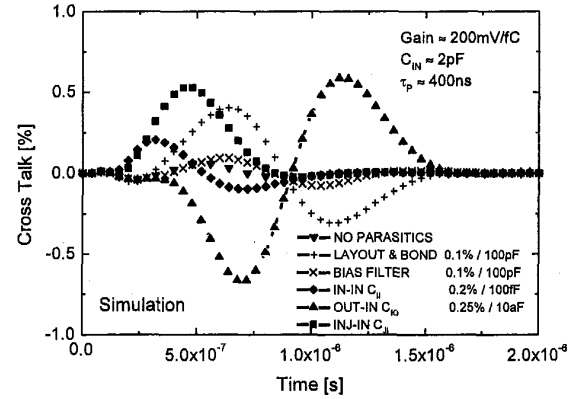

Figure 18: Simulation of the main contributions to the cross-talk.

Another important source of cross-talk was the parasitic capacitance C_{II} between adjacent inputs. A contribution at τ_P ≈ 400ns around ≈ 0.2% per 100fF of C_{II} was measured. An accurate choice of the external filtering capacitance between the power supply and ground is most important in the minimization of the cross-talk. The use of low equivalent series resistor capacitances (low ESR) reduced this contribution down to ≈ 0.1% per 100pF of capacitive output load C_L at τ_P ≈ 400ns. Layout parasitic resistors and inductors contributed a comparable amount.

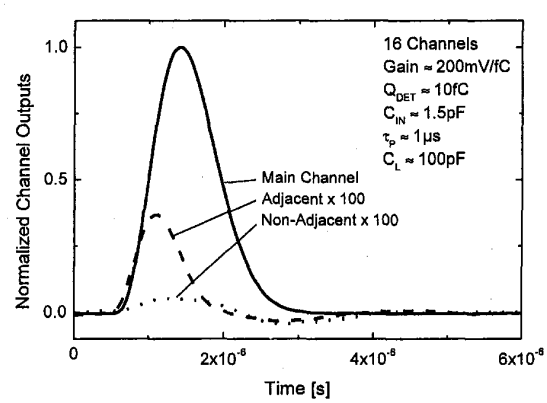

Figure 19: Typical cross-talk measured for adjacent and non-adjacent channels.

In Fig. 19 the typical cross-talk at τ_P ≈ 1μs measured for adjacent and non-adjacent channel is shown. Cross-talk values < 0.4% for adjacent channels and < 0.1% for non-adjacent channels can be observed. The parasitic capacitance C_{II} ≈ 150fF between adjacent inputs (bonds plus board lines) was largely responsible for the difference.

C. Overall Performance

In Table 3 the performance of a 16 channel version are summarized. The input of each channel is provided with ESD protection.

Table 3
Typical measured ASIC performance

Size	5.1mm×3.7mm
Channels	16
Shaping	Unipolar 5th Order Complex Semigaussian
Gain	30mV/fC, 50mV/fC, 100mV/fC, 200mV/fC
Peaking time	0.6μs, 1.2μs, 2.4μs, 4μs
ENC^2 (1.2μs, 200mV/fC)	$\approx 26^2+(27/pF)^2+55^2/\sqrt{nA}+0.17Q/q$
ENC Dispersion (σ)	≈ 10%
Power dissipated	≈ 18mW/ch
Integral Linearity Error	< 0.3% Full Range (12.5fC) at 200mV/fC
Cross Talk (bonded)	< 0.4% (< 0.1% non adjacent)
Baseline Adjustment	-100mV to +400mV
Detector Leakage Current	< 150nA, Self Adaptive
Gain vs C_{IN}	< 0.1% / pF
Baseline vs I_{DET}	< 300μV / nA
Gain vs I_{DET}	< 0.1% / nA
Baseline vs Vdd	< 30μV / mV
Gain vs Vdd	< 0.001% / mV
Baseline vs Temperature	≈ 75μV / °C
Gain vs Temperature	≈ -0.040% / °C (≈ -400 ppm / °C)
Peak. Time vs Temperature	≈ 0.0065% / °C (≈ 65 ppm / °C)
Max Baseline Shift vs Rate	< 8mV at Fixed Rate × Peaking Time ≈ 0.2
Max Gain Change vs Rate	< 0.1% at Fixed Rate × Peaking Time ≈ 0.2
Gain Dispersion (6σ)	≈ 0.32%
Calibration Cap. Disp. (6σ)	≈ 0.13% (nominal value 100fF)

The expression for the ENC reported in Table 3 takes into account the increase in ENC due to the reset system for both the stationary and the non-stationary noise contribution [25]. The value of the capacitance used in the expression must not include input MOSFET gate capacitance (≈ 220fF) and ASIC parasitic capacitance (i.e., pad and bond, ≈ 200fF) which are included in the first term. But it must include detector capacitance and board interconnect parasitic capacitance C_P. The noise contribution from the dielectric losses of C_P must also be considered (see Appendix).

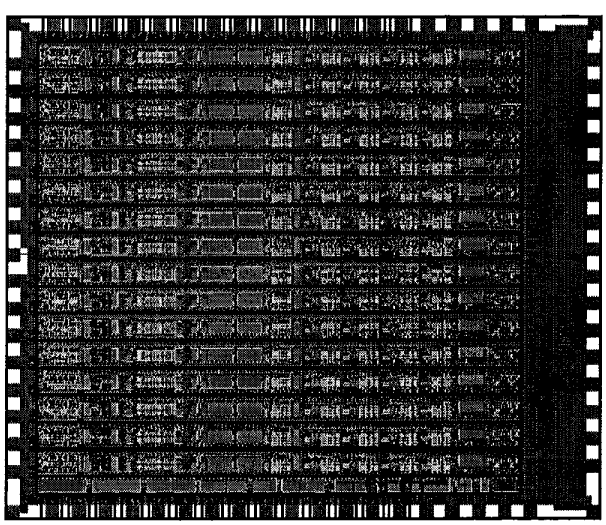

Figure 20: Typical layout of a general purpose 16 channel version (size ≈ 5.1mm × 3.7mm).

As an example, with C_{IN} = 2pF, I_{DET} = 1nA and Q_{DET} = 1fC an ENC ≈ 93e⁻ (FWHM ≈ 1keV for CZT) must be expected. The shot noise contribution from I_{DET} ($\approx 0.77\tau_P I_{DET}/q$) must be added to ENC^2. The noise measurements were in agreement with the theoretical predictions.

From Table 3 it can be observed that these ASICs have typical performance capable of satisfying a large number of applications with at least one order of magnitude savings in power, volume and cost with respect to hybrid or discrete circuits. The typical layout of a 16 channel version is shown in Fig. 20.

D. Tests with CZT Detectors

The ASICs were tested with CZT detectors and radiation sources. In Figs. 21 and 22 the measured energy spectra of ^{241}Am and ^{57}Co are shown in the case of a planar electrode 3×3×7 mm^3 CZT detector. The results were comparable to the ones achieved with the same detector and discrete electronics.

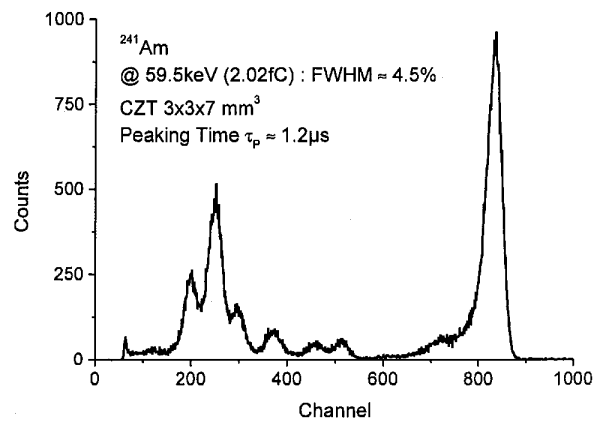

Figure 21: Measured energy spectrum of ^{241}Am (α-particles shielded).

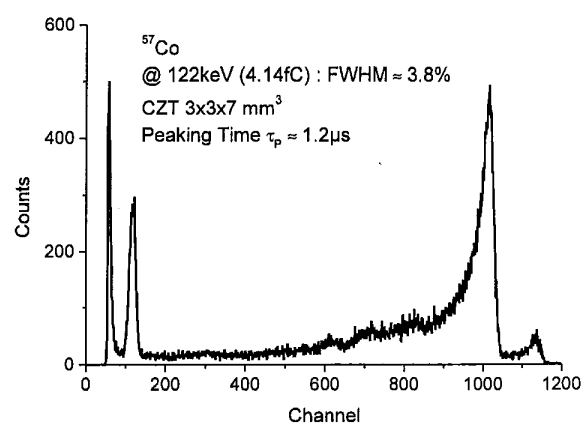

Figure 22: Measured energy spectrum of ^{57}Co.

V. Conclusions and Future Work

As a result of a cooperation between Brookhaven National Laboratory and eV Products a generation of readout ASICs was developed. The good performance of these ASICs, characterized by several innovative solutions, are in agreement with the predictions. They are proposed as valuable alternative to discrete solutions in most CZT applications. The high performance ASICs are a starting point for the development of complete mixed systems provided with self-trigger, automatic gain and baseline equalization, pulse height analysis, counting and storage capabilities.

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VII. Appendix

The approach to the evaluation of dielectric loss contribution to ENC^2 from a capacitor connected between input and ground (i.e., board interconnect parasitic capacitance, external injection/calibration capacitor, etc.) is reported here.

The admittance of the capacitor can be expressed as [44]:

$$Y(j\omega) = \omega C_P \{j + \tan[\delta(\omega)]\} \tag{10}$$

where C_P is the value of the capacitance, δ the loss angle and ω the angular frequency. From Nyquist theorem, the power spectral density S_{inP} of the equivalent parallel noise generator associated to the capacitor is given by [45]:

$$S_{inP} = 2kT \cdot Re[Y(j\omega)] = 2kT \cdot \omega C_P \, tg[\delta(\omega)] \tag{11}$$

The contribution δS_{vn} of this component to the equivalent input series noise generator S_{vn} is given by:

$$\delta S_{vn} = \frac{S_{inP}}{|Y_{IN}|^2} \approx 2kT \frac{\omega C_P \, tg[\delta(\omega)]}{\omega^2 C_{IN}^2} = 2kT \frac{C_P \, tg[\delta(\omega)]}{\omega C_{IN}^2} \tag{12}$$

where Y_{IN} is total input admittance and C_{IN} is the total input capacitance.

By assuming for the dielectric loss factor a value $\tan[\delta(\omega_{SH})]$, where $\tau_{SH} = 1/\omega_{SH}$ is the shaper time constant ($\tau_{SH} \approx 0.4\tau_P$ in our case [25]), and by neglecting its dependence on the frequency [46], the contribution of Eq.(12) turns out to behave like $1/f$ series noise. Its contribution to ENC^2 can now be easily calculated as:

$$\delta ENC^2 \approx A_2 \, 2kT C_P \, tg[\delta(\omega_{SH})] \tag{13}$$

where A_2 is the $1/f$ series noise coefficient for the ENC (≈ 1.048 in our case, typically close to unit).

The values of $\tan[\delta(\omega_{SH})]$ are in the range $5 \cdot 10^{-3}$ - $50 \cdot 10^{-3}$ depending on the quality and material of the dielectric. For $C_P = 0.5$pF, $\tan[\delta(\omega_{SH})] = 30 \cdot 10^{-3}$ it follows from Eq.(13) $\delta ENC^2 \approx 70^2$ squared rms electrons.

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