A CMOS Baseline Holder (BLH) for Readout ASICs[1]

G. De Geronimo[2], P. O'Connor[2] and J. Grosholz[3]
[2]Brookhaven National Laboratory, Instrumentation Division, Bldg 535B, Upton, NY 11973, USA
[3]eV Products, Div. of II-VI Inc., 373 Saxonburg Blvd., Saxonburg, PA16056, USA

Abstract

As a result of a cooperation between Brookhaven National Laboratory and eV Products a generation of high performance readout ASICs was developed. One of the novel circuit solutions implemented in the ASICs is the baseline holder (BLH), a system which provides setting and stabilization of the output baseline both at low frequency and at high rate operation. The BLH is conceptually different from the baseline restorer (BLR). With a output peaking voltage 2V (10fC), a peaking time 400ns and a rate 500kHz, an asymptotic shift of the baseline < 8mV was measured in the periodic case. A resolution higher than 12 bit was found in the random arrival of pulses case.

I. INTRODUCTION

The inherent advantages and rapid improvement of $Cd_xZn_{1-x}Te$ (CZT) detectors led to an increase in the number of their applications [1-4]. Several motivations suggest that most of these applications can benefit from the use of ASIC readout in place of discrete solutions [5]. As a result of a cooperation between Brookhaven National Laboratory and eV Products a generation of novel high performance readout ASICs was developed [5]. The ASICs, realized in CMOS 0.5μm technology, are available in several versions, single or multi-channel and with unipolar or bipolar shaper, in view of their use in research, spectroscopy, medical and industrial applications.

CZT detectors suffer from long hole collection time and charge trapping effects [6]. In order to minimize the ballistic deficit the signal should be processed with a shaping producing a long flat top [7,8]. The unipolar shaping provides a lower curvature of the peak with respect to bipolar shaping while operating at equal rate (i.e., at equal pulse width). The ASIC channels implement high order unipolar semigaussian shaping and the capability to operate dc-coupled to the CZT detectors [9,10], thus exposing the internal nodes and the output baseline to a dependence on the detector leakage current, which in CZT detectors vary over a relatively wide range.

In order to provide the ASIC with a stable output baseline both at dc, low frequency and at high rate operations, the baseline holder (BLH) was developed. In the following, the structure of the BLH is discussed and the first experimental results are reported.

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II. DESCRIPTION OF THE BASELINE HOLDER (BLH)

Fig. 1 shows a simplified schematic of the part of the ASIC readout channel which involves the baseline holder (BLH). The BLH is a stage which compares the output voltage V_{OUT} of the channel to a reference voltage V_{BL} and, after some signal processing, feeds the signal back to the input of the shaper amplifier. In order to minimize the dependence of the output baseline on the process parameters, the output voltage of the channel (and not a channel internal node before the output) is used by the BLH. The signal is then fed back to the input of the shaper amplifier in order to include in the stabilization as many stages as possible. Due to their higher sensitivity to additional noise sources, all stages preceding the shaper amplifier (i.e., charge preamplifier and compensation [5]) are not involved in the BLH. In the following it is assumed that the input of the shaper amplifier is a virtual ground and that a subtraction occurs between the main signal current I_{IN} and the feedback current I_F.

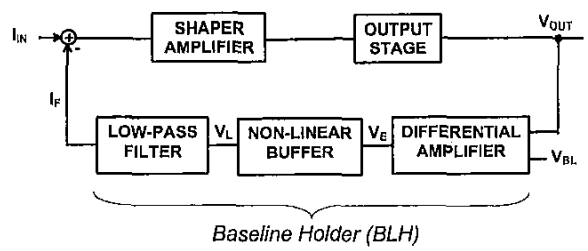

Figure 1: Simplified schematic of the part of the ASIC channel involving the baseline holder (BLH).

The BLH is composed of three stages: a differential amplifier, a non-linear buffer and a low-pass filter. The low-pass filter provides the dominant pole necessary for the stability of the loop. The non-linear buffer dynamically reduces the gain of the feedback loop only in presence of large and fast signals.

Due to the presence of the low-pass filter, the BLH is characterized by a very low bandwidth (has essentially zero response to each pulse). For this reason, it conceptually differs from the feedback baseline restorer (BLR) which, in order to provide a quick baseline restoration before the arrival of following pulse, requires a large bandwidth (it must respond to each pulse) [11-14]. The BLH was used for the first time (and for the only time to our knowledge) by L. V. East [15] in 1970. Our novel approach consists in the way we realized the non-linear buffer through a one-directional slew-rate limited stage. Among the advantages of the BLH on the BLR are no need for a gating signal and negligible modification of the weighting function. Drawback is the residual fluctuation of the

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baseline, discussed later in this section.

In Fig. 2 a more detailed schematic of the BLH is shown. The non-linear dynamic buffer is composed of the p-channel MOSFET MP in follower configuration and of the capacitance C_1. The bias current I_{dP} of MP is set by a p-channel MOSFET through the bias voltage Vg1. If I_{dP} is set to a low value and C_1 is set to a large enough value, the response of the follower to large and fast pulses is one-directional slew-rate limited to I_{dP}/C_1. The low-pass filter is composed of the n-channel MOSFET MN in follower configuration, of the capacitance C_2 and of the output n-channel MOSFET Mo in common source configuration for the voltage-to-current conversion. The bias current I_{dN} of MN is set by a n-channel MOSFET through the bias voltage Vg2. If I_{dN} is set to a very low value and C_2 is set to a very high value, the frequency response of the follower exhibit a pole at very low frequency (i.e., the dominant pole of the loop gain). For small and slow signals no slew-rate limit occurs and the high loop gain keeps $V_{OUT} \approx V_{BL}$. For large and fast signals the attenuation due to the one-directional slew-rate limited stage reduces the loop gain and the main signal flows through the forward stages almost unaffected by the feedback.

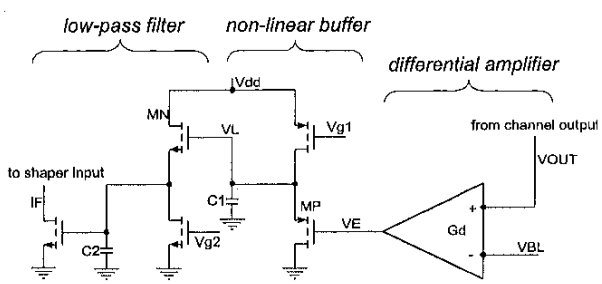

Figure 2: More detailed schematic of the baseline holder (BLH).

For small signals both the non-linear buffer and the low-pass filter exhibit a linear behavior. The feedback transfer function I_F/V_{OUT} is given by:

$$\frac{I_F}{V_{OUT}} \approx \frac{g_{mo}G_d}{\left(1+\frac{sC_1n_PV_T}{I_{dP}}\right)\left(1+\frac{sC_2n_NV_T}{I_{dN}}\right)} \tag{1}$$

where g_{mo} is the transconductance of Mo, G_d is the gain of the differential amplifier, I_{dP} and I_{dN} are respectively the drain currents of MP and MN, which are assumed to operate in weak inversion, and $V_T = kT/q$ is the thermal voltage. The corresponding transconductances are given in a first approximation by I_{dP}/n_PV_T and I_{dN}/n_NV_T respectively, where n_P and n_N are the subthreshold slope coefficients (typically between 1 and 1.5) [16]. It can be easily verified that, under the two conditional assumptions $C_2n_NV_T/I_{dN} >> G_{loop}(0)\tau_{SH}$ (τ_{SH} being the time constant of the shaper amplifier) and $C_2/I_{dN} >> G_{loop}(0)C_1/I_{dp}$, the transfer function V_{OUT}/I_F can be well approximated by:

$$\frac{V_{OUT}}{I_{IN}} \approx \frac{H(s)}{G_{loop}(0)} \frac{1+\frac{sC_2n_NV_T}{I_{dN}}}{1+\frac{sC_2n_NV_T}{I_{dN}G_{loop}(0)}} \tag{2}$$

where H(s) is the forward transfer function (i.e., shaper amplifier plus output stage) and $G_{loop}(0) = I_{dN}g_{mo}G_dH(0)$ is the dc loop gain. It is worth noting that both conditional assumptions lead to the stability of the loop. In order to satisfy these conditions a ratio $C_2/C_1 \approx 10^2$ and a ratio $I_{dP}/I_{dN} \approx 10^3$ with $I_{dN} \approx 10^{-11}$ were chosen.

From Eq.(2) the presence of a zero and a pole, which realize an approximated high-pass filter, can be observed. The filter strongly reduces the channel gain at low frequency down to a factor $G_{loop}(0)$. In Fig. 3 is shown the measured small signal transfer function V_{OUT}/I_{IN} of the ASIC channel where both the shaping component at high frequency and the high-pass corner frequency can be observed.

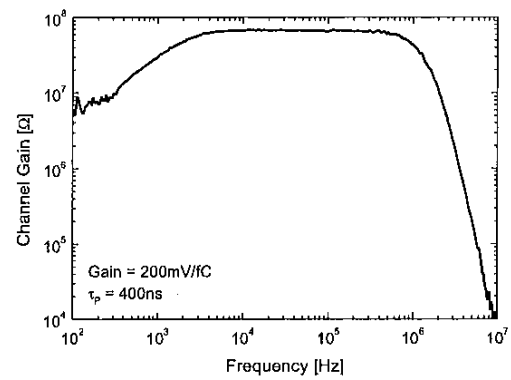

Figure 3: Measured channel small signal transfer function.

A major consequence of the reduction of channel gain at low-frequency is that the sensitivity of the output baseline to the detector leakage current I_{DET} is strongly reduced. In Fig. 4 the measured baseline dependence on I_{DET} is shown, compared to the expected dependence in absence of BLH.

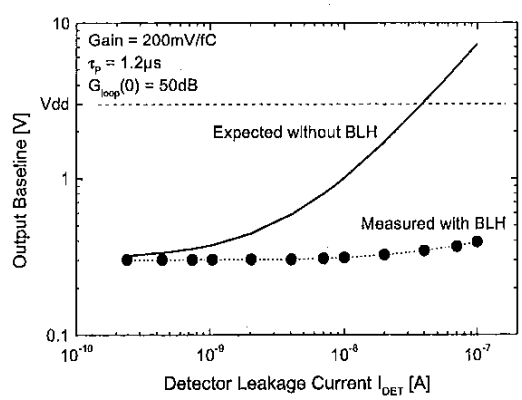

Figure 4: Output baseline dependence on detector leakage current I_{DET}.

In absence of BLH a strong dependence of the output baseline on I_{DET} must be expected up to saturation to the positive supply Vdd = 3V at $I_{DET} \approx 30$nA. With the BLH an increase in baseline ≈ 0.4mV was measured for an increase in I_{DET} from 1nA to 2nA and ≈ 0.7mV from 1nA to 10nA. Further improvements are expected from next versions, designed with higher dc loop gain.

It is well known that, when an ac-coupling (i.e., high-pass filter) is present along the channel with unipolar shaping, the output baseline exhibits a shift as the rate of pulses increases. This shift is originated by the zero-area requirement due to the ac coupling.

In a similar way, due to the presence of the approximated high-pass filter generated by the low-pass filter (see Eq.(2)) a dependence of the baseline on the rate must be expected. But this effect is strongly minimized by the dynamic non-linearity introduced by the slew-rate limited stage. The one-directional limit in slew-rate strongly reduces the area of the pulse before it is processed by the low-pass filter. Only fast and large enough signals are affected, and no limit in gain occurs for slow movements of the baseline.

In order to optimize the design of the BLH, the expected shift of the baseline at a given rate must be evaluated. In the case of ac-coupling, by assuming the output pulse triangular with peaking time τ_P, width $\tau_W \approx 2\tau_P$ and peaking voltage V_P, the shift $-\delta V_{BLO}$ of the output baseline at a rate Rt can be approximated by equating the areas:

$$\frac{1}{2}\frac{(V_P-\delta V_{BLO})^2}{V_P}\tau_W \approx \left(\frac{1}{Rt}-\tau_W\frac{V_P-\delta V_{BLO}/2}{V_P}\right)\delta V_{BLO}\,. \quad (3)$$

It follows for δV_{BLO}:

$$\delta V_{BLO} \approx -V_P\tau_P Rt\,. \quad (4)$$

In the case of BLH and for large values of the differential amplifier gain G_d, the pulse to be processed by the non-linear stage is almost rectangular, clipped to Vdd and having width $\approx 2\tau_P$. The shift $-\delta V_{BLO}$ of the output baseline is now given by:

$$\delta V_{BLO} \approx -2V_{dd}\tau_P Rt\frac{Ka}{G_d} \quad (5)$$

where Ka is the ratio between the area of the pulse at the output of the differential amplifier and the area processed by the low-pass filter. Due to the slew-rate limit, a value of Ka << 1 is expected.

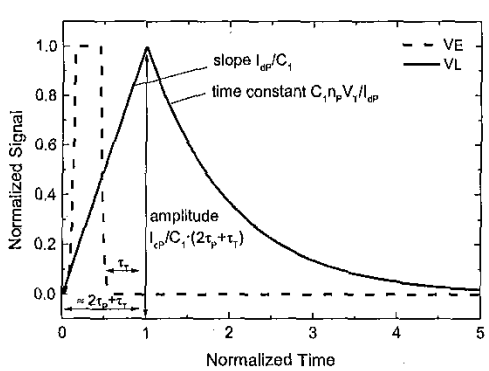

Figure 5: Simulation of normalized signals V_L and V_E for the approximated evaluation of the coefficient Ka.

The coefficient Ka can be evaluated in a very first approximation from Fig. 5, where the normalized signals V_L and V_E (see Fig. 2) are simulated. It follows:

$$Ka \approx \frac{\frac{(2\tau_P+\tau_T)^2}{2}\frac{I_{dP}}{C_1}+\int_0^\infty(2\tau_P+\tau_T)\frac{I_{dP}}{C_1}\exp\left(\frac{-t}{C_1 n_P V_T/I_{dP}}\right)dt}{2\tau_P V_{dd}} = \frac{n_P V_T}{V_{dd}}\left(1+\frac{\tau_T}{2\tau_P}\right)\left[1+\frac{I_{dP}\tau_P}{2n_P V_T C_1}\left(1+\frac{\tau_T}{2\tau_P}\right)\right] \quad (6)$$

where τ_T takes into account the increase in duration of the slew-rate limited component of V_L due to the tail of the output pulse. For a semigaussian shaping τ_T can be approximated by:

$$\tau_T \approx 2\tau_P\sqrt{\ln\frac{V_P G_d}{2\tau_P I_{dP}/C_1}}\,. \quad (7)$$

In Fig. 6 the dependence of Ka on the slew rate I_{dP}/C_1 is reported for different values of τ_P. It is worth noting that Eq.(6) applies for $2\tau_P I_{dP}/C_1 < V_{dd}$.

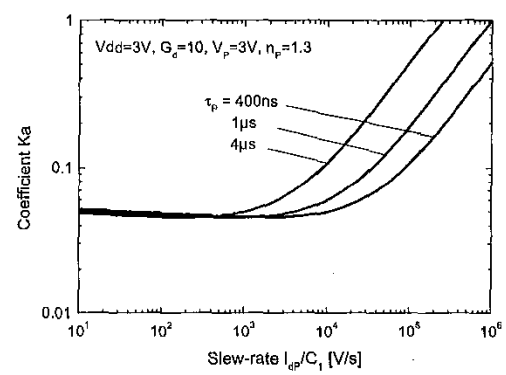

Figure 6: Coeff. Ka vs slew-rate I_{DET}/C_1 for different values of τ_P.

A minimum of Ka ≈ 0.04 is found for $I_{dP}/C_1 < n_P V_T/(6\tau_P)$, and it is almost independent of G_d, V_{dd} and V_P. For $C_1 \approx 200$fF a good choice which satisfies also the previously discussed condition for the stability of the loop is $I_{dP} \approx 1$nA. From Eqs. (5), (6) and (7) and Fig. 6 it follows:

$$\delta V_{BLO} \approx -2\tau_P Rt\frac{0.04}{G_d} \quad (8)$$

The Eq.(8) shows that the baseline shift reaches a maximum almost independent of the output peaking voltage V_P. When $\tau_P Rt = 0.2$ and $G_d = 10$ it follows $\delta V_{BLO} \approx 1.6$mV, to be compared to 40mV without the slew-rate limited stage and to $\approx 0.2V_P$ for an ac coupling with same time constant of the approximated high-pass filter.

Both SPICE simulations and experimental results were found in agreement each other and with Eq.(8) within few tens of percent. Fig. 7 compares the ASIC channel response to a sequence of charges $Q_{DET} \approx 1$fC injected at rate ≈ 500kHz to the response with the BLH disabled and an ac-coupling with

same time constant of the approximated high-pass filter. After 512 samples the asymptotic value of the baseline shift can be measured. A baseline shift < 5mV was measured with the BLH, to be compared to ≈ 25mV for the ac-coupling. In Fig. 8 the same experimental comparison for $Q_{DET} \approx 10fC$ is reported. After 512 samples a baseline shift < 8mV was measured, to be compared to ≈ 300mV for the ac-coupling.

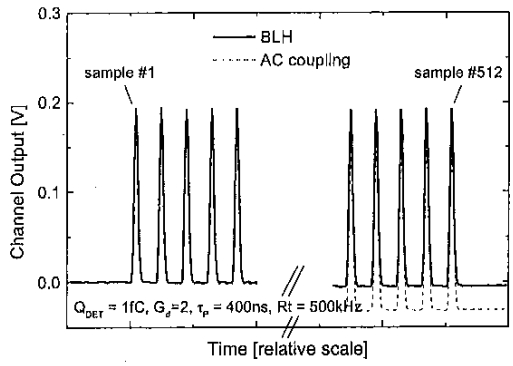

Figure 7: Experimental comparison for $Q_{DET} = 1fC$ and Rt = 500kHz between ASIC channel output and case with BLH disabled and ac-coupling with same time constant of the approximated high-pass filter.

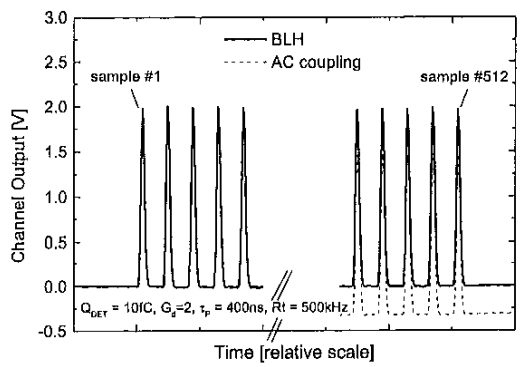

Figure 8: Experimental comparison for $Q_{DET} = 10fC$ and Rt = 500kHz between ASIC channel output and case with BLH disabled and ac-coupling with same time constant of the approximated high-pass filter.

It is worth noting that the stability of the baseline provides also an increase in the voltage headroom for the output pulses because its dc value V_{BLO} can be set closer to the minimum voltage supply V_{ss} of the ASIC (in our ASICs we set $V_{BLO} \approx$ 300mV and V_{ss} = 0V).

Fig. 9 compares the ASIC channel response to $Q_{DET} \approx 12fC$ with rate increasing from 20kHz to 500kHz to the ac-coupling. The negligible movement of the baseline while the rate changes of more than one order of magnitude, can be observed.

Concerning the noise, due to the long time constant of the feedback loop, the weighting function [17,18] is almost unchanged with respect to the case of purely unipolar shaping. Consequently no appreciable decrease in resolution must be expected apart from the thermal noise associated to Mo.

The Eq.(8) predicts in a first approximation the average shift of the baseline as consequence of a change in the average rate of pulses.

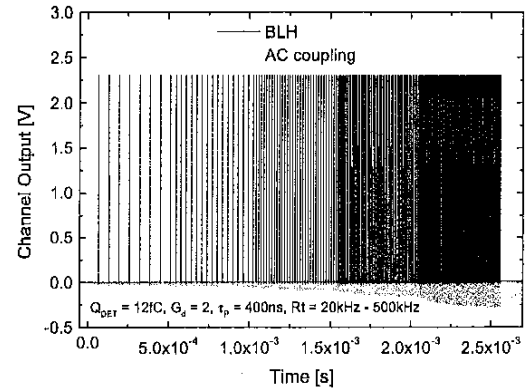

Figure 9: Experimental comparison for $Q_{DET} = 12fC$ and increasing rate Rt = 20kHz - 500kHz between ASIC channel output and case with BLH disabled and ac-coupling with same time constant of the approximated high-pass filter.

Baseline fluctuations can also occur at a given average rate as consequence of the random arrival of the pulses. In the case of an ac-coupling the broadening associated to the baseline fluctuations can be described by the relative standard deviation [19]:

$$\frac{N}{S} \approx \sqrt{\frac{Rt(2\tau_P)^2}{2\tau_{HP}}} \tag{9}$$

where τ_{HP} is the time constant of the high-pass filter associated to the ac-coupling.

In the case of the BLH, due to the dynamic non-linearity introduced by the one-directional slew-rate limited stage, the relative broadening is strongly attenuated and the corresponding relative standard deviation is given from Eqs. (9), (4) and (8) by:

$$\frac{N}{S} \approx \sqrt{\frac{Rt(2\tau_P)^2}{2\tau_{HP}}\left(\frac{2\cdot 0.04}{G_d \cdot V_P}\right)^2} \tag{10}$$

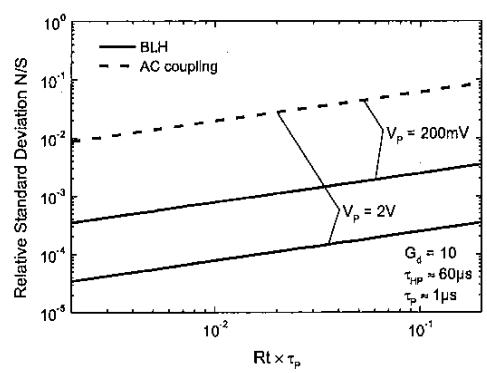

Figure 10: Relative standard deviation vs Rt×τ_P product for different values of output peaking voltage V_P (Eqs. (9) and (10)).

In Fig. 10 the dependence of the relative standard deviation on the product $Rt \times \tau_P$ for different values of V_P is shown, compared to the case of an ac-coupling with same time constant of the approximated high-pass filter. A resolution higher than 12 bit can be observed for $\tau_P \times Rt < 0.1$ and V_P=2V.

Finally, it is worth noting that, due to their non-symmetrical response, both the non-linear dynamic buffer and the low-pass filter shown in the simplified schematic of Fig. 2 could be subject, in case of large and fast signal swings of sign opposite with respect to the main pulses, to undesired charging effects of their high-impedance output nodes.

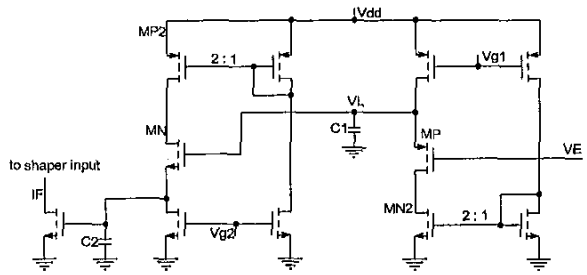

Figure 10: Detailed schematic of the baseline holder (BLH).

In Fig. 10 is shown a more complete configuration which provides a partial protection against undesired charging effects. The mirror output MOSFETs MN2 and MP2, which under normal conditions operate in the linear region, limit the MP and MN drain currents to twice their bias currents in case of large swings of sign opposite with respect to the main pulses.

III. CONCLUSIONS

The baseline holder (BLH), a circuit solution implemented in readout ASICs suitably developed for CZT detectors, was presented. The BLH provides setting and stabilization of the output baseline both at low frequency and at high rate operations. With an output peaking voltage ≈ 2V (≈ 10fC), a peaking time ≈ 400ns and an average rate ≈ 500kHz, the BLH limits the output baseline shift to less than 8mV. The baseline fluctuation due to the random arrival of pulses has negligible impact on S/N performances.

IV. ACKNOWLEDGEMENTS

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