A CMOS Fully Compensated Continuous Reset System[1]

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Abstract

As a result of a cooperation between Brookhaven National Laboratory and eV Products a generation of high performance readout ASICs was developed. One of the novel circuit solutions implemented in the ASICs is a fully compensated continuous reset system capable of handling detector leakage currents up to several tens of nA with high linearity and with noise contribution always lower than the shot noise contribution of the detector. The reset is based on the use of a MOSFET operating above threshold and in saturation. The full compensation is obtained by using a suitable replica of the reset MOSFET. The experimental results are reported. Evaluation and measurement of the noise contribution and of the dependence of the gain on the leakage current are also discussed.

I. INTRODUCTION

The inherent advantages and rapid improvement of $Cd_xZn_{1-x}Te$ (CZT) detectors led to an increase in the number of their applications [1-4]. Several motivations suggest that most of these applications can benefit from the use of ASIC readouts in place of discrete solutions [5].

As a result of a cooperation between Brookhaven National Laboratory and eV Products a generation of novel high performance readout ASICs was developed [5]. The ASICs, realized in CMOS 0.5μm technology, are available in several versions, single or multi-channel and with unipolar or bipolar shaper, in view of their use in research, spectroscopy, medical and industrial applications.

In order to minimize size and parasitic effects, the ASIC are designed to operate dc-coupled to the CZT detectors. A novel circuit solution is implemented to provide a fully compensated continuous reset for the charge preamplifier and, in the mean time, the capability to handle detector leakage currents up to several tens of nA with high linearity and minimum noise contribution. The first experimental results on the novel reset system are reported here. A detailed description, a theoretical analysis, the design criteria and the simulation results were discussed in [6].

II. DESCRIPTION OF THE SYSTEM AND RELATED EXPERIMENTAL RESULTS

The schematic of the compensated continuous reset system is shown in Fig. 1. It is based on the use of a p-channel MOSFET M1 in parallel to the charge preamplifier feedback capacitance C_F (100fF in our case) with source connected to the amplifier output and drain connected to the amplifier input. The gate geometry of M1 (nominally $L = 27\mu m$ and $W = 0.9\mu m$ in our case) and its gate bias voltage are chosen [6] to set the device operating point above threshold and in saturation at the minimum expected leakage current (typically ≈ 1nA for CZT detectors). An N times parallel replica of the overall feedback is used to couple the amplifier output to the second stage input, which is assumed to be a virtual ground with input bias voltage ≈ equal to the preamplifier input bias voltage. The second stage, which provides transimpedance gain Z, can be for example the first stage of the shaper amplifier. The drain-to-source parasitic capacitance of M1 (few aF, depending on the layout) and its drain-to-gate/bulk capacitances (few fF, depending on the layout), are neglected.

It is worth noting that, in order to achieve the matching, the N MOSFETs must be exact replicas of M1. Due to narrow width effects [7,8], the use for the compensation of a single MOSFET having width N times the width of M1 would generate mismatch or would require a large value for the width of M1 (see also next Fig. 5 and subsection 2.5 of [6]).

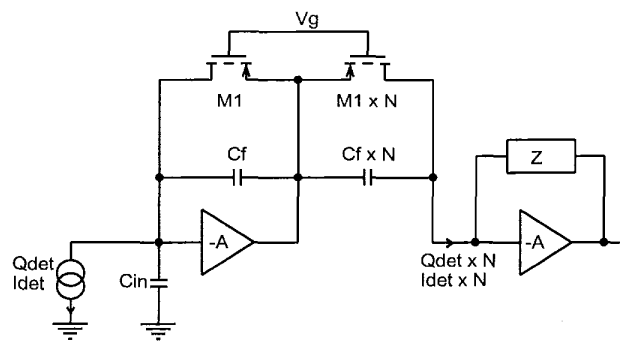

Figure 1: Schematic of the compensated continuous reset system.

A. Static Response

The quadratic relationship between the gate-to-source voltage of the MOSFET and its dc drain current (which equals the detector leakage current I_{DET}) prevents the saturation of the preamplifier output over a wide range of I_{DET}. In Fig. 2 the measured and simulated preamplifier dc output voltage vs I_{DET} are compared. In this measurement I_{DET} was limited to 100pA - 10nA. It can be observed that a change in I_{DET} of several orders of magnitude corresponds to a change in preamplifier dc output of a few hundreds of mV.

It can be easily verified [6] that the dc current injected in the second stage is proportional, with a factor N, to the detector leakage current I_{DET}. For large values of N the real part of the impedance Z can be suitably reduced with negligible increase in the equivalent input parallel noise of the system [6], thus preventing the second stage saturation.

[1] Work supported by the eV Products, Division of II-VI Inc., USA and by the US Department of Energy, Contract No. DE-AC02-98CH10886 and CRADA BNL-C-97-05.

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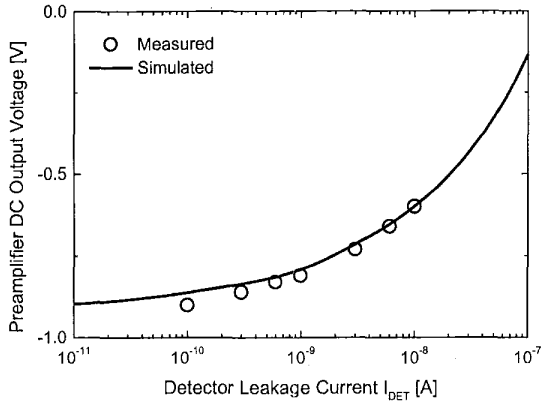

Figure 2: Measured preamplifier dc output vs I_{DET}.

B. Dynamic Response

As response to a negative charge Q_{DET} released by the detector, the gate-to-source voltage of M1 increases. The consequent increase in M1 drain current provides the discharge of the preamplifier input node, thus realizing a continuous reset. Due to the non-linear relationship between the gate-to-source voltage of M1 and its signal drain current (i.e. the reset current), the time required to the discharge decreases as Q_{DET} increases and a non-negligible non-linearity in the preamplifier response is introduced. In Fig. 3 the measured preamplifier responses to charges Q_{DET} = 1fC and Q_{DET} = 10fC, normalized to their maximum amplitude, are compared. The reduction in time required to discharge the larger value of Q_{DET} can be observed [6].

The charge injected in the second stage is proportional, with a factor N, to the charge Q_{DET} released by the detector [6]. Both M1 and its N-times replica share the same gate-to-source voltage. As a consequence the current generated by the N-times replica of M1 discharges the N-times replica of C_F with a current which is N times the reset current, thus providing full compensation in the current injected in the second stage. The compensation includes MOSFET non-linearity and finite transit time [8,9].

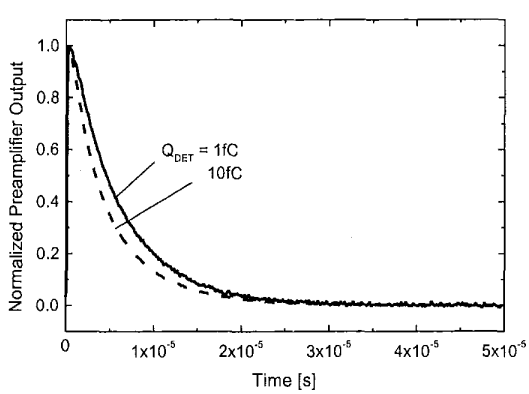

Figure 3: Measured preamplifier response to different values of Q_{DET}.

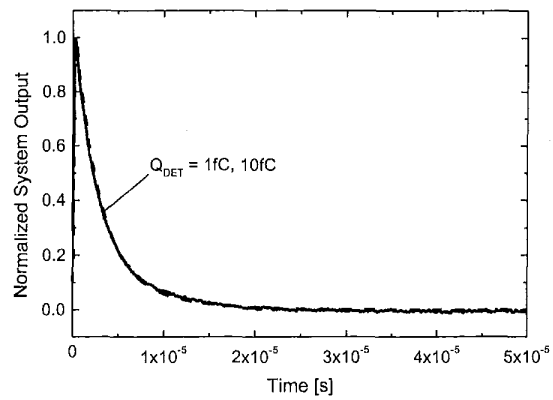

Figure 4: Measured system response to different values of Q_{DET}.

In Fig. 4 the measured response of the compensated system (i.e. the output of the second stage) to charges Q_{DET} = 1fC and Q_{DET} = 10fC, normalized to their maximum amplitude, are compared. The single ≈3μs time constant set by the feedback impedance Z can be observed.

The matching between M1 and its N-times replica plays a determinant role in the accuracy of the compensation. In order to achieve large values of gain N a cascade of two stages was implemented, the first based on p-channel MOSFETs with N1 = 24 and the second based on n-channel MOSFETs with N2 = 6. A total gain N = N1×N2 = 144 was thus achieved. In Fig. 5 the layout of this dual-stage system is shown (area 0.14mm × 0.78mm).

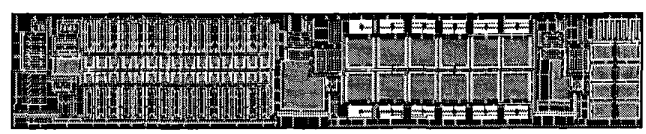

Figure 5: Layout of the dual-stage compensated reset system.

Fig. 6 shows the system response to Q_{DET} = 2fC for different values of detector leakage current I_{DET}. The result was measured for a dual-stage compensated reset system as the one shown in Fig. 5 (the baseline was subtracted).

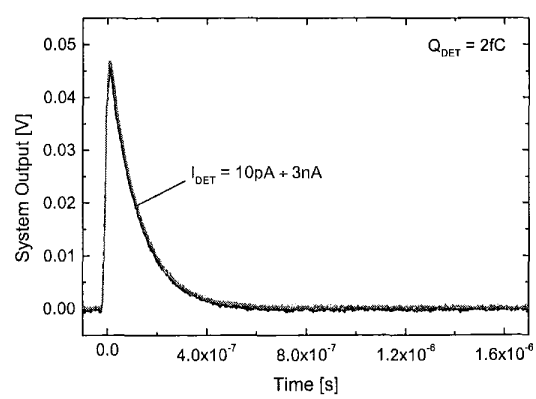

Figure 6: Measured system response for different values of I_{DET}.

The full recovery of the non-linearity was verified experimentally by measurements on the overall ASIC readout channel. An channel integral linearity error < 0.3% was measured for a gain ≈ 200mV/fC, a peaking time ≈ 1μs and an injected charge up to ≈ 12fC. From simulations it was observed that most of the integral linearity error was due to the ASIC channel output stage [5].

The dependence of the gain of the compensated reset system on the detector leakage current I_{DET} requires a more detailed analysis. A compensated continuous reset system can in general be schematized as shown in Fig. 7.

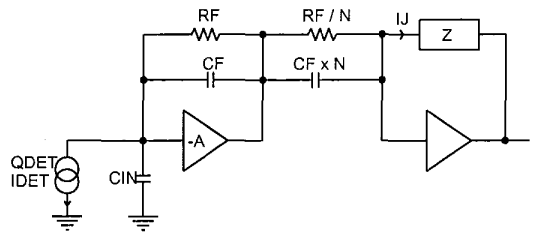

Figure 7: Generalized schematic of a compensated continuous reset system.

If the gain A of the amplifier is characterized by an infinite bandwidth, the current gain of this system equals the ratio N between the feedback impedance and the coupling impedance. In real cases A ≈ 2πGBWP/s, where GBWP is the gain-bandwidth product of the amplifier. The current gain turns out to depend on R_F according to:

$$\frac{I_J}{Q_{DET}} \approx N \frac{1+s\tau_F}{s^2\tau_F\tau_O + s\tau_F + 1} \qquad (1)$$

where $\tau_F = C_F R_F$, $\tau_O = C_{IN}/(2\pi GBWP\ C_F)$, and the assumptions GBWP >> $1/(2\pi\tau_F)$ and $C_{IN} >> C_F$ were made. The dependence of the gain on R_F is due to the fact that, for finite GBWP, the zero and one pole don't cancel each other any more.

If $2\pi GBWP \times \tau_F > 4C_{IN}/C_F$ (i.e. if the loop gain is > 4 at the frequency $1/(2\pi\tau_F)$, which is in most cases verified) the poles are real and Eq.(1) can be simplified as follows:

$$\frac{I_J}{Q_{DET}} \approx N \frac{1+s\tau_F}{(1+s\tau_L)(1+s\tau_H)} \qquad (2)$$

where $\tau_L = \tau_F/(1+\alpha)$ and $\tau_H = \tau_O/(1-\alpha)$ with $\alpha = \tau_O/\tau_F$. The corresponding response to the delta pulse $Q_{DET}\delta(t)$ is given by:

$$I_J \approx \frac{Q_{DET}N}{\tau_L}\left[\left(1-\frac{\tau_F}{\tau_L}\right)\exp\left(-\frac{t}{\tau_L}\right)+\frac{\tau_F}{\tau_H}\exp\left(-\frac{t}{\tau_H}\right)\right] \qquad (3)$$

By integrating Eq.(3) to the time constant of the shaper τ_{SH} and by normalizing to $Q_{DET}N$ it follows for the normalized gain G:

$$G \approx 1+\frac{C_{IN}}{C_F}\frac{1}{2\pi GBWP \times R_F C_F}\exp\left(-\frac{\tau_{SH}}{R_F C_F}\right) \qquad (4)$$

In the proposed reset system the value of $R_F \approx 1/g_{m1}$ depends on the value of I_{DET} according to $g_{m1} \approx (k' I_{DET} W_1/L_1)^{1/2}$ [6]. From Eq.s (2) and (4) it can be observed that the gain is expected to increase as I_{DET} increases (R_F decreases, g_{m1} increases) due to the presence of the zero $1/\tau_F$, which occurs before the dominant pole $1/\tau_L$. When the time constant τ_F becomes much smaller than the shaping time constant τ_{SH}. the opposite behavior is expected.

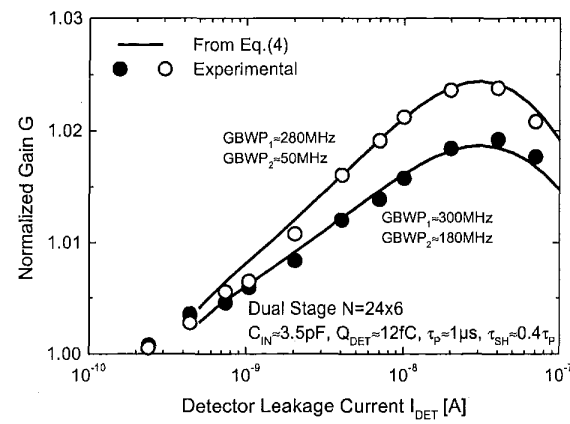

Figure 8: Dependence of the compensated reset system gain on the detector leakage current.

In Fig. 8 the experimental results, compared to the theoretical dependence of Eq.(4) are reported for two cases characterized by different GBWP. In both cases a dual-stage compensated reset system with N = 24×6 was used, which leads to a modification of Eq.(4). A change in gain ≈ 0.23% was measured for a change in I_{DET} from 1nA to 2nA and ≈ 0.97% from 1nA to 10nA. Next versions implement compensation techniques which, at equal dissipated power, are expected to show a slope more than 3 times lower.

In Fig. 9 the pulses measured at the output of the ASIC readout channel for one of the two cases of Fig. 8 are reported (the baseline was subtracted).

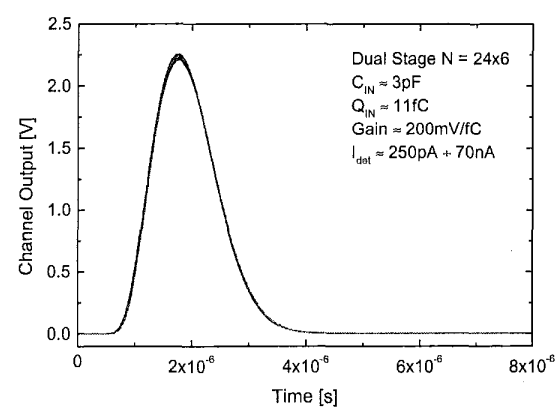

Figure 9: Measured output pulses corresponding to one of the two cases of Figure 8.

From the return to baseline of the pulses shown in Fig. 9 the effectiveness of the compensation over the wide range of leakage currents can be observed. The same figure shows the described dependence of the gain on I_{DET}.

In the implemented reset system the value of $R_F \approx 1/g_{m1}$ depends also on the value of Q_{DET} according to [6]:

$$\delta g_{m1} \approx k' \frac{W_1}{L_1} \frac{2(V_{GS1}-V_{T1})}{\left[2(V_{GS1}-V_{T1})\frac{C_F}{Q_{DET}}+1\right]\exp\left(\frac{t}{C_F}g_{m1}\right)-1} \quad (5)$$

where V_{GS1} is M1 gate-to-source voltage, V_{T1} its threshold voltage, g_{m1} its transconductance at the operating point, L_1 and W_1 respectively its gate length and width and $k' = C_{OX}\mu_P$ (please note sign correction in Eq.s (9) and (4) of [6]). As a consequence it must also be expected that the finite GBWP of A can limit the linearity of the system in an amount which depends on the operating point of M1 (i.e. on I_{DET}). When $Q_{DET}/C_F > |V_{T1}|$ and the operating point of M1 is in the weak inversion region, the increase in integral linearity error can become non-negligible. The analysis of this effect is not straightforward and only the experimental results will be reported. For $Q_{DET}/C_F > 800$mV, an increase ε in the integral linearity error < 0.1% for $I_{DET} \geq 1$nA and < 1% at $I_{DET} \approx 100$pA (M1 operating in weak inversion) were measured.

Three additional design criteria for the compensated reset system are suggested by this analysis: (i) M1 should operate above threshold at the minimum expected value of I_{DET} [6] (in most cases it means that M1 should have long and narrow channel); (ii) C_F should be chosen to satisfy the condition $C_F \geq Q_{DET}/V_{T1}$ at the maximum expected value of Q_{DET} and (iii) the GBWP of A should be maximized. Corresponding criteria apply also to the second stage in case a dual-stage compensated reset system is implemented.

C. Noise

When the reset MOSFET M1 operates below threshold (i.e. below $I_{DET} \approx 1$nA) its noise contribution is shot $\approx 2qI_{det}$. When the reset MOSFET operates above threshold (i.e. above $I_{DET} \approx 1$nA) its noise contribution is thermal $\approx 4kTg_m < 2qI_{DET}$ where g_m is set by I_{DET} [6].

In Fig. 10 the equivalent input parallel noise spectra, measured for different values of a current source I_L with shot noise simulating I_{DET} (which sets M1 operating point below and above threshold) are shown. At low frequency the $1/f$ noise contribution from M1 can be observed in the above threshold cases. The increase in noise observed at high frequency below threshold is related to the limits of the measurement system. All measured noise spectral densities were in agreement with the predictions.

An additional non-stationary noise contribution must also be considered. This contribution, related to the increase in MOSFET drain current during the reset phase, was theoretically discussed in [6].

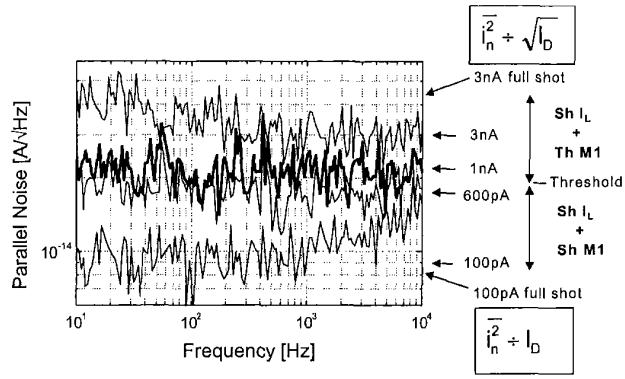

Figure 10: Equivalent input parallel noise spectra for different values of a current source I_L with shot noise simulating detector leakage current I_{DET}.

A simplified expression for the evaluation of this additional contribution can be derived as follows. From Eq.(5) the increase $\delta g_{m1}(t)$ in M1 transconductance during the reset phase can be approximated in a worst case by:

$$\delta g_{m1} \approx k' \frac{W_1}{L_1} \frac{Q_{DET}}{C_F} \exp\left(\frac{t}{C_F} g_{m1}\right) \quad (6)$$

where g_{m1} is M1 transconductance at the operating point, L_1 and W_1 are respectively its gate length and width and $k' = C_{OX}\mu_P$. By using this expression in Eq.(10) of [6] and by assuming in a worst case $C_F/g_{m1} >> \tau_P$, where τ_P is the peaking time of the shaped signal, it follows:

$$\delta ENC^2 \approx \frac{1}{2} 2kT \frac{Q_{DET}}{C_F} k' \tau_P A_3 \quad (7)$$

where A_3 is the parallel white noise coefficient corresponding to the peaking time and the factor 1/2 is an empirical coefficient corrective of the worst case approximation.

From Eq.(7) it follows that, in a first approximation, δENC is independent of g_{m1} (i.e. on I_{DET}). It is worth noting that this contribution can be reduced by increasing the value of C_F without impact on the dynamic range of the system (set by the ratio N), the only major drawback being a more stringent requirement in the driving capability of the amplifier. With $k' \approx 50A/V^2$, $C_F = 100$fF, $A_3 = 0.78$, $W_1/L_1 = 27/0.9$ and $\tau_P = 1\mu s$ it follows:

$$\delta ENC^2 \approx 0.17[\text{Coulomb}] \cdot Q_{DET} \quad (8)$$

In Fig. 11 the experimental results are compared to Eq.(8). The contribution must be added in quadrature to the ENC at low injection ENC_0 [6] ($ENC_0 \approx 100e^-$ at 200mV/fC, $ENC_0 \approx 300e^-$ at 30mV/fC). It is worth noting the minimum impact on the signal-to-noise ratio.

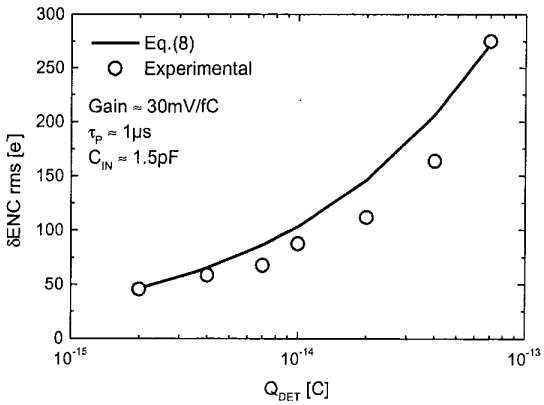

Figure 11: Increase in ENC due to the non-stationary noise contribution of the reset current.

III. CONCLUSIONS

A fully compensated continuous reset system is proposed and tested. The system is implemented in readout ASICs to be dc-coupled to CZT detectors. The experimental results, in full agreement with the predictions, show that the system can self-adapt to leakage currents up to several tens of nA with noise contribution always lower than the shot noise contribution of the detector. Agreement was also found between evaluation and measurement on the dependence of the gain on the leakage current and on the dependence of the noise contribution related to the reset current on the injected charge.

IV. ACKNOWLEDGEMENTS

The authors wish to thank Veljko Radeka (BNL), Emilio Gatti (Milan Polytechnic) and Pavel Rehak (BNL) for useful suggestions and comments, Anand Kandasamy (BNL) for assistance in the layout phase and John Triolo (BNL) for the technical assistance.

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