A 0.9V 960MHz CMOS Radio Front End Employing a Doubly Balanced Transconductance Mixer

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Abstract- A 960MHz CMOS low voltage radio front end architecture is presented. The circuit employs a doubly balanced transconductance mixer. The radio front end achieves a power gain of 6dB, an input referred third order intercept (IIP3) of -3dBm and single sideband noise figure of 11dB at 0.9V supply voltage and 20mW power dissipation. The circuit is realised in 0.6μm CMOS technology; it occupies an area of 1mm× 0.7mm.

Introduction

CMOS RF circuits have been investigated extensively. Thus far research has focused on FET ring mixers [1] and Gilbert Cell variants [2]. A classical mixer topology is the transconductance mixer which has been realised in GaAs MESFET [3] and HBT technology. An integrated version of this topology has proved difficult due to the requirement of combiners which provide the appropriate signal summation. This paper addresses this issue and presents a circuit topology suitable for driving a fully integrated doubly balanced transconductance mixer. The summation networks provide a local oscillator (LO) buffer and RF LNA. Many mobile applications would benefit from single cell battery operation (0.9V) due to weight considerations. This has proved elusive due to the fact that a Gilbert Cell mixer requires a stack of two transistors connected in a cascode circuit in order to produce the desired mixing action. The transconductance mixer architecture employs a parallel structure to overcome this limitation.

Principle Of Operation

Typically in transconductance mixers both local oscillator and signal frequencies are applied to the same gate [3]: Injecting LO and RF into different ports has been investigated [3] but the optimum port allocation was found to be LO and RF signals summed at the gate. The MOSFET device can be described as a square law device. The drain current is a function of the sum of the LO and RF signals squared. The LO and RF signals can be considered sinusoids. The expansion of the square of the sum terms yields a product term of the familiar form given in equation 1. This gives rise to the desired mixing sidebands:

$$V_{IF} = K \cdot V_{LO} \cdot V_{RF} \cdot \left(\cos\left(w_{RF} + w_{LO}\right) \cdot t + \cos\left(w_{RF} - w_{LO}\right)t\right) \quad (1)$$

The circuit diagram of the complete front end is shown in figure 1. The transconductance mixer comprises M1, M2, M3 & M4. Transistors M1, M2, M3 & M4 are driven by the sum of the LO and RF signals. These devices are biased by the P-channel transistors M9, M10, M11 & M12. The capacitors C1,C2,C3 & C4 act as dc blocking capacitors. The transistors have to be driven in an exact order if LO and RF signals are to cancel at the IF output. The two devices with their drains tied to the IF port must be driven by the LO and its antiphase to ensure LO cancellation. A similar argument applies to the other two devices. Mixing occurs by commutation, hence the RF signal output must be reversed on each phase of the LO at the IF and IFN ports. This dictates The RF output signal of the mixer is connected to IF when the LO signal is high and IFN when the LON signal is high. The summation of LO and RF signals is achieved by transistors M5A,M5B,M6A,M6B, M7A,M7B & M8A,M8B. The RF signal and its antiphase are applied to the gates of M5A,M5B,M6A,M6B respectively. The LO signal is applied to the gates of M7A,M7B & M8A,M8B. The summation of LO and RF occurs by connecting the drains of M6B and M8B. Likewise the summation of LON and RFN occurs by connecting the drains of M7A & M5B. These drains are connected to V_{DD} via a package parasitic inductor and an external 5nH inductor. This node is tied to the lower plate of C2, the dc blocking capacitor. Separate RF and LO tuning is achieved by connecting a capacitor between the LO+RFN and LON+RFN V_{DD} lines. The two signals have a common mode RF signal and a differential mode LO signal. The LO is tuned by connecting a resonant capacitor across the two lines; this forms a virtual ground at the LO frequency at this point. RF tuning is accomplished by connecting a capacitor to ground on both lines; the transmission line trace connecting the package pins to V_{DD} is thus used to realise additional inductance at RF. The LO signal is at least an order of magnitude higher than the RF signal: It is wise to run these two lines close together so that the larger LO signal radiation on the board is canceled due to differential signal routing.

Measured Results

To evaluate the performance of the low voltage front end architecture the third order intercept point, conversion gain and single sideband noise figure were measured as a function of supply voltage. The RF port dc bias was 0.6V, the LO port bias was 0.6V and the mixer port was biased at 0.8V. The input RF frequency was 960MHz and the LO frequency was 900MHz. The RF

input return loss was -20dB and the LO return loss was -7dB. The LO power was constant at -8dBm.

- **Conversion Gain**

The measured conversion gain as a function of supply voltage is given in figure 3. 6dB of power gain was achieved at 0.9V. The dependence on conversion gain to power supply is due to the channel modulation effect: The supply current increases as a function of power supply voltage. This can be remedied to a first order by employing a current source in the tails of the LO, RF and mixer stages. This would also allow single ended operation.

- **Third Order Intercept Point**

The measured input intercept point was -2.75dBm at 0.9V. The plot of input referred intercept point versus supply voltage is given in figure 4. As expected the input intercept rises as gain reduces (figure 3).

- **Single Sideband Noise figure**

The plot of measured noise figure versus supply voltage is given in figure 3. The noise figure is 11dB at 0.9V. This could be improved by employing a higher gain LNA as is demonstrated by the general trend of figure 5 with respect to figure 3.

- **Port-Port Isolation**

The measured port-port isolation at the significant ports are given in table 1. The circuits performance depends heavily on device matching. Common centroid geometry and careful PCB board layout kept these isolation values to within that achievable with a standard CMOS Gilbert cell [2].

Conclusions

A low voltage CMOS front end architecture has been demonstrated at 0.9V operation. The circuit achieves 6dB conversion gain, -3dBm IIP3, 11dB SSB noise figure at 0.9V. The circuit was fabricated in a standard 0.6μm CMOS digital technology without any process enhancements.

References

[1]: "Low-Power Radio Frequency IC's For Portable Communications", Asad A. Abidi, Proceedings of the IEEE, VOL. 83, No.4, April 1995.

[2]: "A Low Voltage Evaluation of A Gilbert Cell Mixer", P J Sullivan, B A Xavier, W Ku, 1996 European Solid State Circuits Conference, Nau Chatel Switzerland pp101-105.

[3]: "An Experimental Evaluation of X-Band GaAs MESFET Mixers Using Single & Dual Gate Devices" , S Cripps, 1977 MTT-S Int. Microwave Symposium Digest pp.285-287.

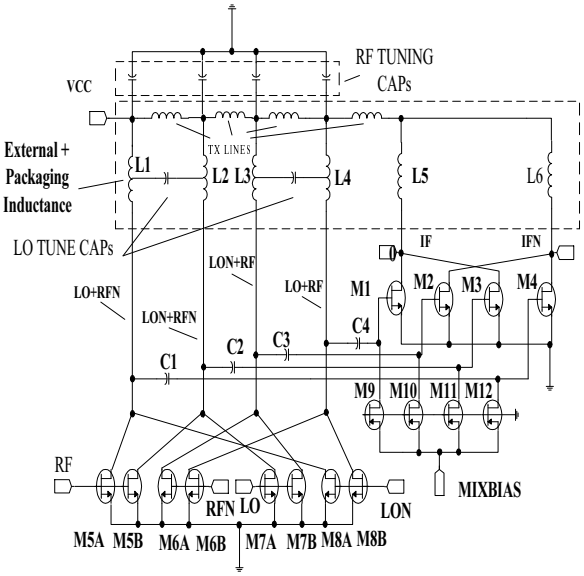

Figure 1: Schematic Of 0.9V CMOS Radio Front End

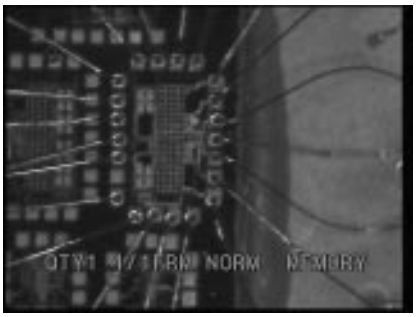

Figure 2: Chip Photomicrograph of 0.9V CMOS Radio Front End

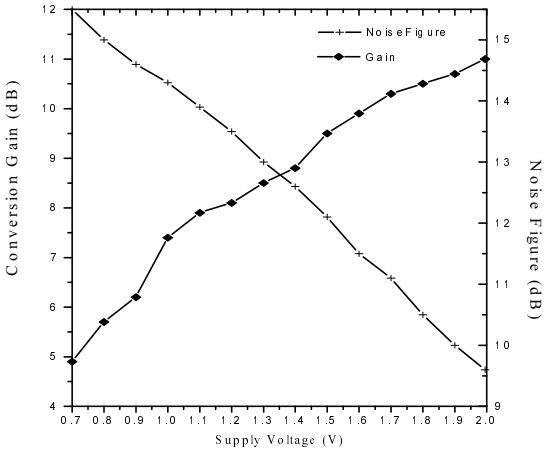

Figure 3: Measured Conversion Gain & Associated Noise Figure of 0.9V CMOS Radio Front End

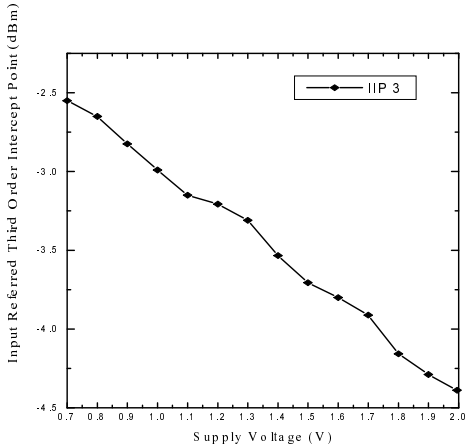

Figure 4: Measured IIP3 of 0.9V CMOS Radio Front End

LO-IF	RF-IF	LO-RF	RF-LO
-24dB	-22dB	-29dB	-20dB

Table 1: Port-Port Isolation