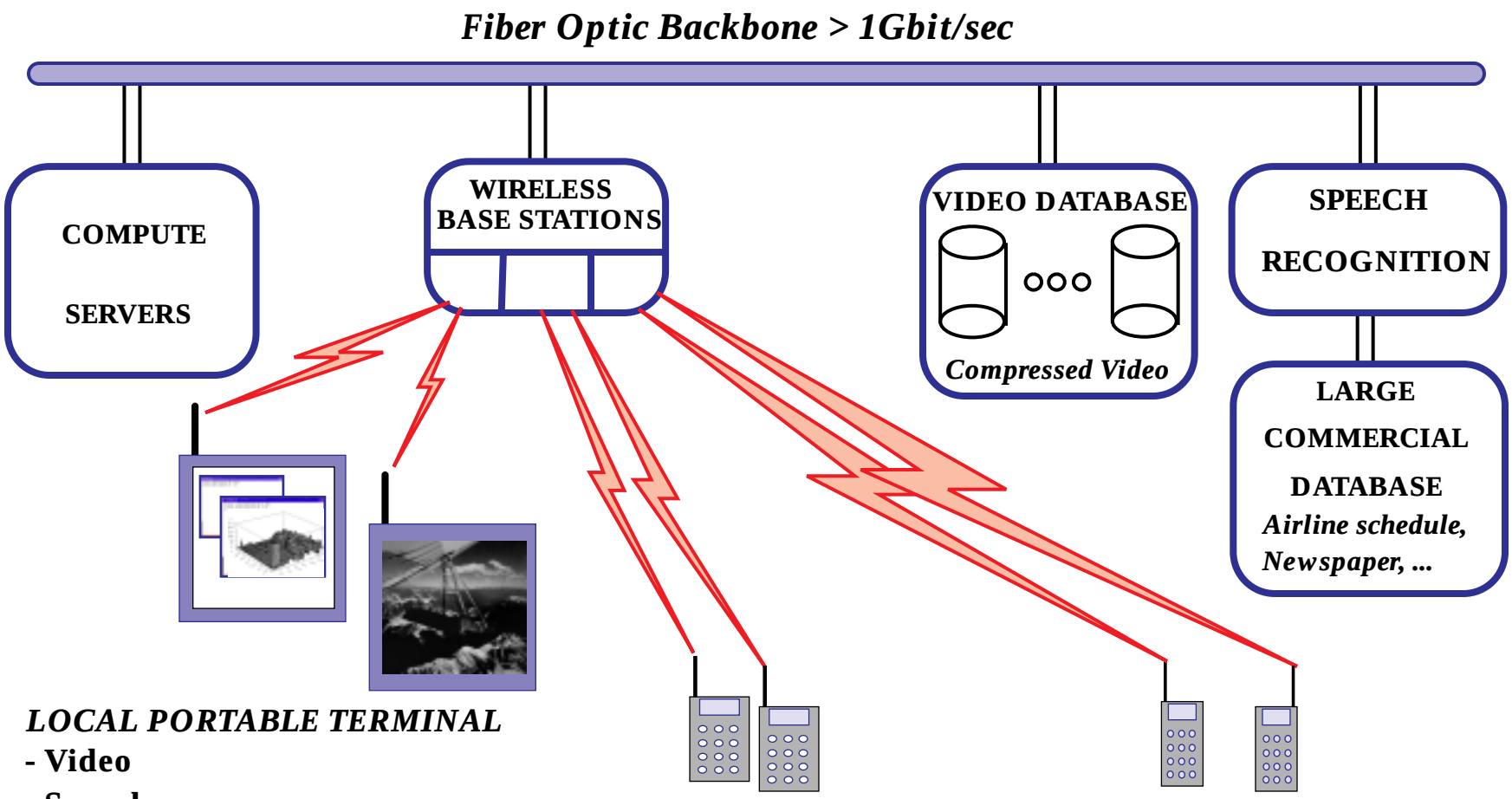
Architectures and Technologies for CMOS RF Transceivers

- RF Transceivers in PCS Systems
- Examples of Current Practice
- Keys to Progress in CMOS Transceivers
- Examples and Current Status

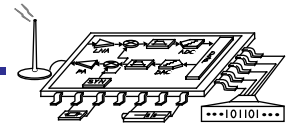
Evolution of PCS in the Communications Infrastructure



LOCAL PORTABLE TERMINAL
- **Video**
- **Speech**
- **X-terminal**

MID-RANGE PERSONAL COMMUNICATORS
- **Cordless PBXs**
- **PCS Systems**

WIDE-AREA PERSONAL COMMUNICATORS
- **Enhanced Cellphones**
- **Personal numbers**
- **World wide coverage**

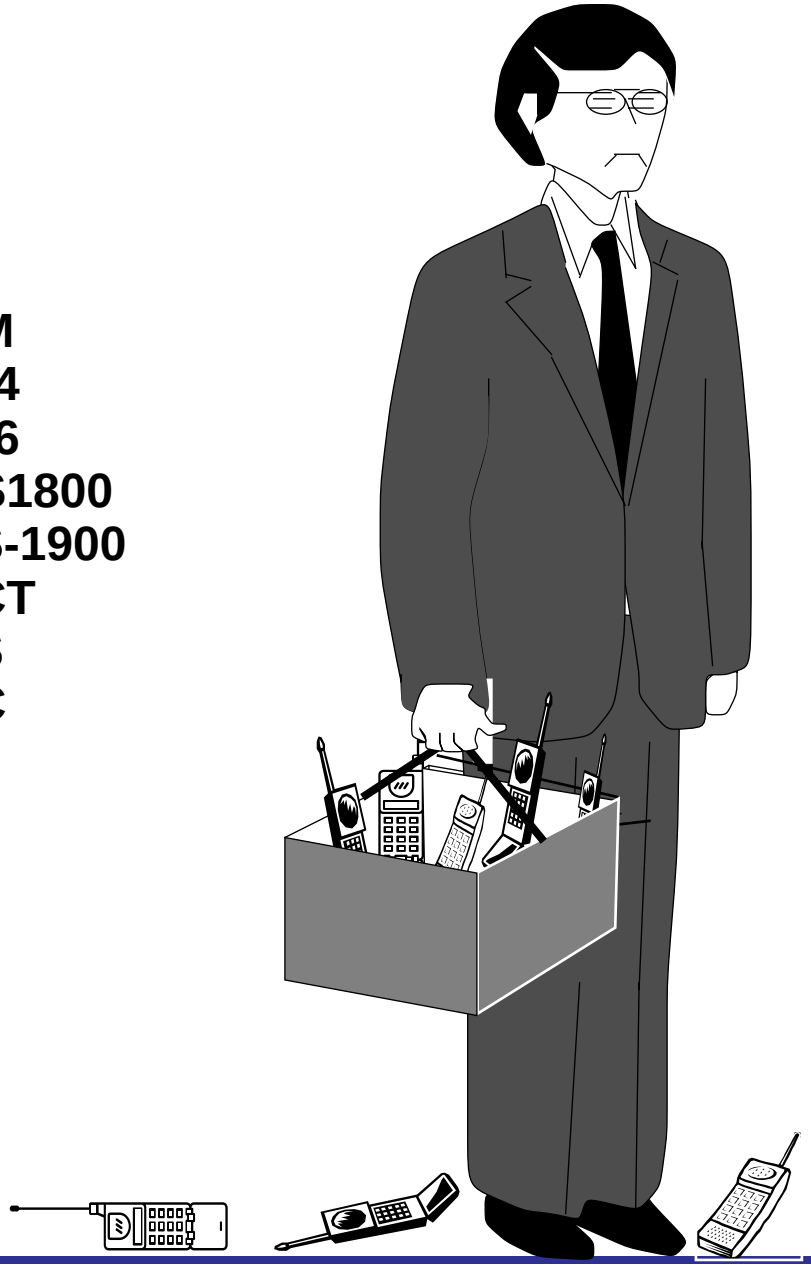


Summary of Cellular Phone, Cordless Phone, LAN PCS Standards

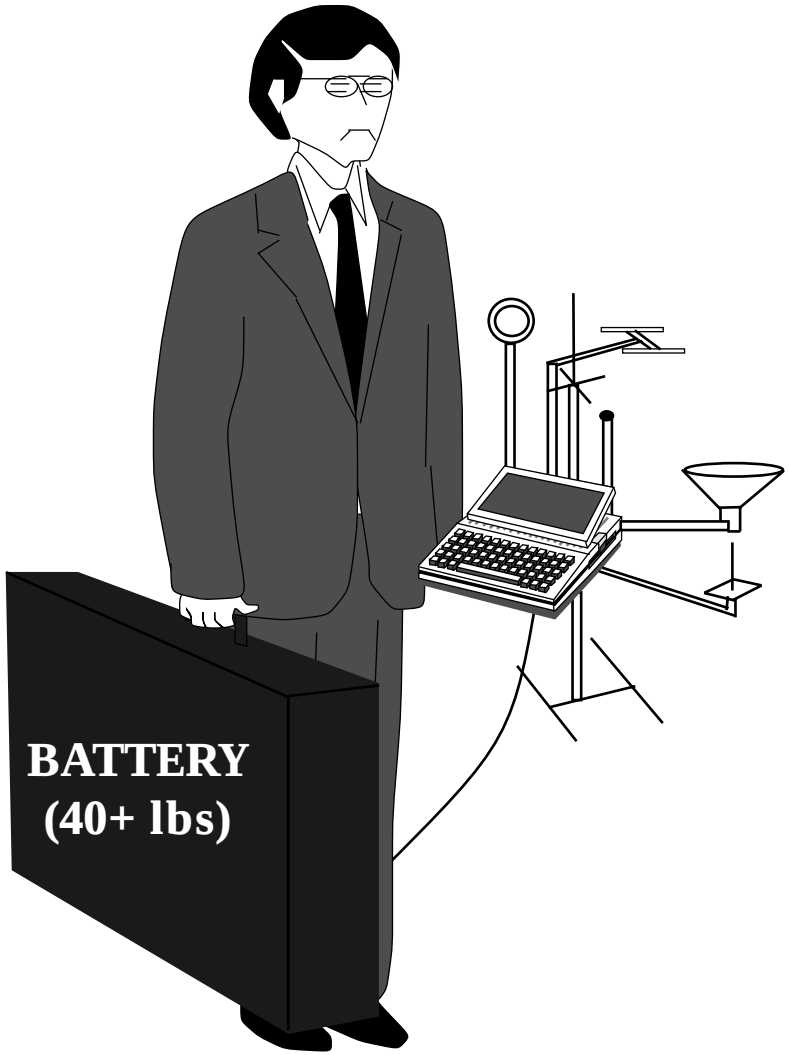
Parameter	AMPS	IS54	GSM	JCP	DECT	CT2	PHP	802.11FH
Origin	EIA/TIA	EIA/TIA	ETSI		ETSI	UK	Japan	IEEE
Access	FDD	FDM/FDD/TDM	FDM/ FDD/ TDM		FDM/TDM/ TDD	FDM/TDD	TDM/TDD	FH/FDM
Modulation	FM	pi/4QPSK	GMSK, diff	pi/4DQPSK	GFSK	GFSK	pi/4-DQPSK	(G)FSK
Baseband filter		Root raised cosine	Root raised cos. beta=0.3	Root raised cosine	Gaussian BT=0.5	Gaussian BT=0.5	Root Nyquist alpha=0.5	500kHz LP
Data rate per RF channel	NA	48kb/sec (2bits/sym-bol)	270.8kb/sec	42kb/sec (2bits/sym-bol)	1.152Mb/sec	72kb/sec	384kb/sec	1Mb/sec/2Mb/sec
FM Deviation	3khz	NA	NA	NA	288kHz	14.4-25.2kHz	NA	~150kHz
RF Channel fre-quencies	824.04-848.97(X) 869.04-893.97(R)	824.04-848.97(X) 869.04-893.97(R)	890-915(X) 935-960(R)		0:1897.344MHz, 9:1881.792MHz	1:864.15MHz 40:868.05MHz	1895-1911MHz	2.4-2.5GHz
No of RF Channels	833	833	124	1600	10	40	52	75
Channel Spacing	30kHz	30kHz	200kHz		1.728MHz	10kHz	300kHz	1MHz
Synthesizer switch-ing speed	slow	slow			30us(BS) 450us(HS)	1ms(ch-ch) 2ms	30us(BS) 1.5ms(HS)	several us
Frequency Accu-racy	2.5ppm	200Hz			50kHz	10kHz	3ppm	
Speech channels per RF Channel (full/half rt)	1	3	8/16	3/6	12/24	1/1	4/8	NA
Speech coding	Analog com-panded	VCELP 8kb/s	RELP-LTP 13kb/sec	VCELP 8kb/sec	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM	NA
Frame Length	NA	40ms			10ms(12Tx+12Rx)	2ms (1Tx+1Rx)	5ms (4Tx+4Rx)	
Peak Power:	3W(6max)	3W(6max)	3W(20max		250mW	10mW	100mW	1 watt?
Power Control rqmt	7 steps	7 steps			no	no		no

1998 Road Warrior Kit

GSM
IS-54
IS-96
DCS1800
PCS-1900
DECT
PHS
PDC
etc



Adaptive, Multistandard RF Modems



Key Goals for ICs for RF Transceiver Implementations

- Minimum Power Dissipation
- Minimum Cost, Form Factor
- Extendable to Higher Data Rates
- Adaptable to Multiple RF Transmission Standards

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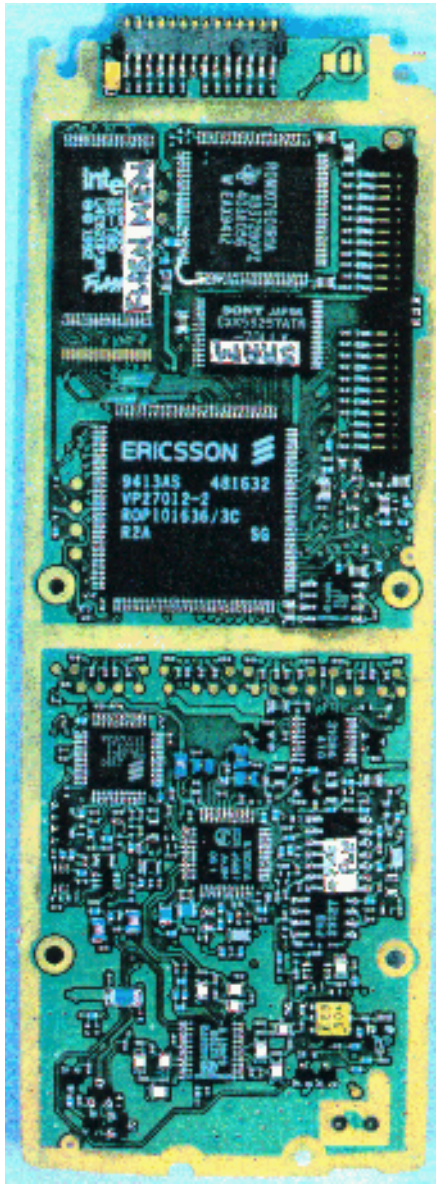
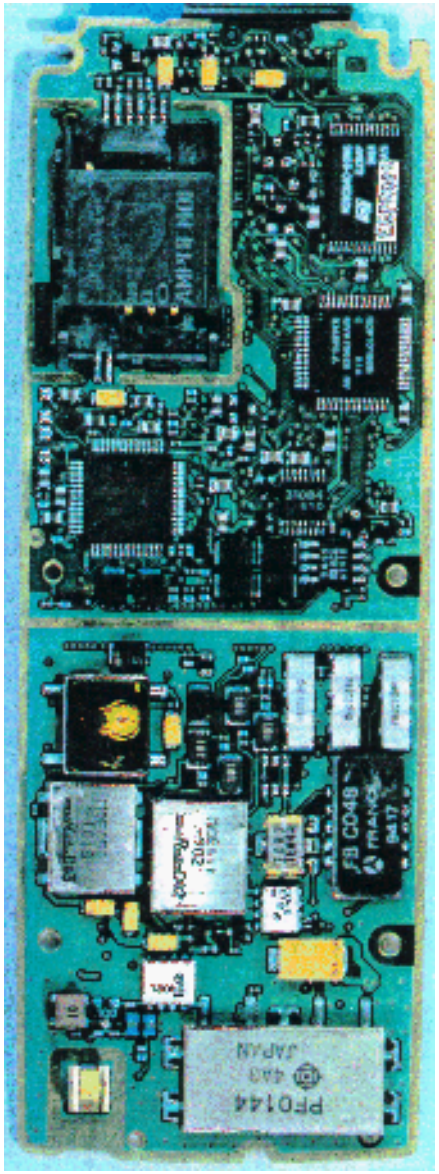
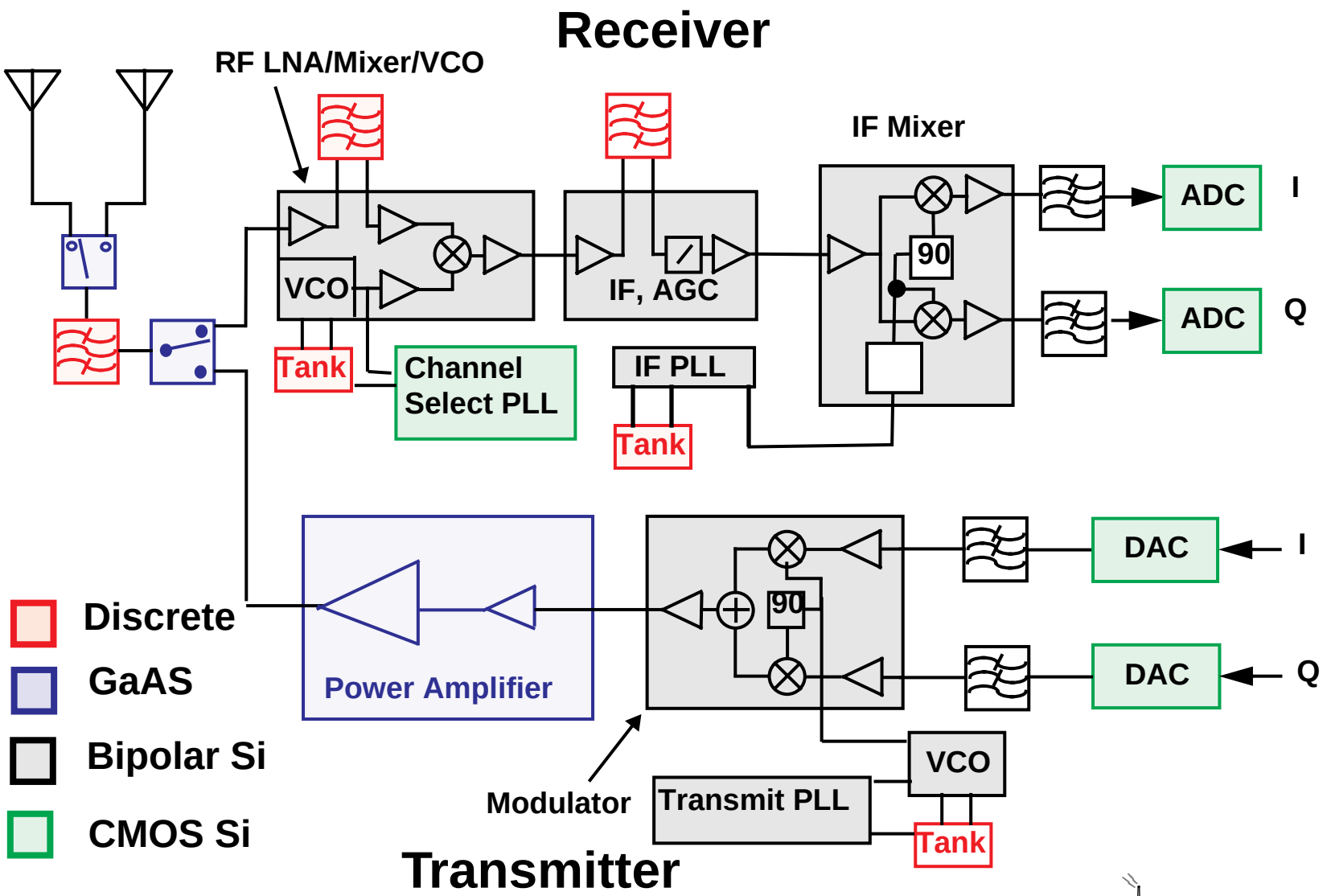
Typical Current RF Transceiver Implementation



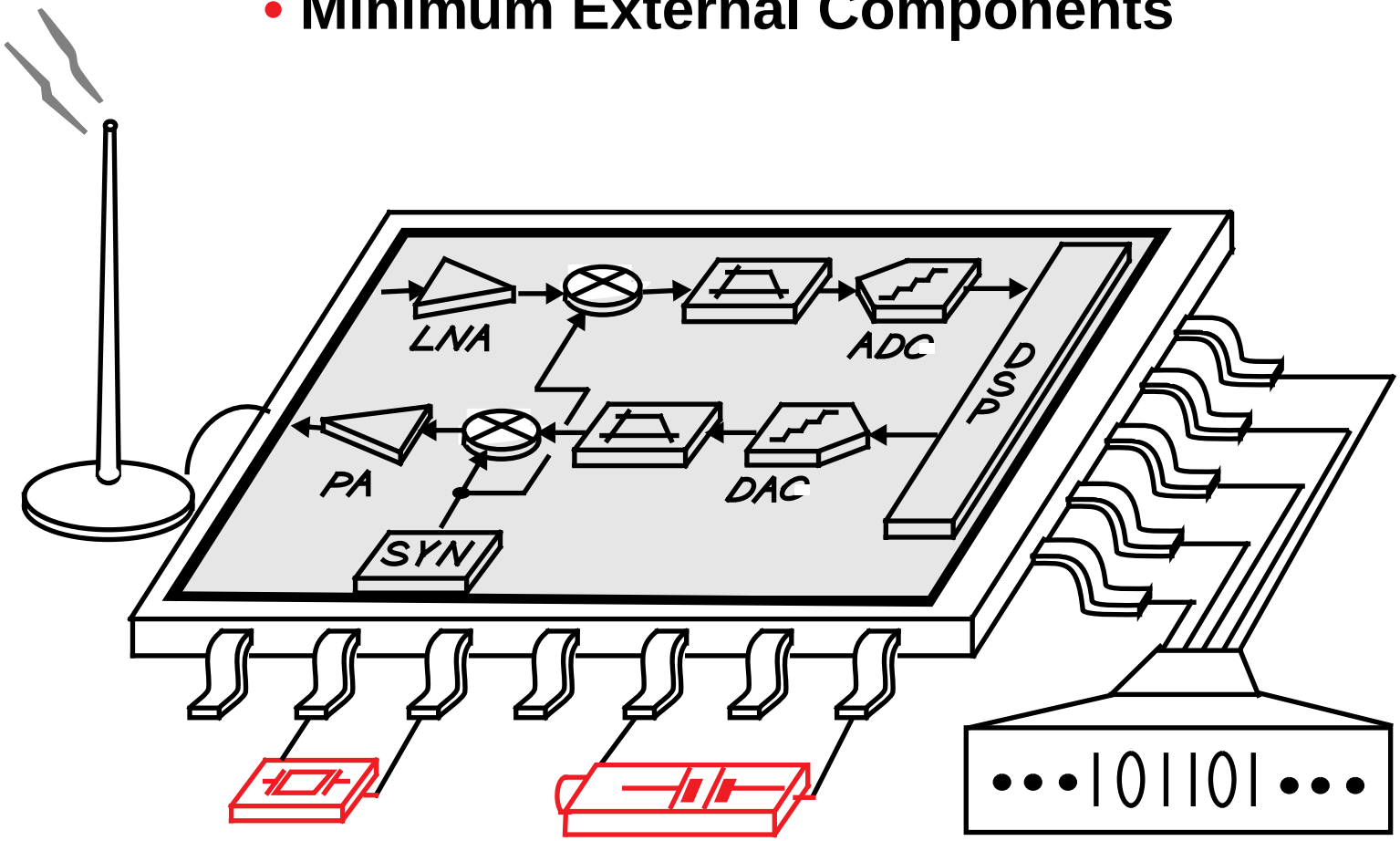


Block Diagram, Typical Multi-Technology RF Transceiver

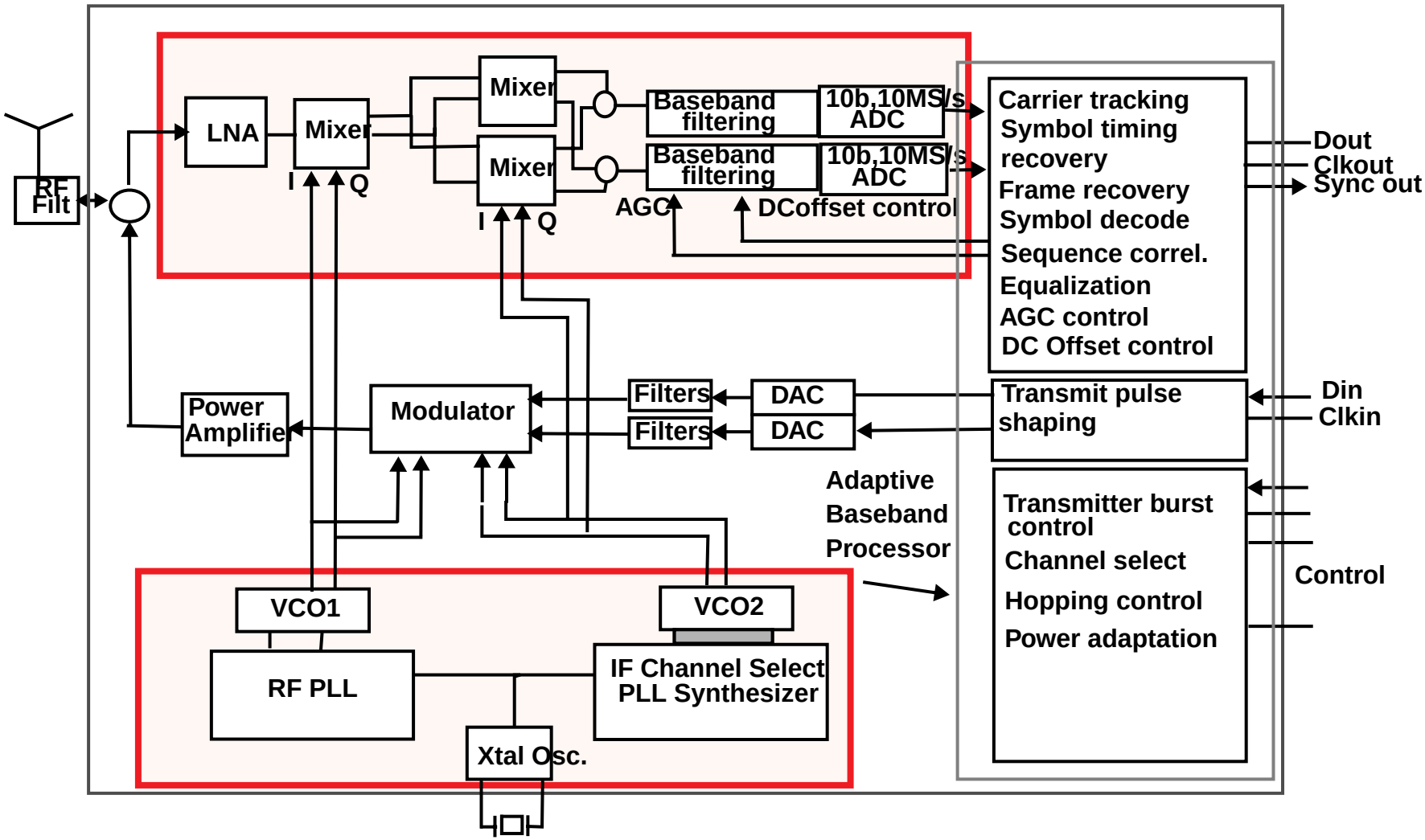


Ultimate Objective:

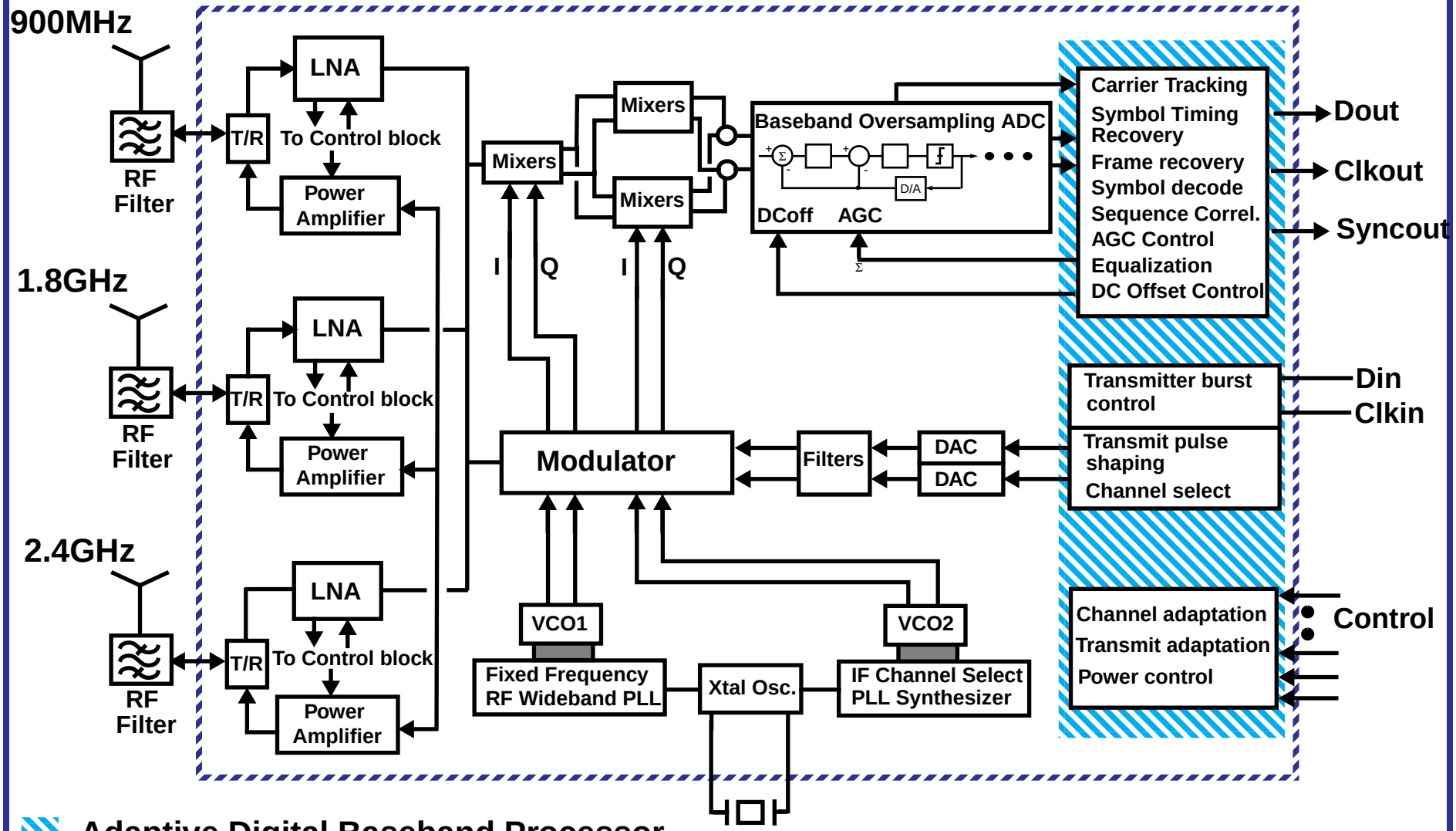
- **Single-Chip, Scaled CMOS or BiCMOS**
- **Minimum External Components**



Example Implementation,High-Integration RF Transceiver



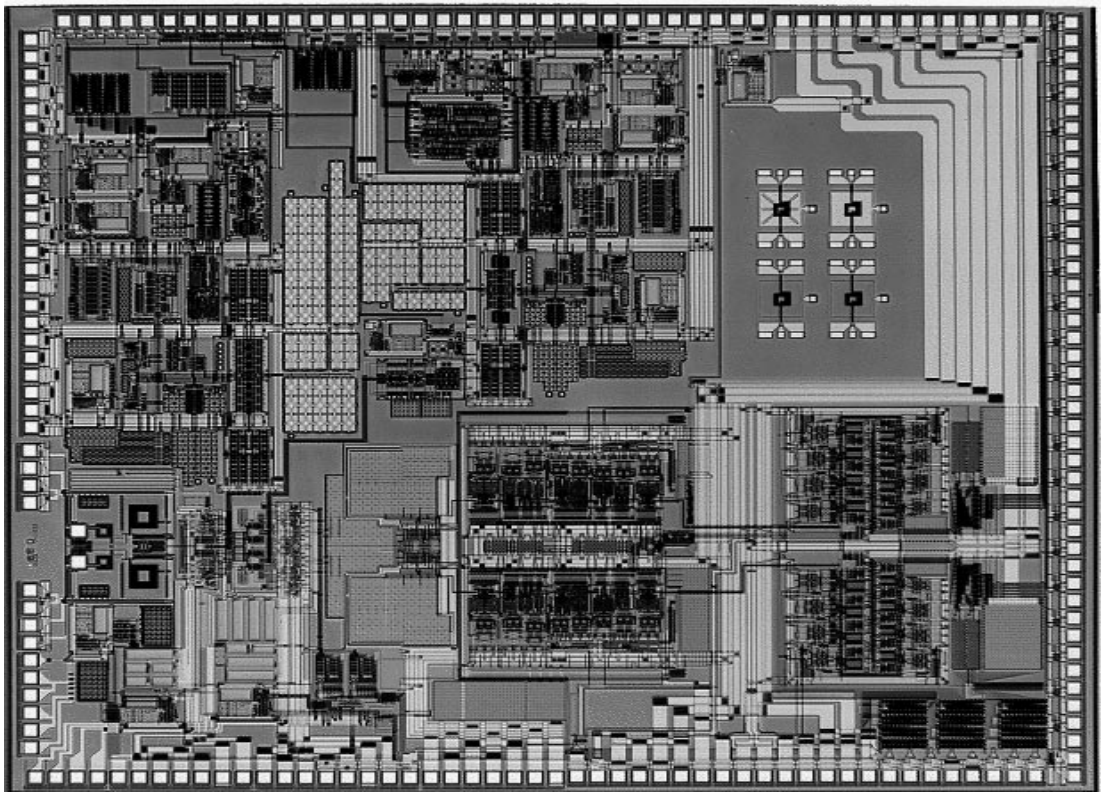
Example Implementation, Multi-Standard Xvr



Adaptive Digital Baseband Processor

Fully Integrated Transceiver Chip

Example Test Device- UCB DECT Rcvr



Example Test Device- UCLA 900Mhz Xvr

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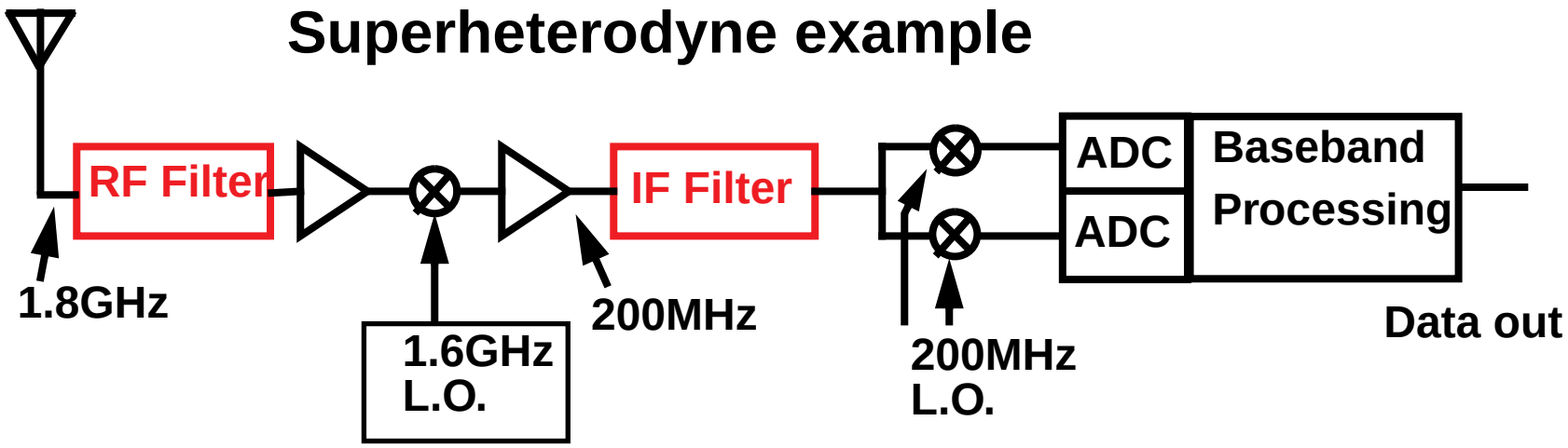
Critical Parameters in High-integration Transceiver Performance

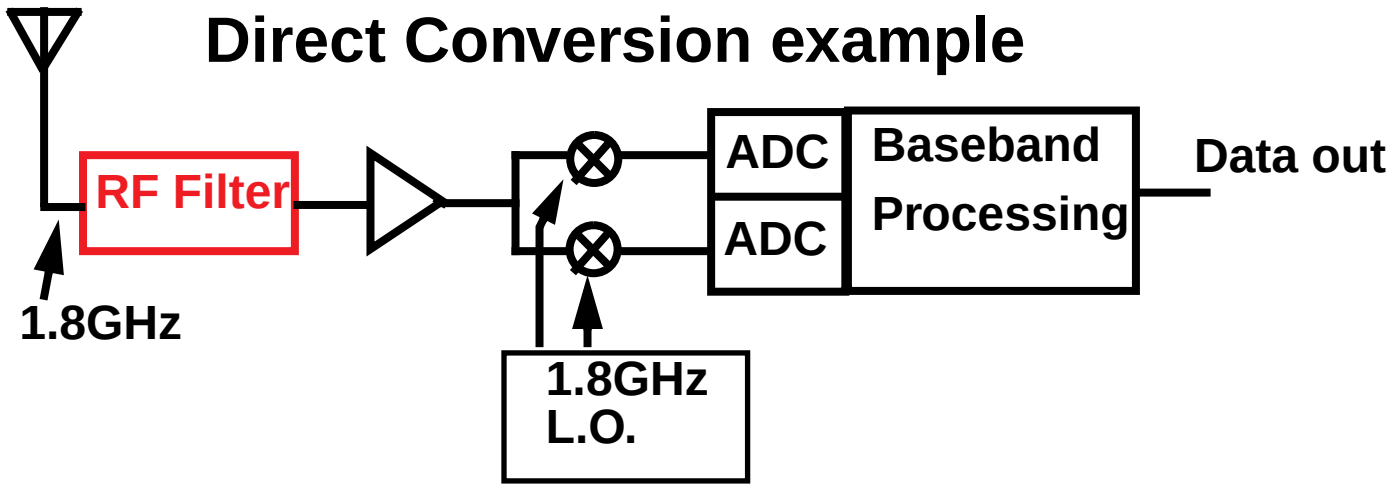
- Channel bandwidth and spacing, data rate
- Receiver sensitivity and noise figure
- Blocking, desensitization in the presence of close-in strong interferers
- Image reject- desens from far blockers
- Intermod performance- desensitization from 2 strong interferers
- Transmit power
- Transmit spectral purity
- Power consumption in Rcv, Xmit, Standby
- Total square mils of silicon

Keys to Progress in Low-Power Adaptive RF Transceiver Design

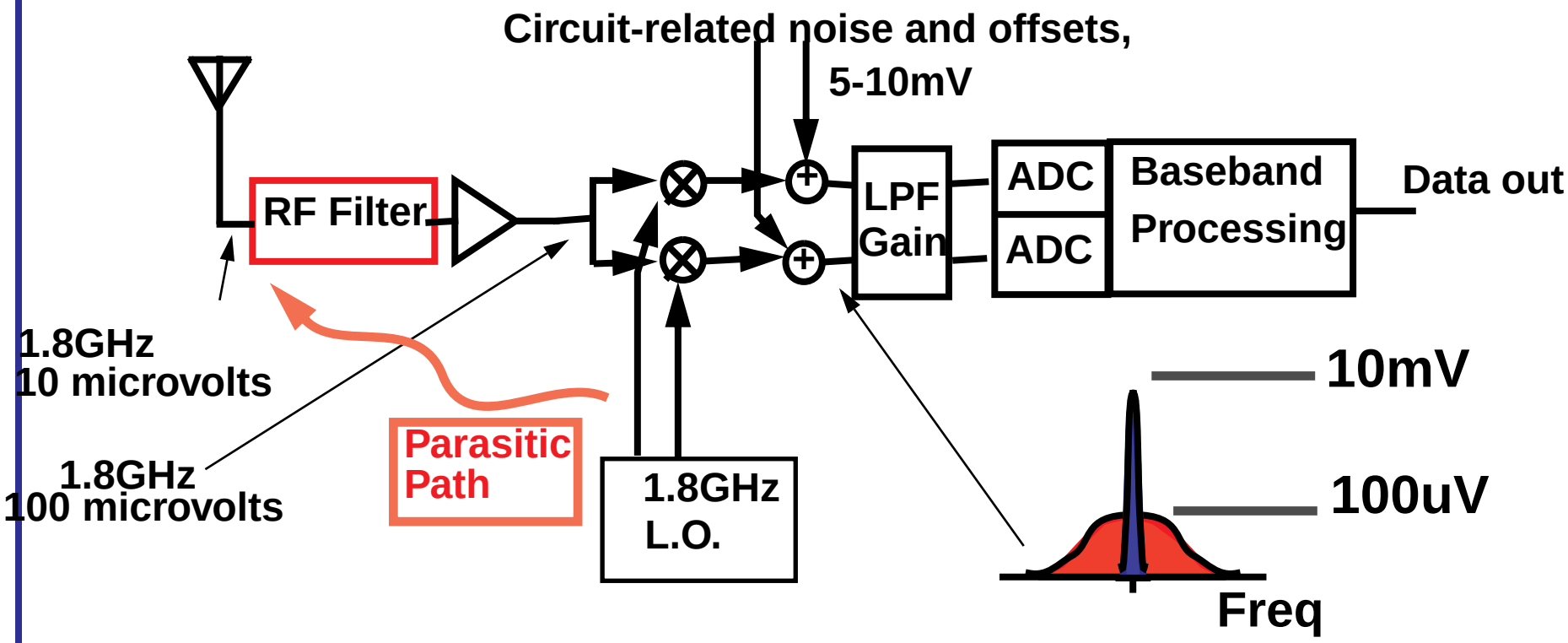
- New Receiver Architectures
- Low-Power CMOS/BiCMOS RF Circuit Design
- New Approaches for Low-Noise On-chip Synthesis
- RF-Compatible CMOS/BiCMOS Technologies
- Low-Power A/D and Digital for Baseband Processing
- Control of Chip, Package Parasitic RF Paths

Direct Conversion RF Transceivers





Low-Frequency Errors in Direct Conversion Receivers



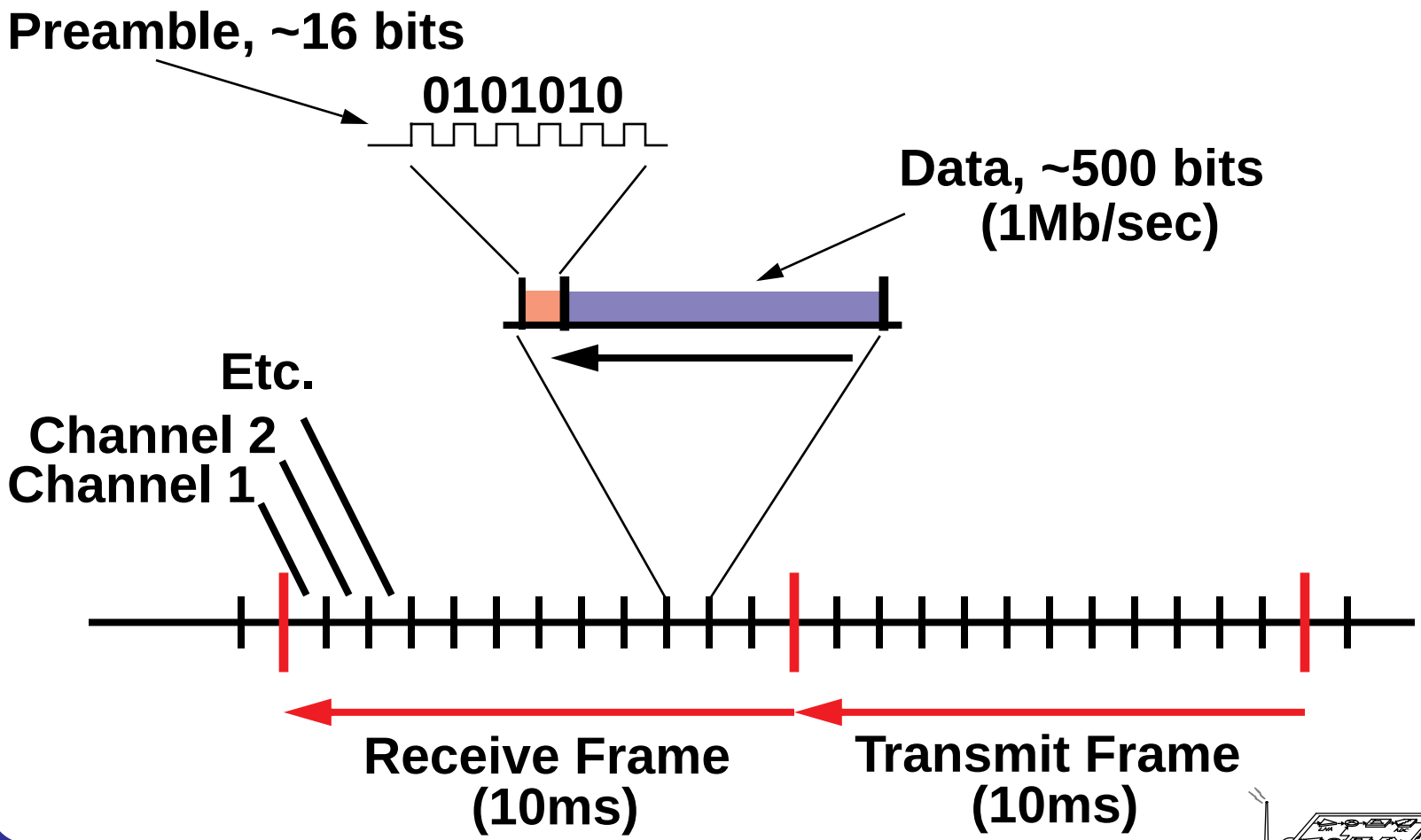
- Desired signal often has L. F. information
- Time-varying offsets 100X bigger than signal

Approaches for Practical Direct Conversion Receivers

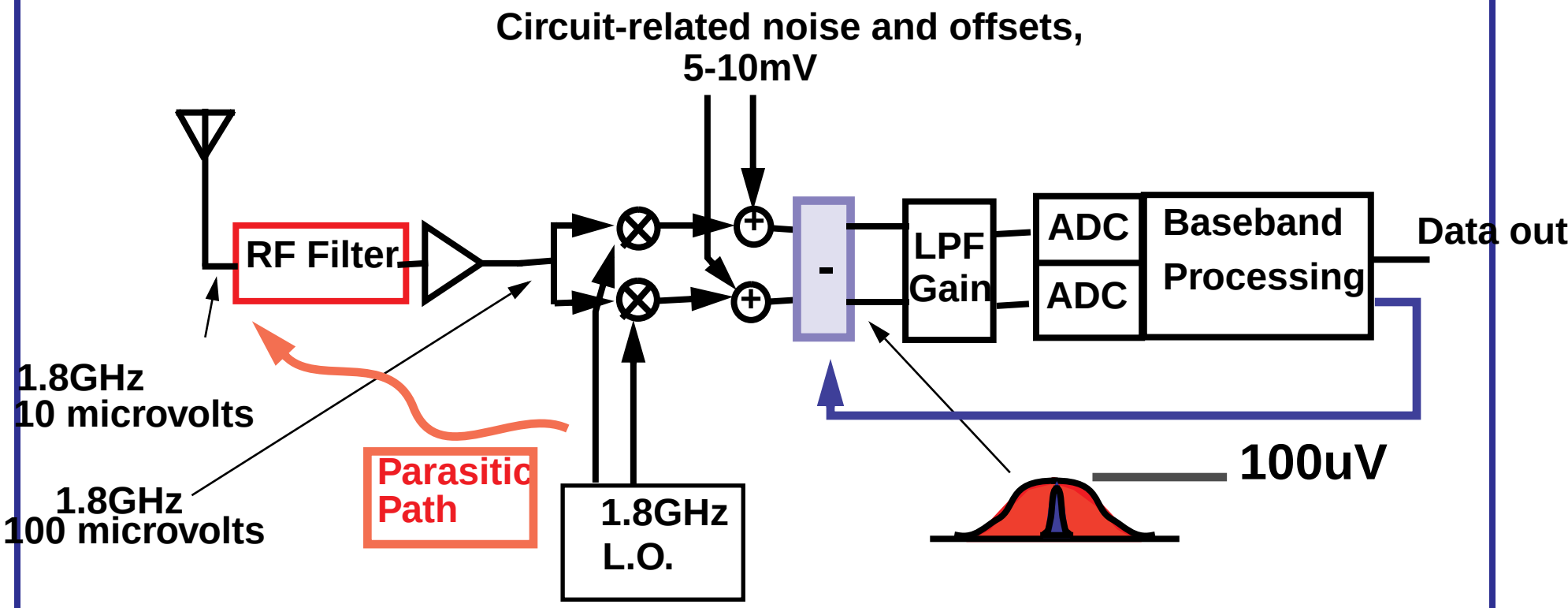
- Optimize coding for short-term DC balance
- Adaptive, Decision-Directed DC offset removal
- Low-IF architectures
- Wideband IF Double Conversion

Decision-Directed Offset Removal

- Utilize DC Balanced Preamble to Data Packet



Decision-Directed Offset Removal



- Time-varying DC Offsets tracked and removed in analog path.
- Fast update cancels 1/f noise in path
- Key problem is rapid Vos, AGC converge

Approaches for Practical Direct Conversion Receivers

- Optimize coding for short-term DC balance
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Low-IF Architectures for CMOS Xvrs

Basic idea: **Move IF from DC to a low frequency where digital or analog integrated IF bandpass filtering can be used.**

Advantage:

- **Solves 1/f noise, offset problem of zero IF**

Disadvantage:

- **Creates a close-in image problem**

The Image Rejection Problem

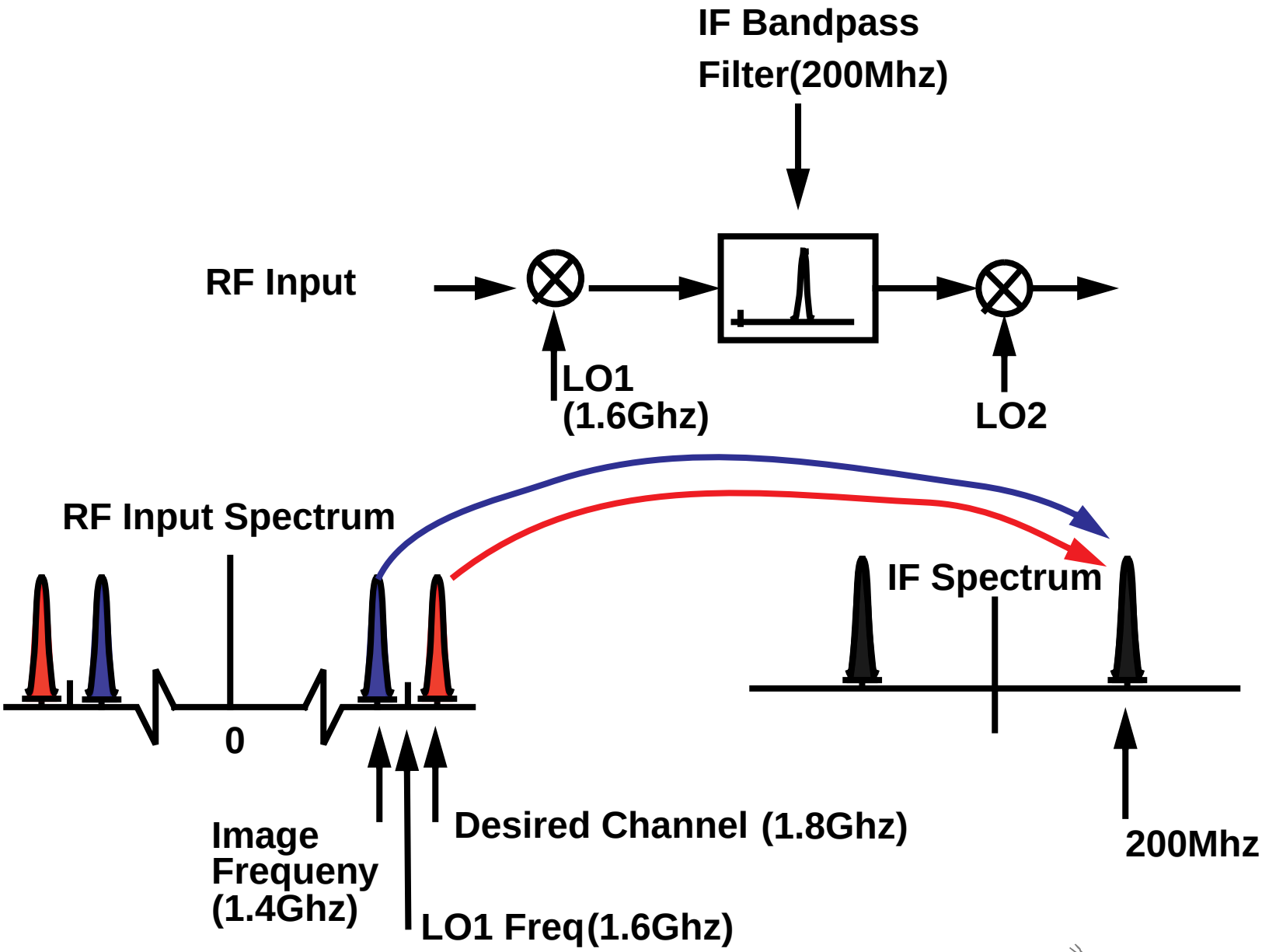
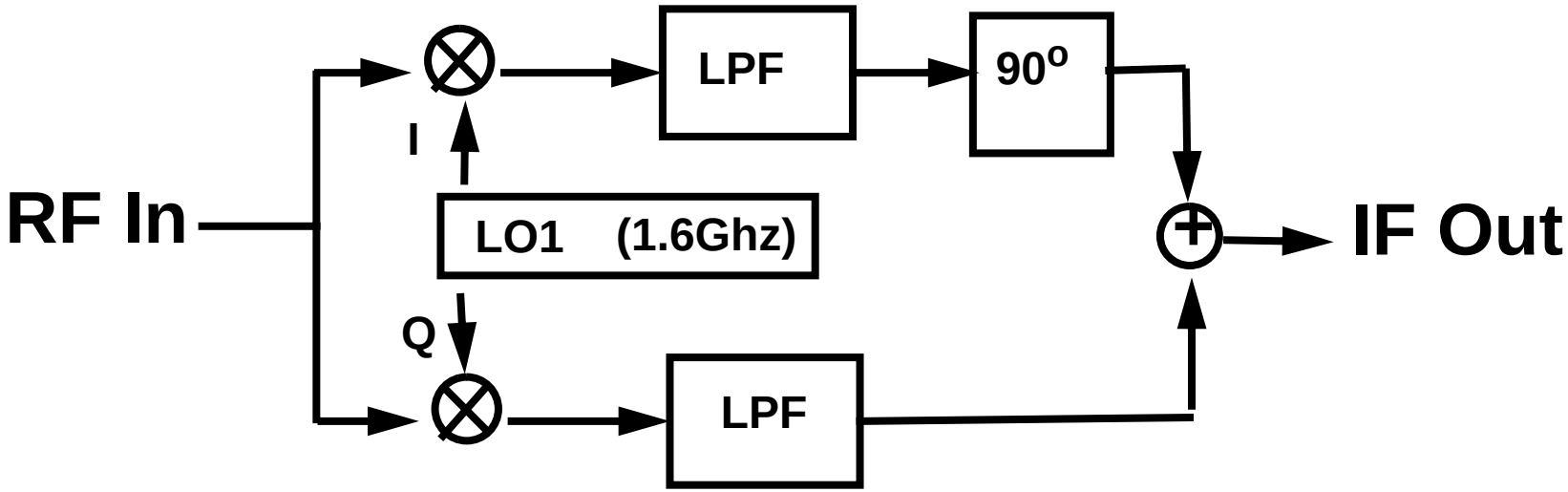


Image Rejection Mixers

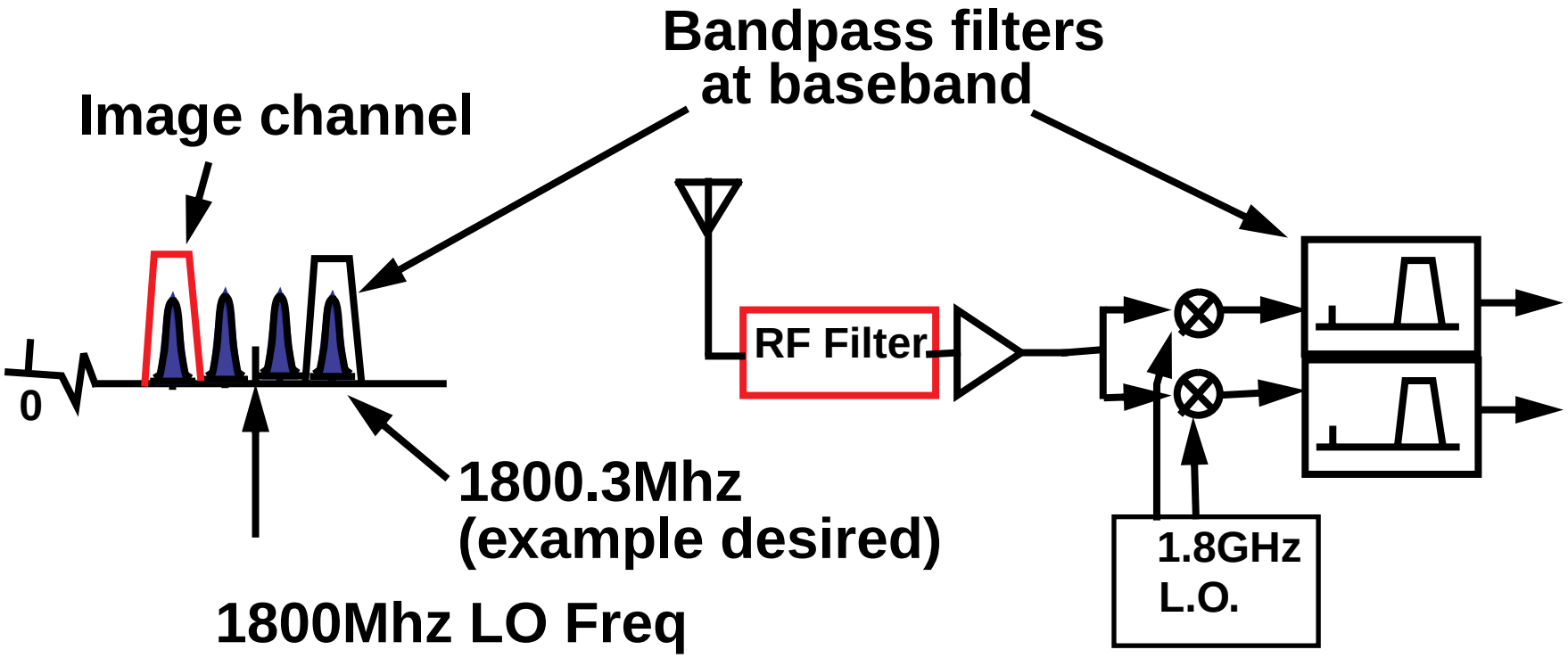
- Key Concept: Use complex signal representation to distinguish image from desired signal.

Example:



- Many variations on basic concept
- Rejection limited to 20-30 dB in most implementations by mismatches
- Most standards need 60-80dB image reject
- Additional image reject filtering or other means needed for adequate rejection. RF Filter usually supplies 30-40dB.

Image Rejection for Low-IF Rcvrs

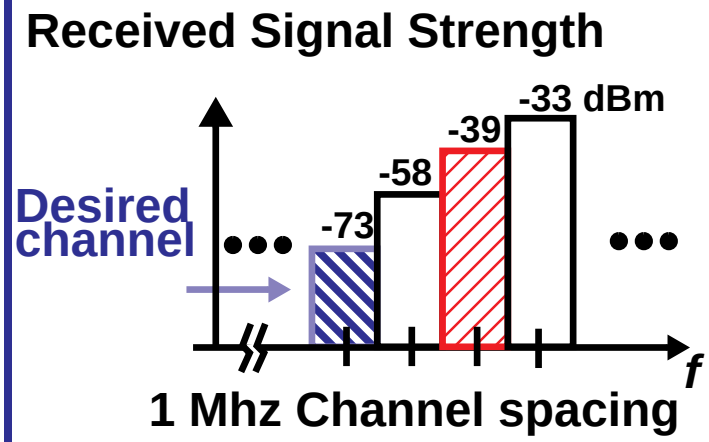


How do we get rid of image channel? (No RF Filter Atten)

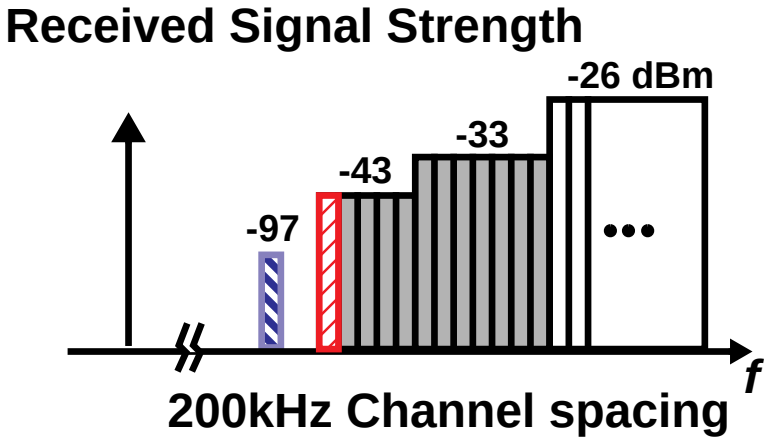
- Polyphase analog filters
- Digital I/Q filter with hi-res ADC
- Strategic image placement

Desensitization Rqmts in DECT, GSM

DECT



GSM (DCS 1800)



Key Points:

- **Image reject rqmts severe for low-IF in general (~60-80dB)**
- **I-Q LO match, filters will limit to maybe 50-60dB**
- **Certain systems guarantee “holes”**

Approaches for Practical Direct Conversion Receivers

- Optimize coding for short-term DC balance
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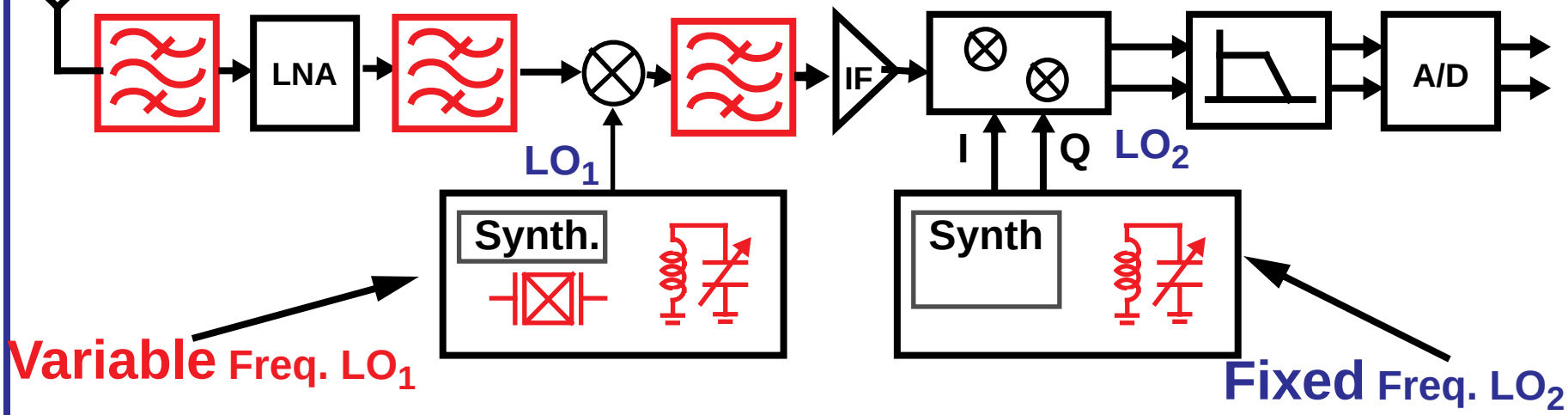
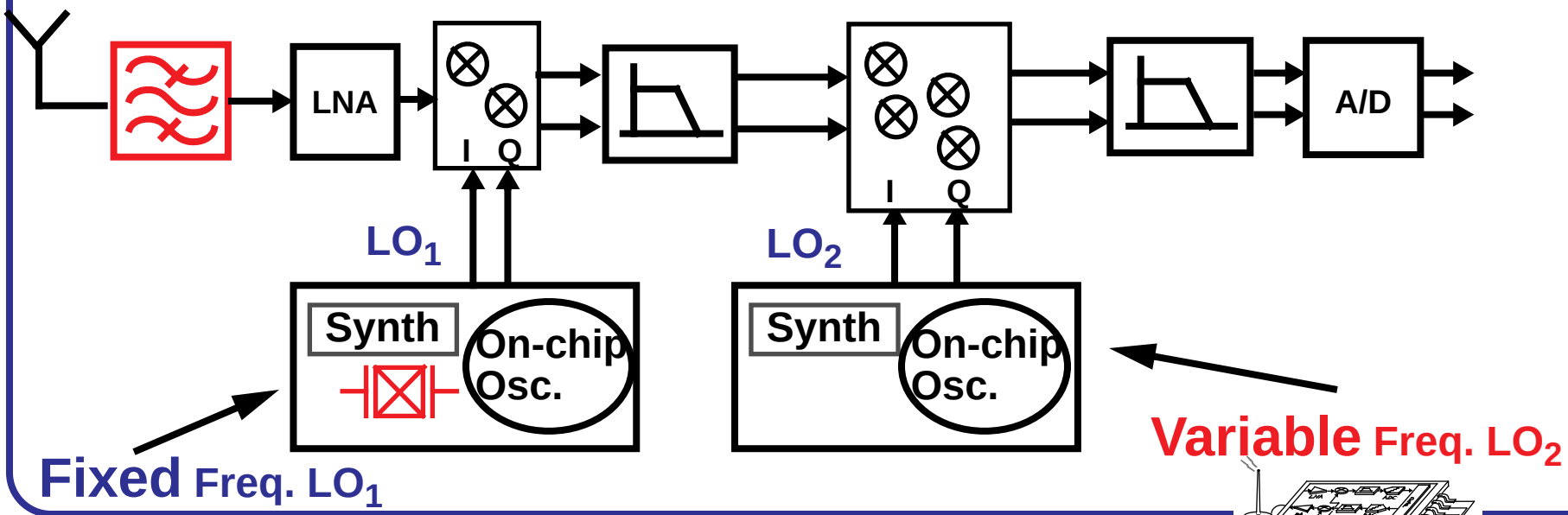
- Low-IF architectures
- Wideband IF Double Conversion

Wideband IF Double Conversion

Conventional Super-Heterodyne



Wideband Double Conversion



WBIFDC- Why Do it?

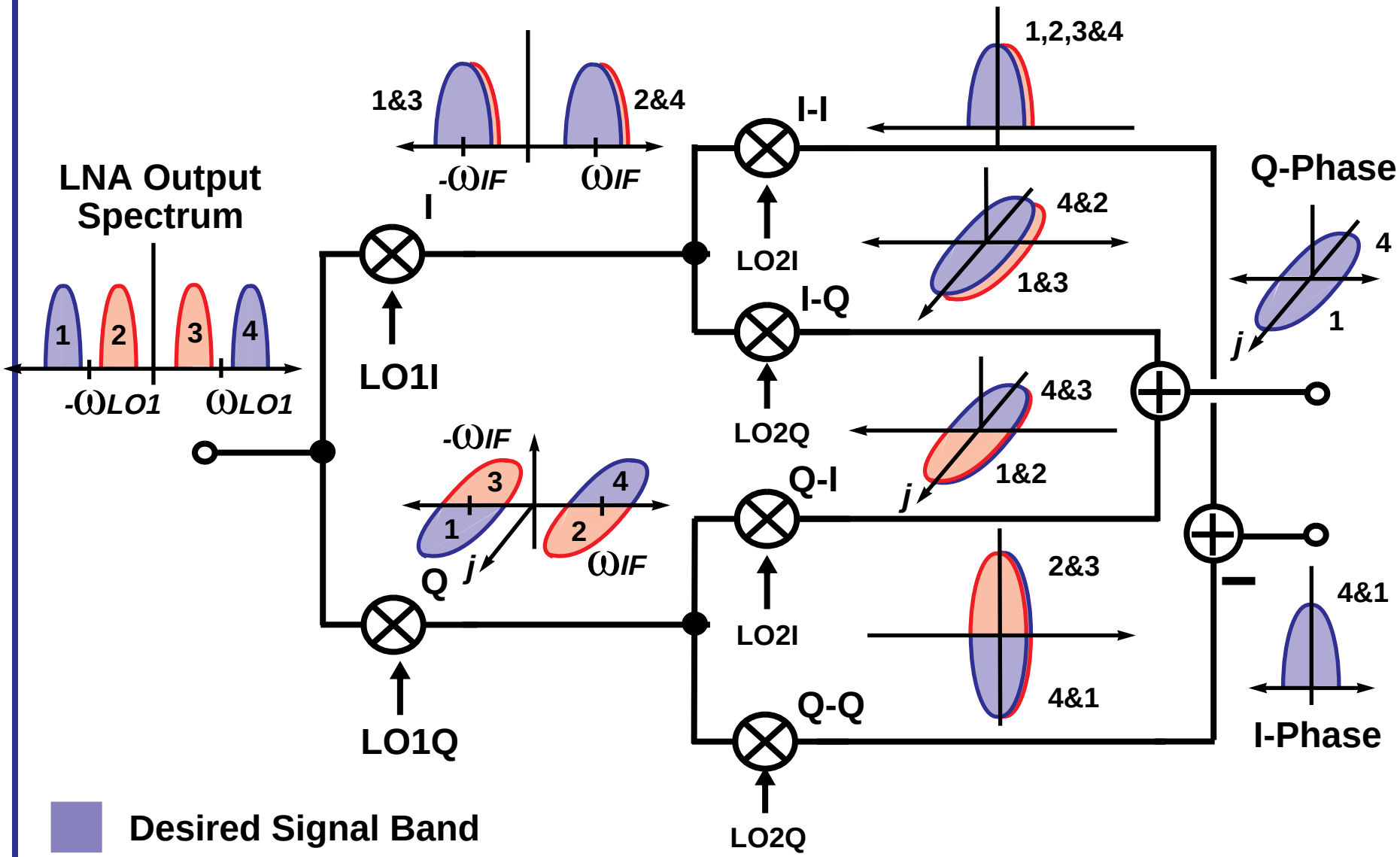
Disadvantages

- **Reintroduces Image Reject issue- Must use image reject architecture**
- **Two mixers in signal path, more IM3**
- **More mixers- more power**

Advantages

- **Greatly alleviates the Synthesizer problem**
- **Matches well to needs of multistandard**

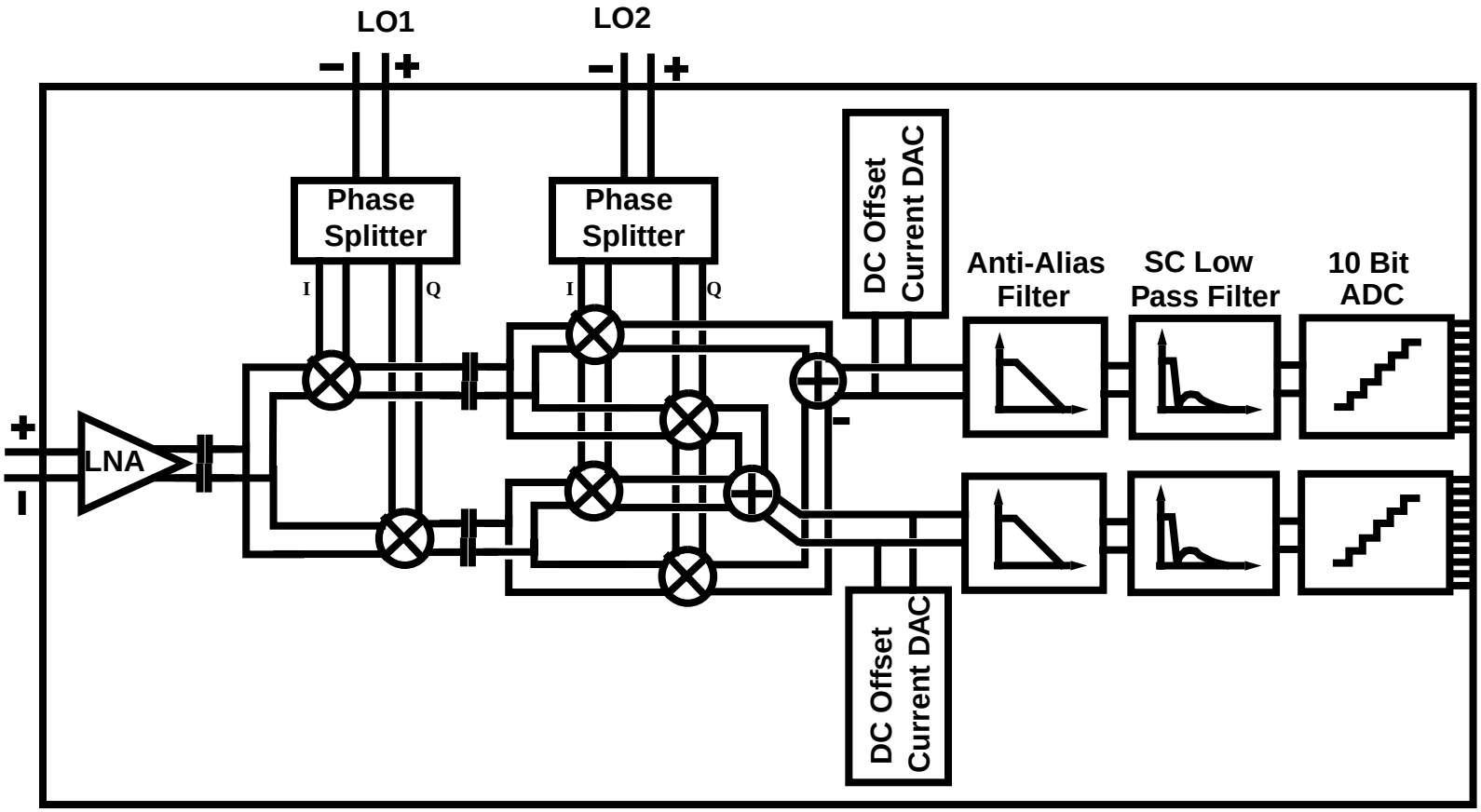
Example Image Cancellation Scheme



Desired Signal Band

Undesired Image Band

Example WBIFDC Rcvr

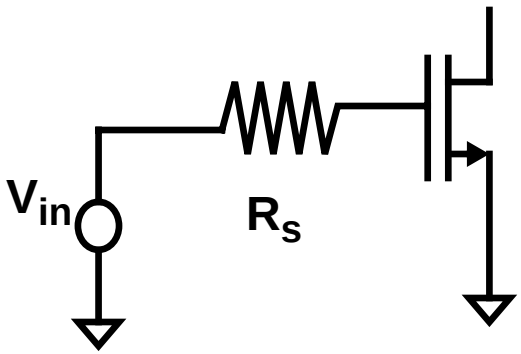


Keys to Progress in Low-Power Adaptive RF Transceiver Design

- New Receiver Architectures
- Low-Power CMOS/BiCMOS RF Circuit Design
- New Approaches for Low-Noise On-chip Synthesis
- RF-Compatible CMOS/BiCMOS Technologies
- Low-Power A/D and Digital for Baseband Processing
- Control of Chip, Package Parasitic RF Paths

Noise Figure in LC-Tuned RF Amplifiers

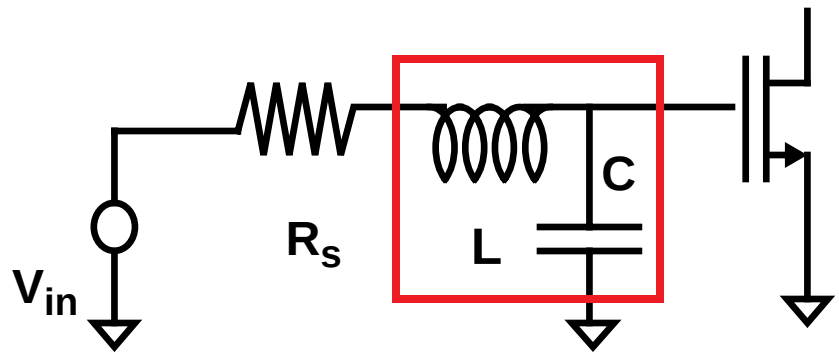
Broadband Case



$f_{signal} << f_t$

$$NF = 1 + \left[\frac{\frac{2}{3}}{g_m R_s}\right] + others$$

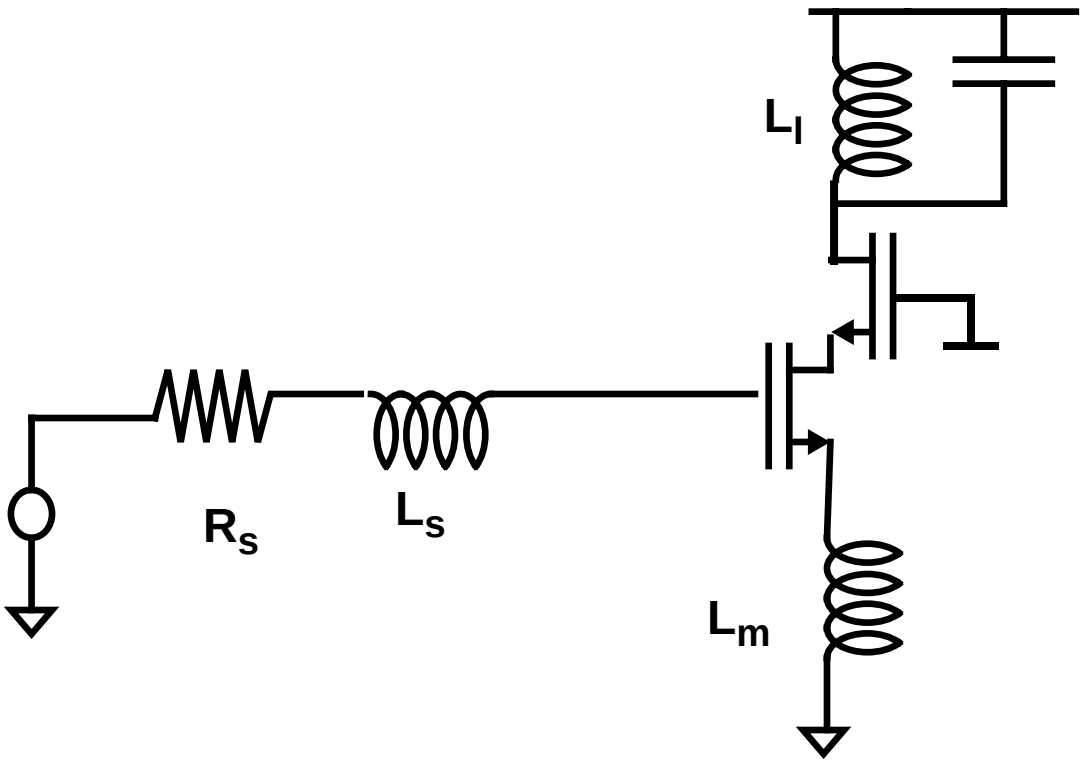
Narrowband Case



$f_{signal} << f_{max}$

$$NF = 1 + \left[\frac{\frac{2}{3}}{K g_m R_s}\right] + others$$

Example Tuned RF Amplifier

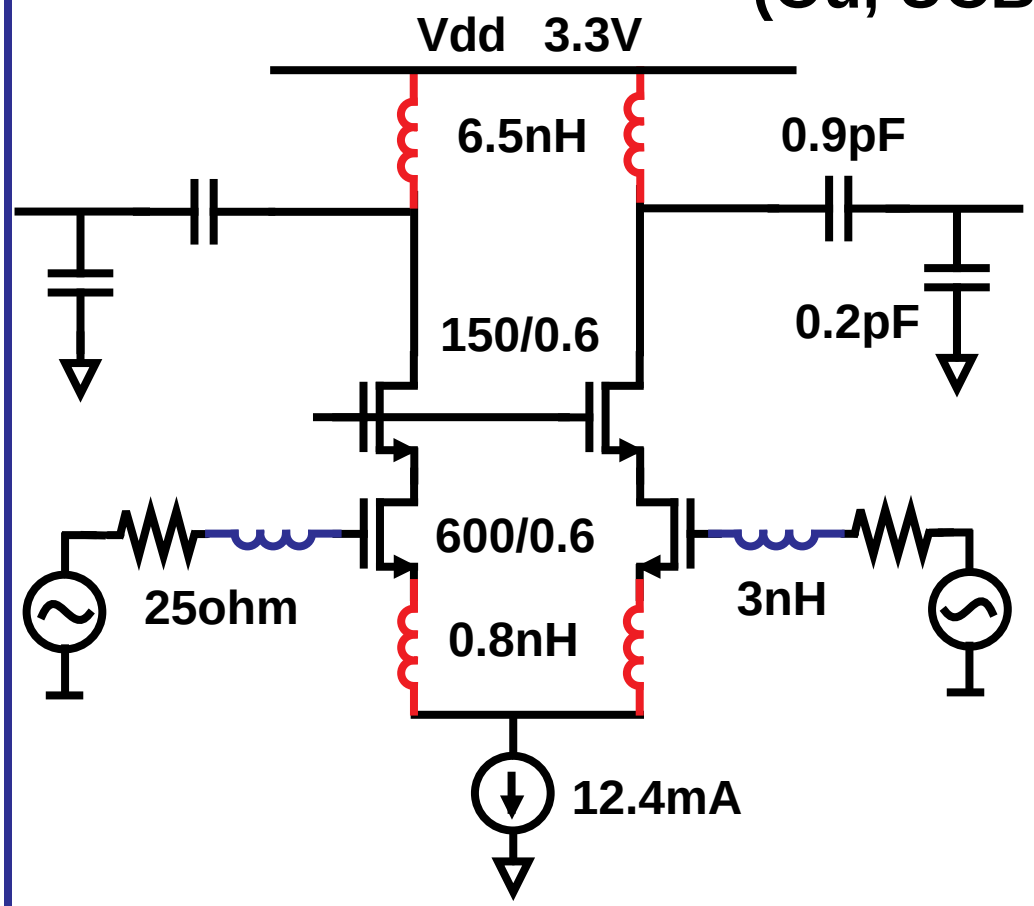


Key Points:

- **L-C Narrowband Design is essential for RF LNA, Power amplifier.**
- **Inductor Q, capacitor Q, and device f_{max} are the critical technology parameters**

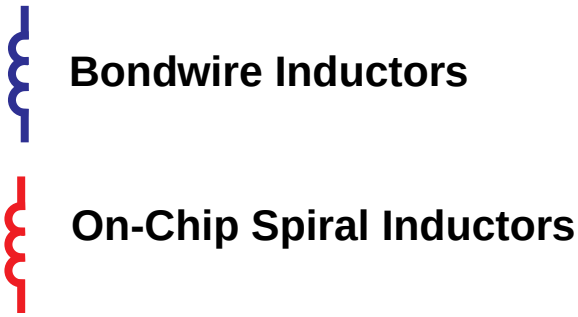
Low Noise Amplifier Example

(Ou, UCB)



Measured Results

Noise Figure	< 5dB
Voltage Gain	22dB
Power@3.3V	41mW
Linearity: IP3@1.9GHz	> -6dBm @input



- **Inductor tuned common-source amplifier using on-chip spiral and bondwire inductors**

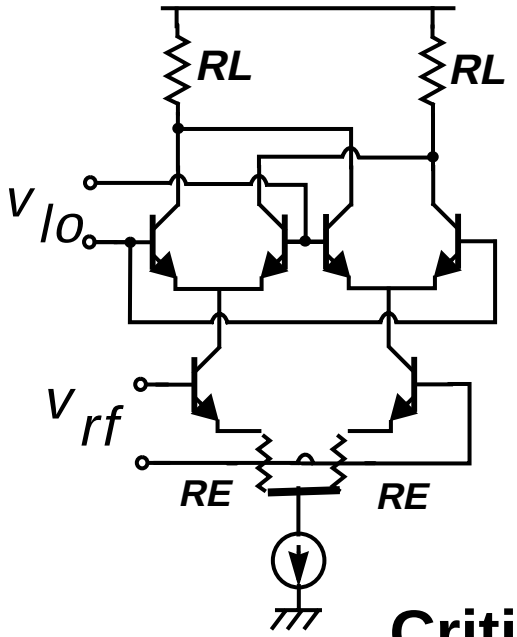
Comparison of CMOS LNAs

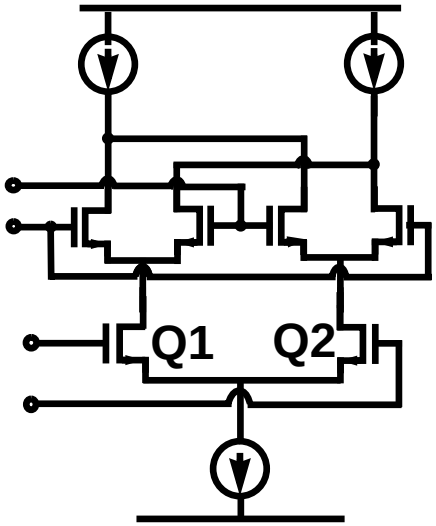
	Chang ED Lett.93	Sheng ISSCC 96	Karani-colas ISSCC 96	Schaef-fer, Lee VLSI96	Abidi,et al, ESSCIRC95	Ou, et al, ISSCC 97
Freq	770MHz	900MHz	900MHz	1.5GHz	900MHz	1.9GHz
NF	6dB	7.5dB	2.2dB	3.5dB	3.2dB	< 5dB
Gain	14dB	11dB	15.6dB	22dB	22dB	22dB
Idc	7mA	11mA	7.4mA	20mA	5.2mA	12.4mA
Tech	2μ	0.8μ	0.5μ	0.6μ	1.0μ	0.6μ

CMOS Mixer Implementation

- Mixer Linearity Limits Rcvr IIM3 Usually
- Mixer Noise often a Major Contributor
- Approaches:
    - Sampling Mixers
    - Ring Mixers
    - Gilbert Cells in CMOS
    - Gilbert Cell Variations (Micromixer, Abidi)

Gilbert Cell Mixer in CMOS





Critical Design Issue:

- Vgs-Vt of Q1-Q2 sets Linearity
- gm of Q1-Q2 sets noise
- Id of Q1-Q2 sets power

$$'_{1p3} = 4\sqrt{\frac{2}{3}}(V_{gs} - V_T$$

$$v^2 = 4kT\left(\frac{2}{3}\right)\left(\frac{2I_d}{V_{gs} - V_T}\right)$$

$$P = I_d V_{dd}$$

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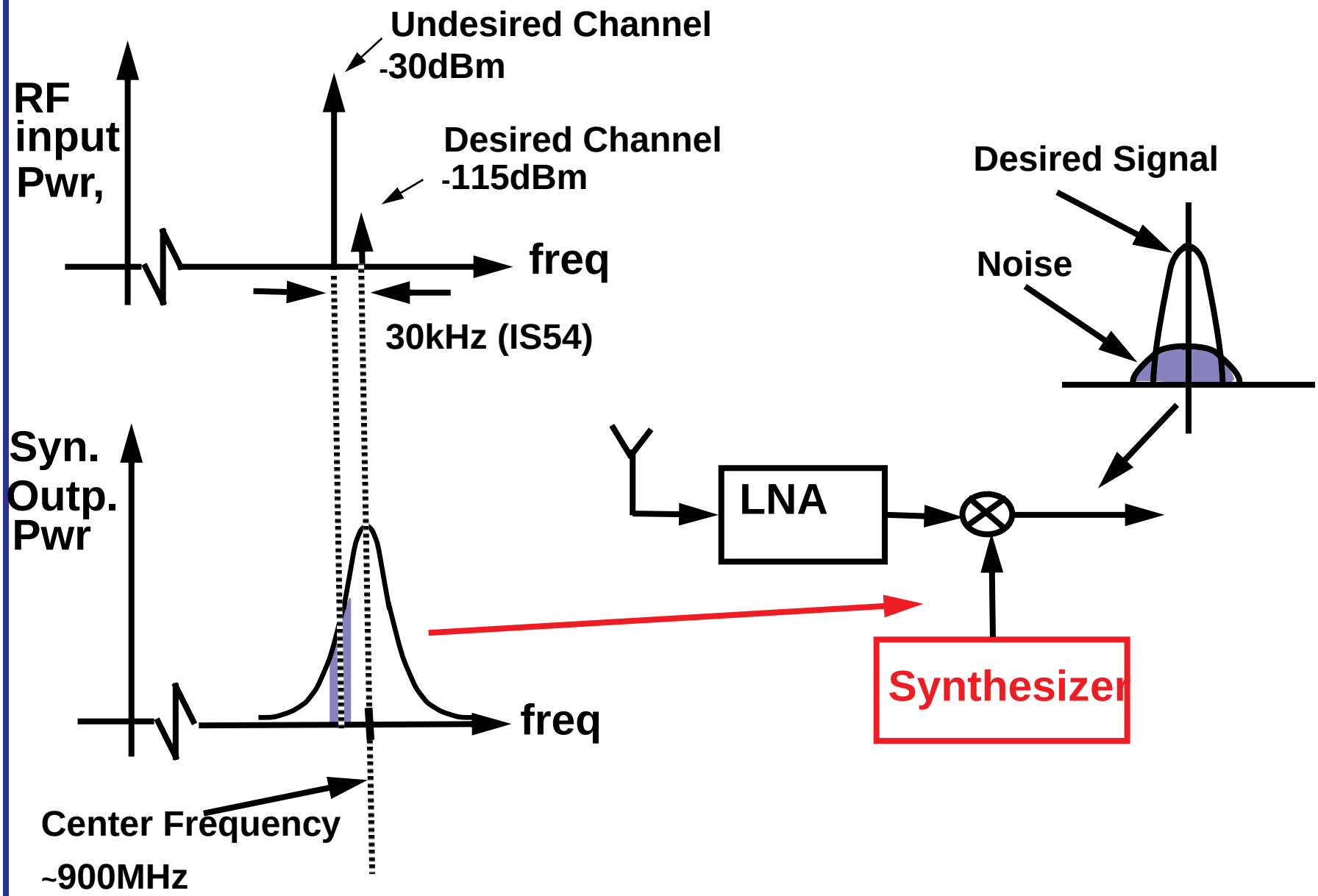
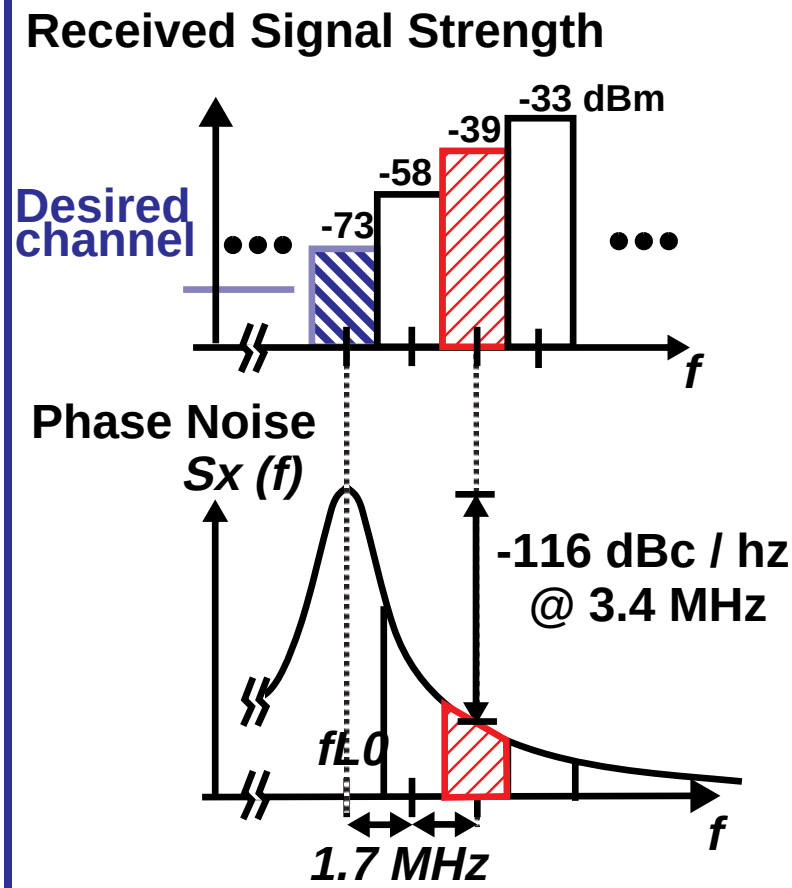
Why is Synthesizer Phase Noise Important?

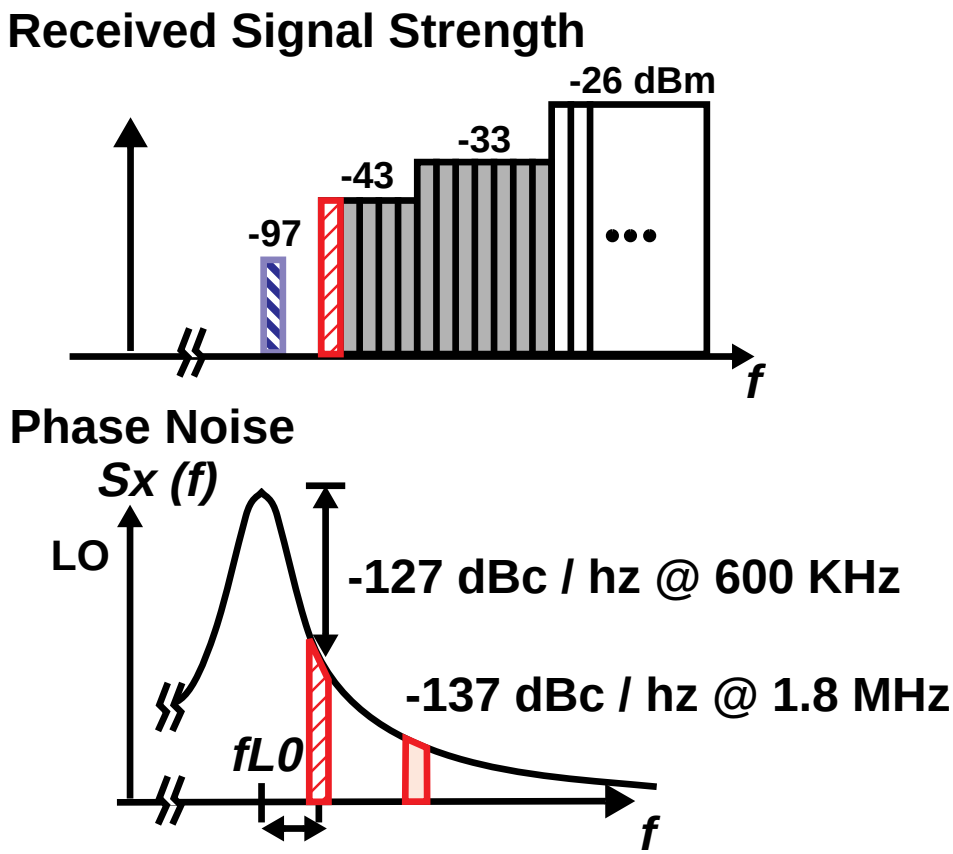


Phase Noise Rqmt in GSM and DECT

DECT



GSM (DCS 1800)



Normalized EQ. Phase Noise @ 100 KHz :

DECT -85 dBc/hz ***GSM -111 dBc/hz***

Integrated Synthesizers for PCS Transceivers

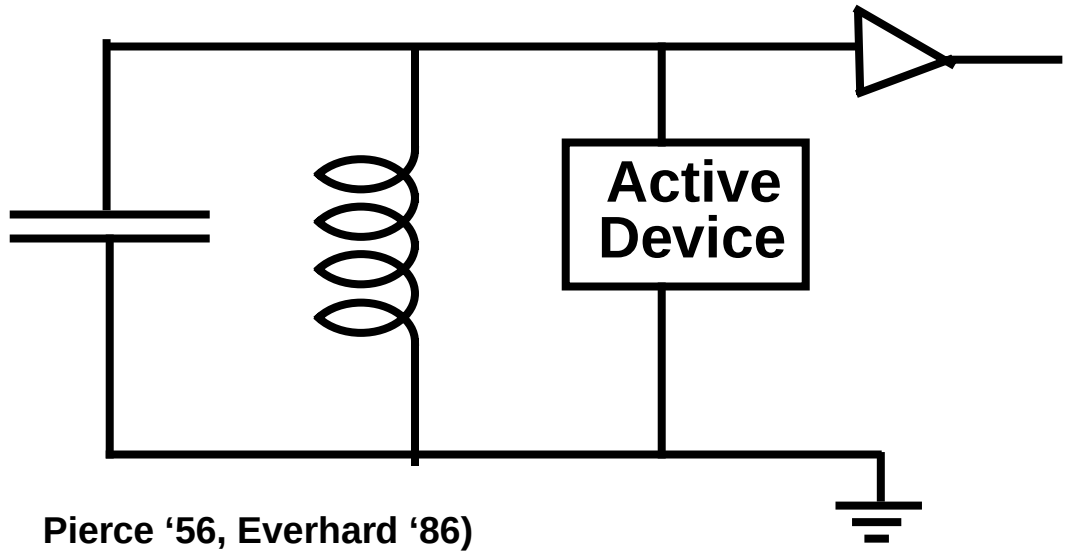
Phase Noise Requirements:

- **Cordless, LAN: -100-120dBC/Hz @200kHz-1MHz**
- **Cellular -115-130dBc/Hz @ 60-250kHz.**

Key Issue:

- **Can we do this with on-chip components at acceptable levels of power dissipation?**

Sources of Oscillator Phase Noise



Pierce '56, Everhard '86)

$$\left(\frac{C}{N}\right) \sim \left(\frac{\varepsilon_{stored}}{kT}\right)$$

$$\frac{\left(\frac{C}{N}\right)}{PWR} \sim \left(\frac{1}{fkT}\right) Q$$

Options for on-chip VCO:

- Compatible on-chip high-Q inductors
- Find a way to use ring oscillators (Q=1)

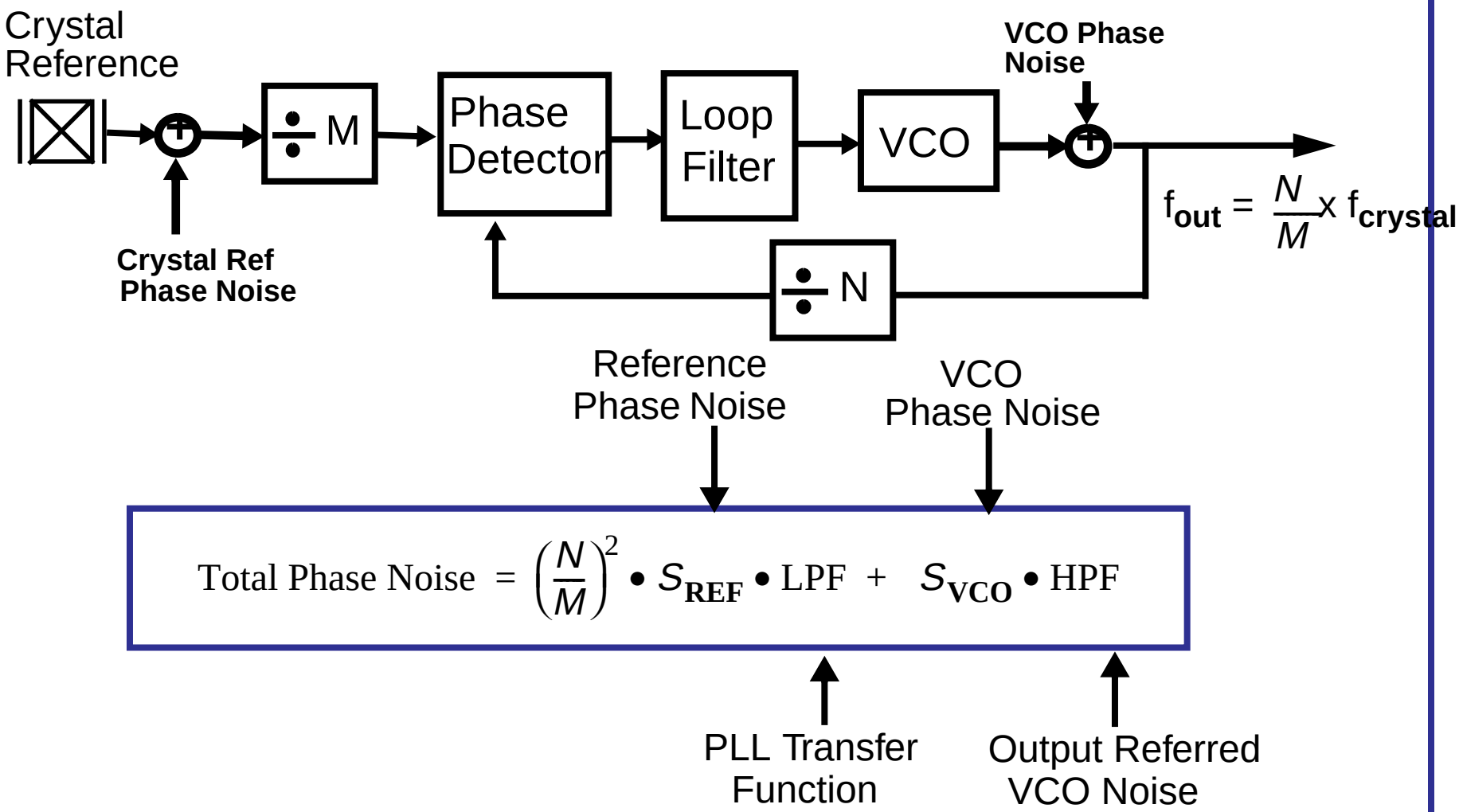
Summary of VCO Noise Results

Table 1:

Author	Pd	Freq	C/N	F	Est Q	K0
Cran-inckx,Steyart, ISSCC95	24mW@3V	1.8Ghz	-85dBc	10kHz	10	2.7×10^{-19}
Rael, Abidi, ISSCC96	43mW@3V	900Mhz	-100dBc/Hz	100kHz	4	2.1×10^{-19}
Souyer, ISSCC96	24mW@3V	4Ghz	-106dBC/Hz	1Mhz	7	2.4×10^{-19}
Thamsirianut, CICC94	7.5mW, 3V	900Mhz	-93dBc/Hz	100kHz	1 (class B RO)	0.47×10^{-19}
Weigandt, ISCAS 94	10mW, 3V	1Ghz	-85dBc/Hz	100kHz	1(class A RO)	3.3×10^{-19}
Cranicks, Ste-yart, VLSI96	6mW, 1.5V	1.8Ghz	-116dBc/Hz	600kHz	5.7	0.10×10^{-19}

$$\frac{N}{C} = K_0 \left(\frac{f_0}{f}\right)^2 \frac{1}{PQ}$$

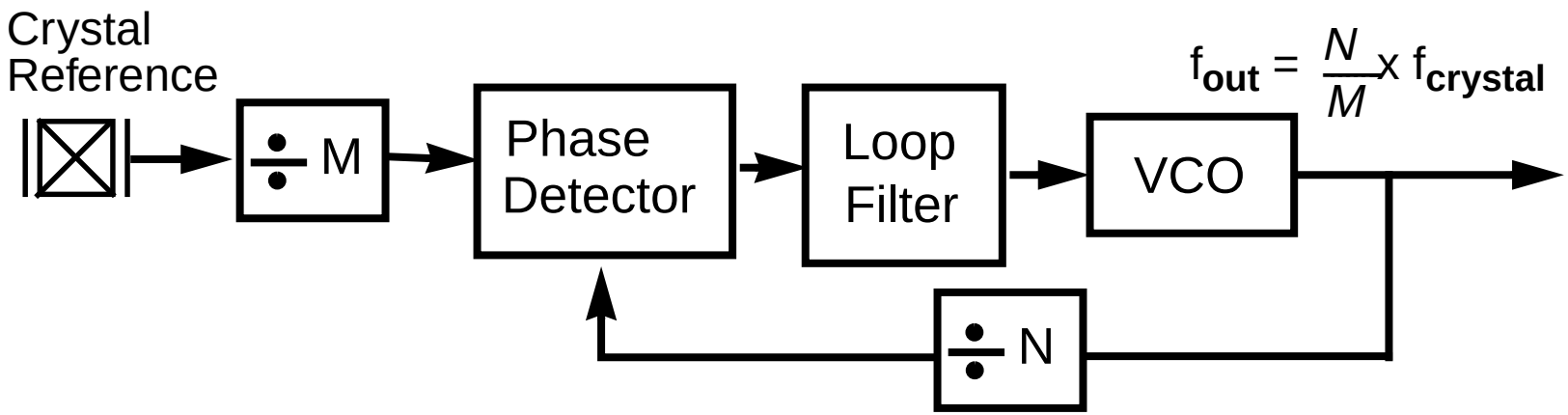
Phase Noise in Freq. Synthesizer PLL

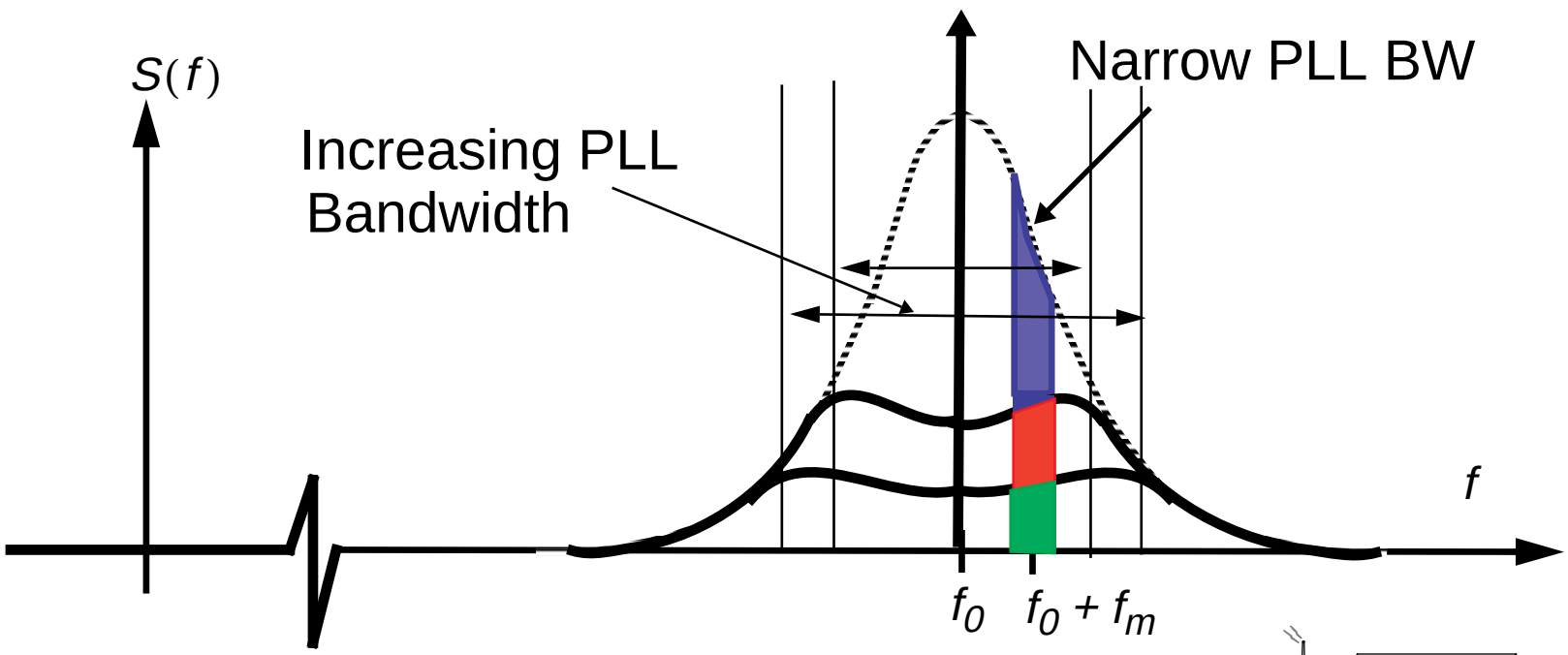


$$\text{Total Phase Noise} = \left(\frac{N}{M}\right)^2 \bullet S_{\mathbf{REF}} \bullet \text{LPF} + S_{\mathbf{VCO}} \bullet \text{HPF}$$

Phase noise optimized through VCO design and largest practical PLL loop bandwidth

Typical Synthesizer Implementation





Phase-Noise-Optimized Synthesizer Design

Problem:

- **Conflict between narrow channel spacing and high comparison frequency**

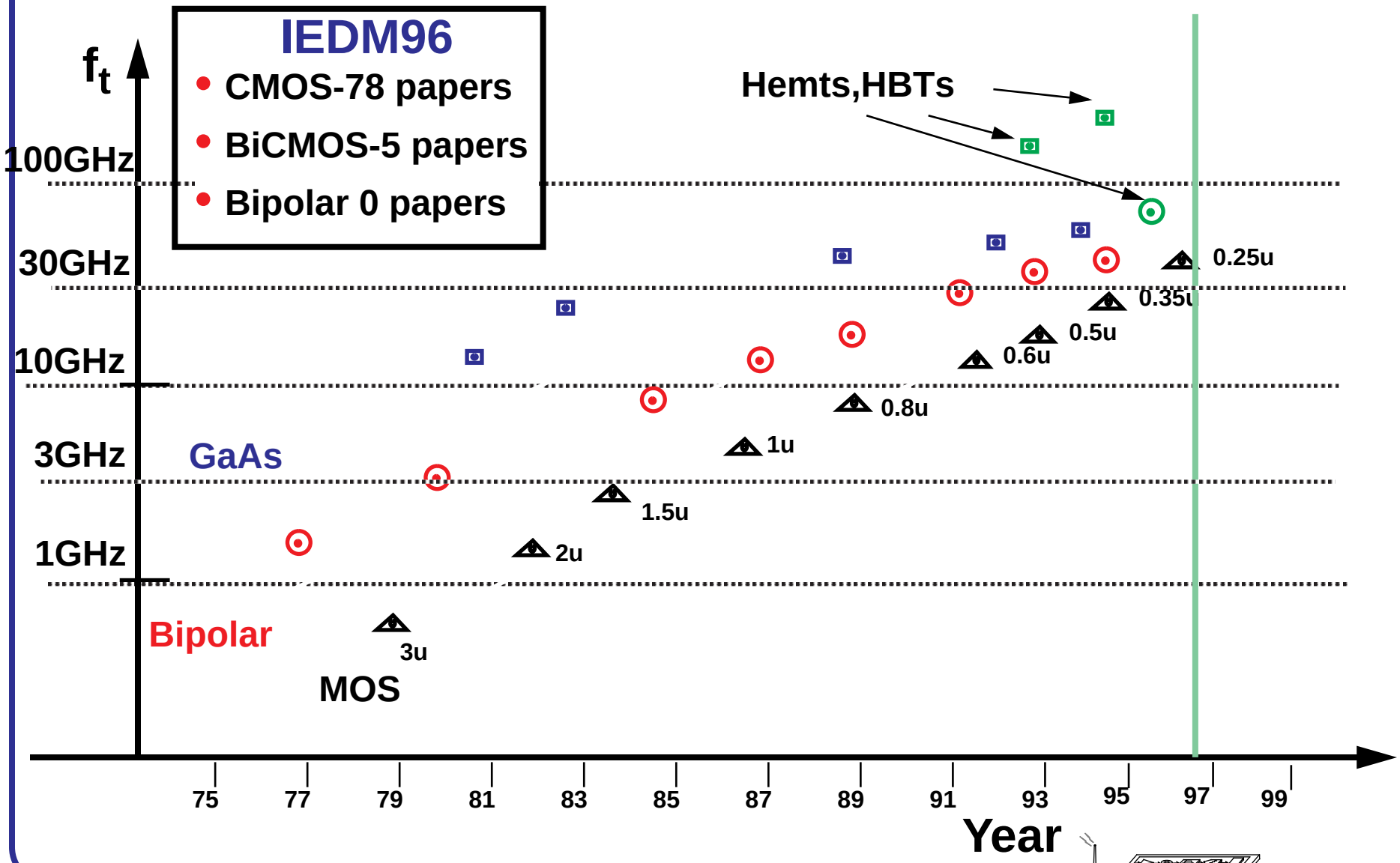
Some Possible Solutions:

- **Wideband double conversion, fixed first LO**
- **Coarse/fine synthesis using DDS or other means for 2nd step**
- **Ring oscillator VCO with noise-shaped multi-tap phase interpolation**

Keys to Progress in Low-Power Adaptive RF Transceiver Design

- New Receiver Architectures
- Low-Power CMOS/BiCMOS RF Circuit Design
- New Approaches for Low-Noise On-chip Synthesis
- RF-Compatible CMOS/BiCMOS Technologies
- Low-Power A/D and Digital for Baseband Processing
- Control of Chip, Package Parasitic RF Paths

Technology Speed Figure of Merit vs Time



RF IC Technology and Design Considerations

- **CMOS, BiCMOS are the only alternatives for high integration**

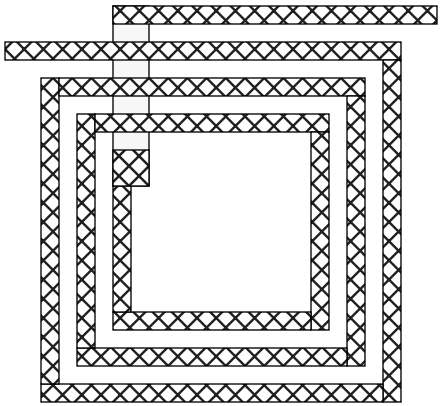
- **Scaled NMOS devices are fast**

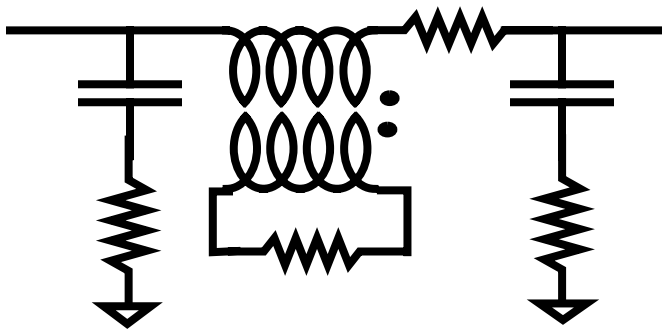
Technology	f_t	f_{max}
0.35 micron	25GHz	40GHz(e)
0.25 micron	40GHz	60-70GHz(e)
0.18 micron	60 GHz(e)	90-100GHz(e)

- **Inductors and Capacitors of reasonable Q are essential**

Inductors in Silicon ICs

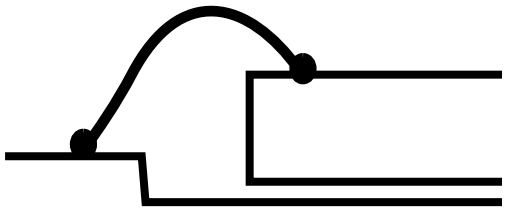
Aluminum Spirals

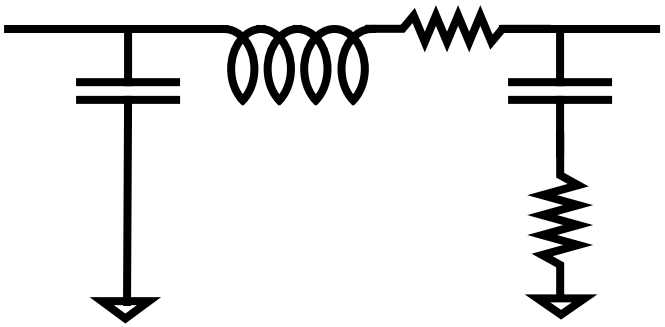




- L=1-10nH
- Q=4-8@2Ghz
- f_{self}~3-10Ghz

Bond Wires





- L=1-5nH
- Q=20-40@2Ghz

Alternatives for High-Q Resonators in Si ICs

- **Standard aluminum spirals or bond wires for inductance**
- **Etched cavities for improved self-resonance**
  (Abidi et al, various refs)
- **Plated-up thick metal for higher Q inductors**
  (Burghartz, IEDM96, Q=40)
- **Micromachined structures for variable capacitors**
  (Boser, Young)
- **Compatible on-chip accoustic resonators, etc.**

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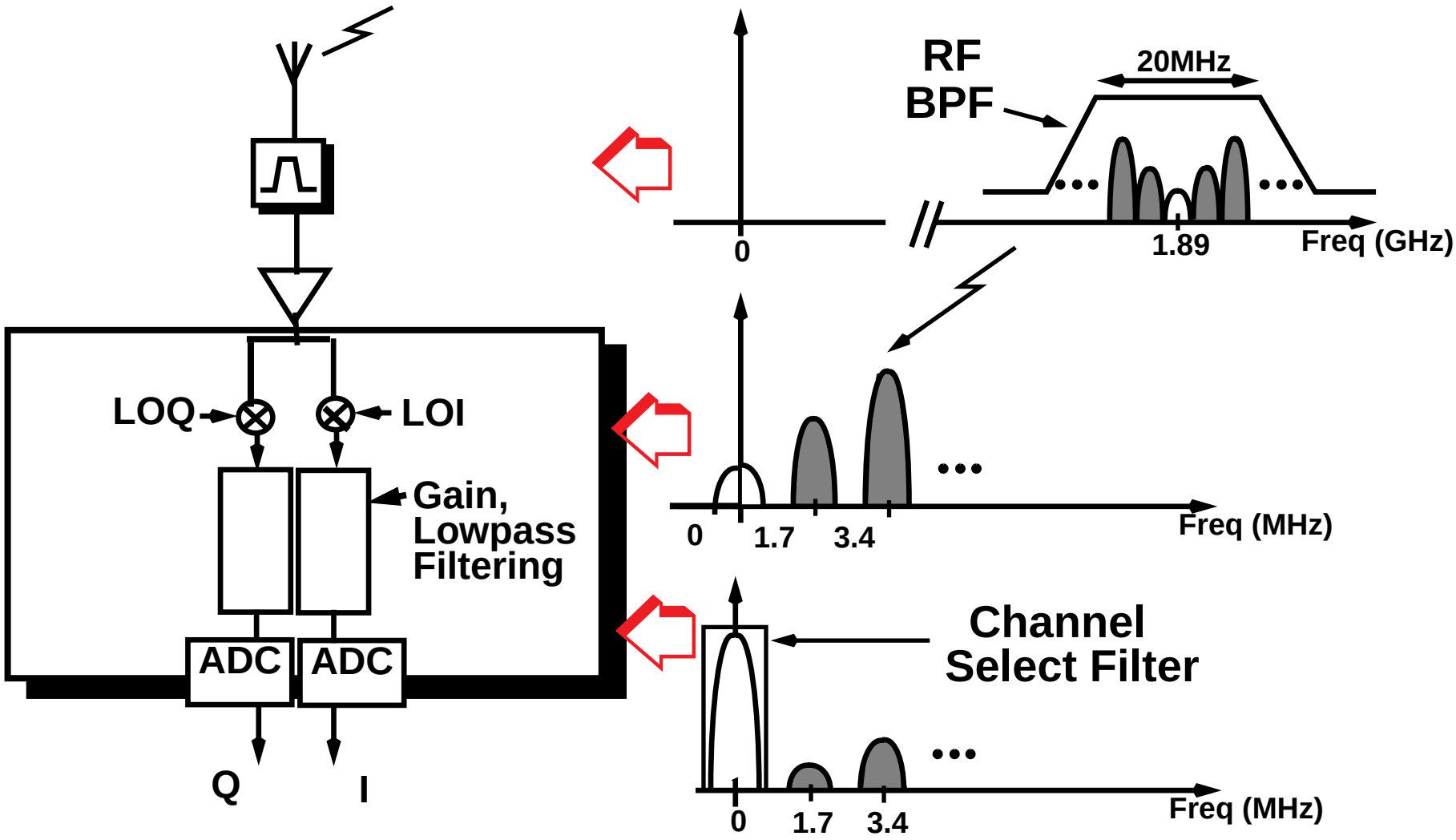
Baseband Processing in Direct Conversion Rcvrs



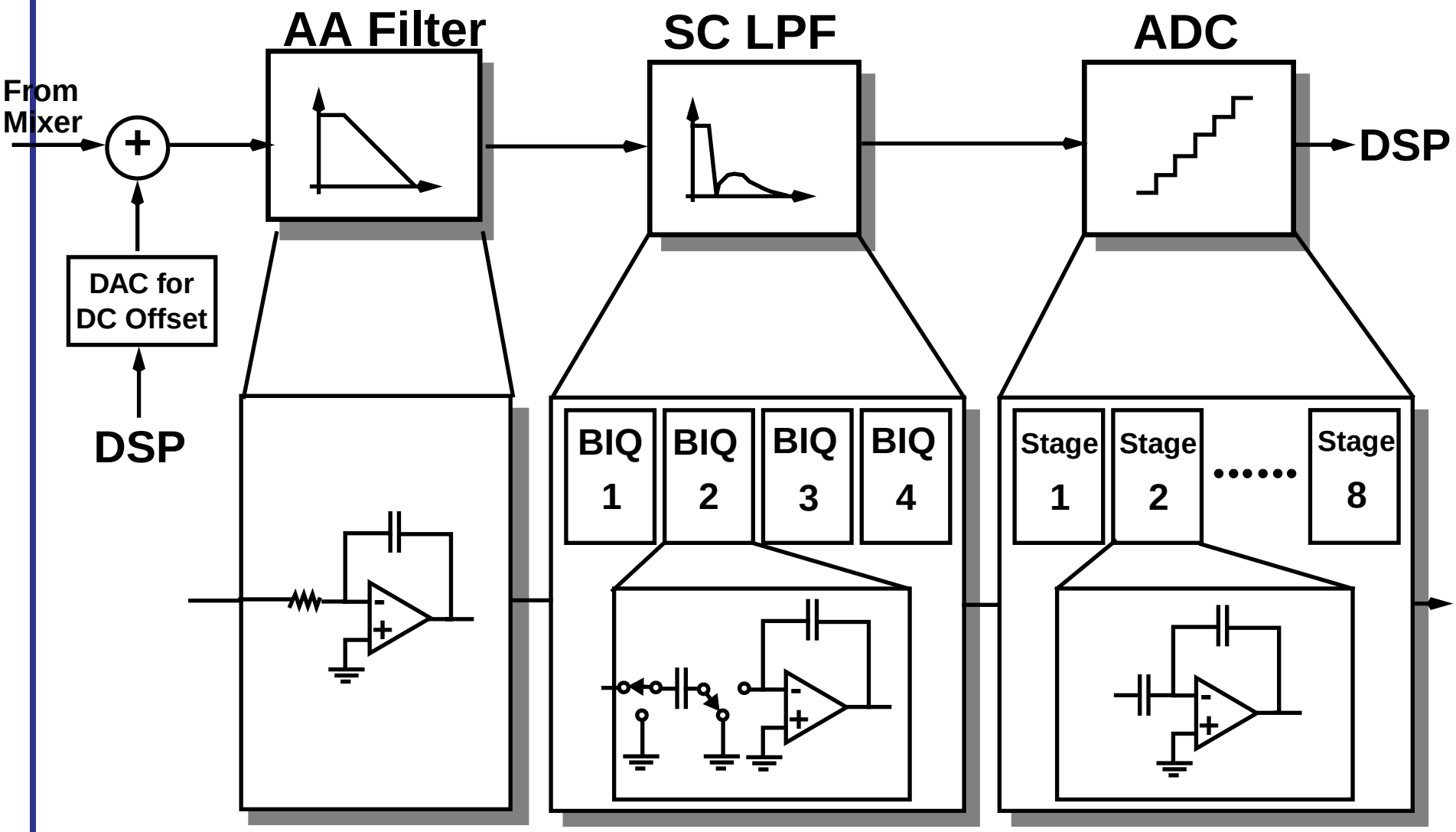
Baseband Filter/Amplifier Design

- Very Low input noise required- Noise Eqiv resistance <<5Kohm
- Intermod performance for large HF signals critical
- Power optimization through aggressive capacitor scaling to kT/C limit required
- Full digitization from mixer output appears possible- requires 13-14 bit res.

See :

- Abidi et al, VLSI 96
- Cho et al VLSI 96

Typical Baseband Filter Implementaton



Keys to Progress in Low-Power Adaptive RF Transceiver Design

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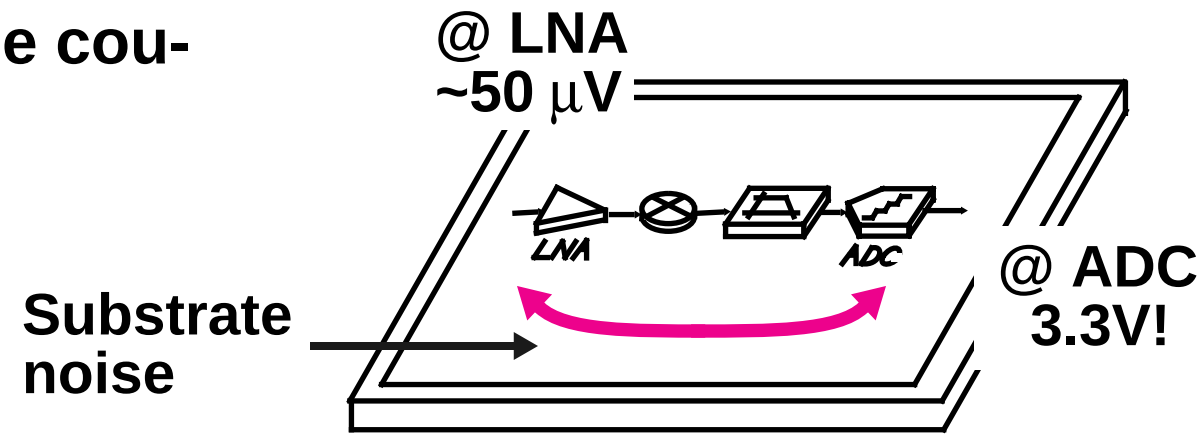
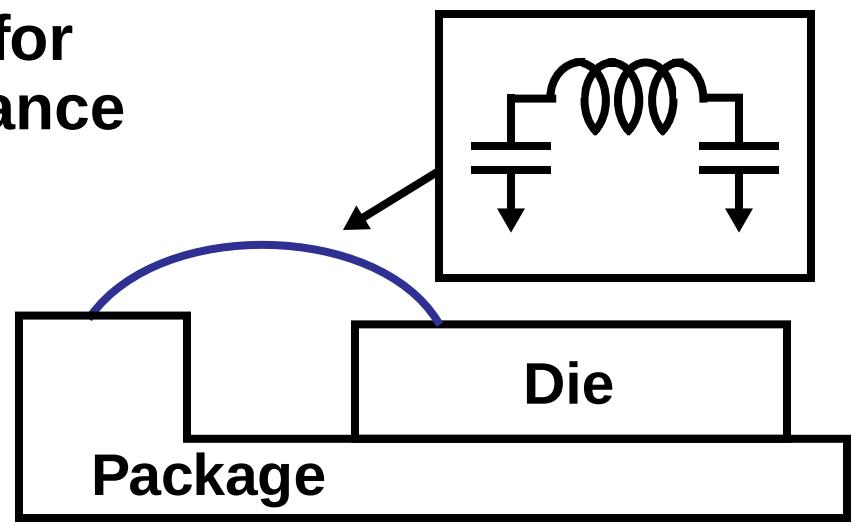
- **Substrate noise coupling**



- **Package modeling**
  - **Bond wire modeling for LNA & PA's I/O impedance matching**



Architectures and Technologies for CMOS RF Transceivers

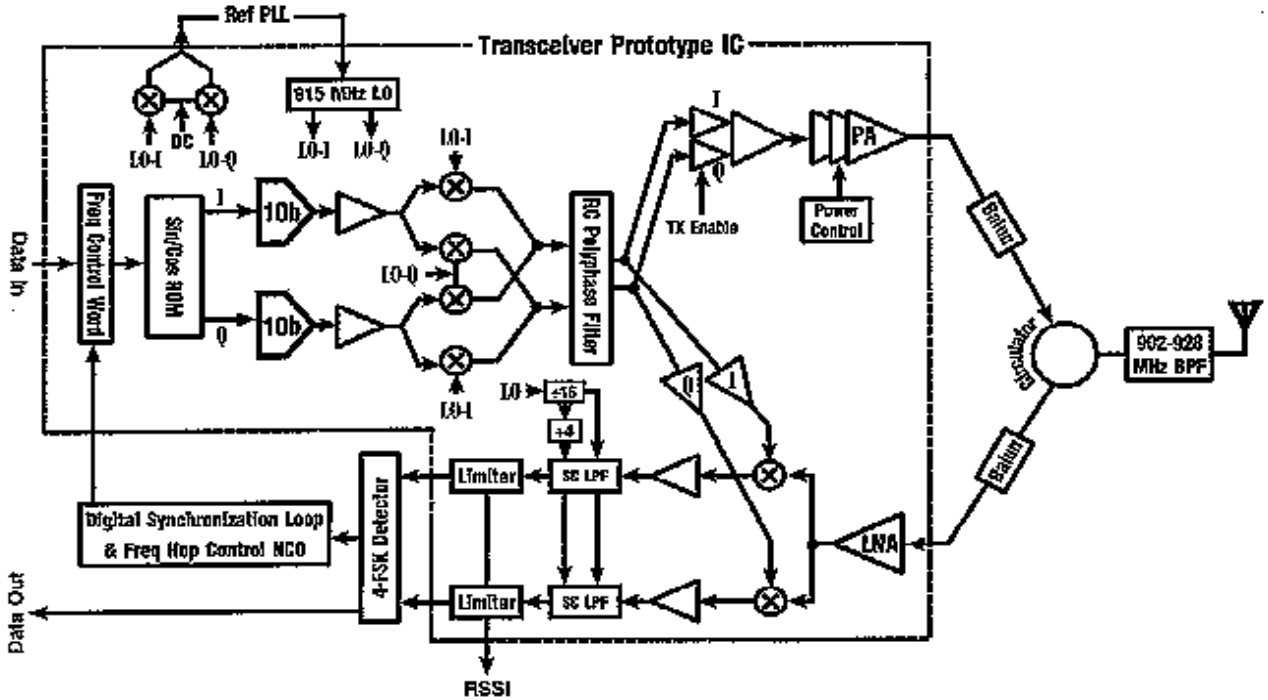
- RF Transceivers in PCS Systems
- Typical Current Implementations
- New Approaches for Low-Power RF Transceivers
- Examples and Current Status

900MHz CMOS Wireless LAN Transceiver

A. Abidi, et al, UCLA, 97ISSCC

- **Frequency-Hopped 900Mhz Spread-Spectrum LAN**
- **2-160kbps Data Rate**
- **Direct Conversion Receiver, AC Baseband path**
- **Fixed VCO+DDS offset frequency**
- **Tuned LNA, Pwr Amp**
- **30mW Variable Transmit Power Amplifier**
- **Dual Direct-Modulation Transmit Mixers**

Block Diagram, UCLA 900Mhz Xvr



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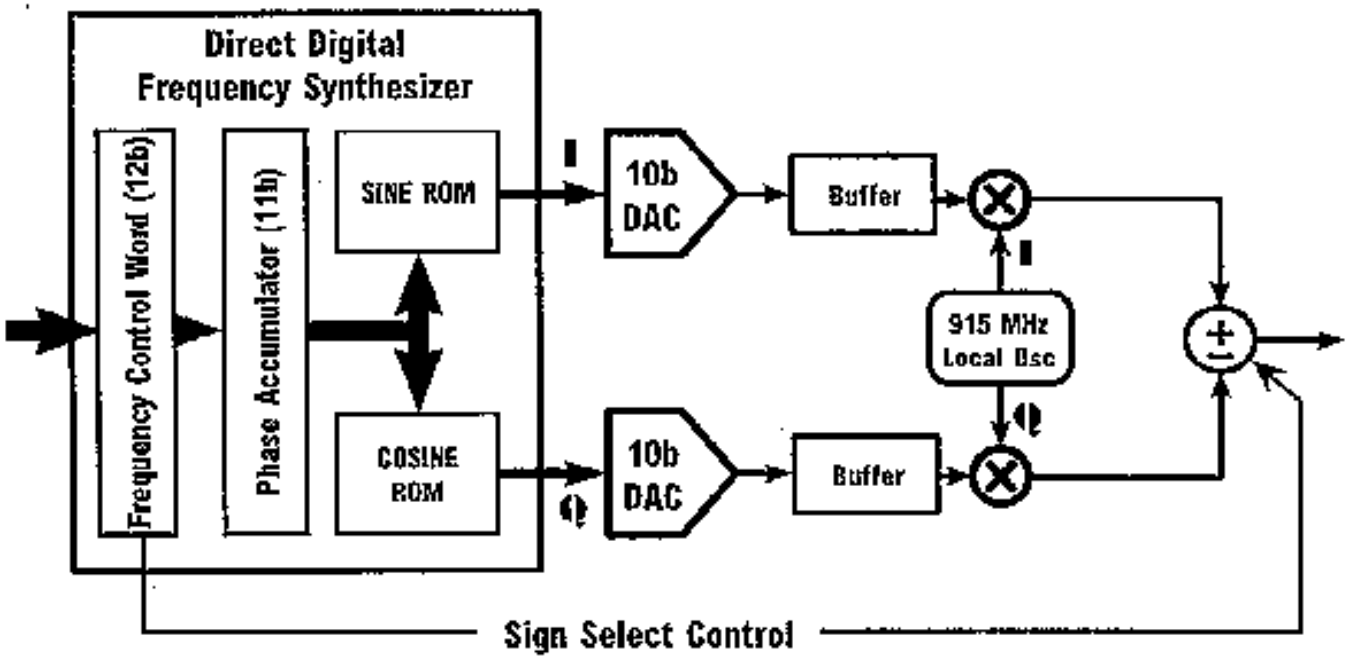
DDS Synthesizer System



Transceiver Performance Summary

Receiver RF Sensitivity	–105dBm@10dB SNR (8.5dB NF@80kHz IF)	*LO Phase Noise*	–101dBc/Hz@100kHz
Total Receiver IIP3	–8.5 dBm	*LO Pulling by PA*	<200 kHz
Total Receiver IIP2	+22 dBm	*LO to RX-in Coupling*	–92 dBm w/ PA off
Channel Filter	220 kHz Passband 57 MHz Stopband	*RX s_{11}* *TX s_{22}*	–11 dB –15 dB
Active RX Current	120 mA	*Frequency Hop Rate*	150 khop/s (max) 20 khop/s (typ)
PA Output Range	–17 to +14 dBm	*Supply*	3 V / 3.5 V
PA Output Noise Floor	–138 dBm/Hz	*Operating Band*	902-928 MHz
Active TX Current	100 mA	*Data Rate*	160 kb/s @ 4-FSK
IC Technology	1μm CMOS p-epi on p^+ substrate	*Active chip area*	10.5×7.3 mm

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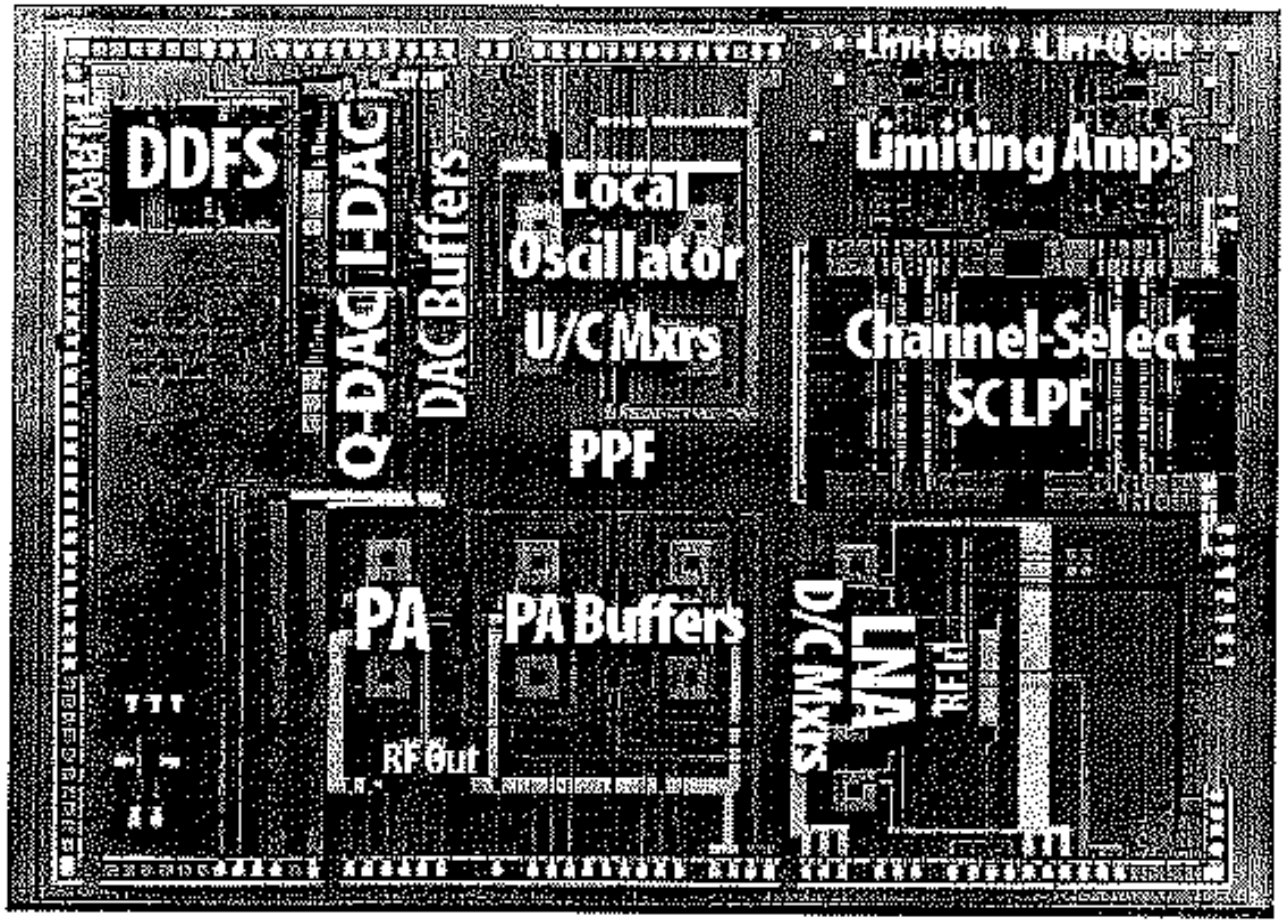
Integrated Prototype

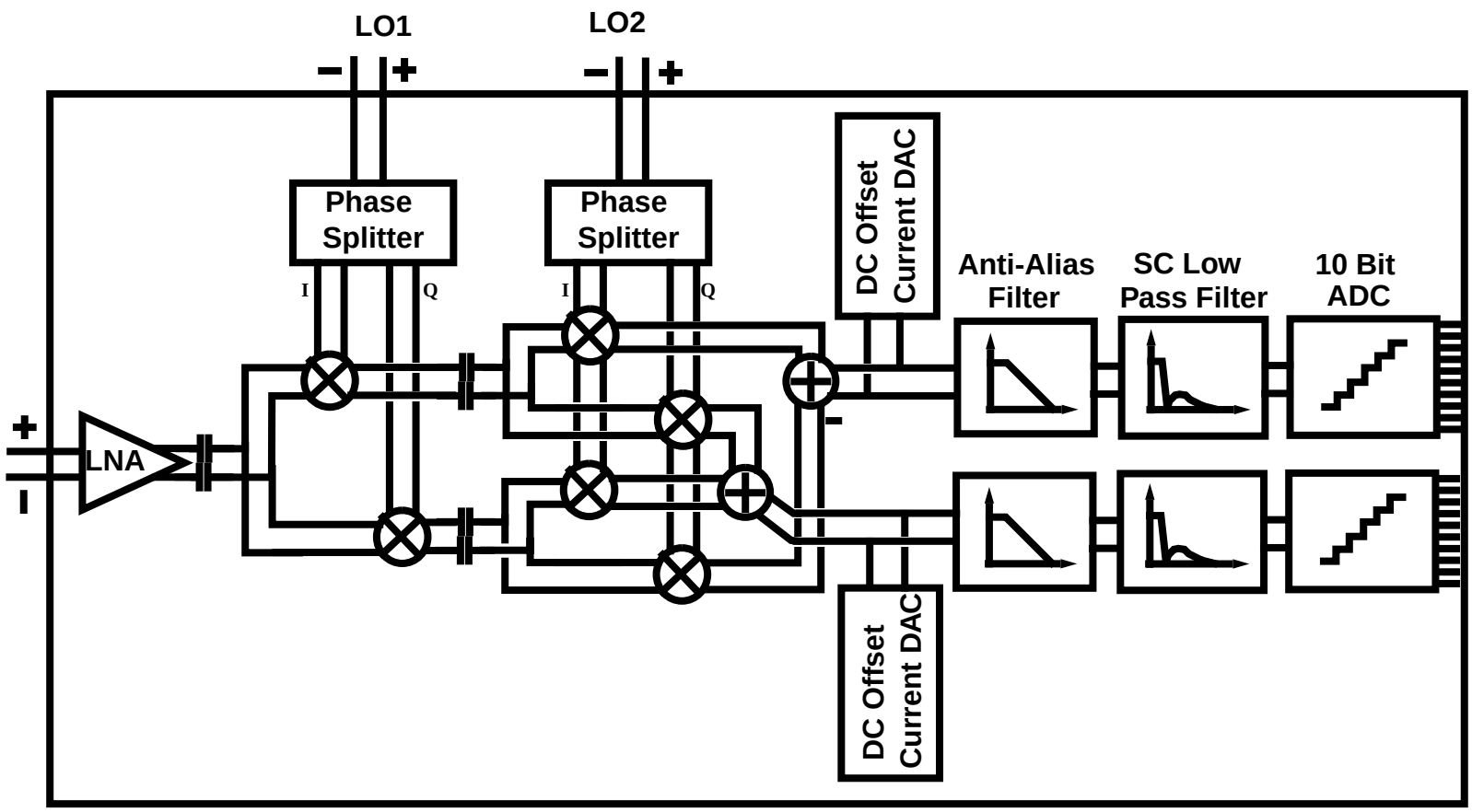


DECT/Multistandard CMOS Adaptive Transceiver Project

Rudell, et al, 97ISSCC

- **1.8Ghz RF Receive Path**
- **Integration of RF, and Baseband Filter/ADC**
- **Wideband Double Conversion Architecture**
- **0.6 Micron Implementation**

Block Diagram, Experimental DECT Receiver



see Rudell, et al ISSCC97

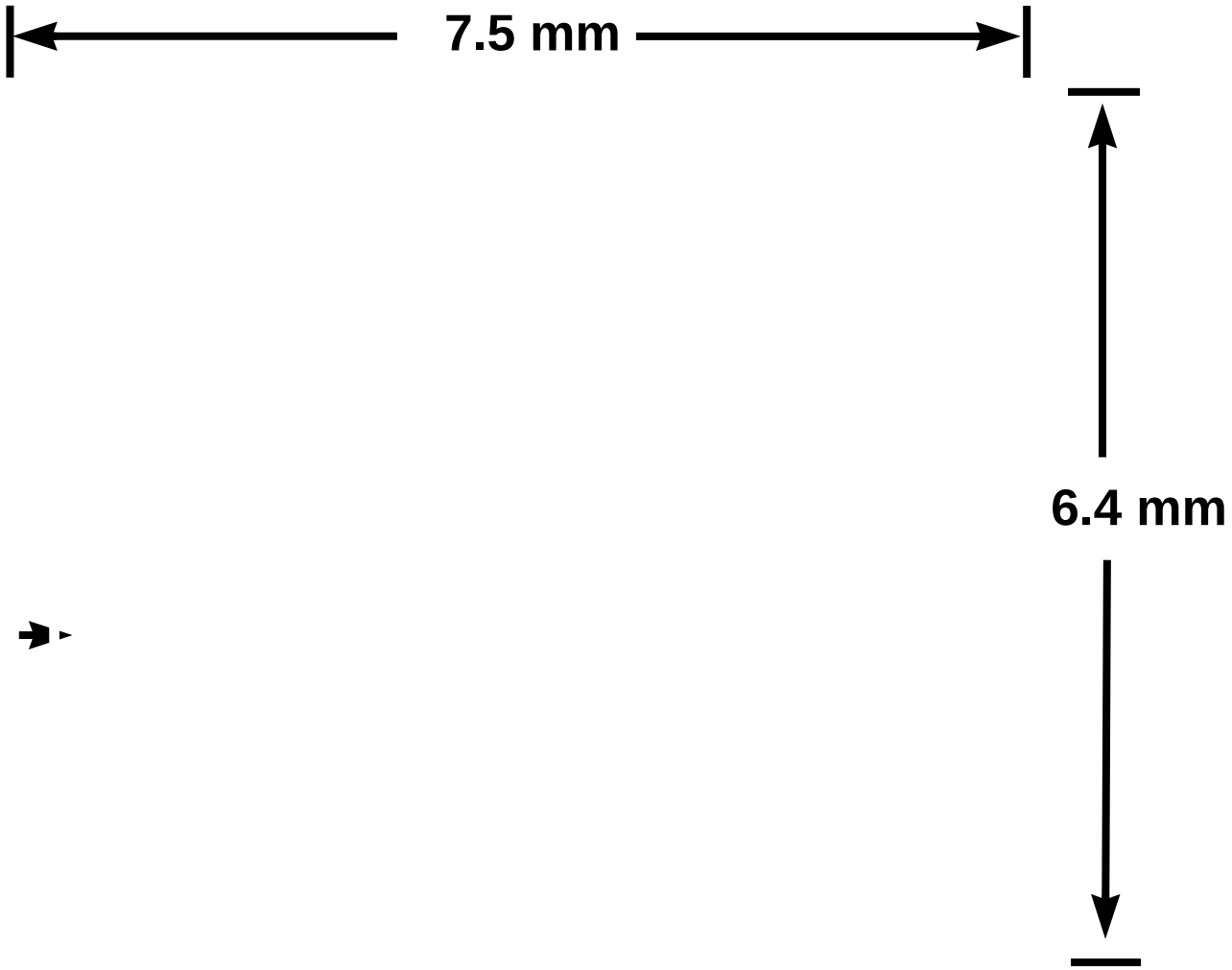
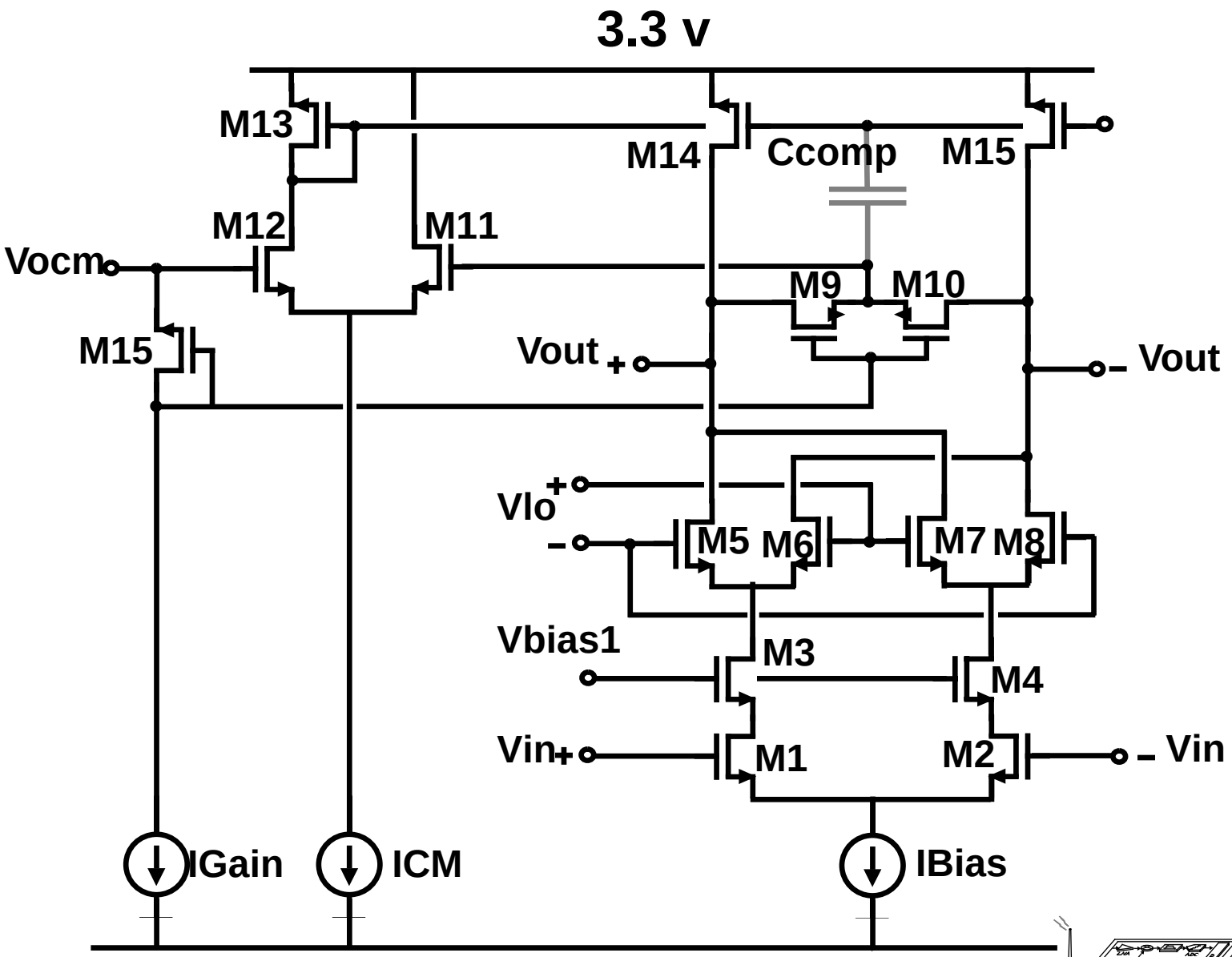
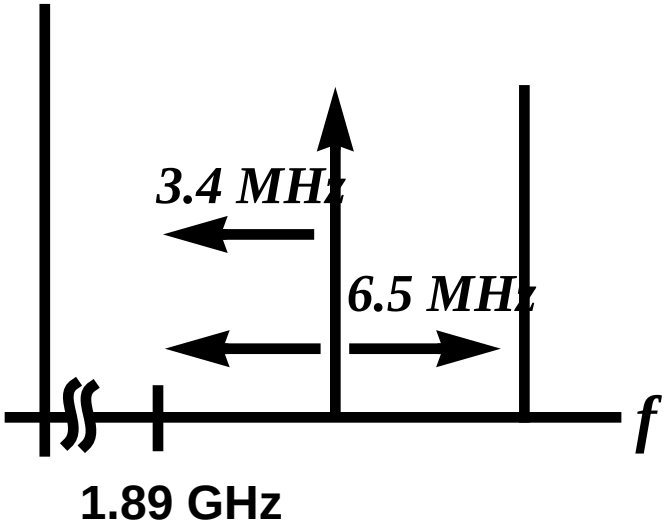


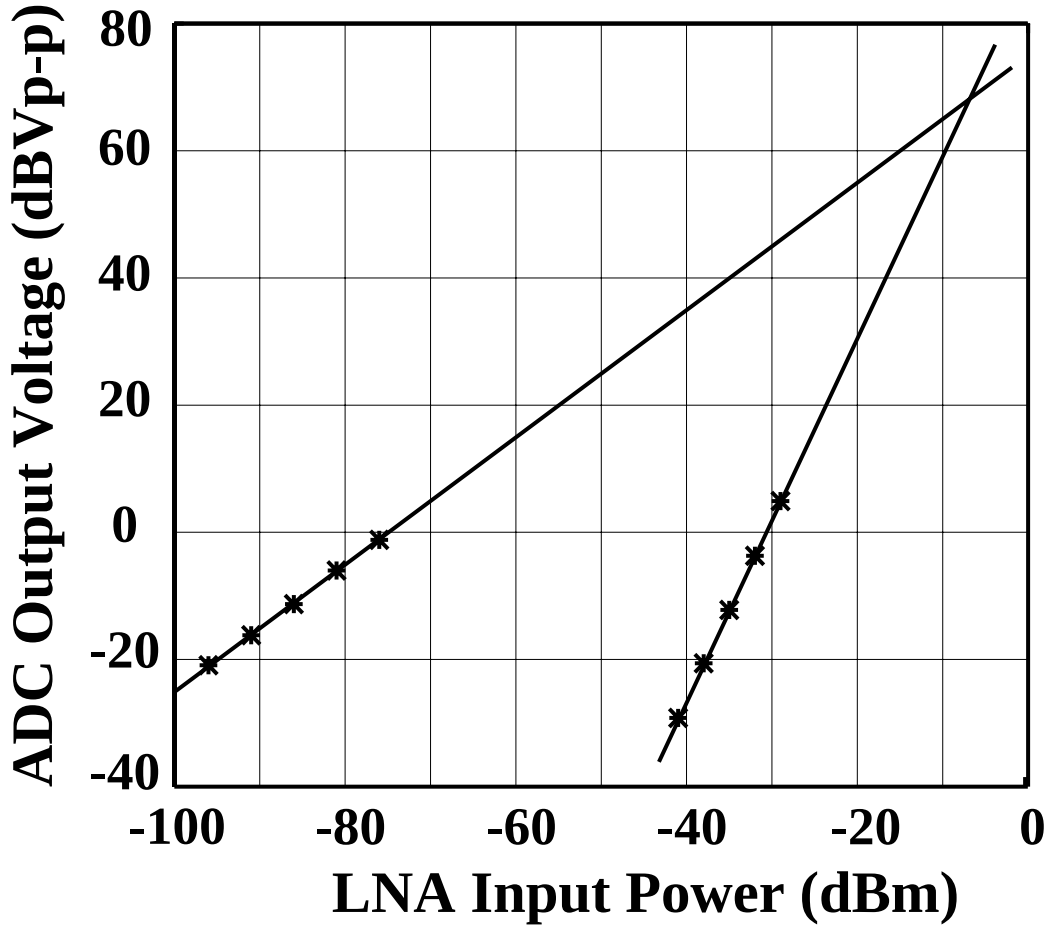
Figure 1: Die Photo

Mixer Implementation



3rd Order Intermodulation

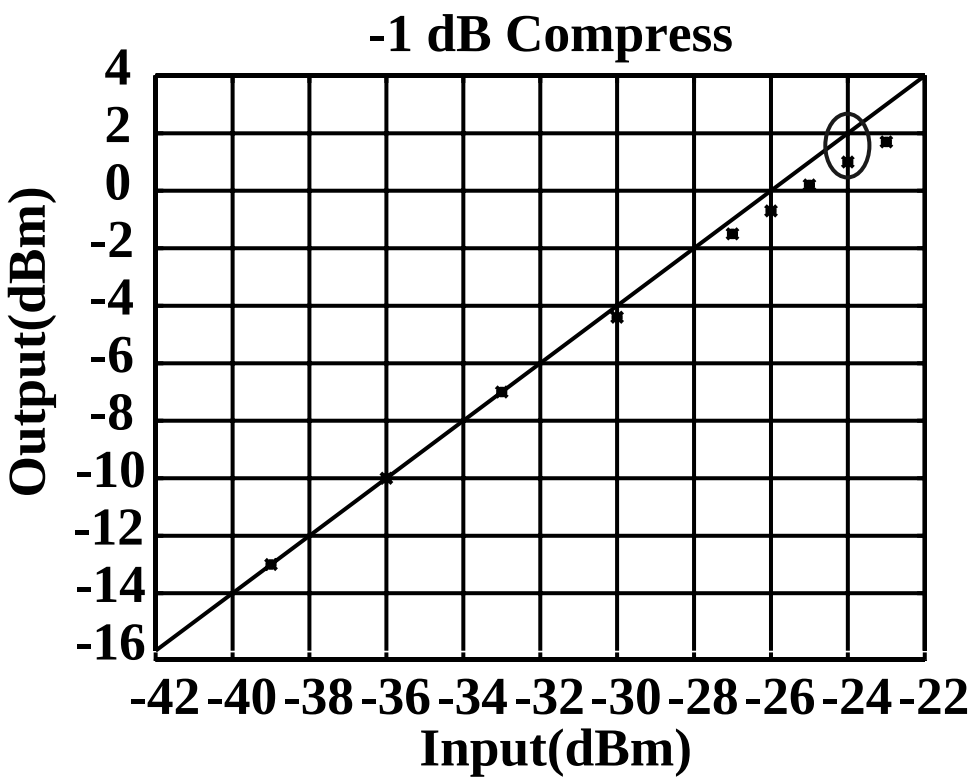




Receiver IP3 of -7dBm referred to the LNA input

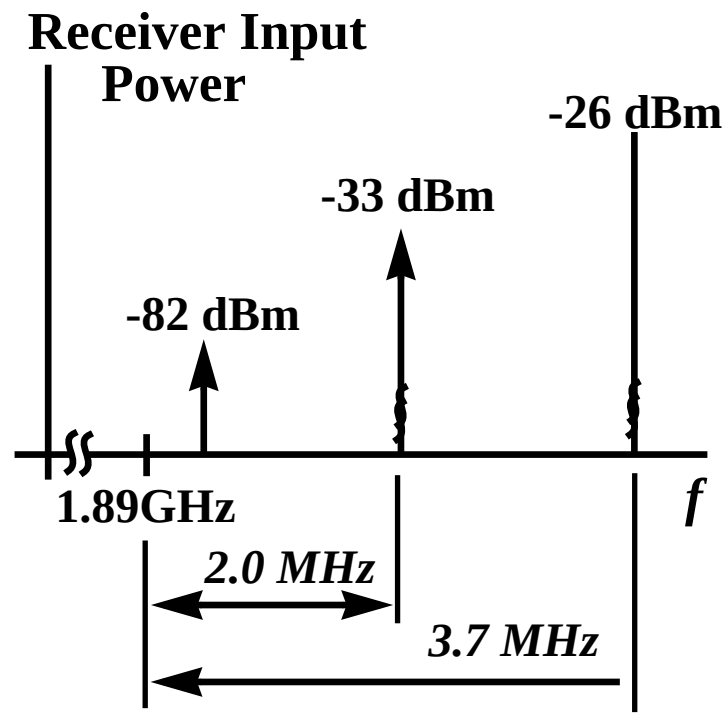
Large Signal Performance

Gain Compression



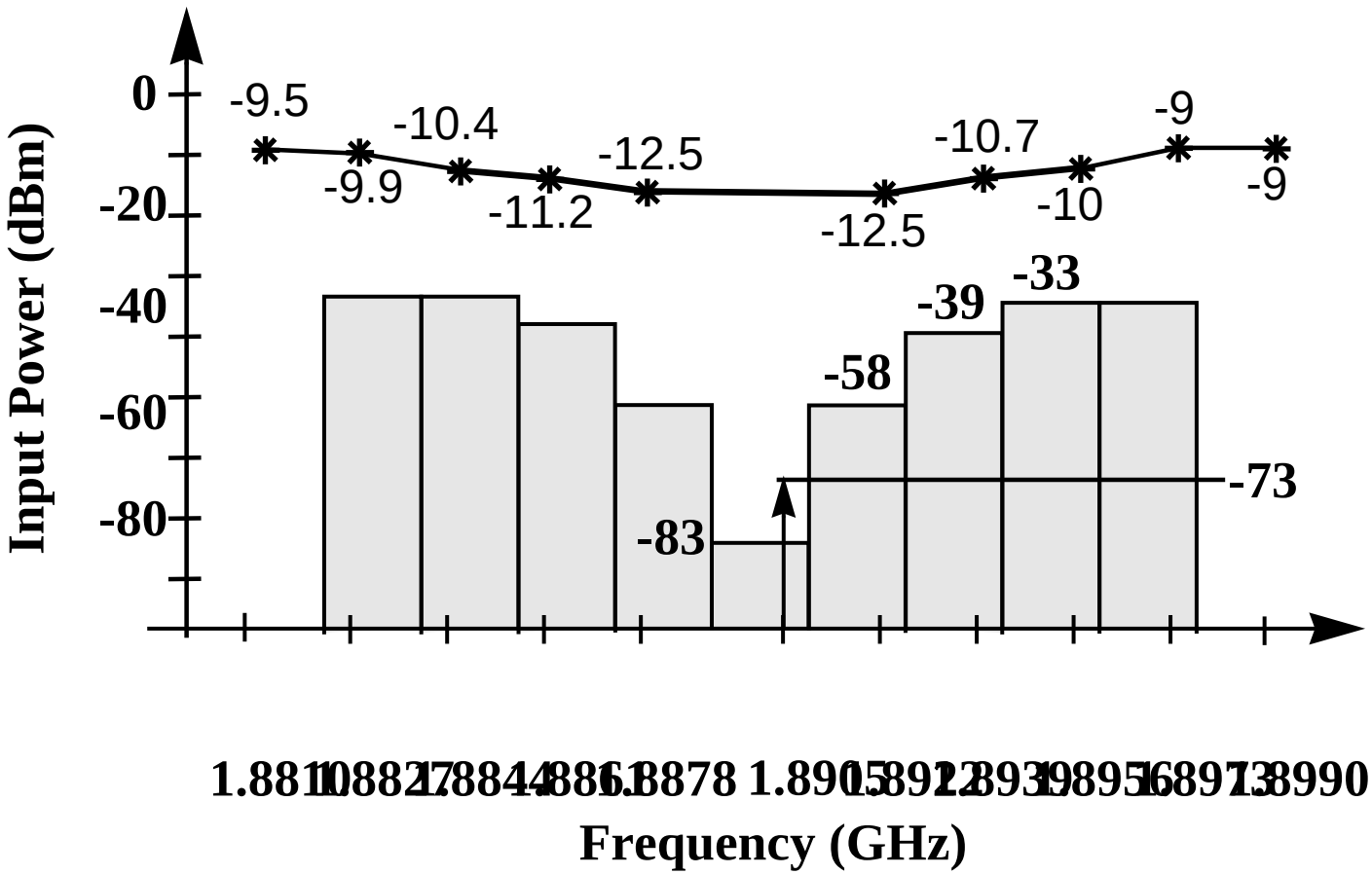
P-1dB = -24 dBm

Out-of-Band Blocking



Pob3dB = -33 dBm

Blocking Performance



DECT blocking requirements.

Desired inband tone used for CNR measurement.

∗ Measured blocker with 10dB CNR for the desired signal.

Image Suppression

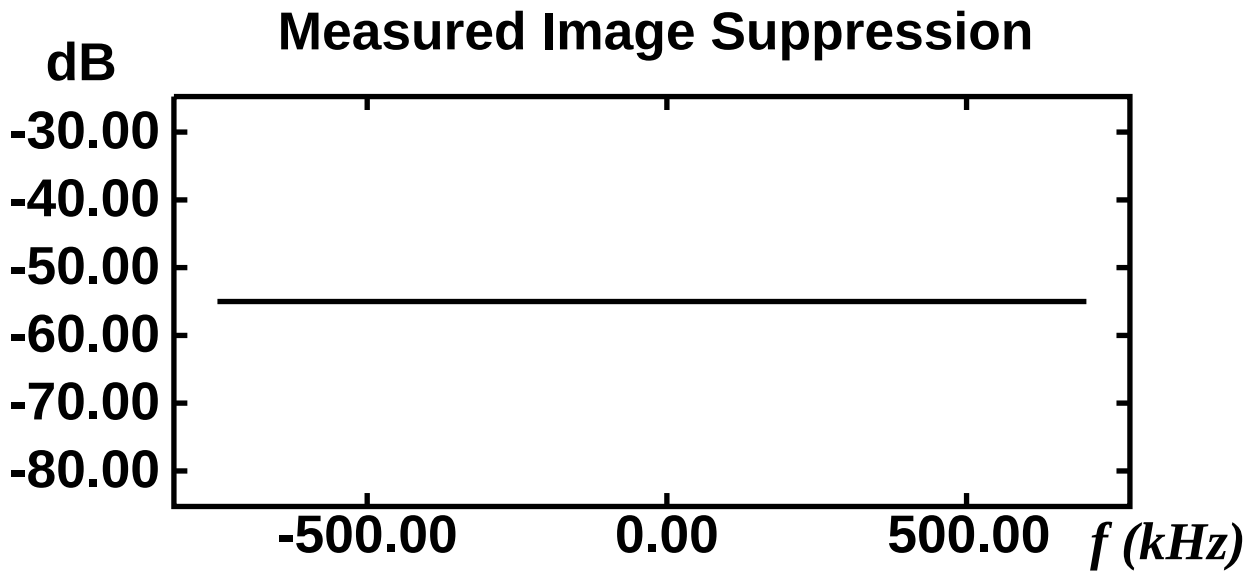


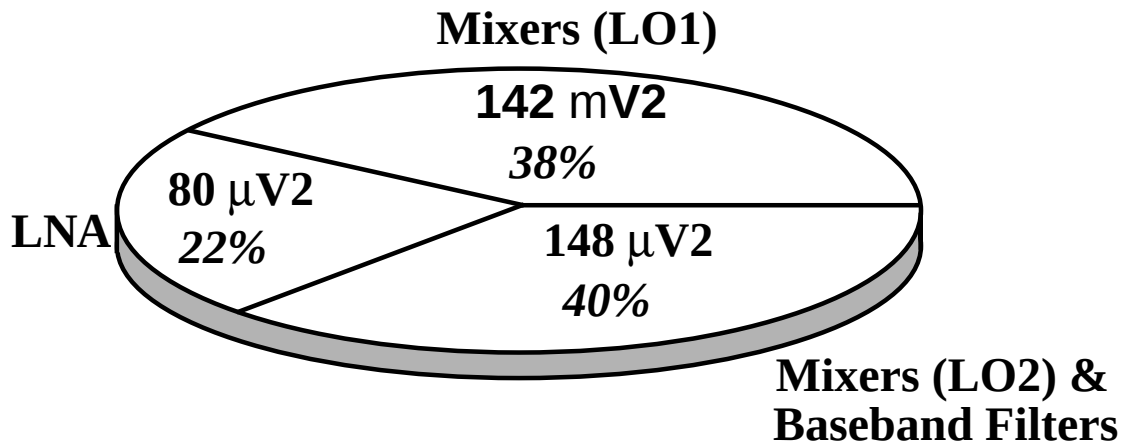
Image-Rejection Contribution

Balun	2dB
LNA	8dB
IR Mixer	45dB
Total IR	55dB

Noise vs. Power Perfor-

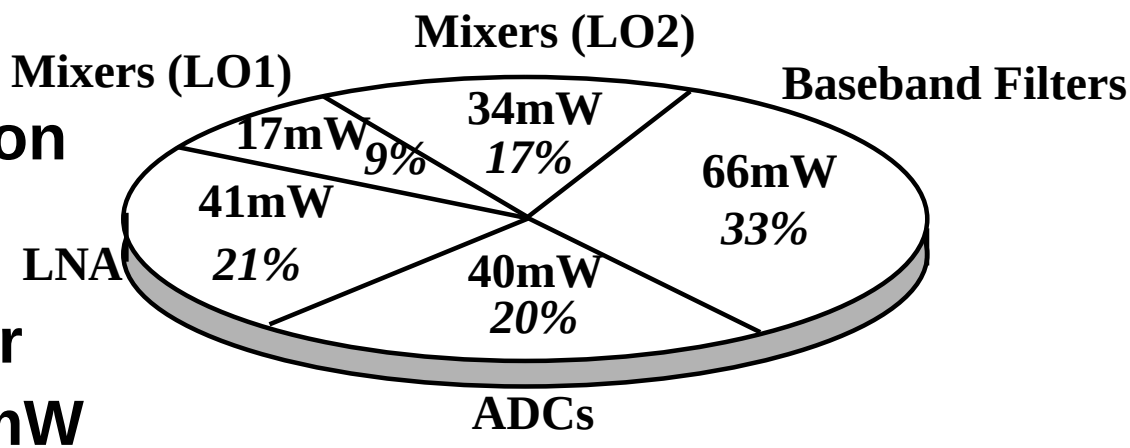
Receiver Sensitivity
-90dBm

Noise Figure
14dB DSB



Total Power Dissipation
198 mW

Power cycled receiver
8% duty cycle = 15.8 mW



Receiver Measured Results

Sensitivity	-90dBm
Input IP3	-7dBm
Pob3dB (Max. gain setting)	-33dBm @ 2MHz
P-1dB (Min gain setting)	-24dBm
Max. Receiver Gain	78dB
Min. Receiver Gain	26dB
Receiver Image Rejection	-55dB
Active Chip Area	15 mm2

Future Directions in RF Transceivers

Old

- Multichip, GaAs, Bip.,CMOS
- Superhet Architecture
- Saw, Ceramic RF,IF Filters
- Varactor Tuned Tank VCOs
- Analog Demodulation
- Single-Standard

New

- Single-chip Scaled CMOS
- Direct, Quasi-Direct Conv
- RF Ceramic Only
- L-C Osc On board
- Digital Baseband Proc.
- Digital Demodulation
- Multi-Standard

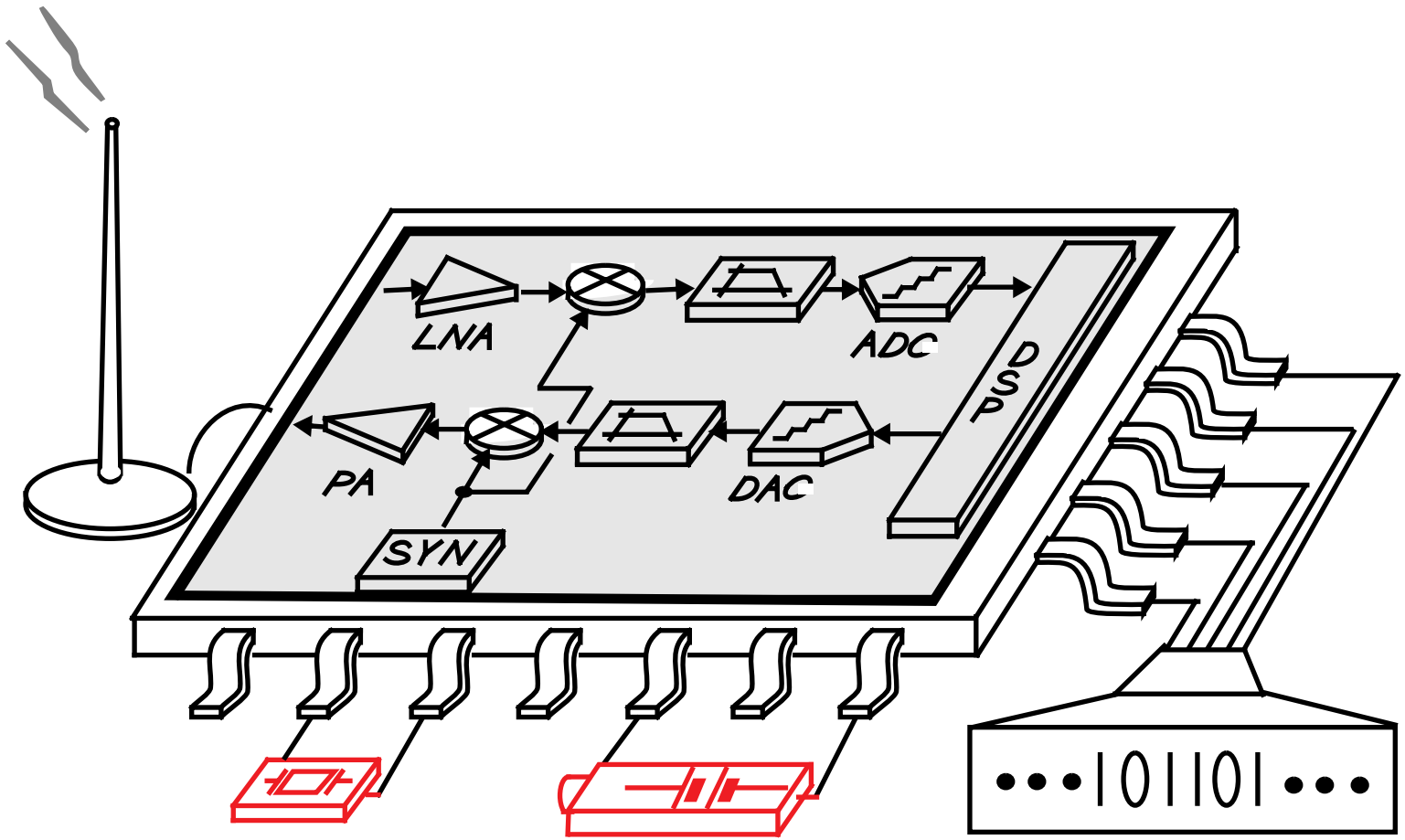
Additional Challenges in High-Integration Multistandard CMOS Transceivers

- Realization of synthesizer phase low enough for Cellular
- Demonstration that on-chip coupling problem can be systematically addressed (CAD tool, layout)
- High-efficiency tuned CMOS Power Amps to 1 Watt
- RF Port Optimization (LNA/PA/Ceramic Resonator/Antenna)

Key Problems for Silicon RF ICs

- Development of CAD tools for package modeling, inductor design, substrate modeling, etc.

- Continued Development of Process Enhancements for on-board high-Q Inductors/resonators/filters

- Exploitation of bands above 2.5Ghz using SiGe or hybrid Si-III-IV approaches

Ultimate Objective: