Silicon RF Technology - The Two Generic Approaches

Joachim N. Burghartz

IBM T. J. Watson Research Center, Yorktown Heights, New York 10598, USA,
E-mail: burgh@watson.ibm.com, Phone: (914)945-3246, FAX: (914)945-2141.

Abstract: *The implementation of a complete RF transceiver system on a single silicon chip is motivated by a rapidly emerging wireless communication market which extends to consumer as well as commercial applications. This paper attempts to identify two generic paths on which the required fabrication processes and device structures can be accomplished. The first approach is conservative and aims for an engineering of the RF functions without altering the existing silicon fabrication scheme. The second, more innovative development path considers the introduction of new materials and process steps in order to overcome the limitations of silicon processes in comparison to hybrid RF technology.*

I. Introduction -- The title of this paper may raise the question, wheather we need to define a new paradigm as we operate circuits on silicon substrates at GHz frequencies. RF transceivers have been successfully implemented on printed circuit boards for years (Fig. 1). This mature technology combines discrete transistors (MESFETs, HEMTs, HBTs on compound semiconductor substrates), lumped-element (spiral inductors, interdigitated capacitors) or distributed components (microstrips) for impedance matching, dielectric resonator filters, quartz crystal oscillators for frequency synthesis, and other elements [1]. The advantages of the printed circuit board design are obvious: it is simple to combine devices which were fabricated by using very different materials to achieve an optimum performance of each component, devices can be individually selected prior to assembly to achieve an optimum parameter set of each component, and post-assembly trimming is easy due to the large size of such an RF system.

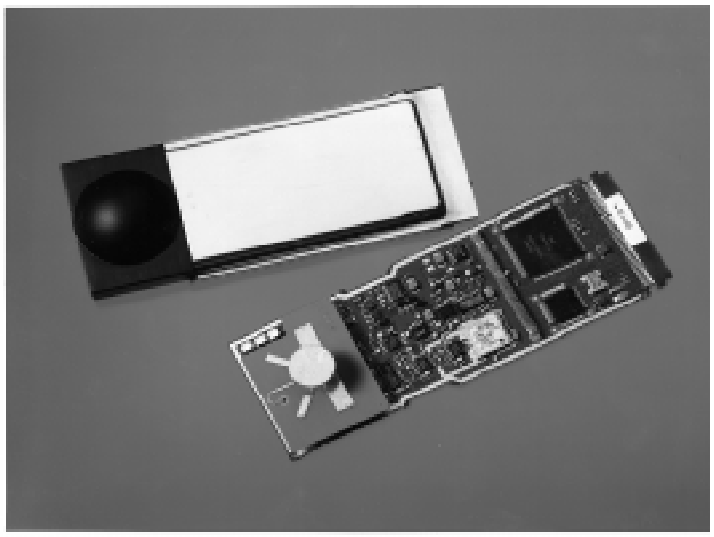

Fig. 1 2.4 GHz PCMCIA local area network adapter (LAN) card in conventional printed board assembly [2],[3].

These features were well suited for the traditional market which was largely focussed on military applications. The new emerging consumer and commercial markets drive other system aspects: the ideal RF transceiver for cellular systems, wide- (WAN), or local-area (LAN) networks is low in cost, small in size, has low power consumption and can be fabricated in large volumes. Those requirements make silicon the pre-eminent technology choice and foster a fully monolithic, i.e. single-chip solution, including all RF building blocks (except the antenna) and the intermediate frequency (IF) circuitry. Certainly, it would be desirable to transfer the extensive experience in printed board RF design directly to silicon, but several marked differences make this development path difficult, if not impossible:

first, many of the discrete components in printed board design have material characteristics which silicon cannot match. The silicon substrate, in particular, is prone to RF losses in contrast to GaAs and printed circuit board [4]. Considerable losses have also to be expected in the interconnects which are typically aluminum (Al) wires combined with tungsten (W) vias, both of limited thickness. Secondly, impedance matching by using microstrips at the currently practical frequencies (900 MHz to 2.4 GHz) is not feasible at silicon chip dimensions. At 2.4 GHz, a quarter wave length (l/4 λ) measures about 1.6 cm while practical chip sizes for RF circuits will most likely not extend beyond 1 cm^2. Finally, the conventional post-assembly trimming techniques are not applicable; the control of the RF silicon device parameters and the interconnects will have to exceed that of the RF discretes, or novel trimming techniques that are compatible with silicon technology will have to be developed. These three differences are the main reason that the conventional RF design concepts cannot directly be transferred to silicon. Some novel RF component structures have to be added to the known silicon technologies to accomplish the desired RF functions, but the techniques of implementing them may be quite different from the established ways.

After this extensive introduction, it becomes obvious that the new challenges associated with the monolithic integration of RF circuits on a silicon substrate justify the introduction of the new paradigm "silicon RF technology". This definition, however, can apply to two generic ways to implement RF functions on a silicon substrate. The first option is a very economic one and focuses on an immediate entry to the RF market: it aims to engineer the required RF components by using the existing fabrication process modules *in different combinations but without any alteration.* The second generic approach considers the introduction of *new, but silicon compatible, process steps and materials* to overcome the mentioned limitations of the lossy substrate and interconnects in standard silicon technology, as well as the introduction of SiGe alloys to improve the active device characteristics.

We will now discuss the various technology areas and describe how the two generic approaches can be applied. First, silicon as an RF substrate and general integration issues will be evaluated in Section II, followed by a qualitative comparison of bipolar and CMOS transistors as active RF devices (Section III). Section IV covers the design and optimization of the RF passive components. The device characterization and modeling issues in silicon RF design will be addressed briefly in Section V. Section VI summarizes the findings and will provide an outlook on trends and open challenges.

II. Silicon as an RF Substrate and General Integration Issues -- At the first view, the properties of silicon seem reasonably suited for use as an RF substrate: the dielectric constant is high and changes little with frequency and temperature, the thermal conductivity is three times that of GaAs, the surface smoothness is excellent, and silicon device integration is mature [5]. The maximum practical resistivity of Czochralski-grown silicon, however, is only about 10 Ω-cm which is several orders of magnitude lower than that of GaAs. At frequencies beyond 1 GHz, the skin depth for 10-Ω-cm silicon exceeds the typical substrate thickness so that RF losses extend over the entire substrate. Resistivities which are about two orders of magnitude higher can be achieved with Float-Zone (FZ) silicon, i.e. high-resistivity (HRS), material, and the previous difficulty in preserving the resistivity after heat treatment could recently be minimized [5]. The wide space-charge regions associated with a low substrate doping, however, limit the integration density significantly if junction isolation is used. An interesting innovative type of substrate, which combines full dielectric isolation through a silicon-on-insulator (SOI) structure with a FZ-silicon substrate, has recently been investigated [6]. Similarly, silicon-on-sapphire (SOS) substrates can be used for even lower RF losses. Another novel approach utilizes bulk-micromachining to remove silicon material under devices which are particularly prone to electromagnetic substrate losses, such as spiral inductors [7]

or transmission lines [8]. Porous silicon formation provides also a way to reduce the substrate losses, but this approach ows yet a practical demonstration in a circuit process [9].

If one decides for the conservative way of integrating RF systems on a silicon chip, one has to cope with the considerable substrate losses, resulting in a relatively high power consumption. This drawback can be partially alleviated, however, by the short distances between RF components on the chip. Also, unlike for discrete device assembly, a match to a 50-Ω impedance is necessary only at the RF output port. Choosing the innovative development path will enable the RF designer to work with RF loss levels that are similar to those in a hybrid system, by using FZ-silicon substrates with SOI device isolation, SOS, or micromachining techniques. This gives the advantage of a much higher integration density at the price of modifying an established silicon fabrication process.

As a result for the high level of integration, crosstalk and thermal cross-coupling will be increasingly important. These concerns exist not only because of the close device proximity on a single chip, but also because parasitic electromagnetic signal propagation through the substrate becomes an additional issue. RF isolation schemes have to be developed for device integration and it is important to recognize that an oxide or junction isolation structure which works satisfactory at dc signal levels may fail in RF operation [10]. Further, silicon has an order of magnitude higher thermal conductivity than oxide. This has an advantage in the design of discrete power amplifiers, but raises the issue of thermal cross-coupling between devices in monolithic transceivers. This is especially a concern if the Power Amplifier (PA) in the transmitter section of the RF transceiver is integrated together with the Low-Noise Amplifier (LNA) of the receiver part on the same chip. It is probably one of the main reasons that currently integrated RF transceivers are offered in the form of chip sets rather than one single chip [11]. The problem can be overcome by using SOI device isolation with a thick buried oxide, which, however, enhances the self-heating of devices [12],[13]. The buried oxide thickness has to be tailored in this case for an optimum trade-off between device self-heating, thermal cross-coupling, and crosstalk. This trade-off can be improved significantly by using a partial instead of a continuous SOI film, but such a structure requires the use of selective epitaxial growth and chemical-mechanical polishing (CMP) [14]. Another innovative approach may come from bulk-micromachining which will allow to remove the silicon locally under devices or circuits, such as the LNA, which dissipate little power and thus are less prone to self-heating, for a better overall isolation [15].

After having addressed many new technical challenges which appear with the monolithic integration of an RF transceiver on silicon, one should highlight one feature of planar silicon process technology that adds a valuable benefit. Multi-level interconnects are a routine part of today's silicon processes. Up to six levels of aluminum (Al) are accomplished at micrometer dimensions, and low-cost processes have at least two metal levels [16]. This allows one to build special RF devices such as spiral inductors, transformers, MIM capacitors, and transmission lines [17]. The reproducibility of the line dimensions and the smooth metal surfaces contribute to an excellent control of the high-frequency parameters. The current progress in silicon interconnect development

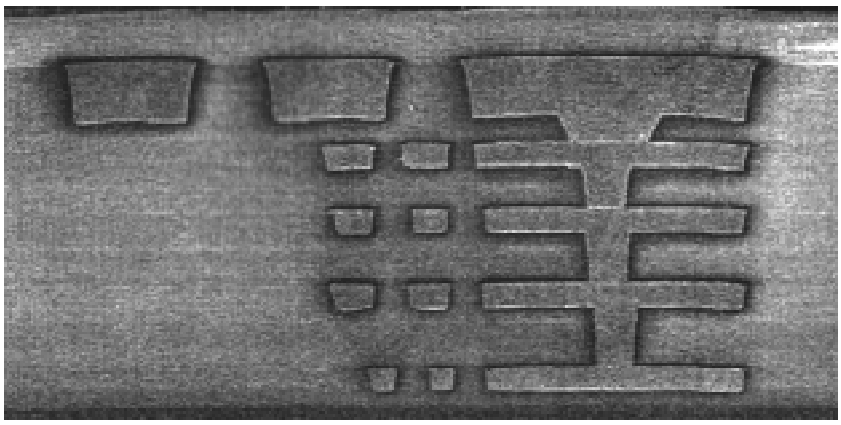

Fig. 2 Cross-section of a five-level Cu-Damascene interconnect structure [18],[19].

may be of further advantage for RF device integration. Advanced multi-level copper interconnect processes, which provide a resistivity reduction by a factor of two and much improved reliability, are at the horizon (Fig. 2), [18]. Details of the fabrication of passive components by using the metal interconnects will be given in Section IV.

III. Bipolar vs. CMOS -- Historically, the bipolar transistor has dominated the high-speed domain, while memories and other high-density circuits were built in CMOS. RF circuits operate at frequencies beyond 1 GHz, so bipolar appears to be the technology of choice for RF applications, but with manufacturable 0.1-μm devices at the horizon, CMOS seems to be a serious candidate as well. In fact, 900 MHz transceiver designs are underway, and RF CMOS systems operating at 2 GHz have been projected [20]. On the other side, bipolar technology has become capable to cope with GaAs due to the advent of SiGe epitaxial growth techniques [21]-[26]. While for digital applications the design of the devices was primarily focused on large-signal switching speed and small device size, a RF design requires sufficient small-signal (ac) amplification at very high frequency, a low minimum noise figure (F_{min}), a high power-added efficiency (PAE) and a high breakdown voltage (for PAs), a good linearity, and other quality aspects of frequency-domain device operation [25]. The transistor speed is typically indicated by the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}); f_{max} can give very different information on device speed depending if it is derived from extrapolation of the maximum available gain (MAG) or the unilateral gain (U) [27].

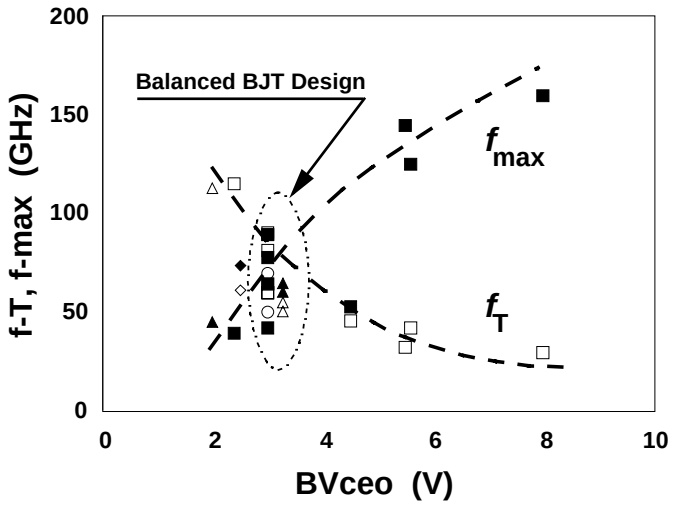

Fig. 3 Cut-off frequency (f_T, open symbol) and maximum oscillation frequency (f_{max}, solid symbols) versus collector-emitter breakdown-voltage (Bvceo) for published Si and SiGe bipolar transistor data [27]-[33].

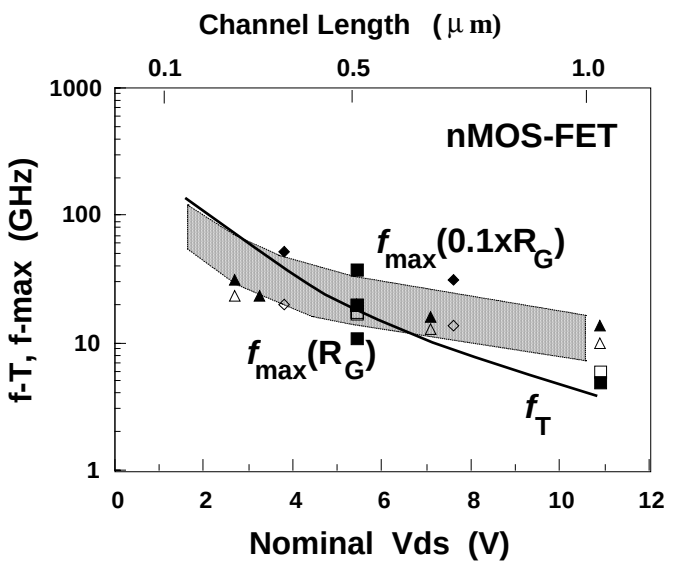

Fig. 4 Cut-off frequency (f_T, open symbol) and maximum oscillation frequency (f_{max}, solid symbols) versus drain-source voltage (V_{DS}) and channel length for published and simulated MOSFETs. The effect of the gate resistance on f_{max} is illustrated [34]-[44].

We will now make an attempt to assess bipolar (BJT and SiGe-HBT) and CMOS device performance for RF application. For that purpose, we have plotted the f_T and the f_{max} values of published devices and of device simulations versus BVceo and V_{DS} in Figs. 3 and 4, respectively. It is obvious that the trends of f_T and f_{max} are quite different for the two types of devices. Those frequencies vary for the BJT as a function of collector and base dopings and widths with opposite trends (Fig. 3), i.e. very high values can be achieved for f_T [33] or f_{max} [27] at the expense of the other figure. A balanced SiGe transistor design provides f_T and f_{max} values of about 60-80 GHz at a BVceo of about 3 V [27]-[32]. For the

nMOSFETs in Fig. 4, both frequency limits increase as the device is scaled down. A channel length of about 0.15 μm is required to match the f_T and f_{max} of the SiGe bipolar transistors, but at a supply voltage of only 1.5 V. The low supply bias is of advantage for low-power operation. Very high f_T and f_{max} numbers at low bias have recently been demonstrated for SiGe-MODFETs, indicating one way to improve MOS technology for RF application through process innovation [45]. It will be explained further below, however, that a low supply voltage may cause difficulty in power amplifier design. Another way to improve the RF performance of a MOS transistor through process modification is to reduce the gate resistance, as indicated in Fig. 4. f_{max} can be increased significantly, or the same f_{max} may be achieved for a longer channel and higher supply voltage, if the FET is fabricated with a T-gate structure, which can reduce the gate resistance by a factor of fourty [39]. Gate resistance minimization is also possible to some extent by using multi-finger FETs, i.e. without any process alteration [36].

Besides the device speed, the noise which is generated by a transistor, relative to the associated gain is an important figure-of-merit. In Fig. 5 the Gain is drawn *versus* the minimum noise figure (F_{min}) at 2 GHz for nMOSFETs with different channel lengths, for SiGe-HBTs, and for a self-aligned BJT. It becomes obvious that both the noise figure and the gain improve towards smaller channel length. Best results were published for nMOSFETs with channel lengths below 0.2 μm. If one compares at the same lithographic minimum line dimension, the SiGe-HBT is superior to the MOS device, as well as to the BJT. From the earlier device speed evaluation and from the noise performance comparison, one can conclude that the SiGe-HBT is a very attractive candidate for RF applications and is superior to the MOSFET. CMOS, however, is the silicon mass production technology today, and if CMOS meets the performance requirements for an RF application, it will be the technology of choice. At present, an upper frequency limit of 2 GHz is projected for CMOS [20], while SiGe-HBT technology may find preferred application above 5 GHz. It should be pointed out, however, that for specific applications one device type may dominate more clearly over the other. For instance, RF power switches are preferably built by using MOS devices due to the low standby power level [50]. In contrast, bipolar transistors have advantages in power amplifier design, because they offer high speed at sufficiently high voltage, while the MOSFET, and so the supply voltage, have to be scaled down in order to provide adequate ac performance. For a large power level and at a high operating frequency, the MOS transistor is operated at a considerably larger current than a BJT. Further, the MOSFET needs to be sized in proportion to the required current. The large current may cause considerable voltage drops along the interconnects at low supply voltage, thus degrading the PAE of the device. Higher PAE values can therefore be expected for BJTs and SiGe-HBTs. Obviously, the ideal RF fabrication process would provide both CMOS and bipolar transistors on the same chip, provided that the integration does not lead to detrimental performance trade-offs. A recent comparison of state-of-the-art BiCMOS technologies has shown that several companies offer today fabrication processes which provide transistors that are comparable in performance to those fabricated using CMOS or bipolar stand-alone processes [51]. The paper explains further, that in high-performance BiCMOS many process steps and structural

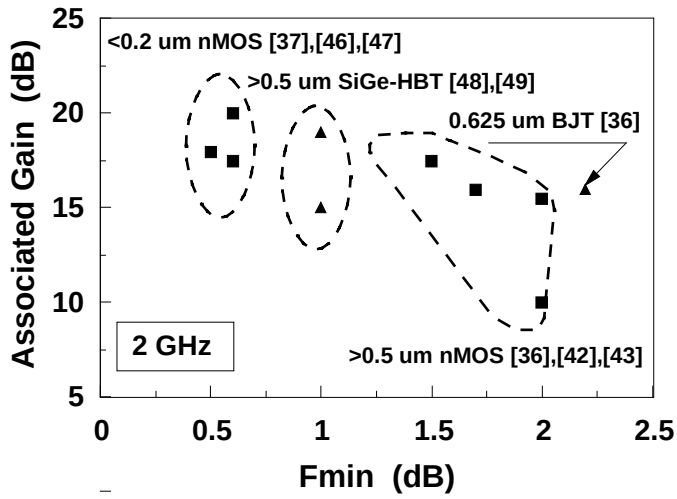

Fig. 5 Associated gain versus minimum noise figure of various published MOSFETs, BJT, and SiGe-HBTs.

elements are shared between the two types of devices, making the cost overhead more acceptable than in the early years of BiCMOS. It is the authors belief that for these reasons BiCMOS or SiGe-BiCMOS [48], will be the preferred technology for future single-chip High-Tier PCS systems, while CMOS may lead in Low-Tier PCS [52].

IV. Passive Components - The Bottleneck -- Little attention has historically been given to passive components in comparison to the active devices, with the exception of DRAMs and specialized technologies. CMOS can be managed without any passives, while bipolar technology suffices with resistors in the simplest case. The new focus on silicon RF technology changes this picture dramatically. The circuit operation at GHz frequencies requires impedance matching between circuit building blocks. Thus devices which are new to silicon technology, like inductors, transformers, varactors, and transmission lines are needed [17]. The optimization of these components is focused on maximizing the quality factor (Q) through a reduction of the resistive losses and the capacitive or inductive parasitics, depending on the type of device.

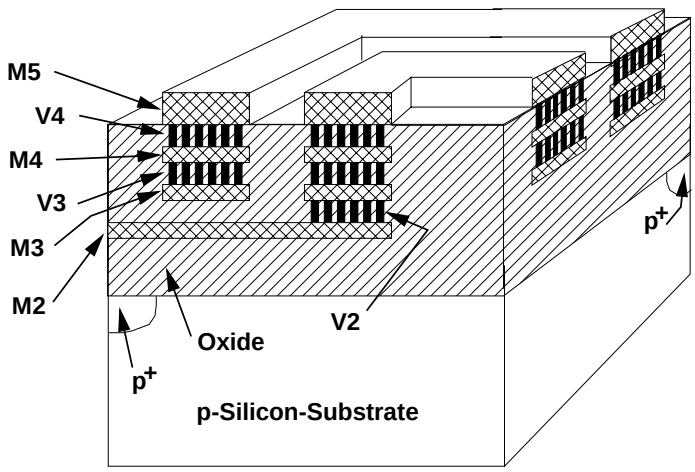

Fig. 6 Cross-sectional view of a spiral inductor fabricated in a 5-level Al interconnect process [57].

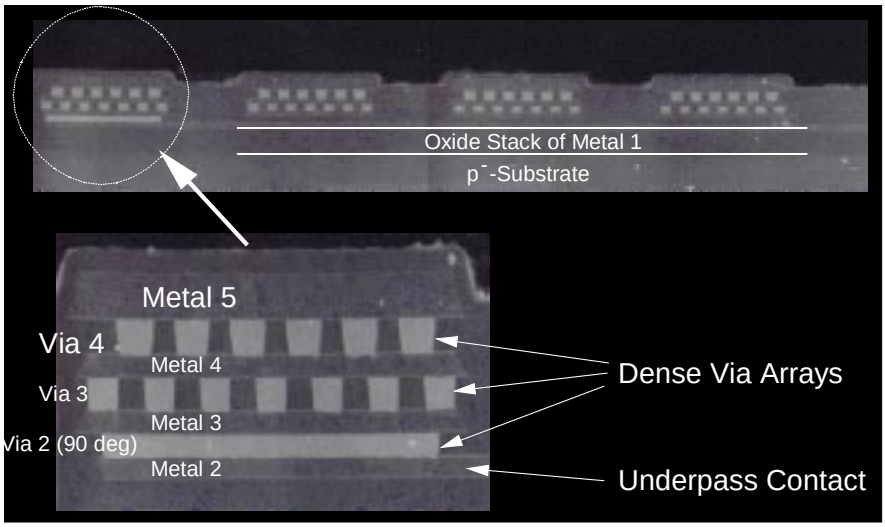

Fig. 7 SEM cross-sectional view along the center line of the spiral inductor structure shown in Fig.6 [57].

Spiral inductors on silicon have been demonstrated with useful Qs only recently [53], and a great deal of effort is currently underway to further optimize this device [17], [53], [55]-[60]. The integration of a spiral inductor on silicon is a challenge because significant RF losses occur in the substrate (see Section II) and in the Al conductor. Fortunately, the development of multi-level interconnects has been pursued with great urgency due to the increasing importance of wire *RC* delays and increasing circuit complexity [54]. Such interconnect structures can be exploited by shunting several metal layers in parallel to overcome the limitation in metal thickness, given by the small interconnect pitch in VLSI technology (Fig. 6) [55], [56]. The substrate losses can be reduced by spacing the spiral coil structure away from the silicon substrate. This has been achieved by building the spiral coil and the

underpass contact of the device at the upper metal levels, leaving out one or several of the lowest metal levels [57]. In the inductor in Fig. 6, the coil was formed by shunting the metal layers M3, M4, and M5 in parallel to reduce the metal ohmic losses, and the layer M1 was omitted to reduce the substrate losses. A cross-sectional view of the fabricated device is shown in Fig. 7. It is highlighted there that the via arrays connecting the three metal layers of the spiral coil are placed with the utmost density in order to achieve the highest possible Q [56], [57]. Besides the conventional planar coil structure discussed so far, it is possible to build stacked coils in multi-level interconnects. This can lead either to a solenoidal inductor structure, which provides a larger inductance for a given area [58], or to transformer structures which can be useful in RF circuits for impedance matching [57].

The inductor implementations discussed so far follow the first, conservative development path to RF circuit integration [17], [55]-[58]. Several other activities are underway which attempt to introduce new process steps, structural features, or materials to silicon processing in order to achieve further improvement of the inductor-Q [6]-[8], [44],[59],[60]. The ohmic losses in the spiral coil can be reduced by replacing aluminum with a less resistive metal,
such as gold (Au) or Cu, and by increasing the thickness of the interconnect layers [59],[60]. Besides generating sufficient spacing of the inductor coil from the substrate, high-resistivity silicon [59],[60], suspension of the inductor structure [7], sapphire substrates [60], or porous silicon [9] can be applied to reduce the substrate losses. The highest Q for inductors fabricated in a manufacturing process to date is 24 [57]. An inductor with the same lateral dimensions but built in a Cu-Damascene process over a sapphire substrate has a Q of 40, which is presently the overall highest Q demonstrated in silicon technology [60]. Fig. 8 shows a summary of various inductor results achieved at IBM over the past three years. The chart visualizes that useful Qs were achieved already with three Al-levels, with clearly increasing Qs as metal layers were added. The combination of Cu-interconnects and sapphire substrates has resulted in a 4x improvement over an Al structure on bulk-Si with the same number of levels. It is also obvious that large inductances have lower Qs than

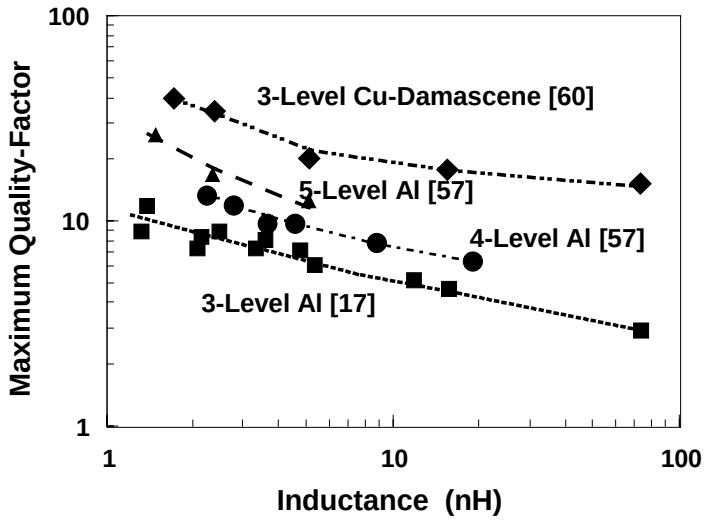

Fig. 8 Quality-factor versus inductance for inductors fabricated in different IBM silicon technologies.

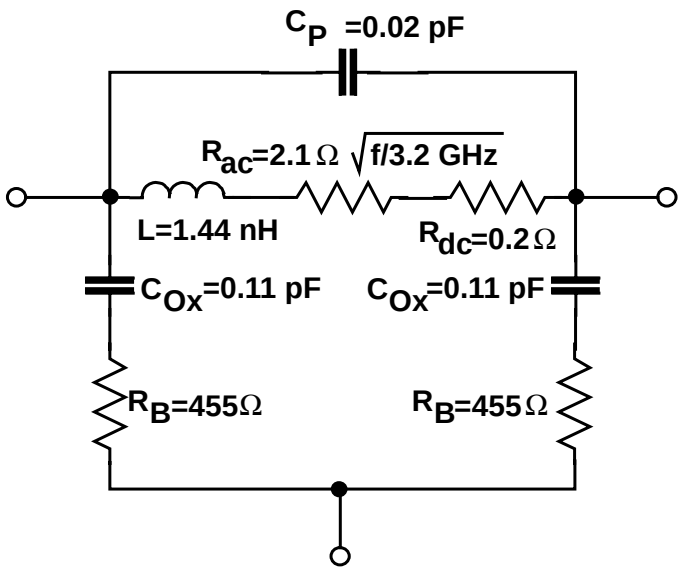

Fig. 9 Lumped-element model of an 1.5 nH spiral inductor fabricated in a 3-level Al interconnect technology [17].

small inductances. This has been explained as the result of the capacitance between coil and substrate, which does not change in proportion to the number of turns for a given area [17],[57]. Fortunately, high Qs in combination with small inductances are required at high frequencies, whereas smaller Qs are sufficient at low frequencies at which large inductances are needed. Since the maximum Q also appears at higher frequencies for smaller inductances, one can conclude that the spiral inductor on silicon is to first order scaleable with the operating frequency.

Other passive RF components, such as metal-insulator-metal (MIM) capacitors, varactors, and transformers, have been investigated over the past few years as well [17],[57]. The associated Qs were found to be significantly larger than those of inductors, making the spiral inductor the performance limiting passive element in silicon rf technology. Therefore, we have restricted ourselves in this paper to the discussion of this device.

V. Characterization and Modeling -- Device modeling may become ultimately the most important issue in silicon RF circuit design and fabrication. Unlike in hybrids, where post-assembly trimming is routinely used, the device parameters have to be accurately predicted and controlled through statistical modeling techniques. High-frequency measurements are generally required for active and passive device parameter extraction to establish the characteristic S-parameters which are needed for impedance matching. An example is given below for the spiral inductor. The high-frequency characteristics of the device can be described by the lumped-element model in Fig. 9. In this model, the spiral coil structure is represented by the ideal inductance L, the series resistances R_{dc} and R_{ac}, and an interwire capacitance C_P. R_{ac} describes the frequency-dependent resistance change due to the skin effect in the coil conductor and in the substrate [61]. The oxide capacitance between the spiral coil and the substrate is given by C_{ox}, and the substrate resistance by R_B. Eventhough the elements in the model are not exactly physical (e.g. R_{ac}), the agreement between measurement and simulation is excellent as shown in Fig. 10. Similar degrees of accuracy can be achieved for the capacitors and varactors [17],[57]. The lumped-element models have successfully been used in RF circuit design [62],[63]. For most devices, such models allow to extrapolate accurately to other device dimensions, which appears to be insufficiently exact for spiral inductors and transformers. Extensive efforts in predictive analytical inductor modeling are therefore underway [64]-[67].

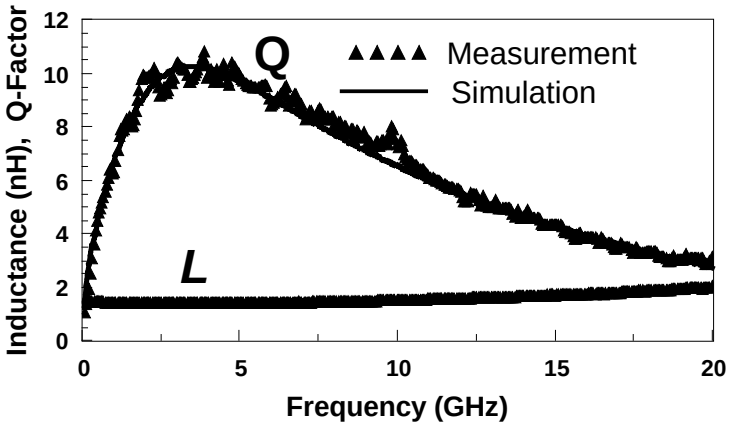

Fig. 10 Comparison of the measured inductance and Q to the simulated characteristics using the model in Fig.9 as a function of frequency [17].

Similar modeling challenges as for the inductor exist for transmission lines on silicon substrates. Ohmic losses dominate at low frequencies, while at high frequencies the transmission line suffers from dielectric losses [68]. The ohmic losses cannot easily be reduced by widening the conductor because it has to be sized for a given impedance, and the skin effect can be significant at high frequency [61]. Approaches to reduce the ohmic losses include the use of Au [59],[69],[70] and Cu [71]. The dielectric and substrate losses can be lowered by using high-resistivity silicon [71],[72], SOS substrates [71], or micro machining techniques [73]. Another very effective, but less silicon-compatible approach takes advantage of the fact that the silicon substrate can almost entirely be

depleted if the conductor is brought in contact with very high-resistive silicon [72]. A problem with this type of transmission line may be that its characteristics are sensitive to variations of the substrate doping [68] and that the structure may generate crosstalk through the substrate because the high-resistive substrate does not serve well as a ground plane. The crosstalk effects can be reduced and the impedance matching can be improved by using microstrips or coplanar waveguides to contain the RF signal [74],[75]. Multi-level interconnects provide a simple way to build these two types of transmission lines, but with certain limitations. The microstrip is prone to high losses due to the narrow vertical dimensions, and thus required narrow metal lines, in planar technology, and the coplanar waveguide requires excessive real estate. Microstrip losses can be somewhat reduced by using Au over thick polyimide insulator as the top level of the interconnect structure [48], and smaller losses of the coplanar waveguide can be achieved in the same way as for the ordinary transmission line discussed above [71]-[73]. Typical losses at 2 GHz range from 15 dB/cm for Al lines over substrates as used for CMOS [73] to 1-2 dB/cm for Cu lines over HRS substrates [71] and Al over micromachined substrates [73], about 0.1 dB/cm for thick Au layers over HRS with very low doping [72], and <0.1 dB/cm for Au conductors in direct contact with HRS [72].

VI. Summary and Outlook -- In this paper we have presented our view of the developments in process integration of silicon RF systems as they may occur over the coming years. Possible directions in integration concepts, active and passive device design, and device and interconnect modeling were highlighted. Two generic paths have been identified on which RF silicon integration processes may evolve. In the early stage, integration which utilizes presently available process steps and materials may be the preferred choice. We have shown that in spite of this restriction most of the required RF components can be engineered by using existing process steps in new ways. As the RF market emerges, novel process steps, materials, and device structures are likely to be introduced to silicon in order to improve the quality of the RF components and so the performance of the integrated RF system. In light of the new ways of utilizing the established silicon processes and the potential innovations, “silicon RF technology” qualifies as a new paradigm.

Acknowledgement

The author wishes to acknowledge Khalid Ismail and Mehmet Soyuer for valueable discussions and a careful reading of the manuscript, as well as his colleagues Keith Jenkins, Brian Gaucher, Young Kwark, Herschel Ainspan, Jean-Olivier Plouchart, and John Ewen for stimulating discussions and support.

References

[1] R. A. Pucel, “Design Considerations for Monolithic Microwave Circuits”, IEEE Trans. Microwave Theory and Techn., vol. MTT-29, no. 6, pp. 513-534, 1981.

[2] B. Gaucher, personal communication.

[3] W. O. Camp, A. Fieek, W. Nunnery, R. Yeager, M. Bracco, “Low Cost BPSK 2.4 GHz Radio for Wireless LAN”, Dig. 6th Symposium on Wireless, pp. 33-43, 1996.

[4] A. C. Reyes, S. M. El-Ghazaly, S. Dorn, M. Dydyk, D. K. Schröder, “Silicon as a Microwave Substrate”, Dig. Symp. on Microwave Theory and Techn., pp. 1759-1762, 1994.

[5] S. R. Taub and S. A. Alterovitz, “Silicon Techologies adjust to RF Applications”, Microwaves&RF, vol. 33, no. 10, pp. 60-74, 1994.

[6] A. K. Agrawal, M. C. Driver, M. H. Hanes, H. M. Hobgood, P. G. McMullin, H. C. Nathanson, T. W. O’Keefe, T. J. Smith, J. R. Szendon, R. N. Thomas, “MICROX - An Advanced Silicon Technology for Microwave Circuits up to X-Band”, Techn. Dig. IEDM, pp. 687-690, 1991.

[7] J. Y.-C. Chang, A. A. Abidi, M. Gaitan, “Large Suspended Inductors on Silicon and their Use in a 2-mm CMOS RF Amplifier”, IEEE El. Dev. Lett., vol. 14, no. 5, pp. 246-248, 1993.

[8] V. Milanovic, M. Gaitan, E. D. Bowen, M. E. Zaghloul, “Micromachined Coplanar Waveguides in CMOS Technology”, IEEE Microwave and Guided Wave Lett., vol. 6, no. 10, pp. 380-381, 1996.

[9] Y. Xie, M. Frei, A. Becker, C. King, D. Kossives, L. Gomez, “An Approach for Fabricating High Performance Inductors on Low Resistivity Substrates, BCTM 1997, to be published.

[10] K. Joardar, “Signal Isolation in BiCMOS Mixed Mode Integrated Circuits”, Proc. BCTM, pp. 178-181, 1995.

[11] W. Kilgore, A. Petrick, D. Schultz, “Four-Chip Set Supports High-Speed DSSS PCMCIA Applications”, RF Design, pp. 42-51, October 1995.

[12] P. R. Ganci, J.-J.J. Hajjar, T. Clark, P. Humphries, J. Lapham, D. Buss, “Self-Heating in High-Performance Bipolar Transistors Fabricated on SOI Substrates”, Techn. Dig. IEDM, pp. 417-420, 1992.

[13] K. Kato and K. Taniguchi, “Numerical Analysis of Switching Characteristics in SOI MOSFET’s”, IEEE Trans. El. Dev., vol. 33, pp. 133-139, 1986.

[14] J. N. Burghartz, R. C. McIntosh, C. L. Stanis, “A Low-Capacitance Bipolar/BiCMOS Isolation Technology, Parts I and II, IEEE Trans. El. Dev., vol. 41, no. 8, pp. 1379-1395, 1994.

[15] H. Baltes, O. Paul, J. G. Korvink, M. Schneider, J. Buehler, N. Schneeberger, D. Jaeggi, P. Malcovati, M. Hornung, A. Haeberli, M. von Arx, F. Mayer, J. Funk, “IC MEMS Microtransducers”, Tech. Dig. IEDM, pp. 521-524, 1996.

[16] S. Wolf, “Silicon Processing for the VLSI Era, Volume 2 - Process Integration”, Lattive Press, 1990.

[17] J. N. Burghartz, M. Soyuer, K. A. Jenkins, M. Kies, P. Dolan, K. Stein, J. Malinowski, D. L. Harame, “RF Components Implemented in an Analog SiGe Bipolar Technology”, Proc. BCTM, pp. 138-141, 1996.

[18] D. C. Edelstein, “Advantages of Copper Interconnects”, Proc. 10th Intern. VLSI Multi-Level Interconn. Conf., pp. 301-307, 1996.

[19] D. Edelstein, personal communication.

[20] A. A. Abidi, “CMOS-only RF and Baseband Circuits for a Monolithic 900 MHz Wireless Transceiver”, Proc. BCTM, pp. 35-42, 1996.

[21] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbé, G. J. Scilla, E. De Frésart, J. M. C. Stork, J. Y.-C. Sun, D. L. Harame, J. N. Burghartz, “75-GHz f_T SiGe-Base Heterojunction Bipolar Transistors”, IEEE El. Dev. Lett., vol. 11, no. 4, pp. 171-173, 1990.

[22] E. Kasper, A. Gruhle, H. Kibbel, “High-Speed SiGe-HBT With Very Low Base Sheet Resistance”, Techn. Dig. IEDM, pp. 79-81, 1993.

[23] F. Sato, H. Takemura, T. Tashiro, H. Hirayama, M. Hiroi, K. Koyama, M. Nakamae, “A Self-Aligned Selective MBE Technology for High-Performance Bipolar Transistors”, Techn. Dig. IEDM, pp. 607-610, 1990.

[24] J. N. Burghartz, T. O. Sedgwick, D. A. Grützmacher, D. Nguyen-Ngoc, K. A. Jenkins, “APCVD-Grown Self-Aligned SiGe-Base HBTs”, Proc. BCTM, pp. 55-62, 1993.

[25] C. A. Liechti, “Microwave Field-Effect Transistors - 1976”, IEEE Trans. Microw. Theory Techn., vol. 24, no. 6, pp. 279-299, 1976.

[26] S. M. Sze, “Physics of Semiconductor Devices”, Wiley&Sons, 1981.

[27] A. Schüppen, U. Erben, A. Gruhle, H. Kibbel, H. Schumacher, U. König, “Enhanced SiGe Heterojunction Bipolar Transistors with 160 GHz-f_{max}”, Techn. Dig. IEDM, pp. 743-746, 1995.

[28] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbé, J. Y.-C. Sun, B. S. Meyerson, T. Tice, “Si/SiGe Epitaxial Base Transistors, Parts I and II, IEEE Trans. El. Dev., vol. 42, no. 3, pp. 455-482, 1995.

[29] F. Sato, T. Hashimoto, T. Tatsumi, M. Soda, H. Tezuka, T. Suzaki, T. Tashiro, “A Self-Aligned SiGe Base Bipolar Technology Using Cold Wall UHV/CVD and Its Application to Optical Communication IC’s”, Proc. BCTM, pp. 82-85, 1995.

[30] T. F. Meister, H. Schäfer, M. Franosch, W. Molzer, K. Aufinger, U. Scheler, C. Walz, M. Stolz, S. Boguth, J. Böck, “SiGe Base Bipolar Technology with 74 GHz f_{max} and 11 ps Gate Delay”, Techn. Dig. IEDM, pp. 739-742, 1995.

[31] M. Kondo, K. Oda, E. Ohue, H. Shimamoto, M. Tanabe, T. Onai, K. Washio, “Sub-10-fJ ECL/68-mA 4.7-GHz Divider Ultra-Low-Power SiGe Base Bipolar Transistors with a Wedge-Shaped CVD-SiO_2 Isolation Structure and a BPSG-Refilled Trench”, Techn. Dig. IEDM, pp. 245-248, 1996.

[32] A. Pruijmboom, D. Terpstra, C. E. Timmering, W. B. de Boer, M. J. J. Teunissen, J. W. Slotboom, R. J. E. Hueting, J. J. E. M. Hageraats, “Selective-Epitaxial Base Technology with 14 ps ECL-Gate Delay, for Low Power Wide-Band Communication Systems”, Techn. Dig. IEDM, pp. 747-750, 1995.

[33] E. F. Crabbé, B. S. Meyerson, J. M. C. Stork, D. L. Harame, “Vertical Profile Optimization of Very High Frequency Epitaxial Si- and SiGe-Base Bipolar Transistors”, Techn. Dig. IEDM, pp. 83-86, 1993.

[34] D. C. Shaver, “Microwave Operation of Submicrometer Channel-Length Silicon MOSFET’s”, IEEE El. Dev. Lett., vol. 6, no. 1, pp. 36-39, 1984.

[35] R. R. J. Vanoppen, J. A. M. Geelen, D. B. M. Klaasen, “The High-Frequency Analogue Performance of MOSFET’s”, Techn. Dig. IEDM, pp. 173-176, 1994.

[36] Voinigescu, S. W. Tarasewicz, T. MacElwee, J. Ilowski, “An Assessment of the State-of-the-Art 0.5 µm Bulk CMOS Technology for RF Applications”, Techn. Dig. IEDM, pp. 721-724, 1995.

[37] H. S. Momose, E. Morifuji, T. Yoshitomi, T. Ohguro, M. Saito, T. Morimoto, Y. Katsumata, H. Iwai, “High-Frequency AC Characteristics of 1.5 nm Gate Oxide MOSFETS”, Techn. Dig. IEDM, pp. 105-108, 1996.

[38] C. Raynaud, J. Gautier, G. Guegan, M. Lerme, E. Playez, G. Dambrine, “High-Frequency Performance of Submicrometer Channel-Length Silicon MOSFET’s”, IEEE El. Dev. Lett., vol. 12, no. 12, pp. 667-669, 1991.

[39] A. E. Schmitz, R. H. Walden, L. E. Larsen, S. E. Rosenbaum, R. A. Metzger, J. R. Behnke, P. A. Macdonald, “A Deep-Submicrometer Microwave/Digital CMOS/SOS Technology”, IEEE El. Dev. Lett., vol. 12, no. 1, pp. 16-17, 1991.

[40] A. L. Caviglia, R. C. Potter, L. J. West, “Microwave Performance of SOI n-MOSFET’s and Coplanar Waveguides”, IEEE El. Dev. Lett, vol. 12, no. 1, 1991.

[41] M. H. Hanes et al., “MICROX - An All-Silicon Technology for Monolithic Microwave Integrated Circuits”, IEEE El. Dev. Lett., vol. 14, no. 5, 1993.

[42] P. R. de la Houssaye, C. E. Chang, B. Offord, G. Imthurn, R. Johnson, P. M. Asbeck, G. A. Garcia, I. Lagnado, “Microwave Performance of Optically Fabricated T-Gate Thin Film Silicon-on-Sapphire Based MOSFET’s”, IEEE El. Dev. Lett., vol. 16, no. 6, 1995.

[43] J. P. Colinge, J. Chen, D. Flandre, J. P. Raskin, R. Gillon, D. Vanhoenacker, "A Low-Voltage, Low-Power Microwave SOI MOSFET", Proc. IEEE Int. SOI Conf., pp. 128-129, 1996.

[44] A. Hürrich, P. Huebler, D. Eggert, H. Kueck, W. Barthel, W. Budde, M. Raab, "SOI-CMOS Technology with Monolithically Integrated Active and Passive RF Devices on High Resistivity SIMOX Substrates", Proc. IEEE SOI Conf., pp. 130-131, 1996.

[45] K. Ismail, "Si/SiGe High-Speed Field-Effect Transistors", Techn. Dig. IEDM, pp. 509-512, 1995; also K. Ismail, personal communication.

[46] D. Hisamoto, S. Tanaka, T. Tanimoto, Y. Nakamura, S. Kimura, "Silicon RF Devices Fabricated by ULSI Process Featuring 0.1-µm SOI-CMOS and Suspended Inductors", Dig. Techn. P. Symp. VLSI Techn., pp. 104-105, 1996.

[47] 0.2 µm analog CMOS with Very Low Noise Figure at 2 GHz Operation"**,** Dig. Techn. P. Symp. VLSI Techn., pp. 132-133, 1996.

[48] D. Harame et al., "SiGe HBT Technology: Device and Application Issues", Techn. Dig. IEDM, pp. 731-734, 1995.

[49] A. Schüppen, H. Dietrich, S. Gerlach, H. Hohnemann, J. Arndt, U. Seiler, R. Götzfried, U. Erben, H. Schumacher, "SiGe-Technology and Components for Mobile Communication Systems", Proc. BCTM, pp. 130-133, 1995.

[50] M. Soyuer, J. N. Burghartz, K. A. Jenkins, H. A. Ainspan, F. Canora, "RF and Microwave Building Blocks in a Standard BiCMOSTechnology", Proc. ISCAS, pp. 89-92, 1996.

[51] J. N. Burghartz, BiCMOS Process Integration and Device Optimization: Basic Concepts and New Trends", Electrical Eng., vol. 79, pp. 313-327, 1996.

[52] L. E. Larson, "Integrated Circuit Technology Options for RFICs - Present Status and Future Directions", Proc. CICC, pp. 169-176, 1997.

[53] N. M. Nguyen, R. G. Meyer, "Si IC -Compatible Inductors and LC Passive Filters", IEEE J. Sol. St. Circ., vol. 25, no. 4, pp. 1028-1031, 1990.

[54] G. A. Sai-Halasz, "Performance Trends in High End Processors", Proc. IEEE, vol. 83, no. 1, pp. 20-36, 1995.

[55] M. Soyuer, J. N. Burghartz, K. A. Jenkins, S. Ponnapalli, J. F. Ewen, W. E. Pence, "Multi-Level Monolithic Inductors in Silicon Technology", El. Lett., vol. 31, no. 5, pp. 359-360, 1995.

[56] J. N. Burghartz, M. Soyuer, K. A. Jenkins, "Microwave Inductors and Capacitors in Standard Multi-Level Interconnect Silicon Technology", IEEE Trans. Microw. Theory Techn., vol. 44, no. 1, pp. 100-104, 1996.

[57] J. N. Burghartz, M. Soyuer, K. A. Jenkins, "Integrated RF and Microwave Components in BiCMOS Technology", IEEE Trans. El. Dev. , vol. 43, no. 9, pp. 1559-1570, 1996.

[58] J. N. Burghartz, K. A. Jenkins, M. Soyuer, "Multilevel-Spiral Inductors Using VLSI Interconnect Technology", IEEE El. Dev. Lett., vol. 17, no. 9, pp. 428-430, 1996.

[59] K. B. Ashby, W. C. Finley, J. J. Bastek, S. Moinian, "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process", Proc. BCTM, pp. 179-182, 1994.

[60] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, C. Jahnes, C. Uzoh, E. J. O'Sullivan, K. K. Chan, M. Soyuer, P. Roper, S. Cordes, "Monolithic Spiral Inductors Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates", Techn. Dig. IEDM, pp. 99-102, 1996.

[61] H. A. Wheeler, "Formulas for the Skin Effect", Proc. IRE, no. 9, pp. 412-424, 1942.

[62] M. Soyuer, J. Burghartz, H. Ainspan, K. Jenkins, P. Xiao, A. Shahani, M. Dolan, D. Harame, "An 11-GHz 3-V SiGe Voltage-Controlled Oscillator with Integrated Resonator", Proc. BCTM, pp. 169-172, 1996.

[63] H. Ainspan, M. Soyuer, J.-O. Plouchart, J. Burghartz, "A 6.25-GHz Low Power Low-Noise Amplifier in SiGe", Proc. CICC, pp. 177-180, 1997.

[64] J. R. Long, M. A. Copeland, "Modeling, Characterization and Design of Monolithic Inductors for Silicon RF Ics", Proc. CICC, pp. 185-188, 1996.

[65] J. Crols, P. Kinget, J. Craninckx, M. Steyaert, "An Analytical Model of Planar Inductors on Lowly Doped Silicon Substrates for High Frequency Analog Design up to 3 GHz, Dig. Techn. P. Symp. VLSI Techn., pp. 28-29, 1996.

[66] C. Yue, C. Ryu, J. Lau, T. Lee, S. Wong, "A Physical Model for Planar Spiral Inductors on Silicon", Techn. Dig. IEDM, pp. 155-158, 1996.

[67] A. Nkinejad, R. G. Meyer, "Analysis and Optimization of Monolithic Inductors and Transformers for RF Ics", Proc. CICC, pp. 375-378, 1997.

[68] Y. Eo, W. R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-Parameter Measurements", IEEE Trans. Comp. Hybrids Manufat. Techn., vol. 16, no. 5, pp. 555-562.

[69] T. Yamaguchi, S. Uppili, S. S. Lee, G. H. Kawamoto, T. Dosluoglu, S. Simpkins, "Process and Device Characterization for a 30-GHz -f_T Submicrometer Double Poly-Si Bipolar Technology Using BF_2-Implanted Base With Rapid Thermal Process", IEEE Trans. El. Dev., vol. 40, no. 8, pp. 1483-1495, 1993.

[70] T. Yamaguchi, personal communication.

[71] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, Y. Kwark, "Spiral Inductors and Transmission Lines in Silicon Technology Using Copper-Damascene Interconnects and Low-Loss Substrates", in IEEE Microw. Theory Techn., Special Issue on Interconnects and Packaging, 1997, to be published.

[72] A. C. Reyes, S. M. El-Ghazaly, S. J. Dorn, M. Dydyk, D. K. Schroder, H. Patterson, "Coplanar Waveguides and Microwave Inductors on Silicon Substrates", IEEE Trans. Microw. Theory Techn., vol. 43, no. 9, pp. 2016-2021, 1995.

[73] V. Milanovic, M. Gaitan, E. D. Bowen, M. E. Zaghloul, "Micromachined Microwave Transmission Lines in CMOS Technology", IEEE Trans. Microw. Theory Techn., vol. 45, no. 5, pp. 630-635, 1997.

[74] H. Sobol, "Applications of Integrated Circuit Technology to Microwave Frequencies", Proc. IEEE, vol. 59, no. 8, pp. 1200-1211, 1971.

[75] R. A. Pucel, "Design Considerations for Monolithic Microwave Circuits", IEEE Trans. Microw. Theory Techn., vol. 29, no. 6, pp. 513-534, 1981.