PHENIX TEC

Front End Analog Signal Processing Electronics

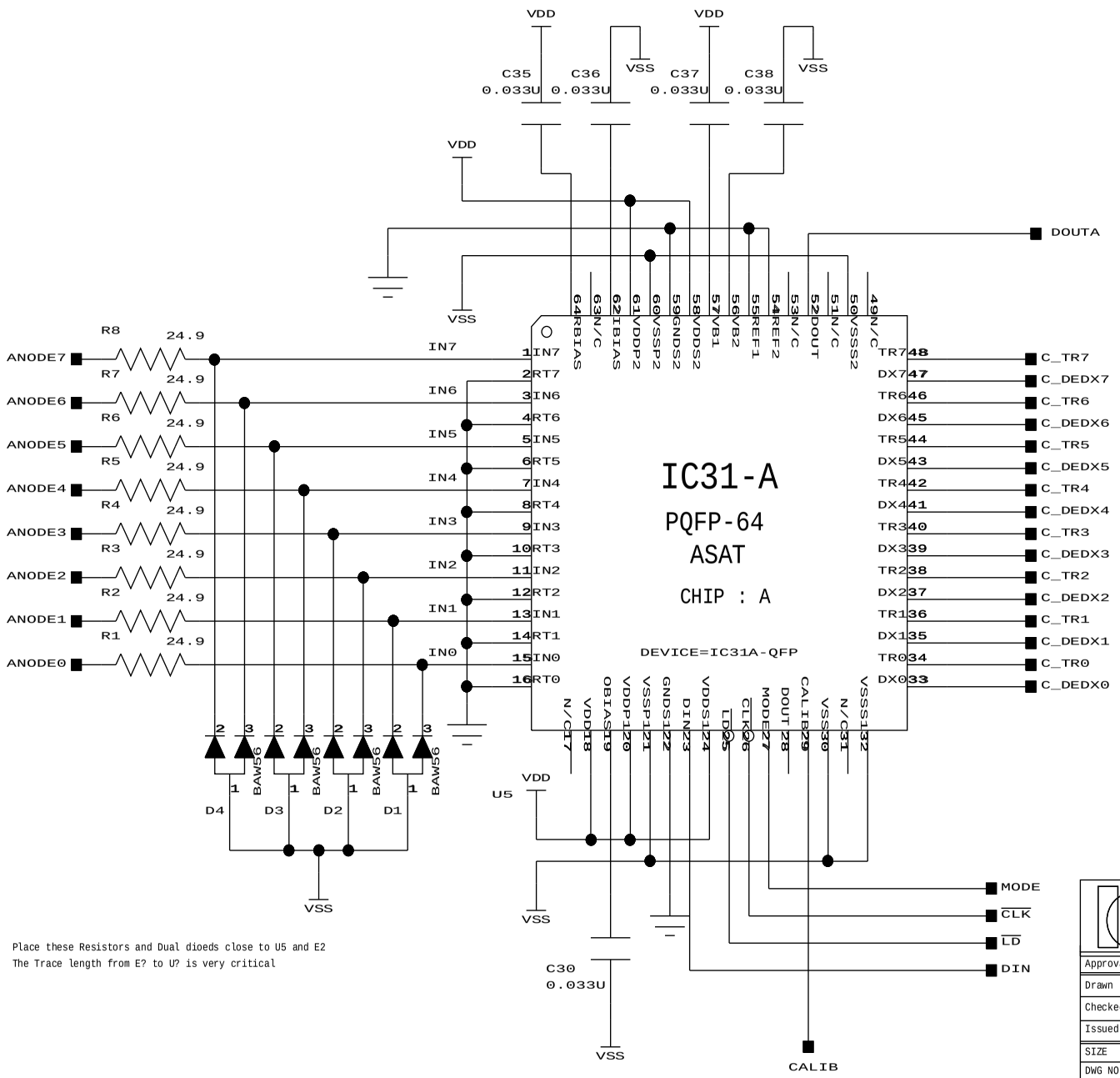
Paul O' Connor

Anand Kandasamy

Instrumentation Division

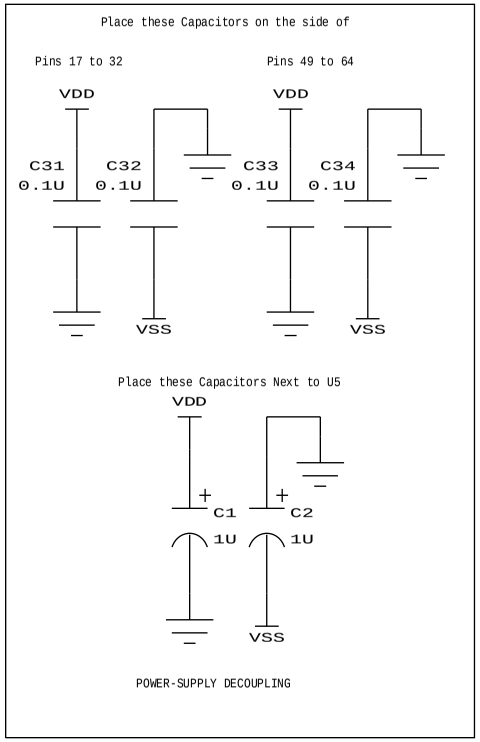
Brookhaven National Laboratory

Upton, NY 11973



Place these Resistors and Dual dioeds close to U5 and E2
The Trace length from E? to U? is very critical

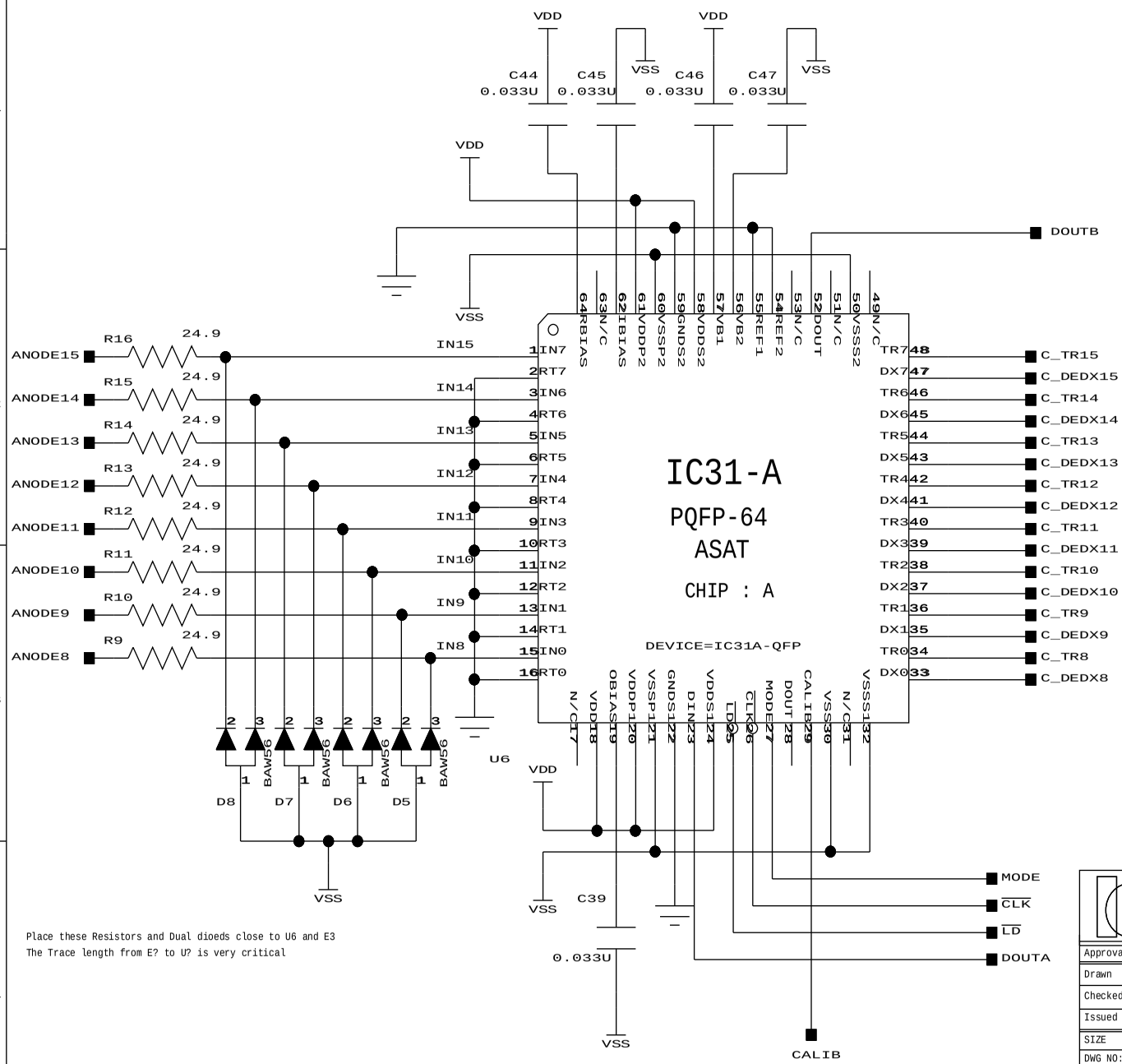
@DATETIME=3-4-1997_13:05



Brookhaven National Laboratory Instrumentation Division Upton, NY 11973		
Approvals	Date	Drawing: PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Drawn		
Checked		
Issued		
SIZE	B	TEC-PS REV2
DWG NO:		
REV NO:	3	
SCALE		

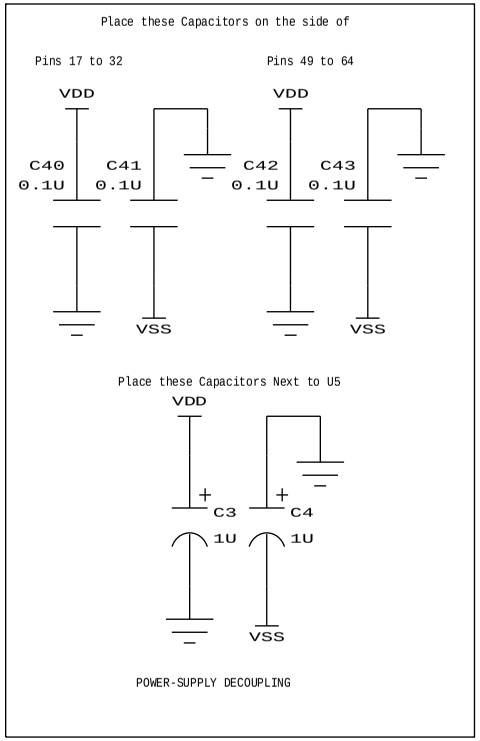
Drawn By:
Anand Kandasamy
516-344-5486
anand@bnl.gov

Sheet: 1 OF 31



Place these Resistors and Dual dioeds close to U6 and E3
The Trace length from E? to U? is very critical

@DATETIME=3-4-1997_13:05



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Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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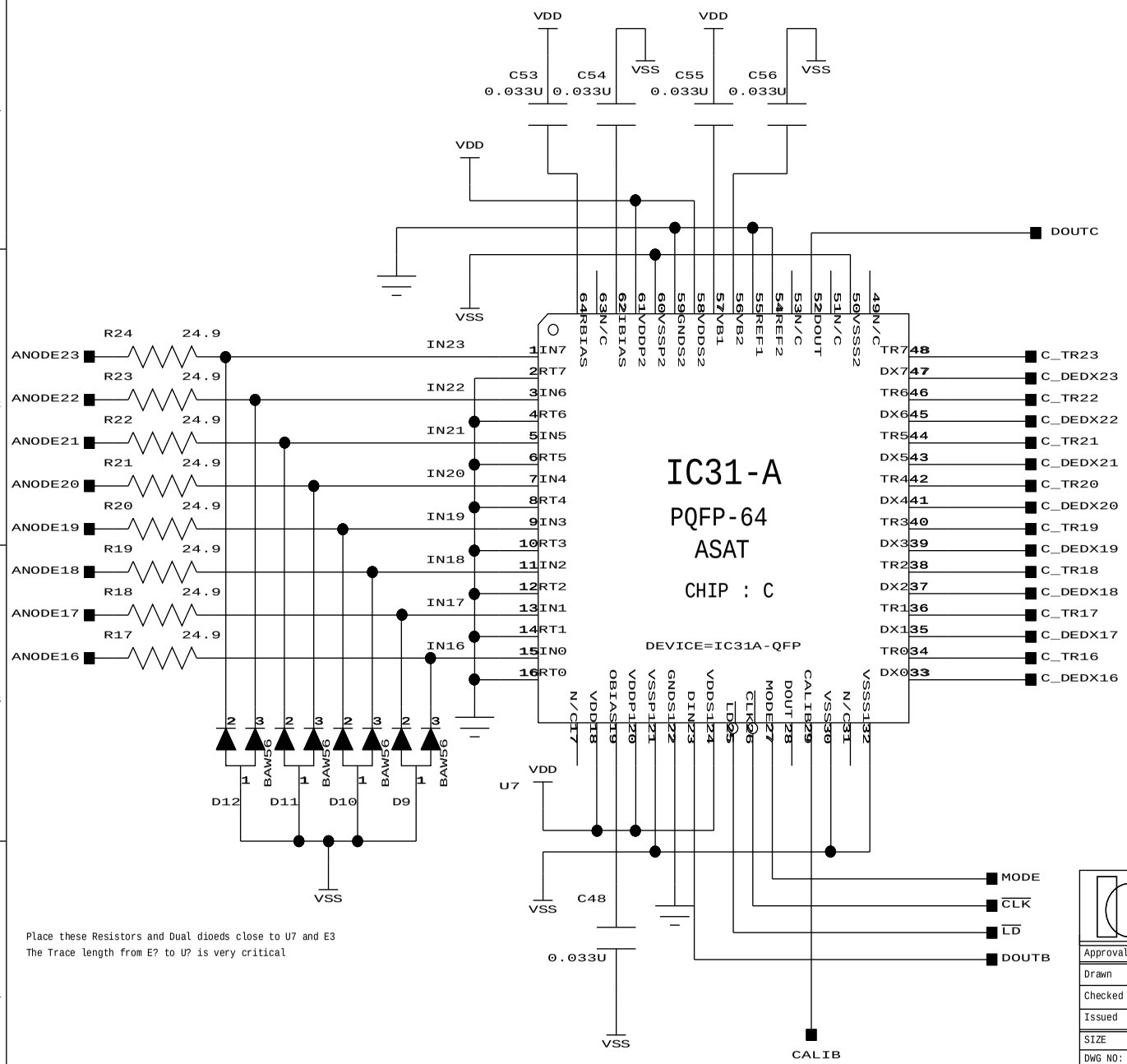
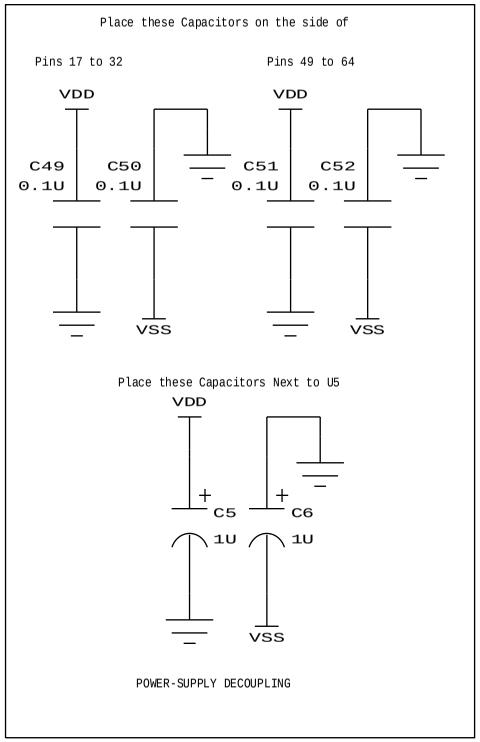
Sheet: 2 OF 31



Place these Resistors and Dual dioeds close to U7 and E3
The Trace length from E? to U? is very critical

@DATETIME=3-4-1997_13:05



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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

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SCALE	

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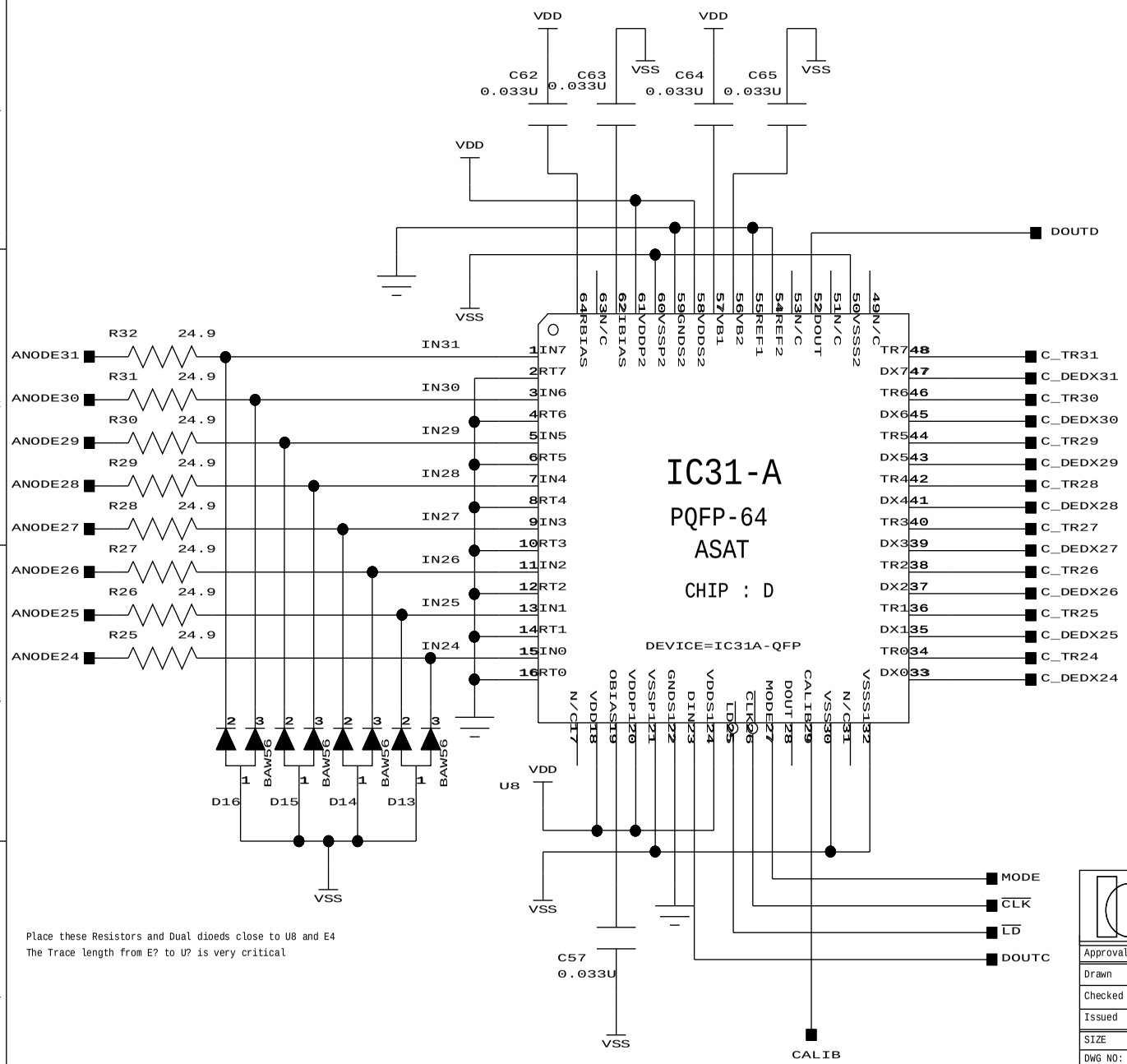
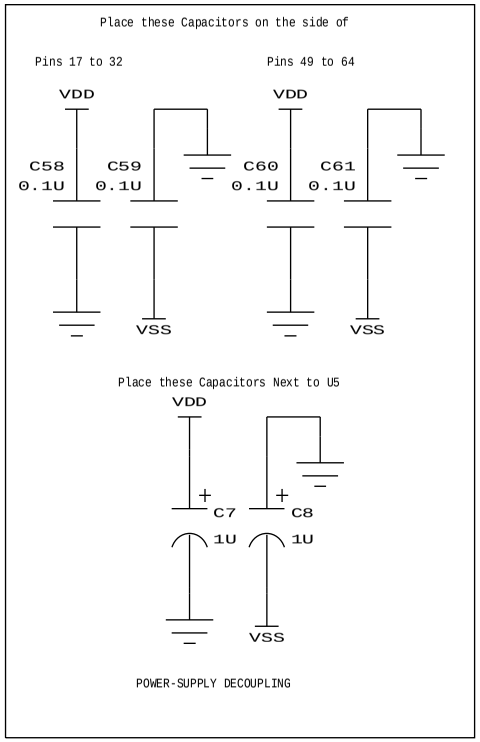


Place these Resistors and Dual dioeds close to U8 and E4
The Trace length from E? to U? is very critical

@DATETIME=3-4-1997_13:05



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PHENIX Time Expansion Chamber
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SIZE	B
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SCALE	

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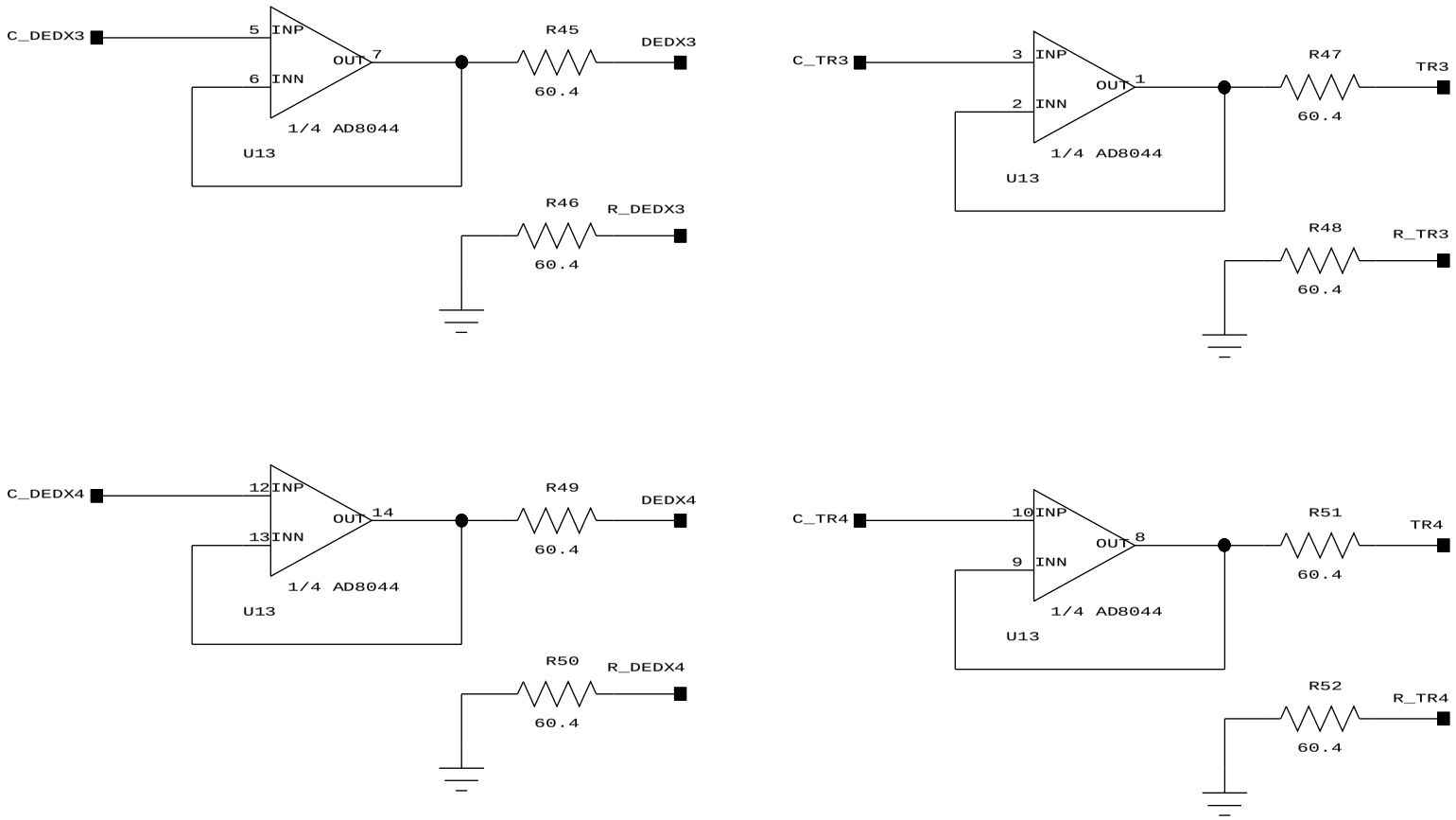
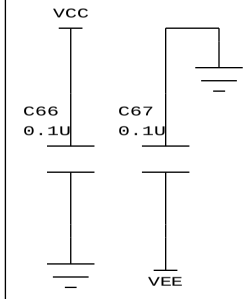
Sheet: 4 OF 31



Place these Capacitors Next to U13

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U13		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

DRIVER 1

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PHENIX Time Expansion Chamber
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SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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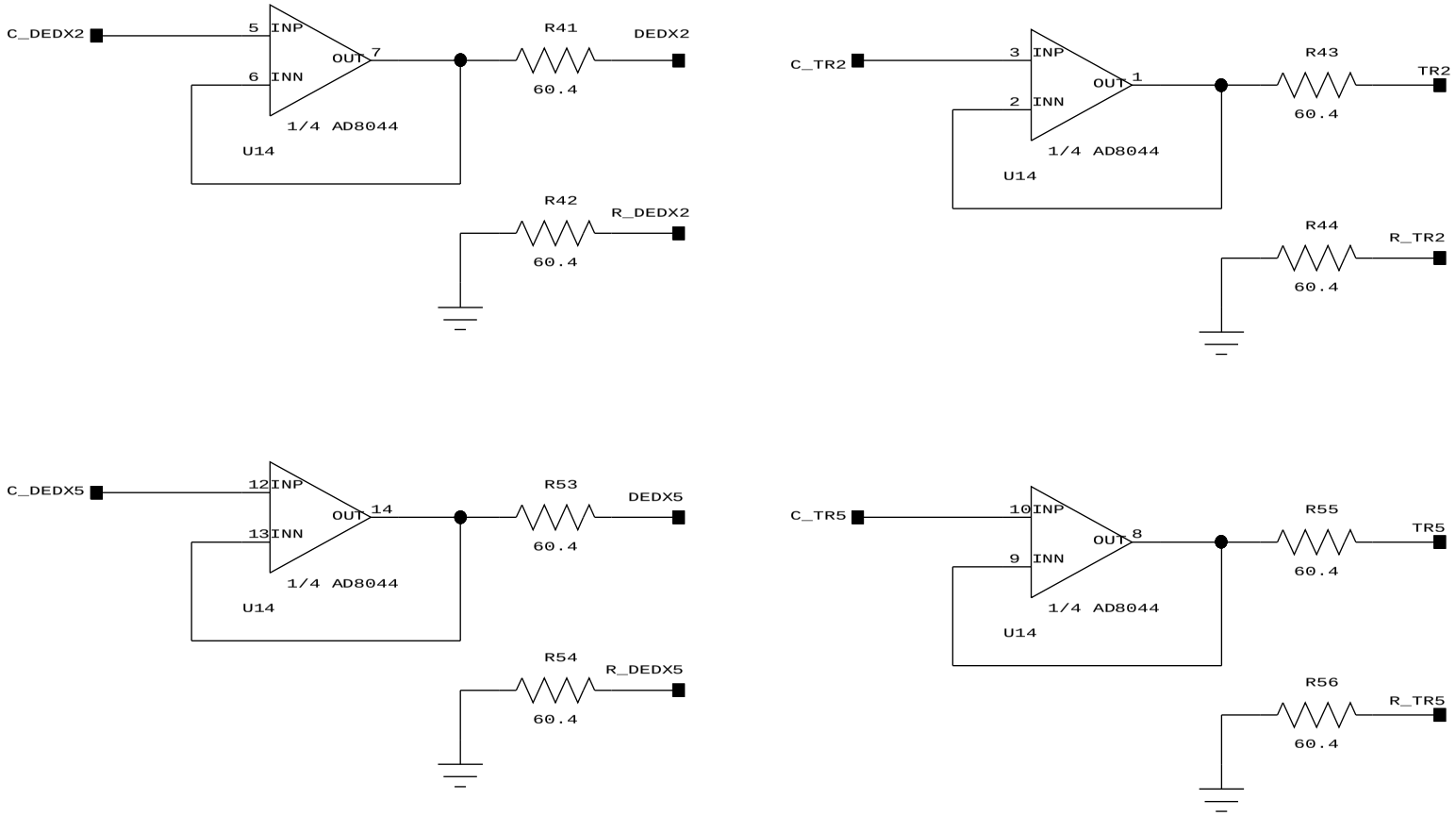

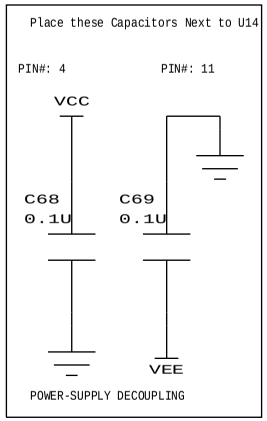

POWER U14		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

DRIVER 2

@DATETIME=3-4-1997_13:06

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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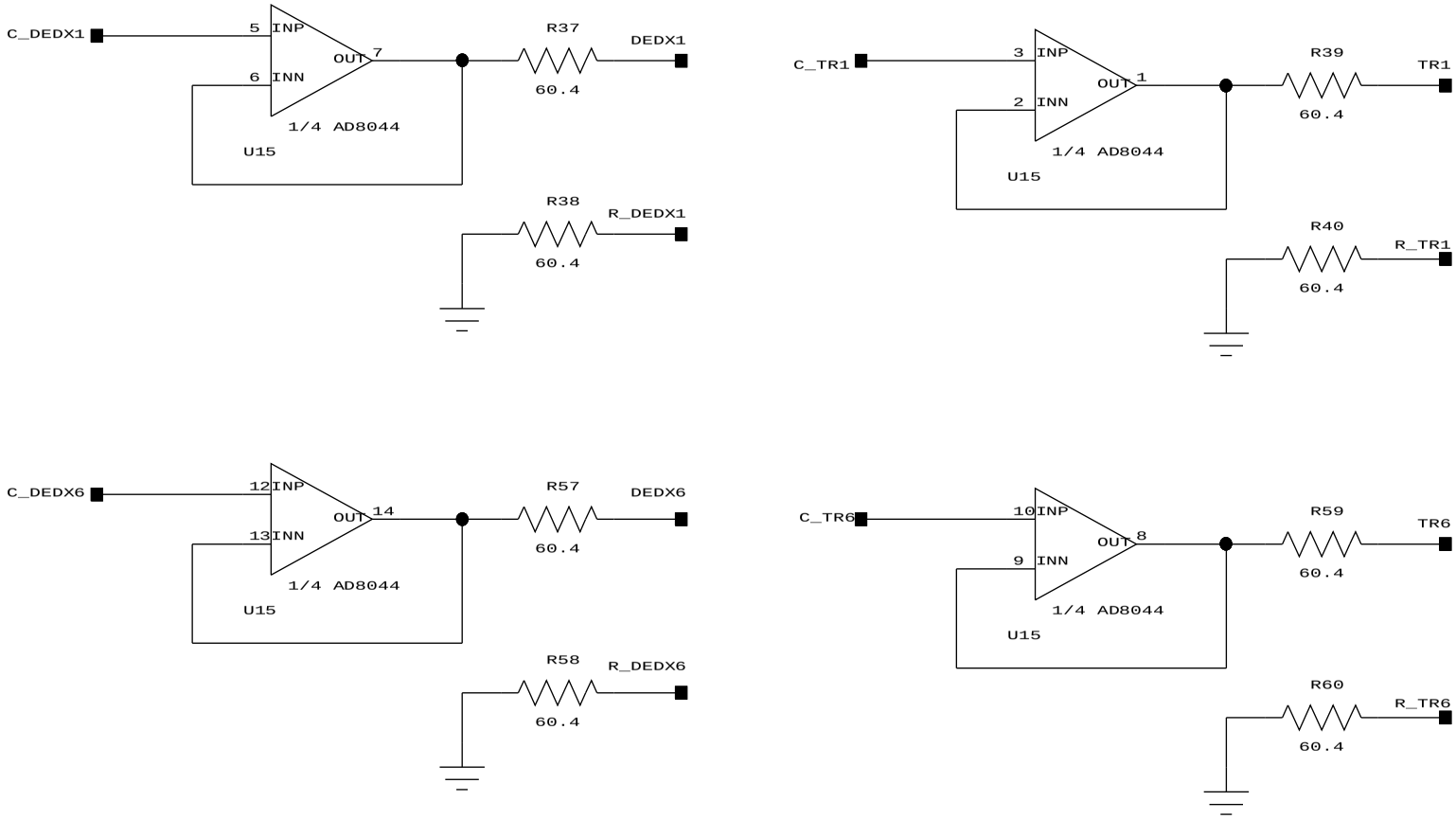
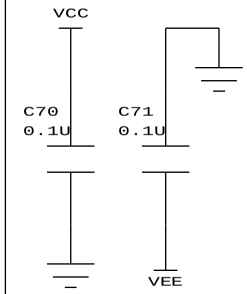


Place these Capacitors Next to U15

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U15		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 3

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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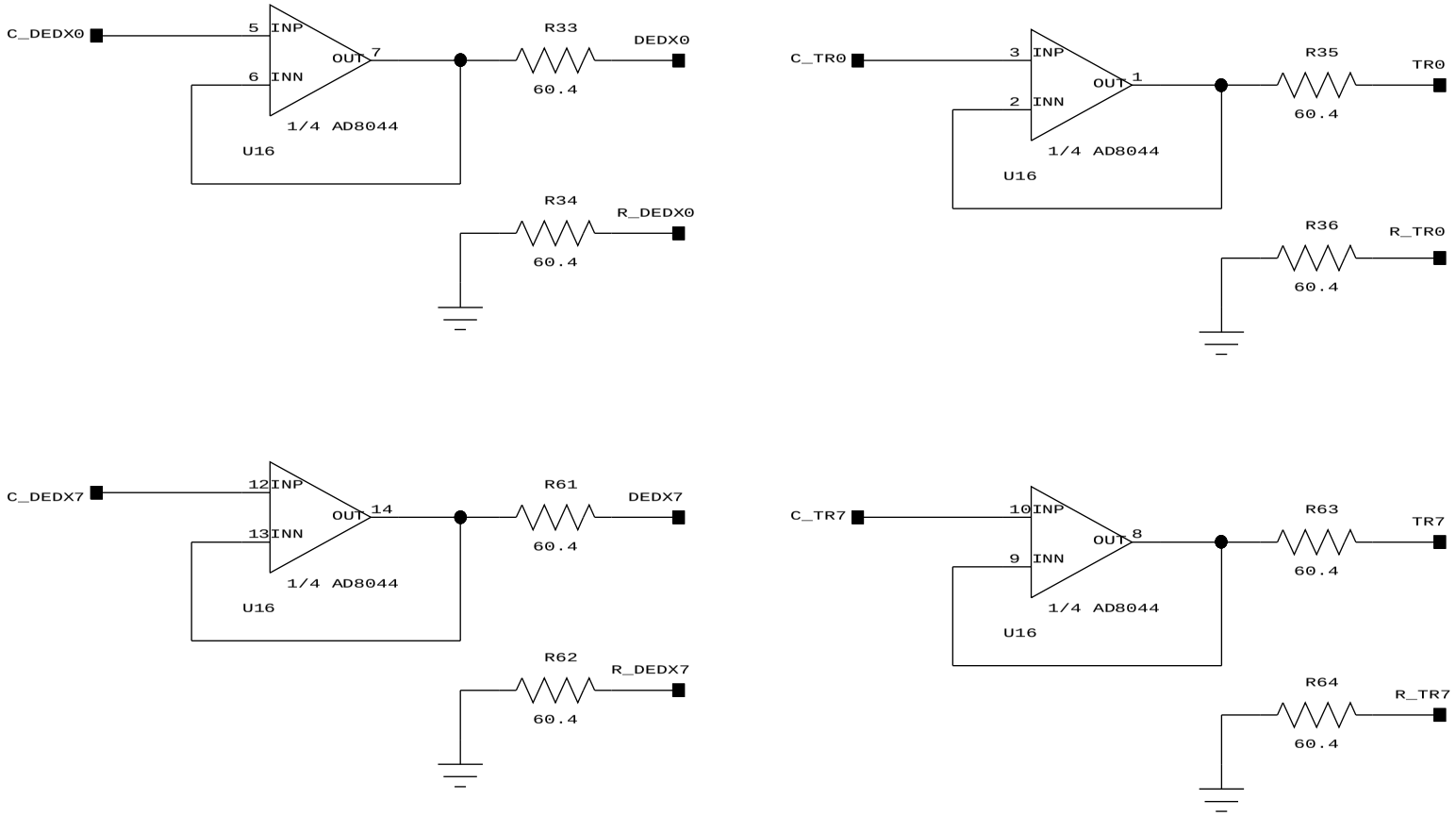
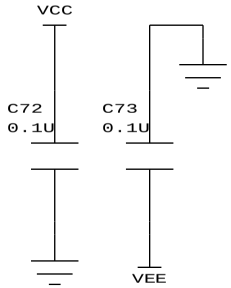


Place these Capacitors Next to U16

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U16		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 4

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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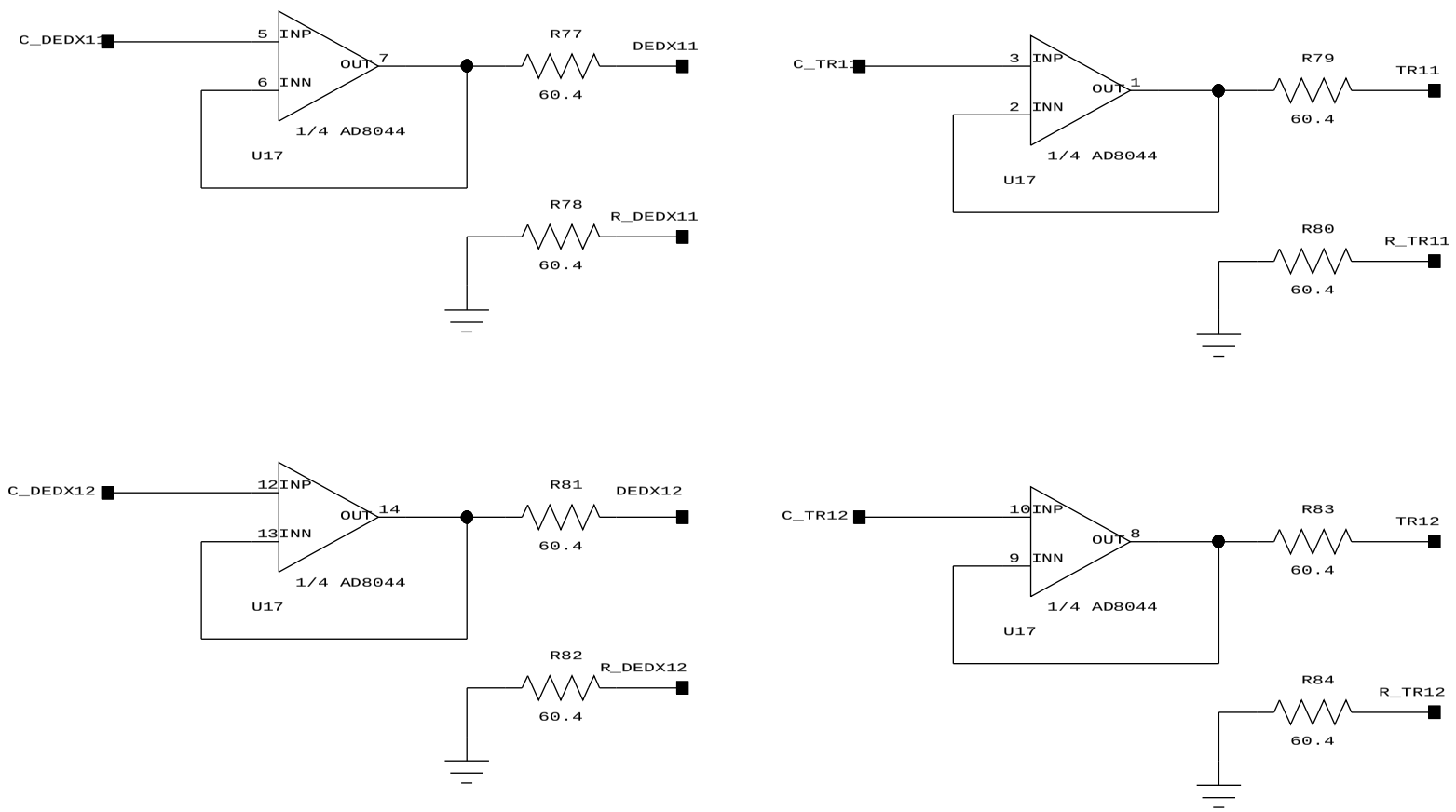
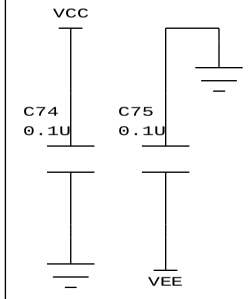


Place these Capacitors Next to U17

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U17		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

DRIVER 5

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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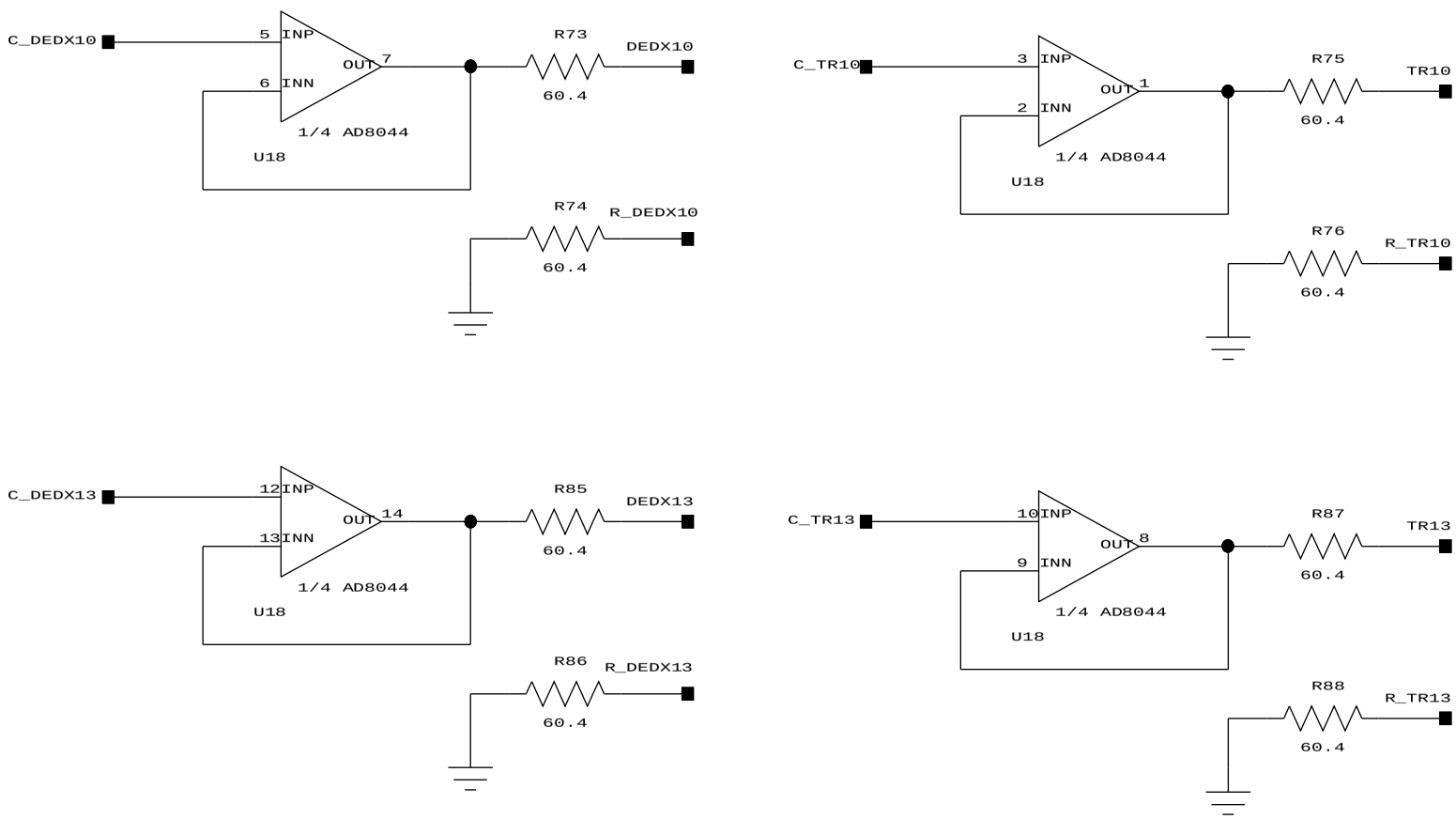

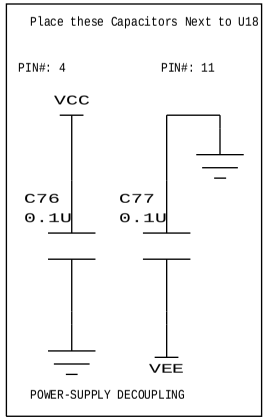

POWER U18		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 6

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PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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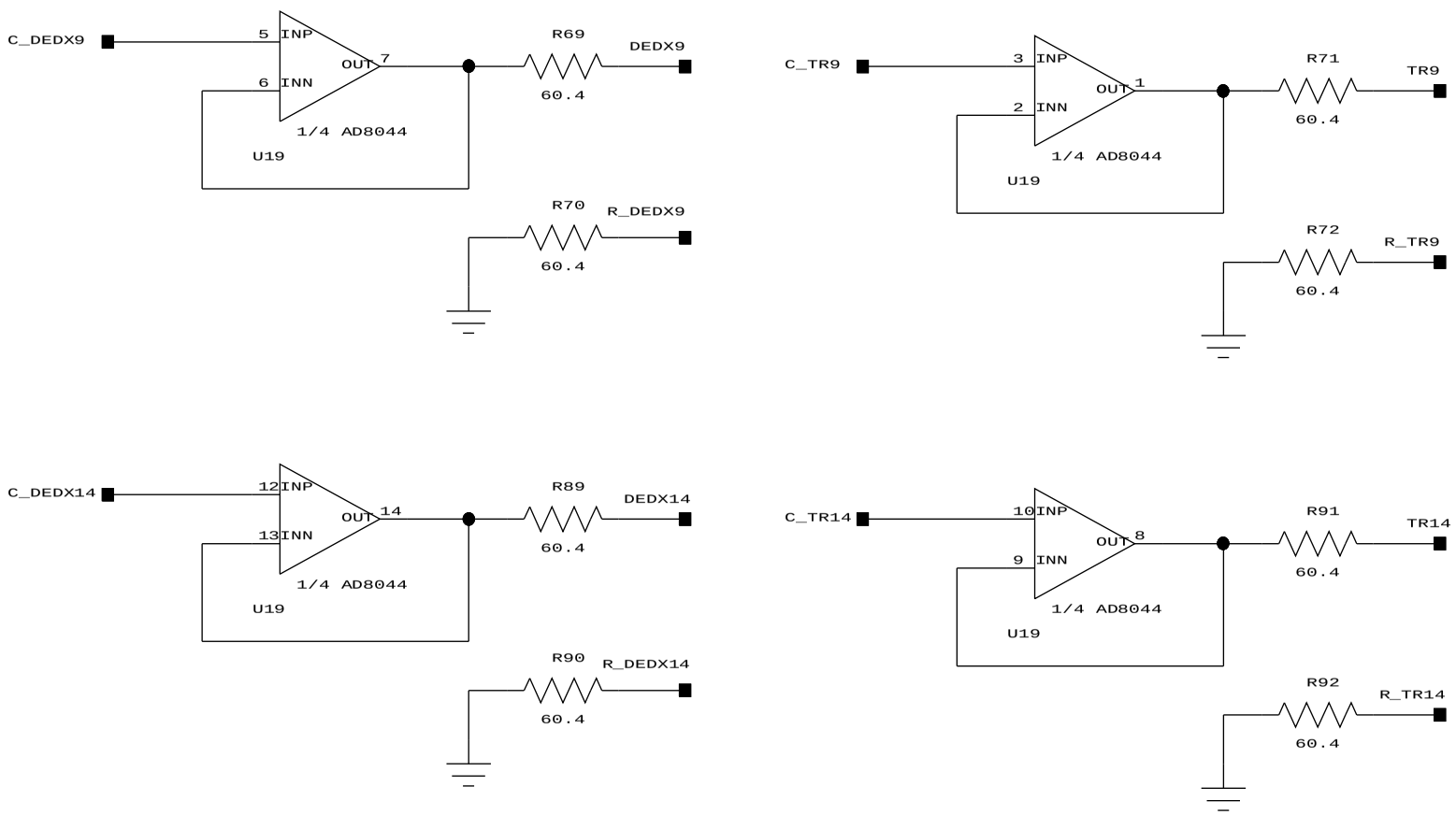
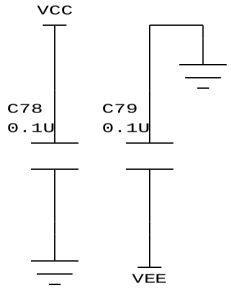


Place these Capacitors Next to U19

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U19		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 7

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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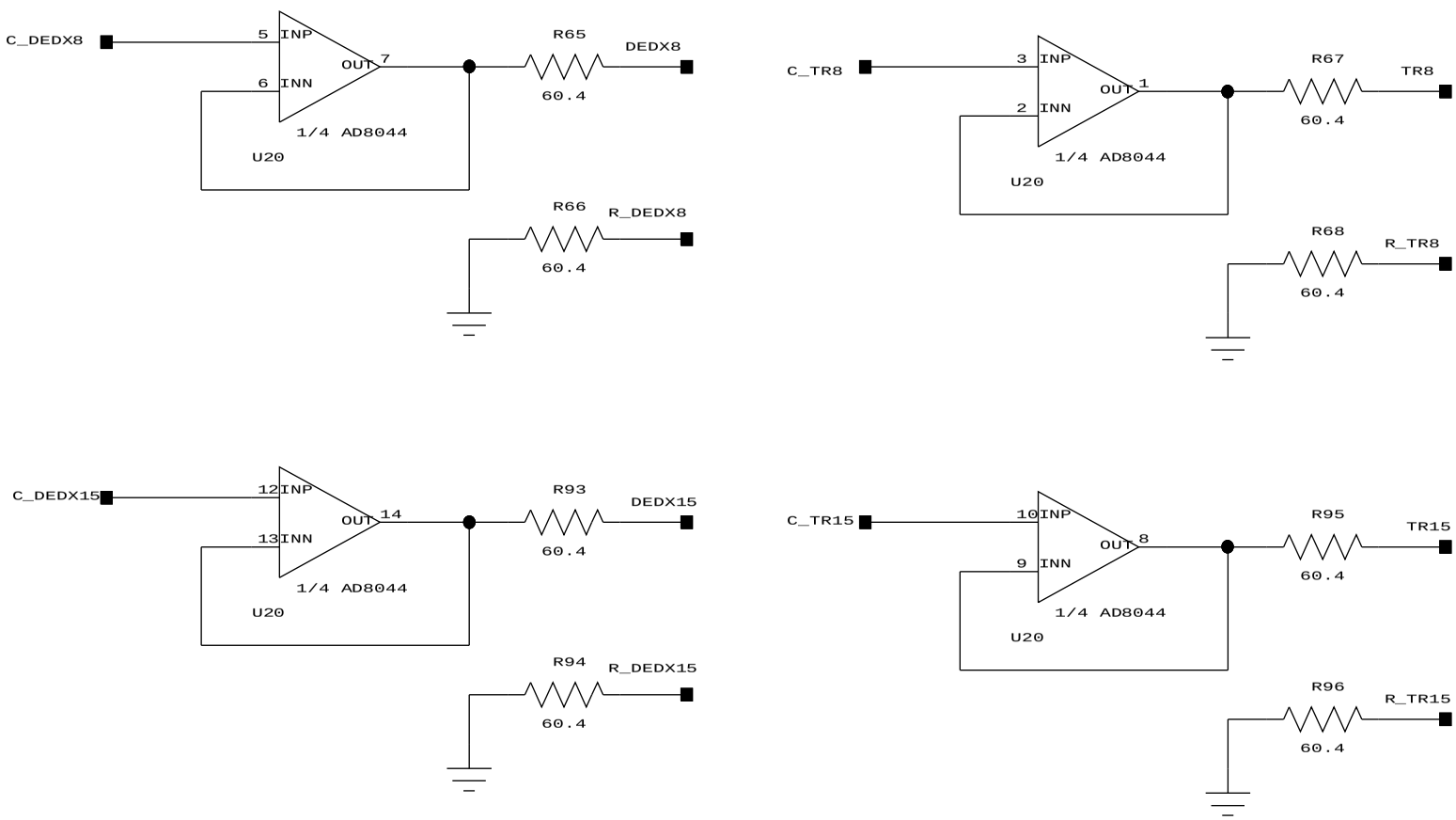
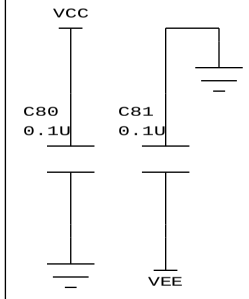


Place these Capacitors Next to U20

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U20		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 8

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
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REV NO:	3
SCALE	

TEC-PS REV2

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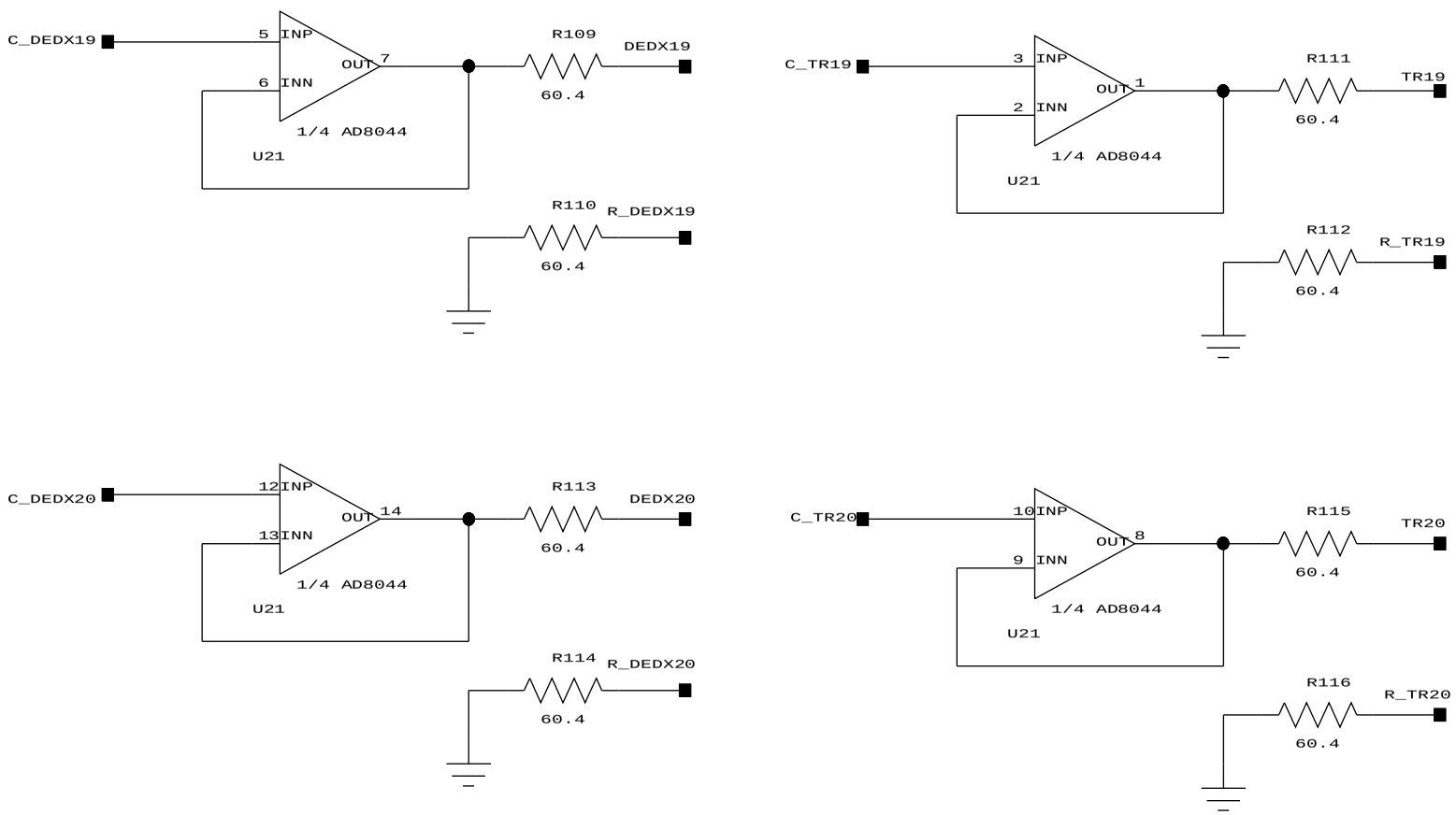
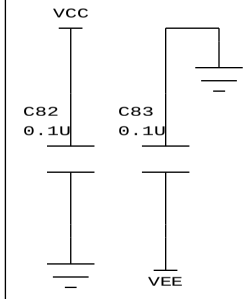


Place these Capacitors Next to U21

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U21		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 9

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Drawing:
PHENIX Time Expansion Chamber
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SCALE	

TEC-PS REV2

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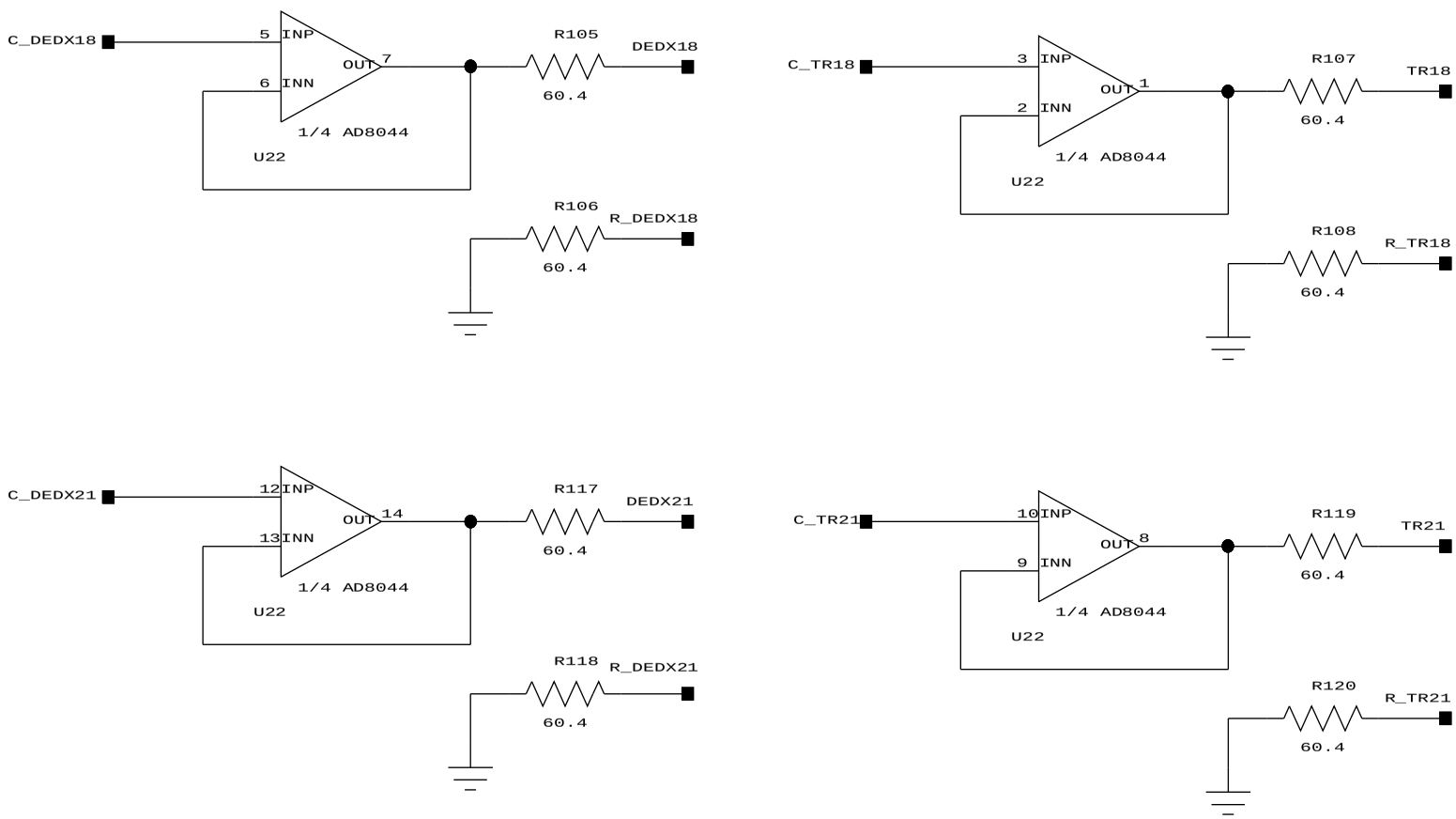
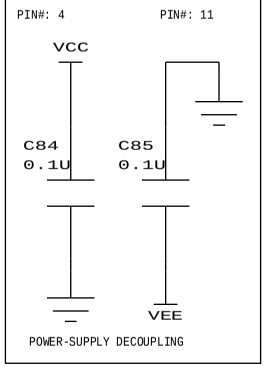
Sheet: 13 OF 31



Place these Capacitors Next to U22



POWER U22		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

@DATETIME=3-4-1997_13:08

DRIVER 10

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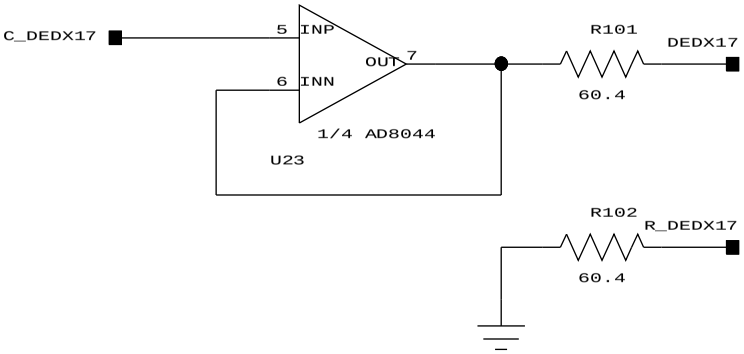
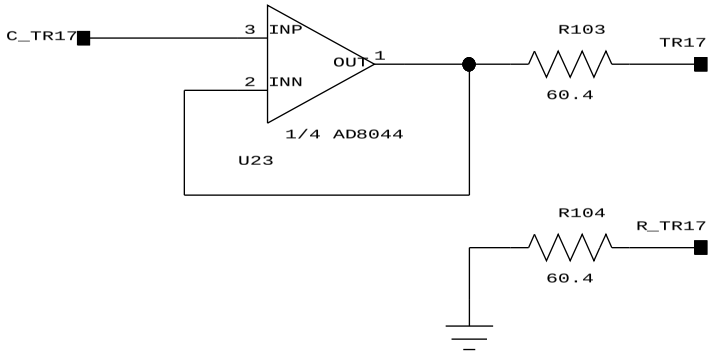
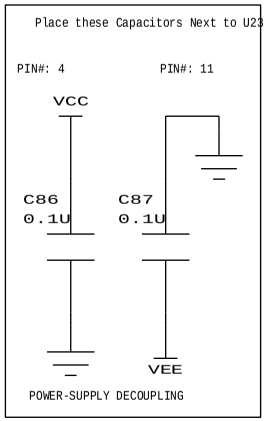
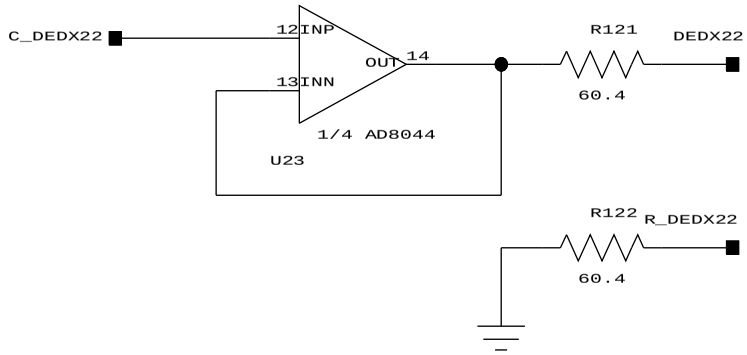
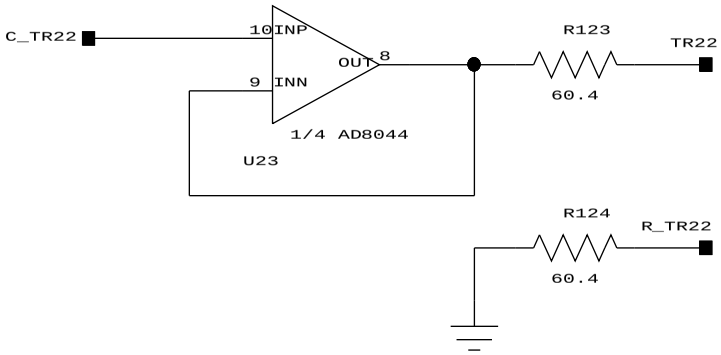






POWER U23		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V





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DRIVER 11

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Checked	
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PHENIX Time Expansion Chamber
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SIZE	B
DWG NO:	
REV NO:	3
SCALE	

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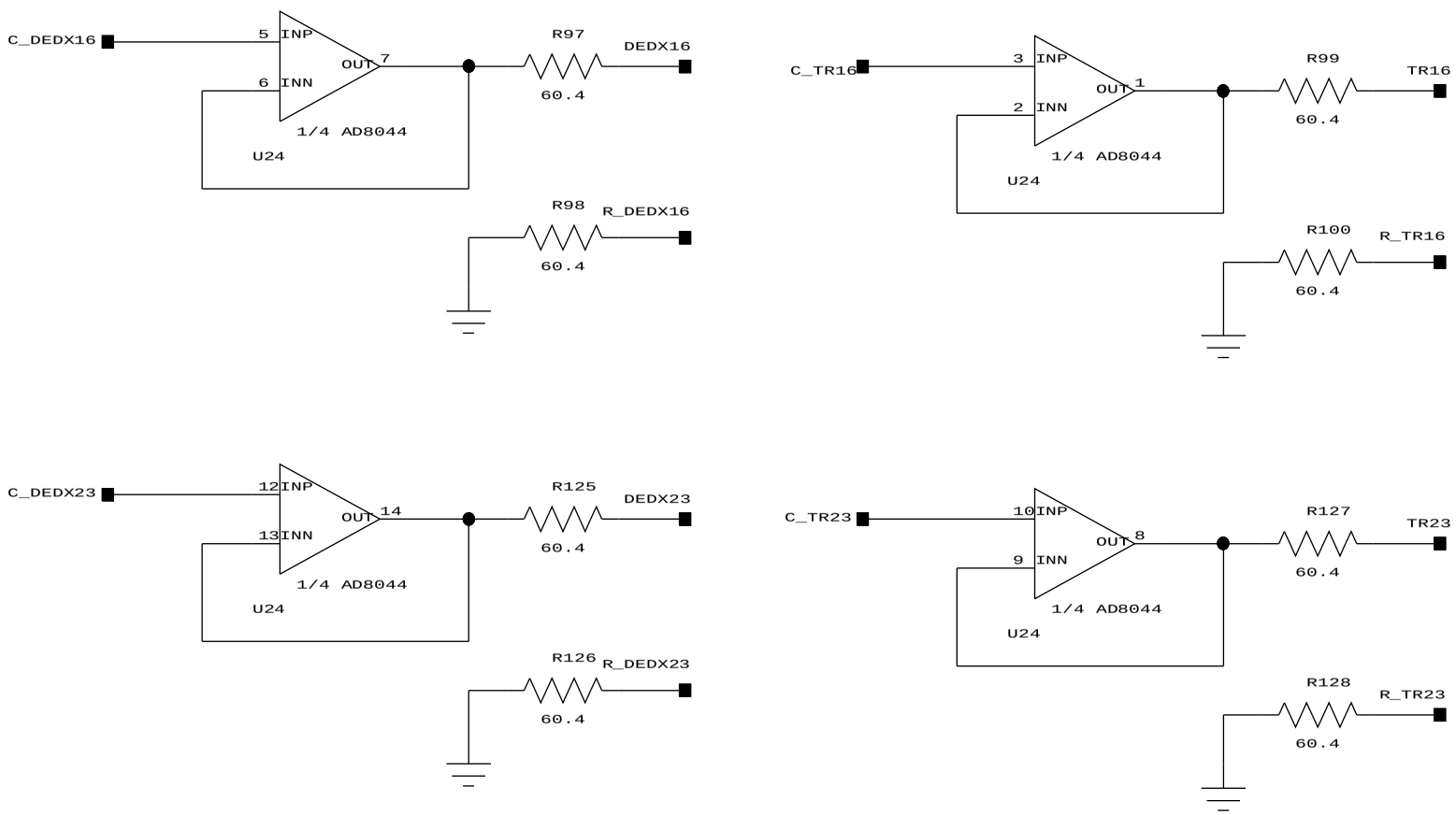
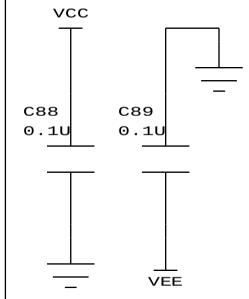


Place these Capacitors Next to U24

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U24		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 12

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Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
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REV NO:	3
SCALE	

TEC-PS REV2

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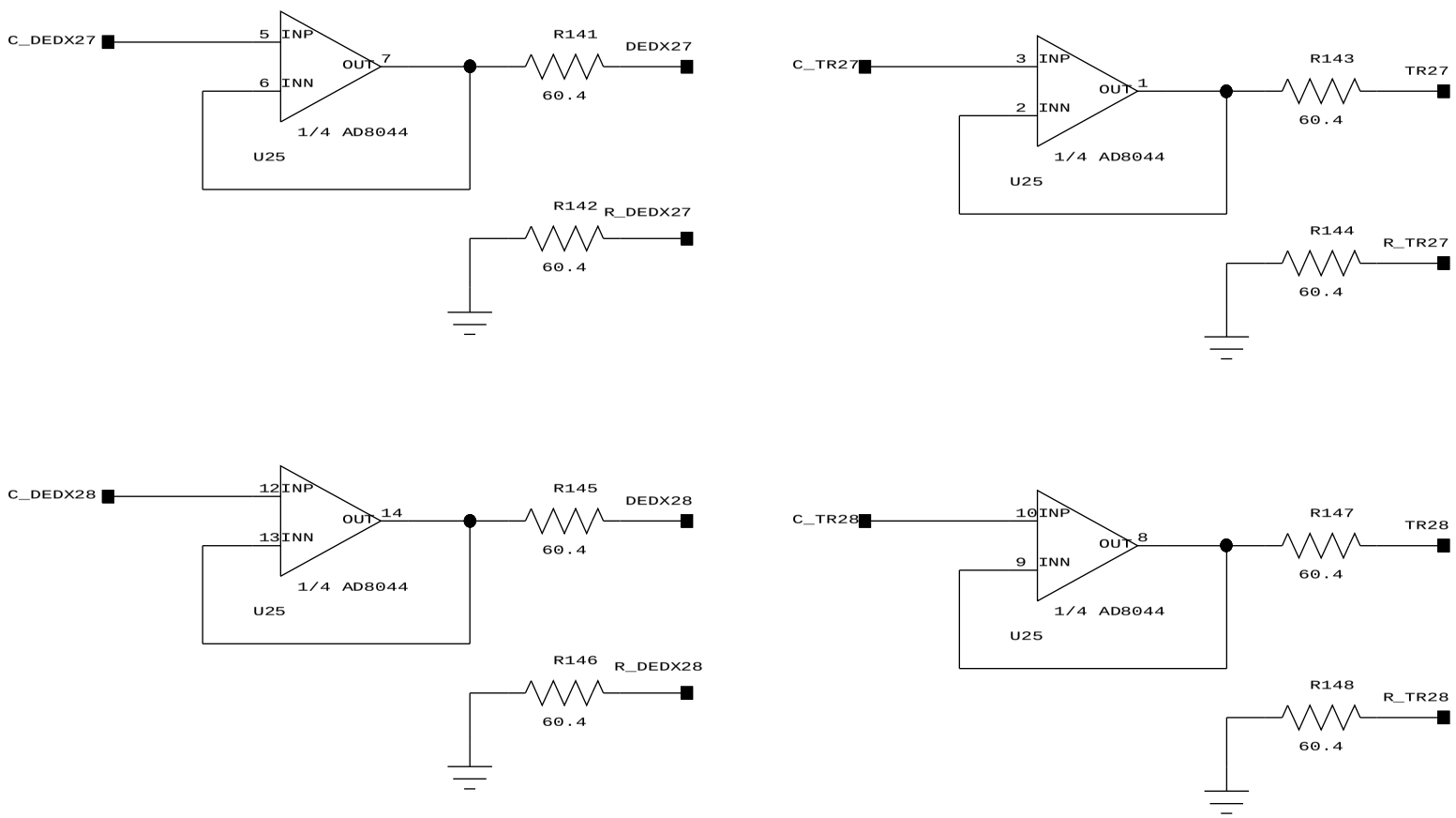
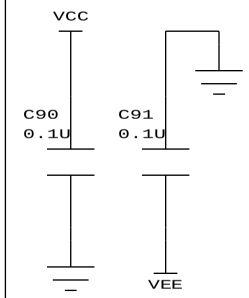


Place these Capacitors Next to U25



POWER-SUPPLY DECOUPLING

POWER U25		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

@DATETIME=3-4-1997_13:09

DRIVER 13

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Drawing:
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SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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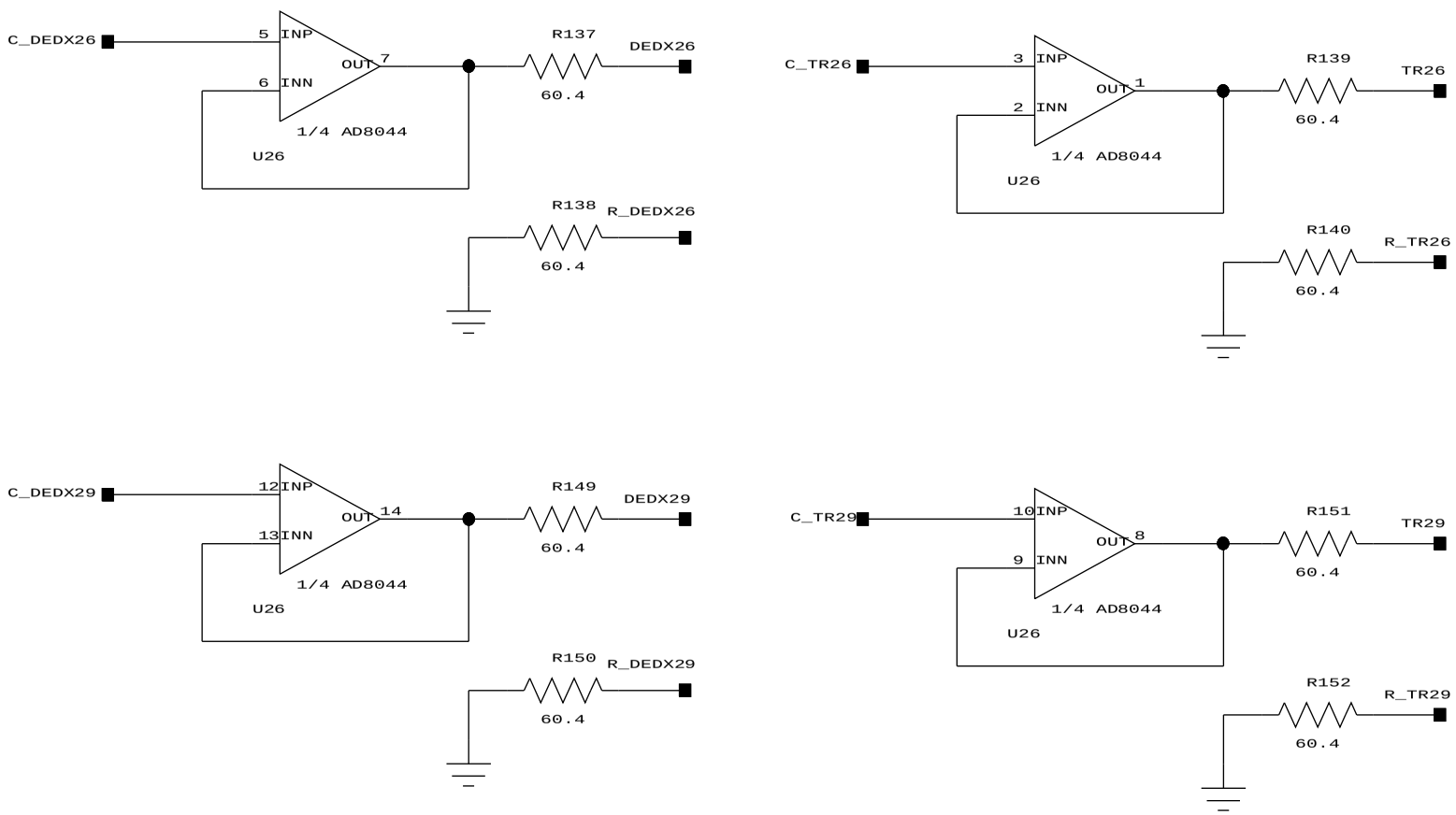
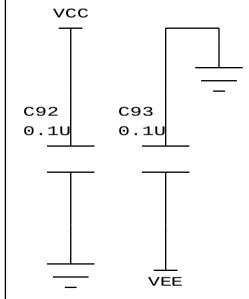
anand@bnl.gov



Place these Capacitors Next to U26

PIN#: 4 PIN#: 11



POWER-SUPPLY DECOUPLING

POWER U26		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

@DATETIME=3-4-1997_13:09

DRIVER 14

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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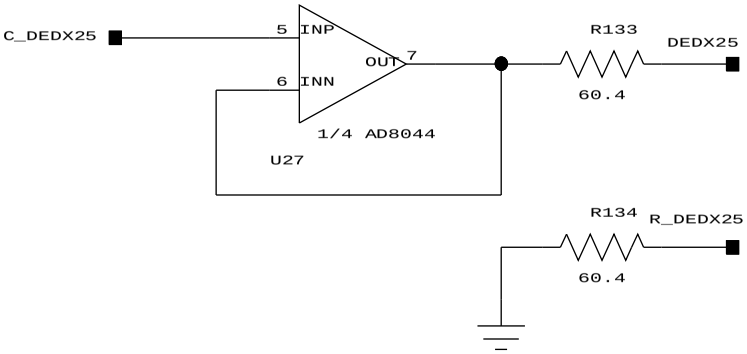
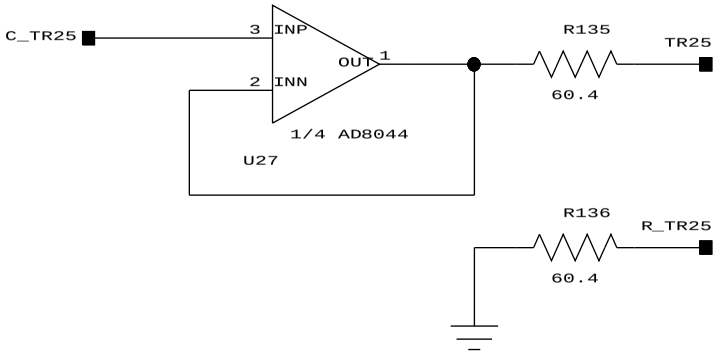
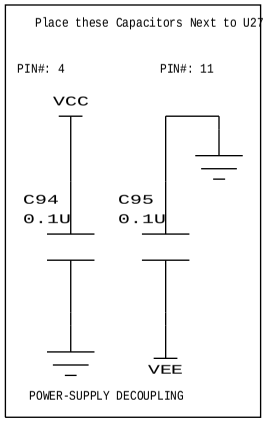
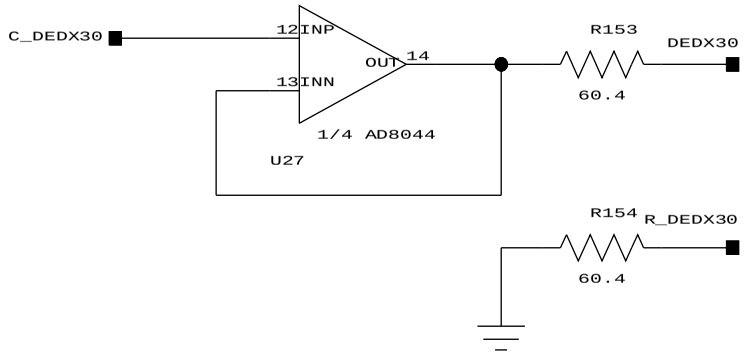
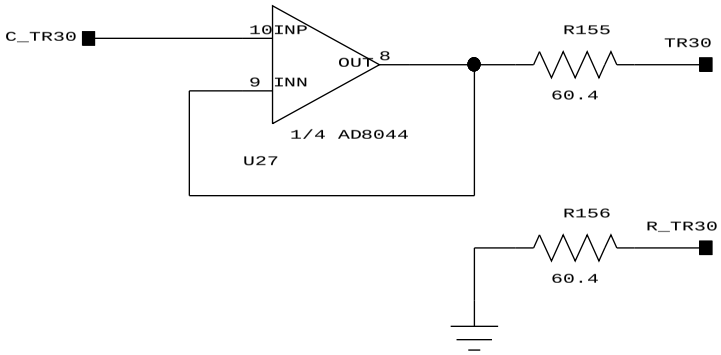






POWER U27		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V





@DATETIME=3-4-1997_13:09

DRIVER 15

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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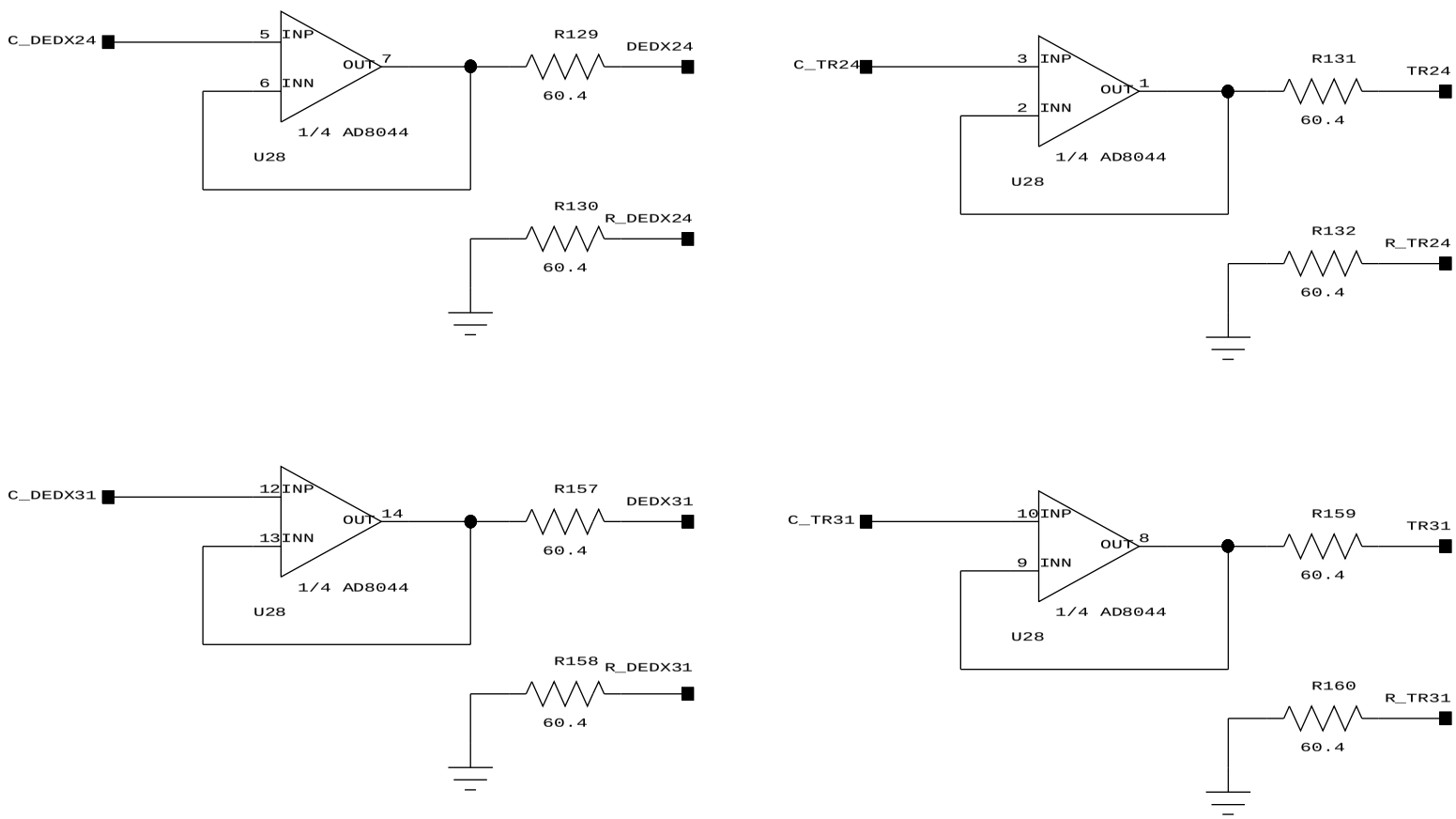
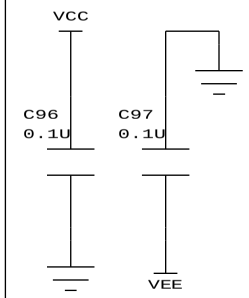


Place these Capacitors Next to U28



POWER-SUPPLY DECOUPLING

POWER U28		
PIN#: 4	VCC	+5V
PIN#: 11	VEE	-5V

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DRIVER 16

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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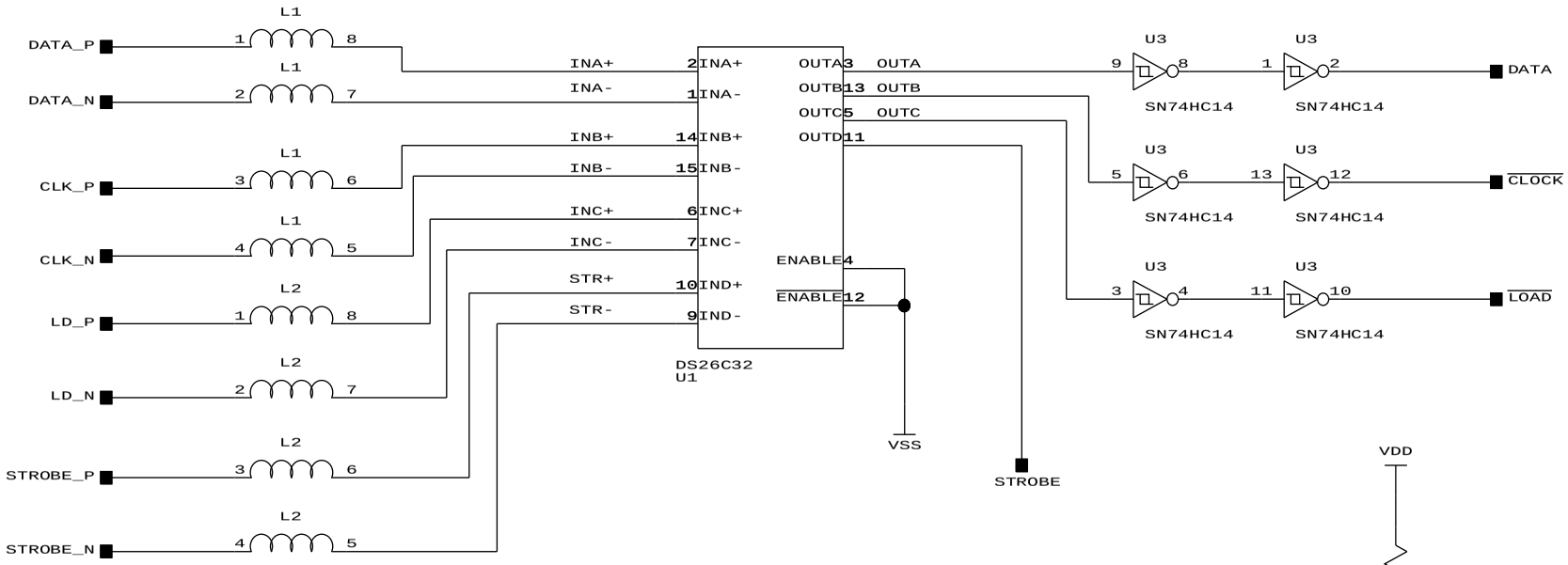
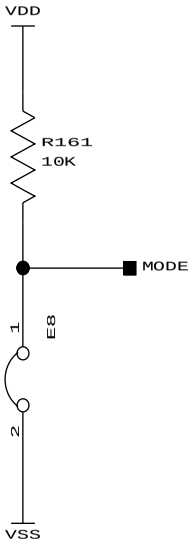
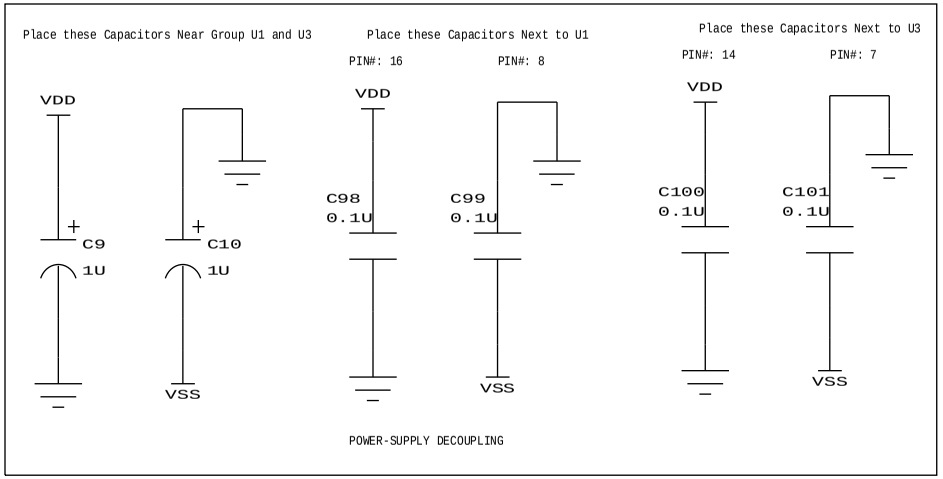




POWER U1		
PIN#: 16	VDD	+2.5V
PIN#: 8	VSS	-2.5V

POWER U3		
PIN#: 14	VDD	+2.5V
PIN#: 7	VSS	-2.5V



@DATETIME=3-4-1997_13:10

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Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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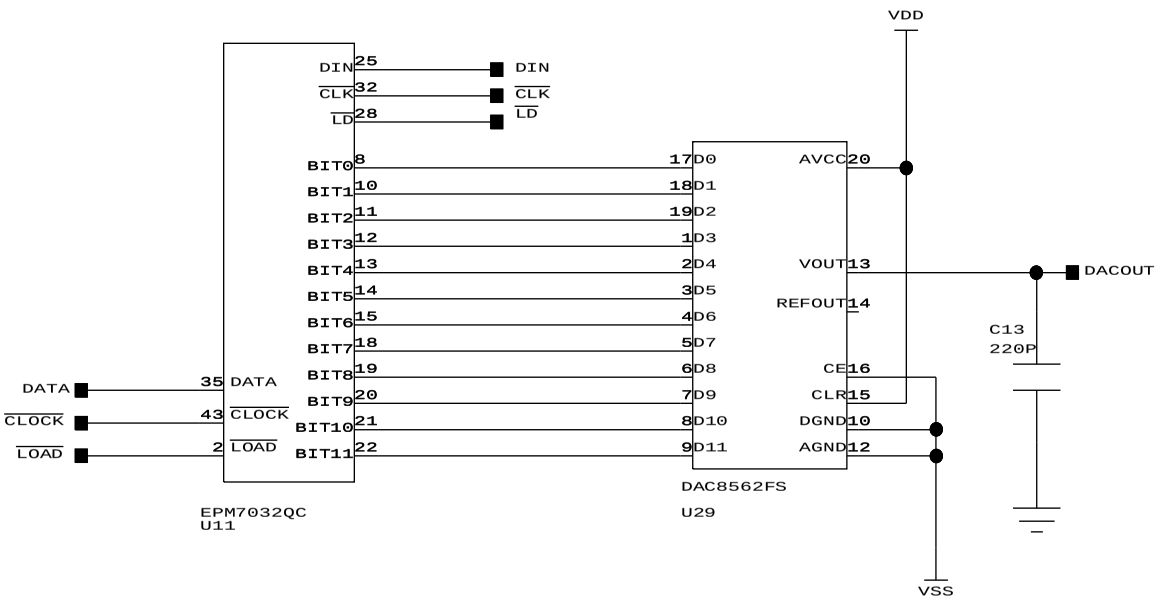
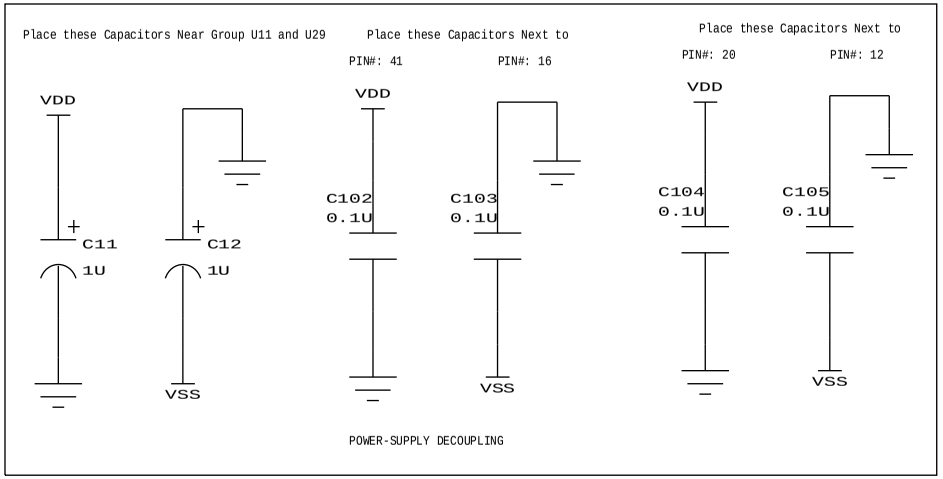


POWER U11 and U29		
PIN#: 9,17,29,41	VDD	+2.5V
PIN#: 4,16,24,36,37,38,39,40	VSS	-2.5V



@DATETIME=3-15-1997_7:43

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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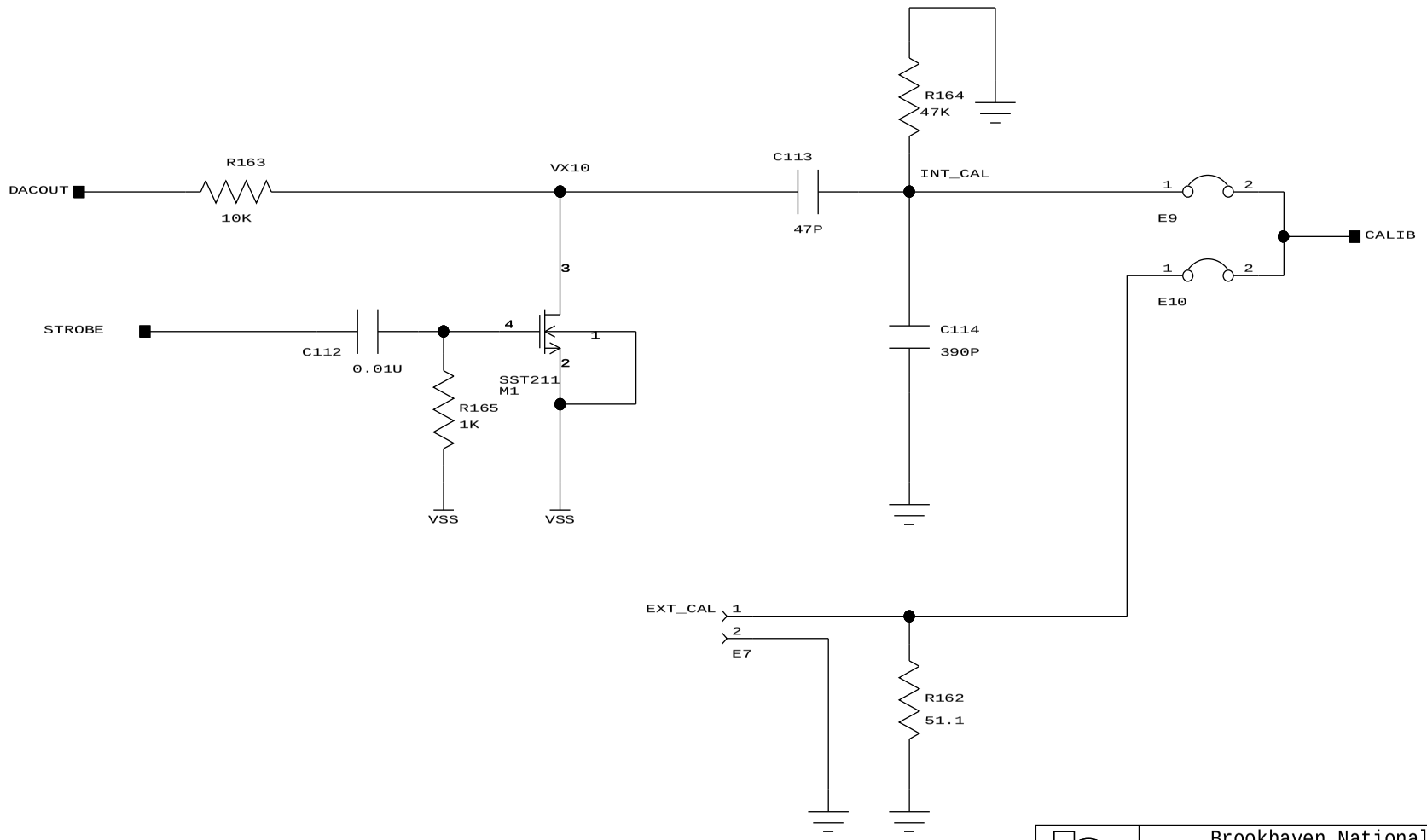

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

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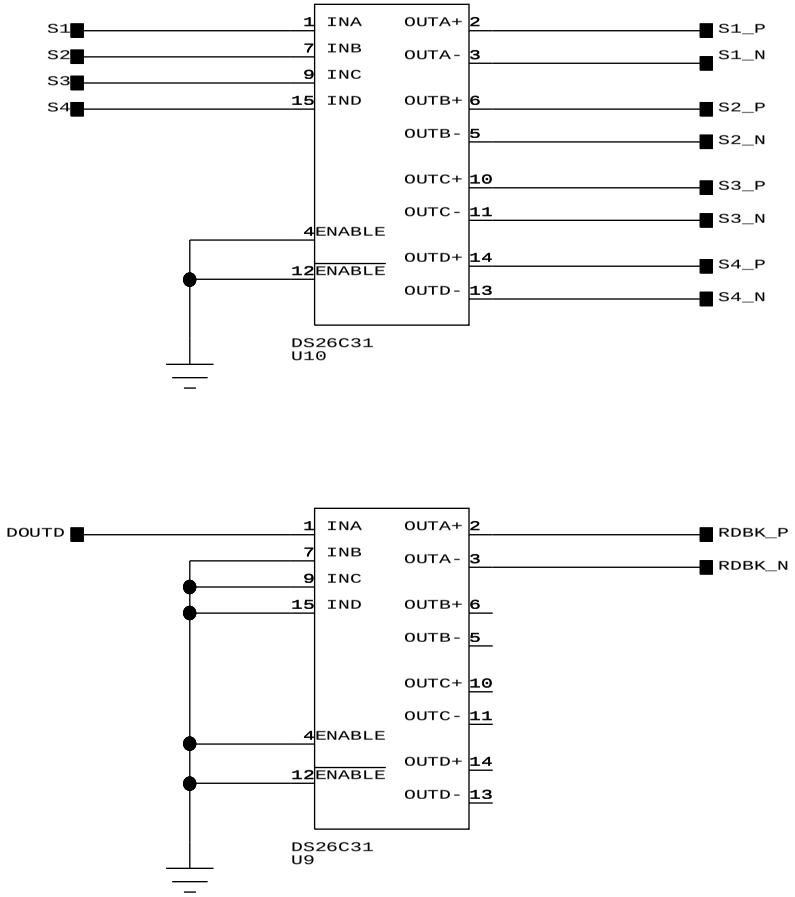
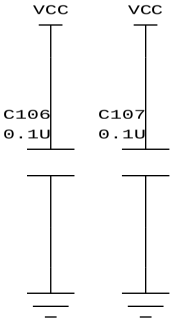
@DATETIME=3-15-1997_7:45



POWER U9 and U10		
PIN#: 16	VCC	+5V
PIN#: 8	GND	0V

Place these Capacitors Next to U9 and U10

PIN#: 16



POWER-SUPPLY DECOUPLING

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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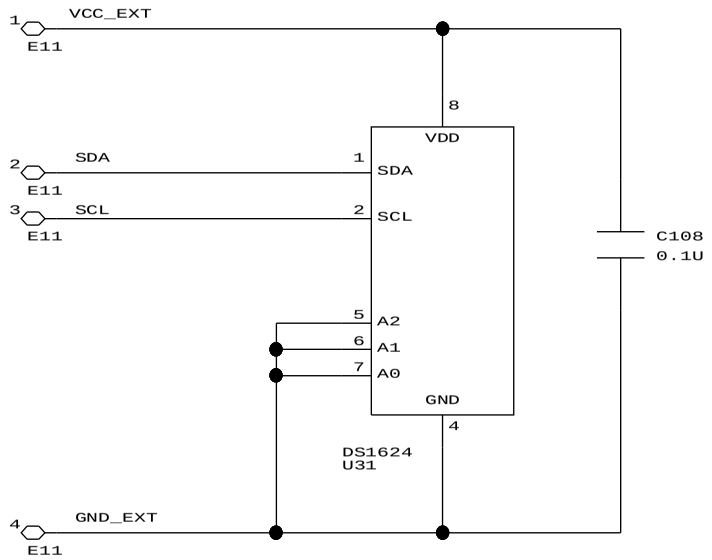
anand@bnl.gov

@DATETIME=3-4-1997_13:10



@DATETIME=3-4-1997_13:10

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Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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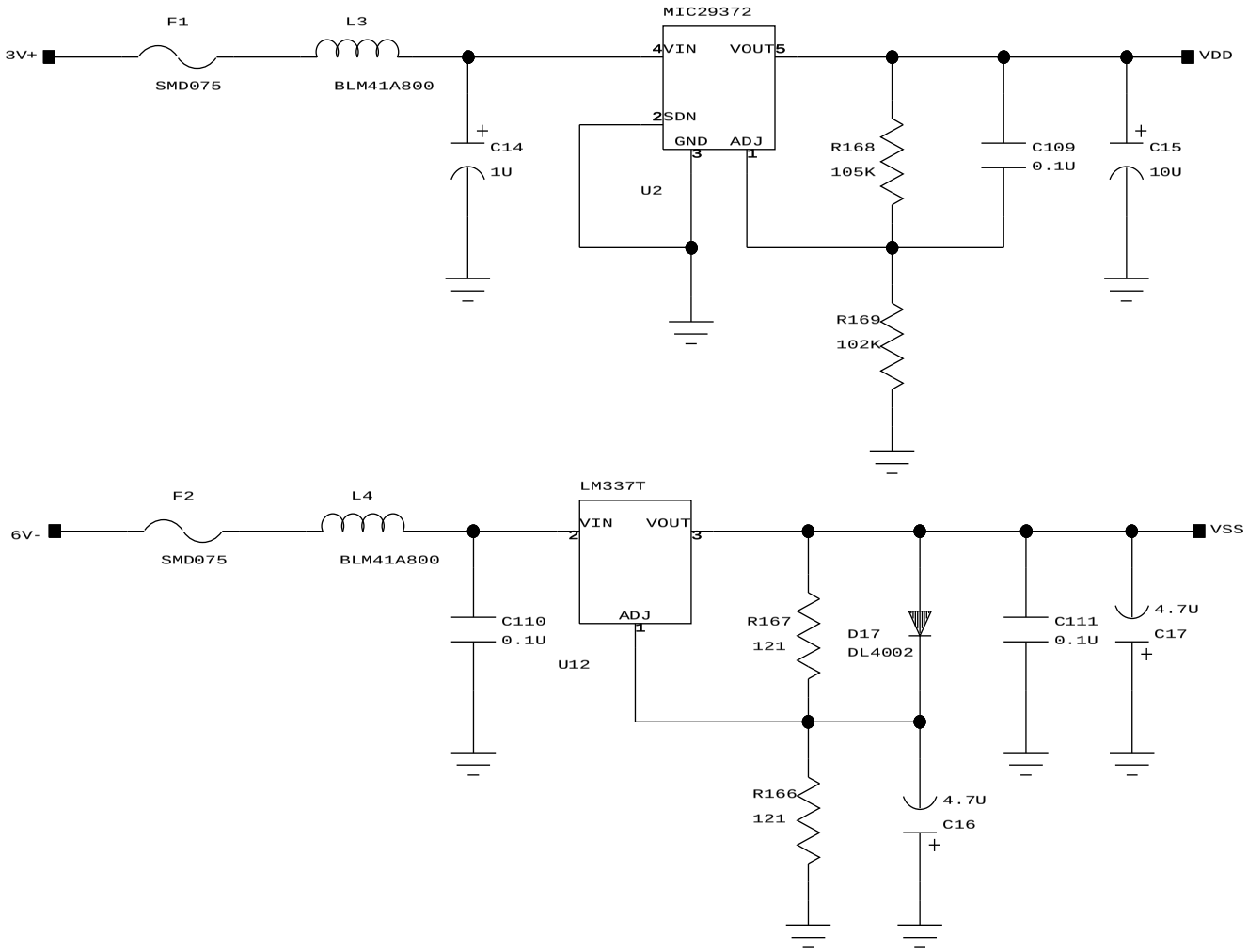

POWER SUPPLY REGULATION		
Unregulated Supply	Regulated Supply	Voltage
+3V	VDD	+2.5V
+6V	VCC	+5.0V
-6V	VEE	-5.0V
-6V	VSS	-2.5V

@DATETIME=3-4-1997_13:10

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Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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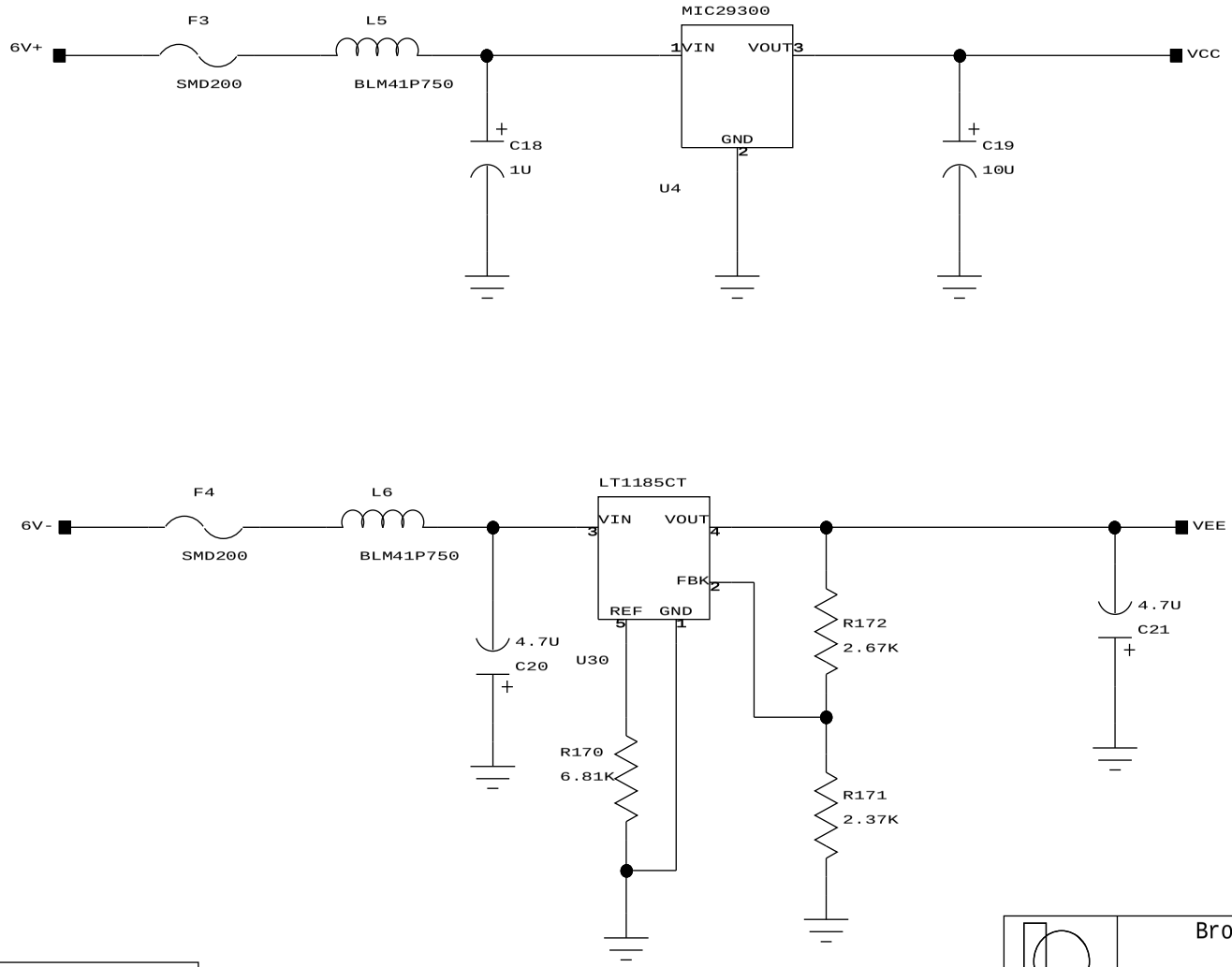

POWER SUPPLY REGULATION		
Unregulated Supply	Regulated Supply	Voltage
+3V	VDD	+2.5V
+6V	VCC	+5.0V
-6V	VEE	-5.0V
-6V	VSS	-2.5V

@DATETIME=3-10-1997_7:14

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Upton, NY 11973

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Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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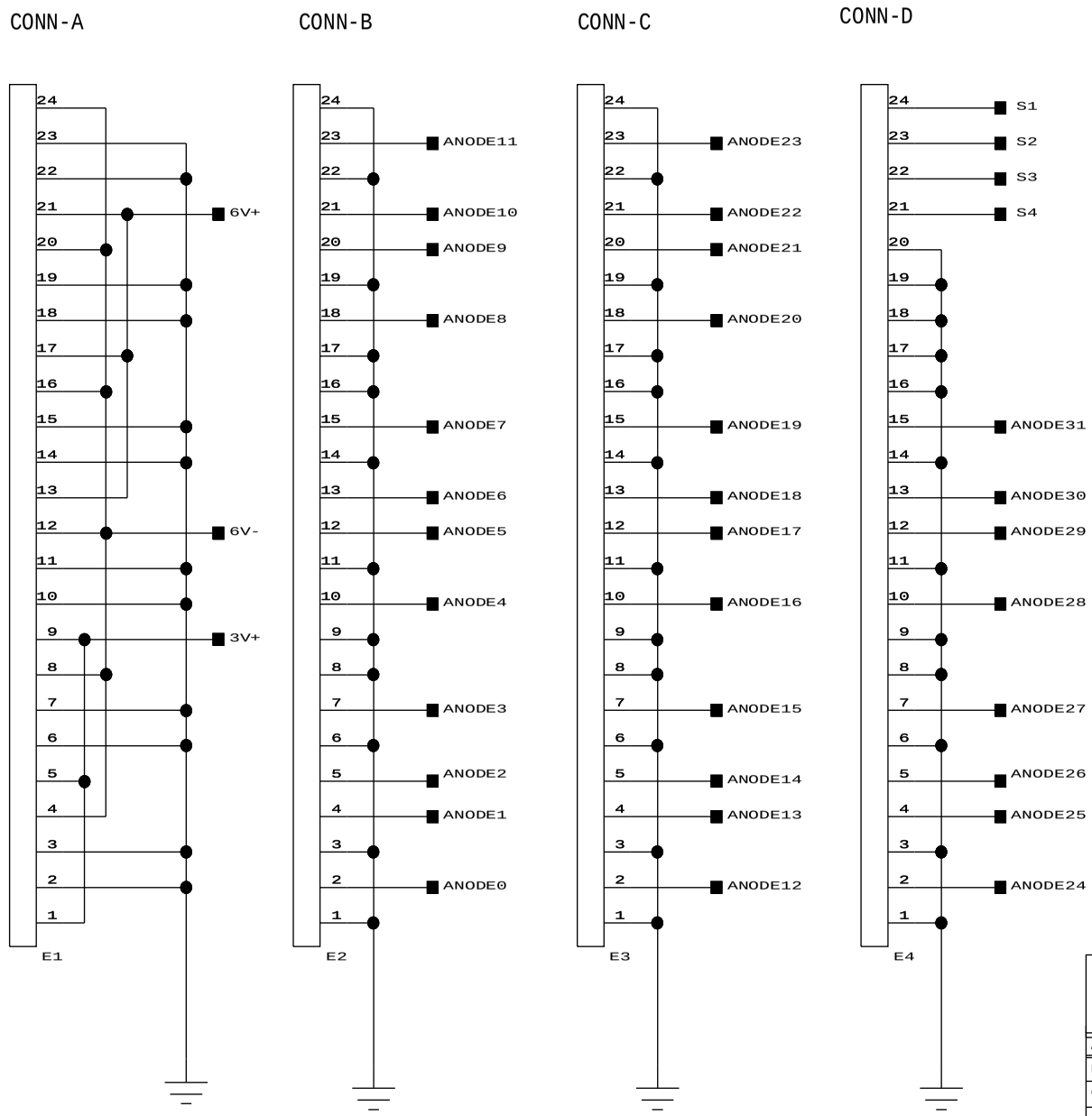

@DATETIME=3-4-1997_13:11

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Instrumentation Division
Upton, NY 11973

Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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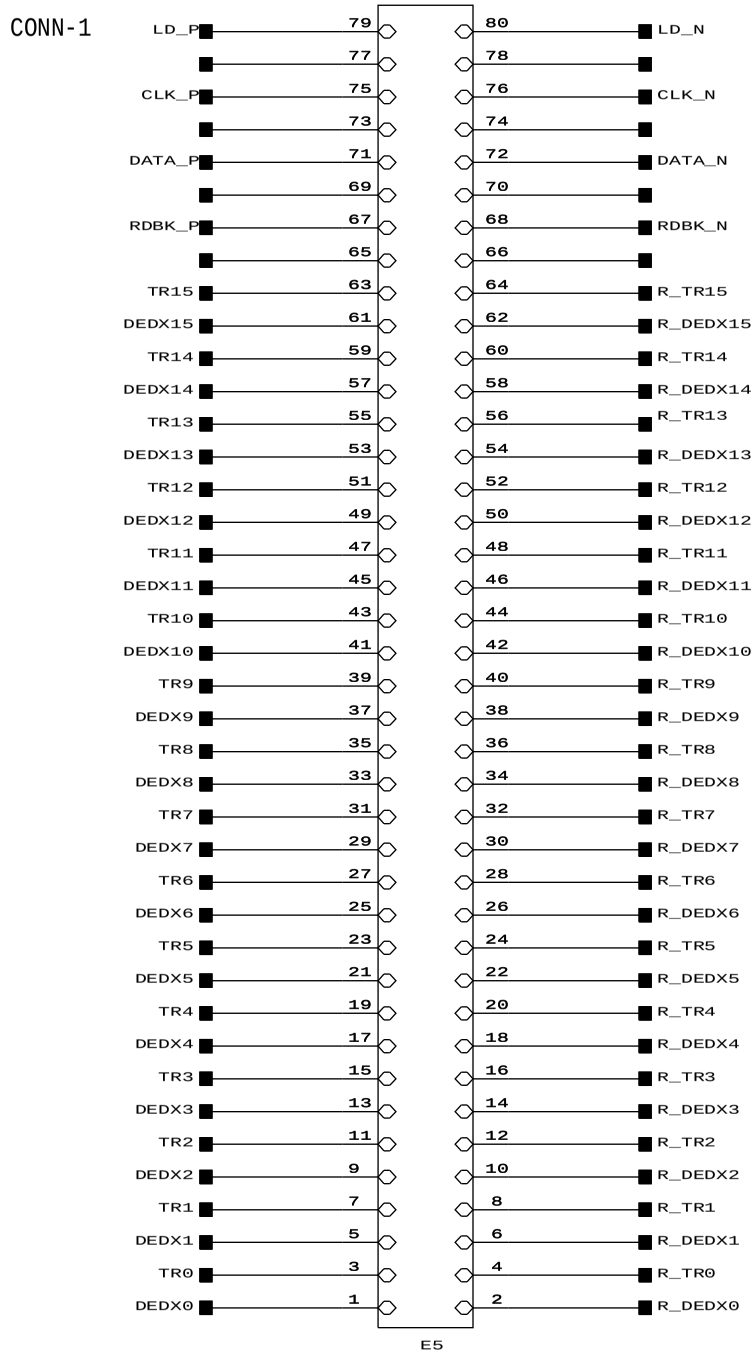

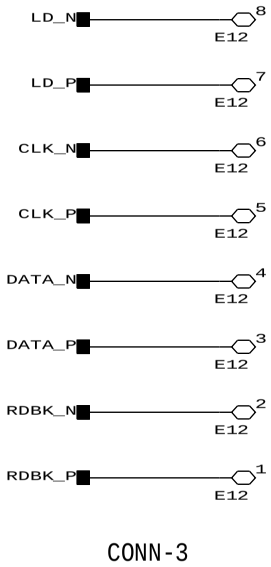

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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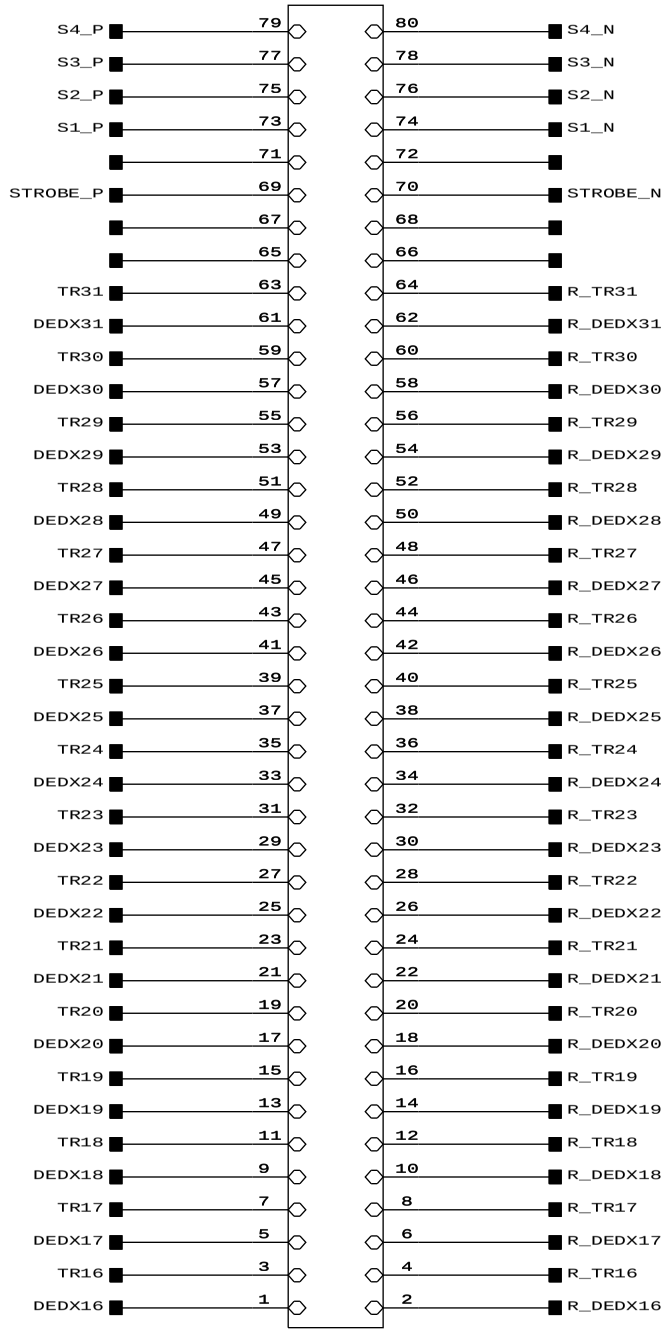
CONN-2



@DATETIME=3-4-1997_13:11

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Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	3
SCALE	

TEC-PS REV2

Drawn By:
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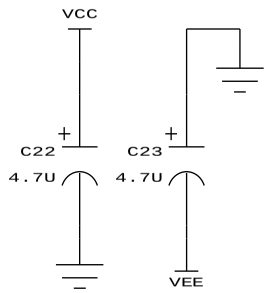
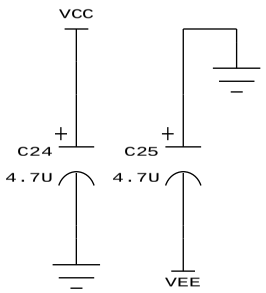
Place these Capacitors Near Group
U13, U14, U15 and U16



POWER-SUPPLY DECOUPLING FOR LINE DRIVERS

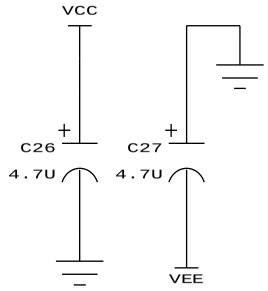
Place these Capacitors Near Group
U17, U18, U19 and U20



POWER-SUPPLY DECOUPLING FOR LINE DRIVERS

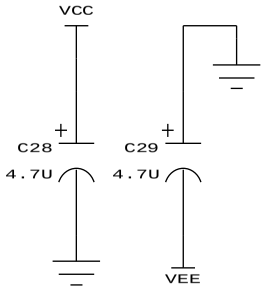
POWER-SUPPLY TEST POINTS

Place these Capacitors Near Group
U21, U22, U23 and U24



POWER-SUPPLY DECOUPLING FOR LINE DRIVERS

Place these Capacitors Near Group
U25, U26, U27 and U28



POWER-SUPPLY DECOUPLING FOR LINE DRIVERS

@DATETIME=3-4-1997_13:11

Brookhaven National Laboratory Instrumentation Division Upton, NY 11973		
Approvals	Date	Drawing:
Drawn		PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Checked		
Issued		
SIZE	B	TEC-PS REV2
DWG NO:		
REV NO:	3	
SCALE		

Drawn By:
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Overview:

The PHENIX TEC- Preamp/Shaper CMOS Integrated circuit is designed for the PHENIX tracking system. The tracking system of PHENIX is designed to locate all charged tracks of interest within their fiducial volume, measure the particle momenta, help in identifying which of the tracks are electrons, and contribute trigger information to the PHENIX detector.

The sub-detector namely the Time-Expansion Chamber (TEC), for which the monolithic circuit is designed for preforms both particle Identification and tracking functions in PHENIX. Through measurement of charged particles ionization losses (dE/dx), the detector allows separation of Electrons from Pions over a momentum range of 250 MeV/c to 3.0GeV/c.

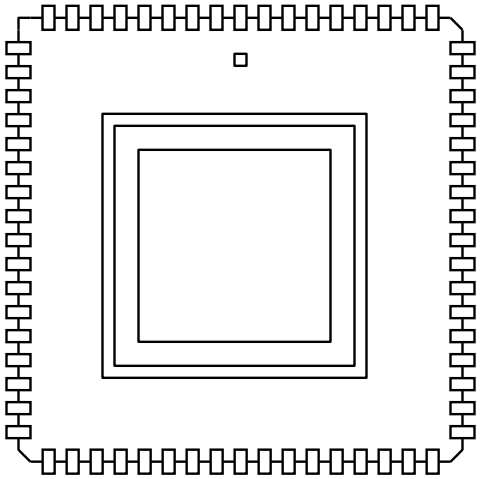
The TEC front-end electronics consists of a preamplifier and a 70ns shaping amplifier chain, is implemented in the monolithic circuit. The parameters of the electronics are determined by the requirements of both TEC's dE/dx and TRD operations. A shaping time of 70ns is chosen so that the FADC clock runs at a fraction of the shaping time to assure good position resolution. The Shaping time is also appropriate for the Transition Radiation (TR) measurements, where the shaping time chosen will allow containment of the total signal from the TR X-Ray absorbed by the gas chamber. The output of the shaper is split into two, so that the FADC has sensitivity for both low dE/dx signals (0.2 - 0.3 KeV for Xe gas), and the Transition Radiation signals (3 - 10 Kev for Xe gas). The preamplifier-shaper electronis is designed for 70ns shaping time and a FWHM < 100ns. The ENC to be less than 1500 electrons (70ns, 30-40pF) to ensure Electron - Pion separation. The shaping function is unipolar, with a Semi-Gaussian impulse response

Features:

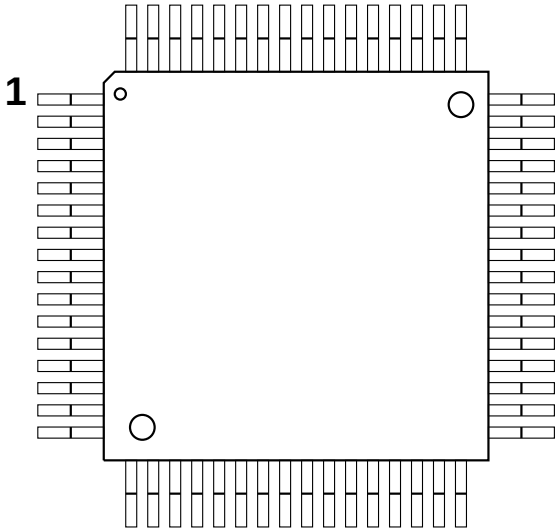
♦Multi-Channel (Eight).
♦Low and High gain outputs for TR and dE/dx.
♦Onchip Calibration capacitors for every channel.
♦Digitally programmable calibration mask.
♦Digitally programmable peaking time, 4 steps.
♦Digitally programmable gain, 8 steps.
♦Digitally programmable Tail cancellation, 8 steps.
♦Digitally programmable Channel masks.
♦All programmable bits implemented using serial interface logic, and chips can be daisy chained.
♦Low Power, 44mWatts /channel.
♦Size: 3.5mm x 5mm.

Package Description:

68-J-Leaded Ceramic:



64 PQFP:



Pin Description:

Pin descriptions for both the packages are showing in Table 1

Table 1: Pin Description

68 LDCC	64 PQFP	PIN
1	8	RET 4
2	9	IN 3
3	10	RET 3
4	11	IN 2
5	12	RET 2
6	13	IN 1
7	14	RET 1
8	15	IN 0
9	16	RET 0
10	18	VDD
11	19	OBIAS
12	20	VDDP1
13	21	VSSP1
14	22	GNDS1
15	23	DIN
16	24	VDDP1
17	25	LD
18		
19	26	CLK
20	27	MODE
21	28	DOUT
22	29	CALIB
23		
24	30	VSS
25	32	VSSS1
26	33	DE/DX 0
27	34	TR 0
28	35	DE/DX 1
29	36	TR 1
30	37	DE/DX 2
31	38	TR 2
32	39	DE/DX 3
33	40	TR 3
34	41	DE/DX 4
35	42	TR 4

Table 1: Pin Description

68 LDCC	64 PQFP	PIN
36	43	DE/DX 5
37	44	TR 5
38	45	DE/DX 6
39	46	TR 6
40	47	DE/DX 7
41	48	TR 7
42		
43		
44	50	VSSS2
45		
46		
47	52	DOUT
48		
49		
50	54	REF 2
51	55	REF 1
52	56	VB 2
53	57	VB 1
54	58	VDDS2
55	59	GNDS2
56	60	VSSP2
57	61	VDDP1
58	62	IBIAS
59	64	RBIAS
60		
61		
62	**1**	IN 7
63	2	RET 7
64	3	IN 6
65	4	RET 6
66	5	IN 5
67	6	RET 5
68	7	IN 4

N/C: 68 LDCC: 18,23,42,43,45,46,48,49,60,61
N/C: 64 PQFP: 17,31,49,51,53,63

Pin Details:
Analog Section:

IN [0:7]: Preamp Inputs channel 0 to channel 7.
RET [0:7]: Preamp Returns channel 0 to channel 7.

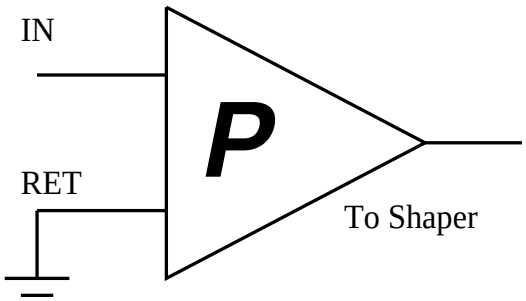


Fig 1. Preamplifier.

TR[0:7]: Transition Radiation output.
dE/dx[0:7]: Ionization energy loss output [x5].

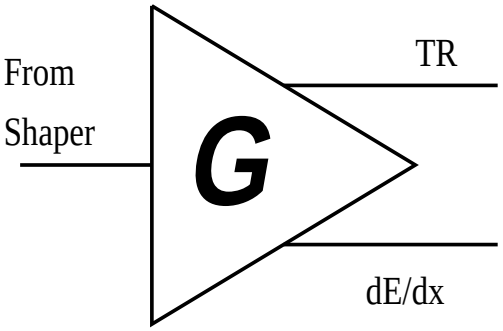


Fig 2. Output gain stage.

REF 1 and **REF 2:** DC offset correction control, if unused connected to GND. Should be decoupled.

CALIB: Calibration signal input.

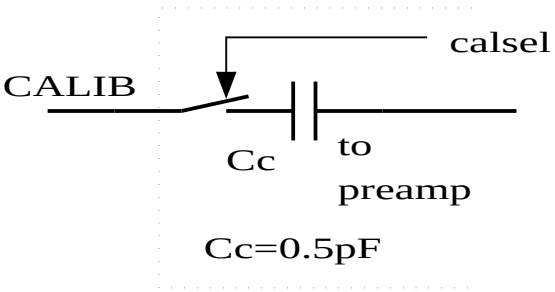


Fig 3. Calibration module.

The CALIB is the external signal applied to the chip for calibration, The Calibration capacitor used on chip is 0.5pF, and the calibration switch for each channel is selected using serial configuration.

IBIAS, RBIAS, OBIAS: Shaping stage Bias lines.
VB1 and VB2: Preamplifier Bias lines. These lines should be decoupled using 0.1uF ceramic chip capacitors close to the pins, as shown below.

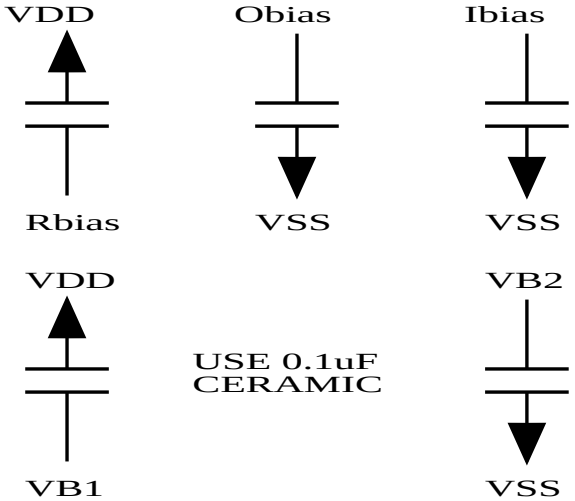


Fig 4. Bias line decoupling.

Digital Section:

CLK: Serial interface registers shift clock, (Negative edge triggered registers).
DIN: Serial interface Data input
DOUT: Serial interface Data output to daisy chain and readback. [4mA output driver].
LD: Parallel registers Load signal, (Negative edge triggered registers).
MODE: Serial interface function selector,
Mode = 0; Default all channels enabled with calibration on and with default circuit parameters:
Mode = 1; Serial interface enables, and data set it from download stream.

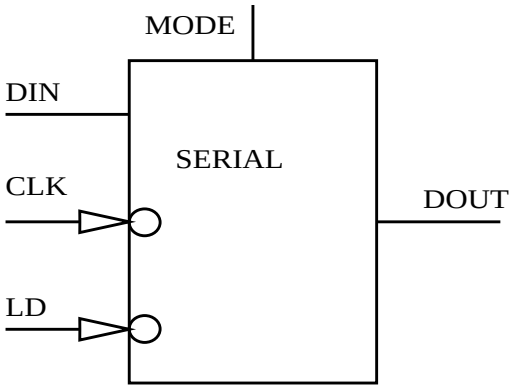


Fig 5. Serial Interface.

The mode line has a internal pull-down resistor of 8K to VSS.

Power Supply:

VDD: ESD ring positive supply (+2.5V).
VSS: ESD ring negative supply (-2.5V).
VDDP1, VDDP2: Preamplifier positive supply (+2.5V)
VSSP1, VSSP2: Preamplifier negative supply (-2.5V).
VDDS1, VDDS2: Shaper positive supply (+2.5V).
VSSS1, VSSS2: Shaper negative supply (-2.5V).
GNDS1, GNDS2: Shaper ground (0V).
Decoupling the supply pins are essential.

Serial Interface Module:

The serial interface module in the integrated circuit is used for setting circuit parameters of the preamp-shaper chain. The circuit parameters that are configured using the serial interface are 4 steps of Peaking time, 8 steps of ion tail cancellation and 8 steps of coarse gain adjustment.

The serial interface is also used to control two other functions namely the calibration and channel enable/disable mask. By default when at MODE=0 the IC is set to the following state.

Shaping Time: TP1:TP0 = 01
Ion Tail cancellation: TC2:TC1:TC0 = 011
Gain: G2:G1:G0 = 101
Calibration: channel 0 to 7: Enabled.
Channel 0 to 7: Enabled.

The internal architecture of the serial interface is shown in figure 6.

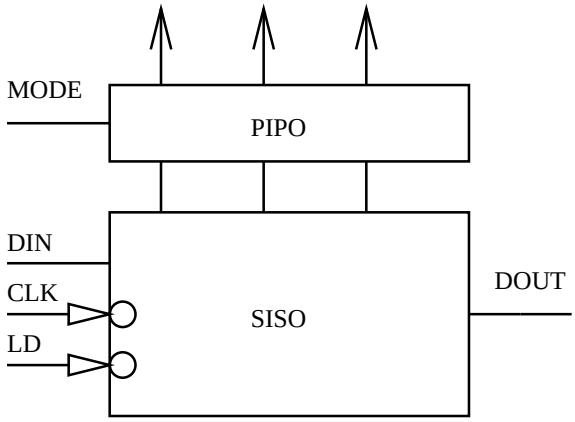


Fig 6. Internal architecture of the serial interface.

The serial interface is made up of a 24 bit, Serial-In-Serial-Out (SISO) shift register, another 24 bit Parallel-In-Parallel-Out (PIPO) latch, a output multiplexer for multiplexing serial data and default data using MODE control and a 1/2 cycle delay register.

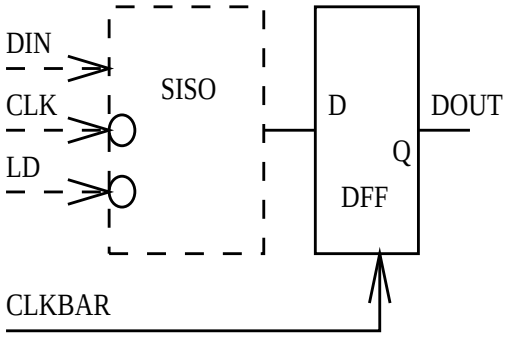


Fig 7. 1/2 cycle Delay cell.

The delay cell is necessary to preserve the data and clock timing offset, to ease the setup and hold conditions.

Serial control word:

The serial control word is 3 bytes long. The bit-wise information is shown in figure 8.

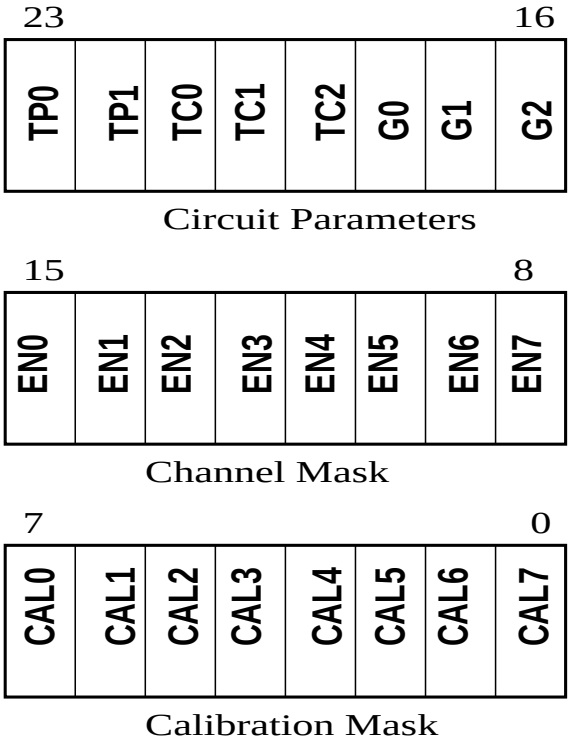


Fig 8. Serial Control word.

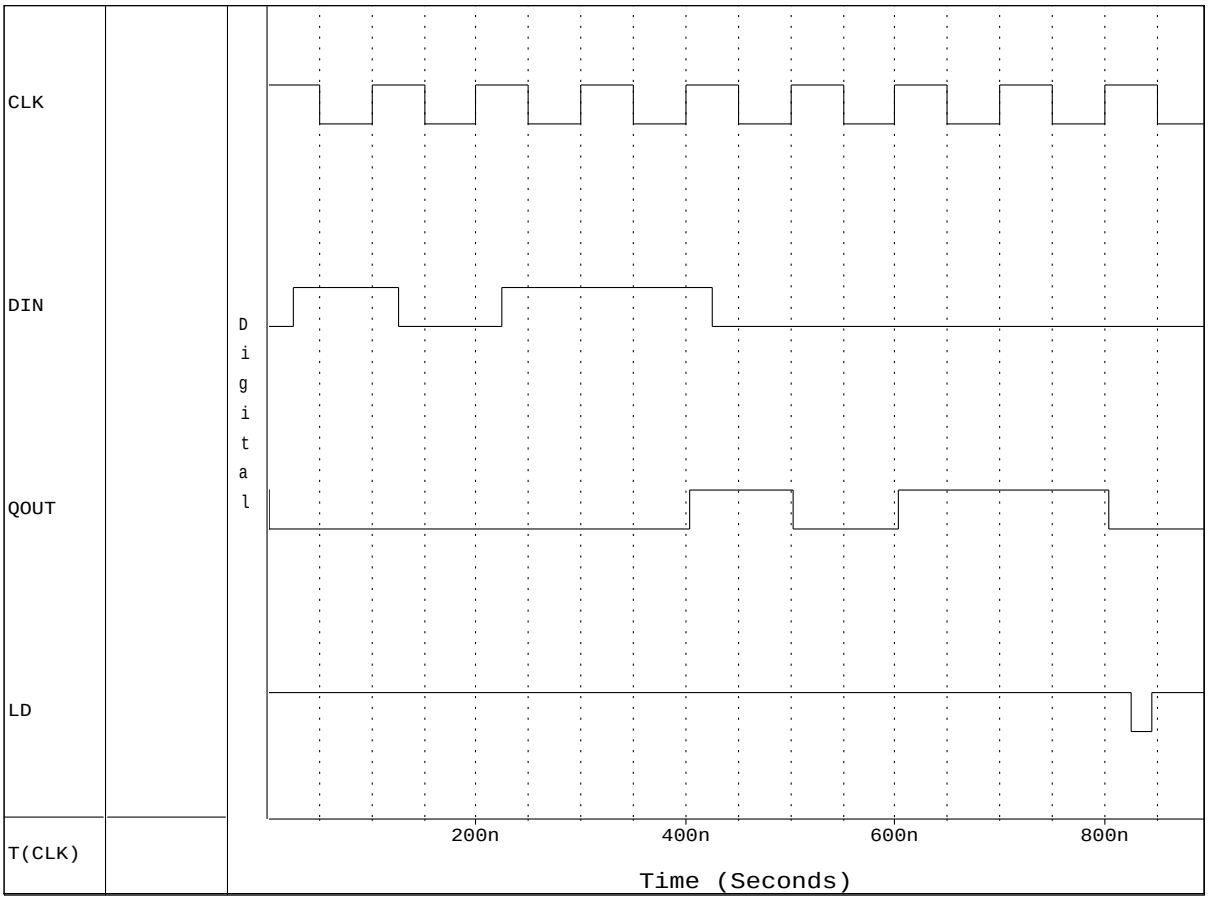


Fig. 9. Serial Interface Logic Diagram example.

The worst case timing condition taken from the SCMOS standard cell library for the D-Flip Flop used in the shift registers are shown in table 2.

Table 2: D-FF Timing

Parameter	Value
Setup time	3.56ns
Hold time	1.49ns
CLK pulse width	5.29ns

The inputs to the shift registers are buffered using Schmitt-trigger input pads. Noise immunity can even be further improved by adding non-inverting schmitt trigger inverter chain. A typical scheme is shown in figure 10, which consists of a RS-422 receiver to receive TTL signals and also for level translation to the compatible logic levels for the chip which is +2.5 (logic High) and -2.5 (logic Low)

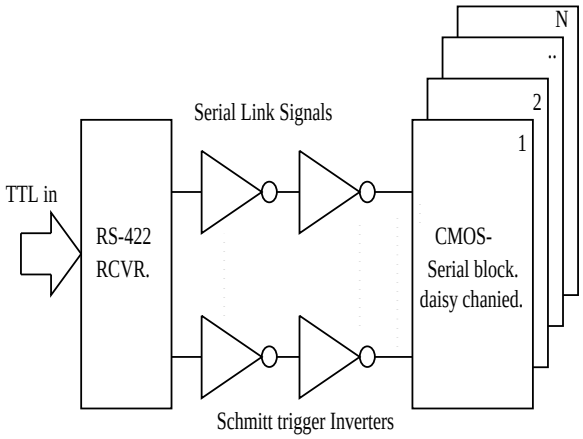


Fig 10. Typical Serial link scheme.

The data output of each TEC-PS can be daisychained, and the output driver can drive upto 4mA of current. The logic conversion of TTL to custom level of ±2.5V is done by the RS-422 receiver, running of ±2.5V.

Electrical Specifications:

Parameter		TYP	Note[a]
GAIN (mv/fC)	TR	4.3	Gain and Shaping time ranges for the dE/dx give below in mV/fC and nSecs respectively. Gain: 12 to 50 in 8 steps Shaping time: 60 to 120 in 4 steps
	dE/dx	21.3	
Shaping Time (nS)	TR	73.6	
	dE/dx	74.3	
Offset (mV)	TR	-3.63	
	dE/dx	-0.066	
ENC (r.m.s electrons) [Cdetector = 18pF]	TR	1697	
	dE/dx	1251	

a. There are 256 combinations of gain and shaping time due to Gain, Peaking and Tail cancellation settings only a few of the gain settings are listed here to show the gain range.

Power Supply:

Supply			Units
VDD	Voltage	+2.5	Volts
	Current	57	mA
VSS	Voltage	-2.5	Volts
	Current	52	mA
GROUND/RETURN	Current	5	mA

The power supply numbers above correspond to the multi-channel chip (8) and not a single channel. The electrical parameters were obtained under the following test conditions. Vdd = +2.5 V; Vss = -2.5V; REF1 = 0V; REF2 = 0V Each channel was tested by injecting a known charge, by applying a voltage step to the internal calibration capacitors, and the output was observed using a scope terminated at 50 Ω, The TR and dE/dx output was buffered using analog devices AD811, with a Gain = +1, operating from ±15V. The block diagram of the test setup is shown in figure 11.

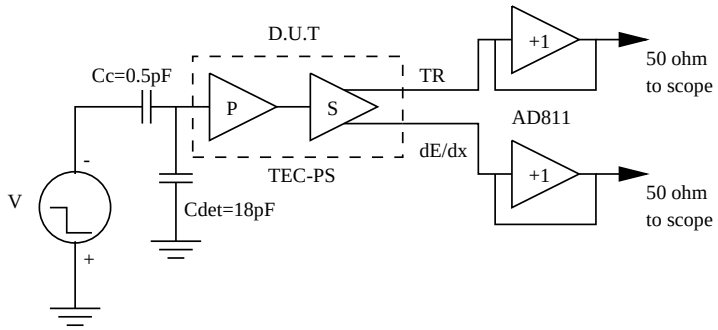


Fig 11. Test Setup for Electrical parameter measurement.

Figure 12, shows the two dE/dx and TR waveforms of a single TEC-PS channel injected with 100mV negative step into a 0.5pF injection capacitor,[charge of 50fC]. [Note the Vertical scale change].

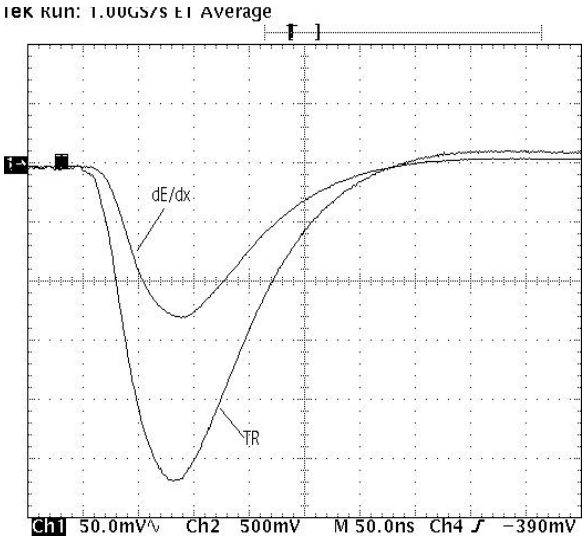


Fig 12. TR and dE/dx output waveform.

The CMOS can be tested for a first order working condition by monitoring the bias voltages, and the input bias condition of the pre-amplifier. Table 3 provides the bias voltages levels expected out of a functioning chip.

Table 3: Monitor outputs.

Node		Units
VB1	102	mV
VB2	-953	mV
RBIAS	-1.145	V
IBIAS	-1.136	V
OBIAS	-1.437	V
PREAMP-INPUT	1.187	V

The monitor output values are typical values.

Test Beam results:

Results obtained from the May 1996, Beam test at the AGS facility at BNL are shown in figures. 13 to 15. The TEC-PS was tested connected to one plane of the TEC in the AGS environment.

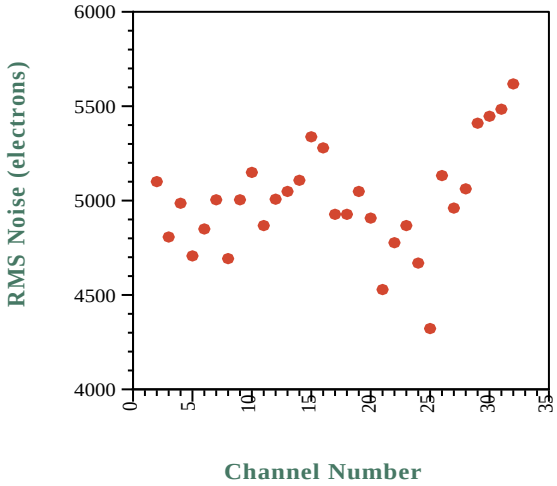


Fig 13. RMS noise in Chamber.

Figure 13, shows the total rms noise of the chamber and the CMOS electronics during.

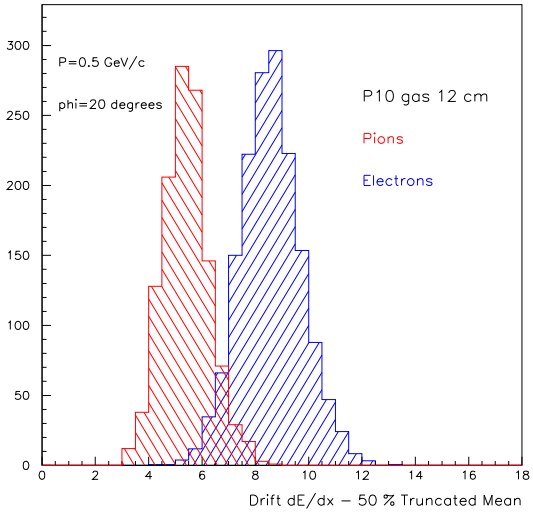


Fig 14. electrons-pions identification.

Electron and pions were identified using the Cherenkov and Lead Glass information. The dE/dx distribution was calculated by taking the average of the Nevis Fadc time bins eliminating the highest 50% of the FADC values.

Figure 15, pion efficiency figure: To evaluate the electron-pion separation we select a FADC value for which 90% of the electron are identified correctly and we calculate the "pion efficiency", the probability of misidentifying a pion as an electron. A comparison of the

"pion efficiency" hybrid electronics and the CMOS preamp shaper shows that overall the CMOS electronics performs better than the hybrid although the noise was on the higher side. We think this difference could be due to the CMOS better tail cancellation characteristics.

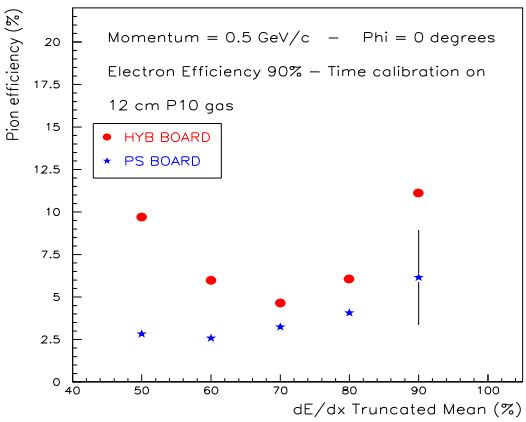


Fig 15. Pion efficiency of the TEC-PS.

Process specifications:

The CMOS preamp-shaper for the TEC is fabricated using Hewlett Packard's 1.2 micron Analog process with Poly-silicon resitors and linear capacitors, namely CMOS34/AMOSI.

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Original document page contains the layout of TECPS die

Obtain original document here

TECPS die layout

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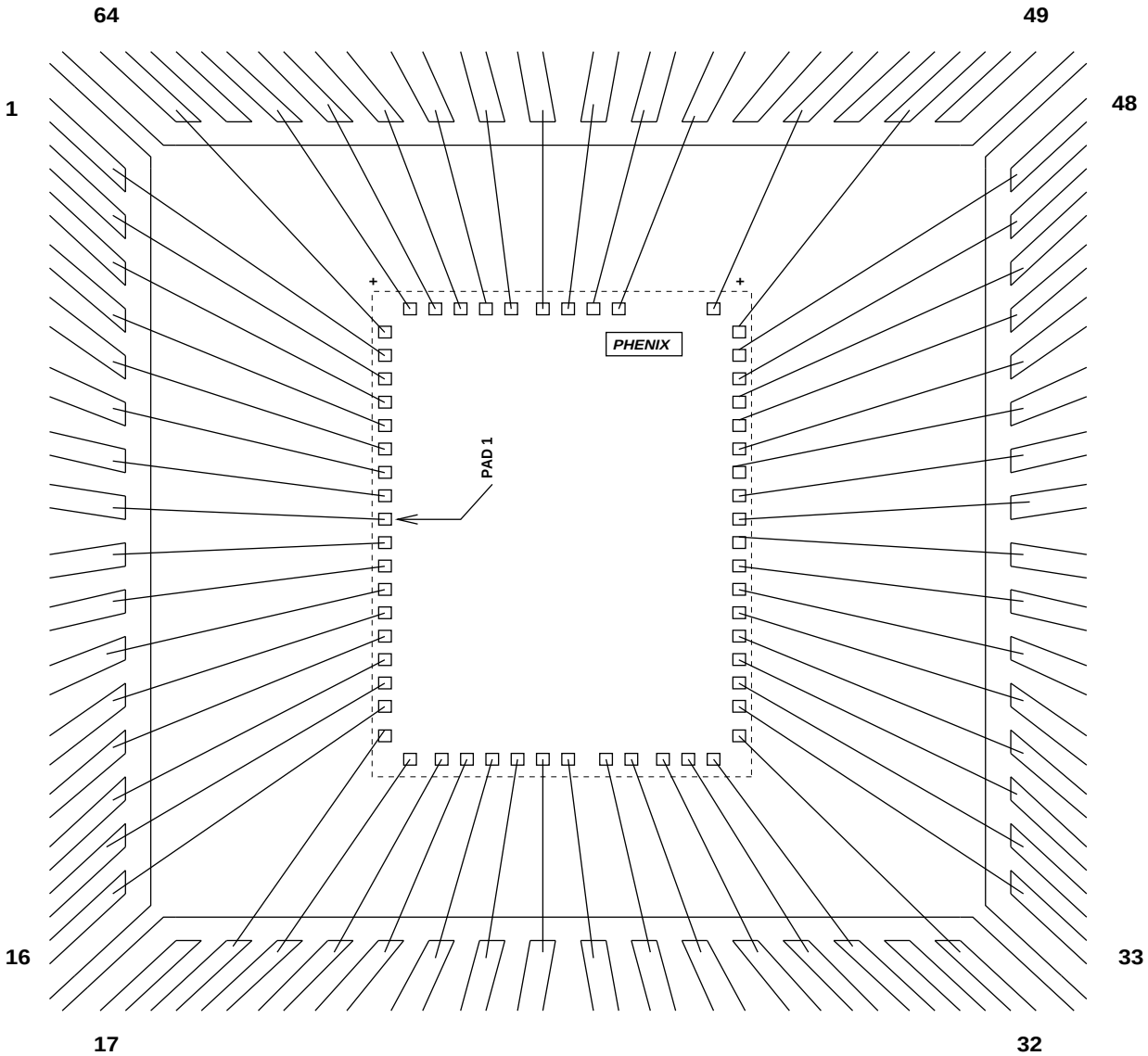
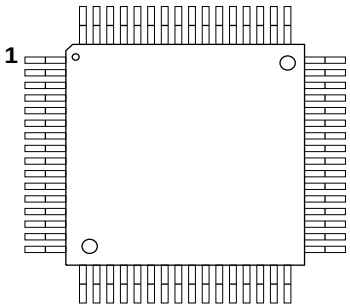
TEC-PS 64 pin PQFP Bonding Diagram:



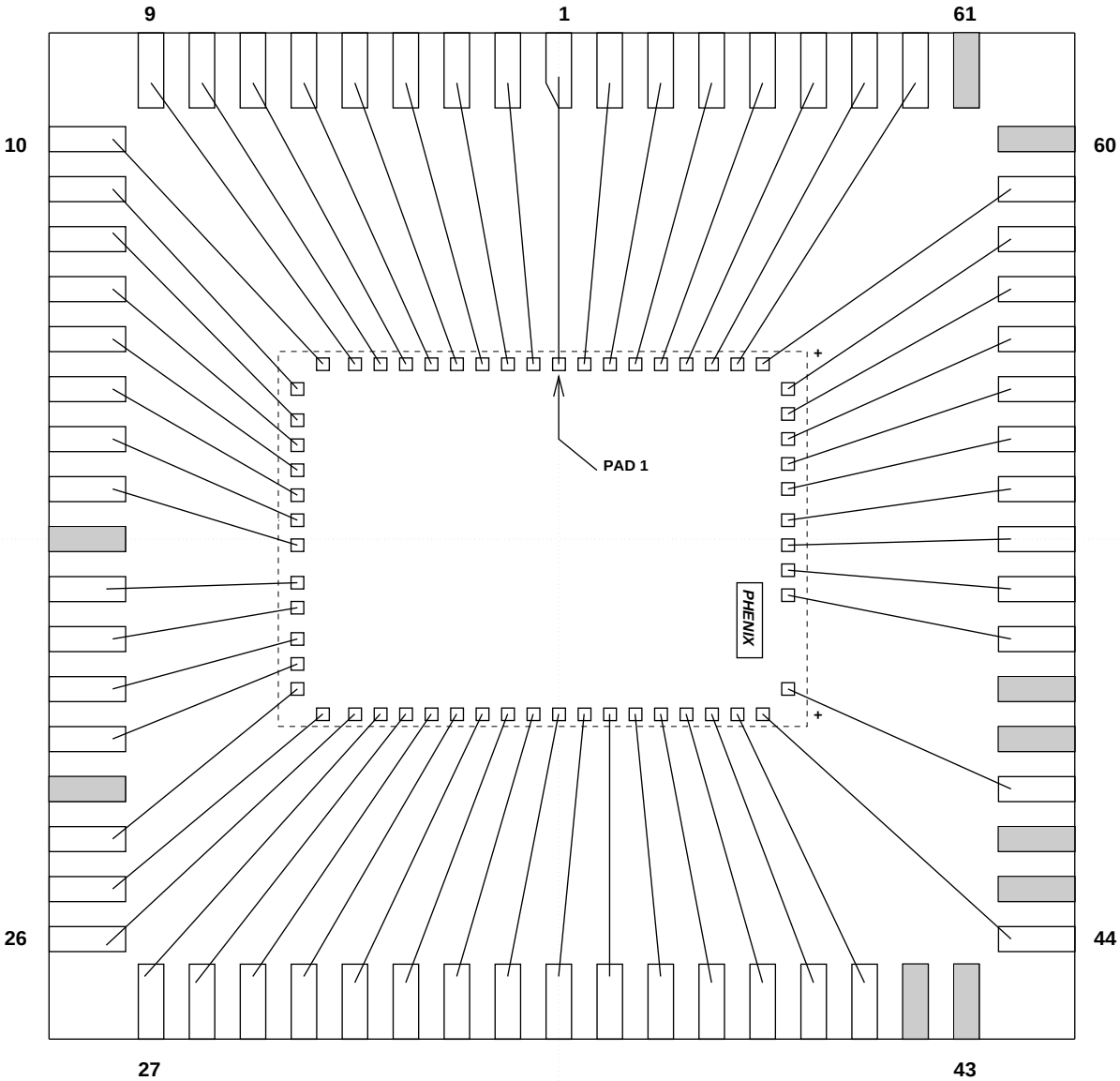


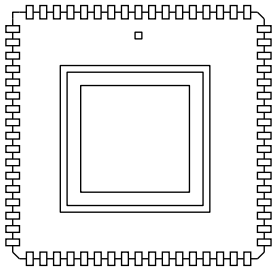
DIE SIZE: 4.491mm x 3.394mm (UNCUT)

Package Type: 64 Pin PQFP

Fig 17. TEC-PS 64 Pin PQFP Bonding Diagram.

TEC-PS 68 pin LDCC Bonding Diagram:



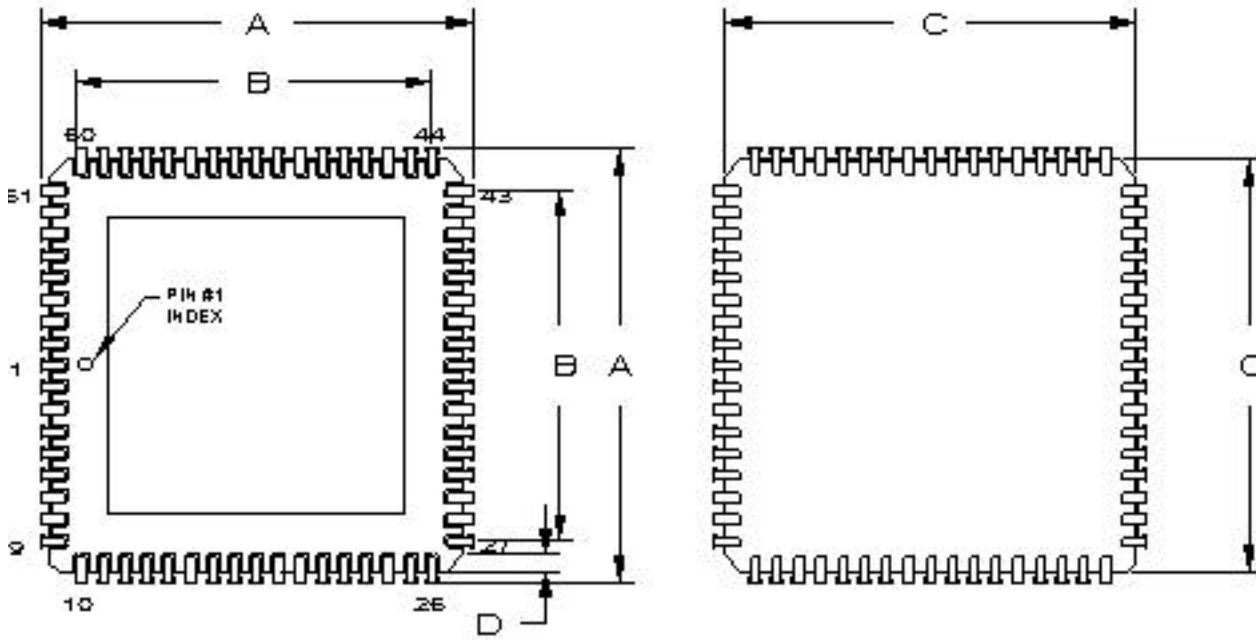


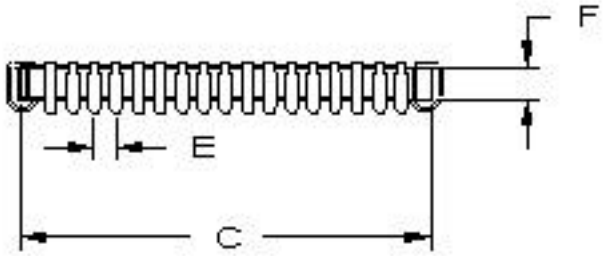
DIE SIZE: 4.491mm x 3.394mm (UNCUT)

Package Type: 68 J-LDCC, 0.400 SQ CAVITY

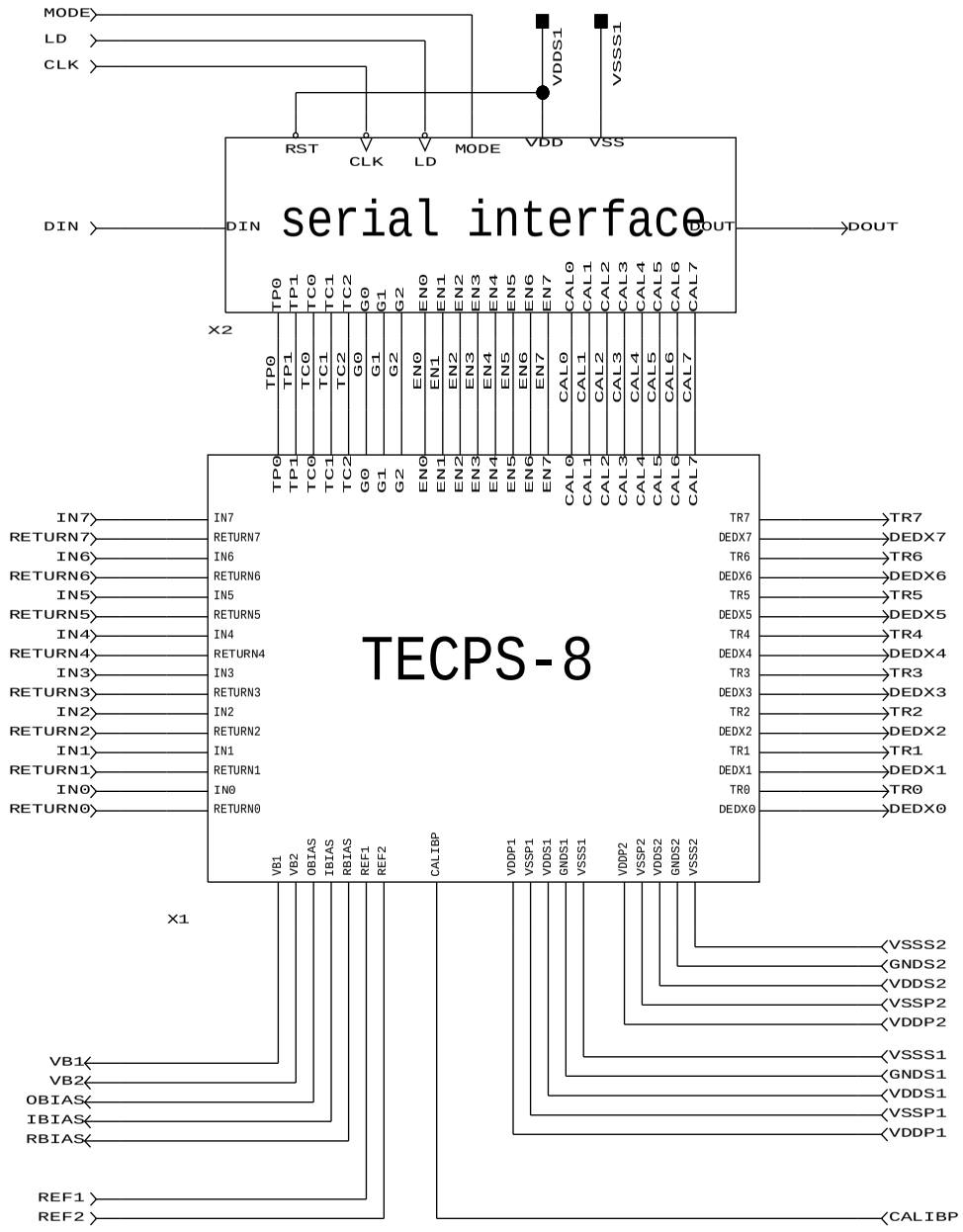
Fig 18. TEC-PS 68 pin LDCC Bonding Diagram.

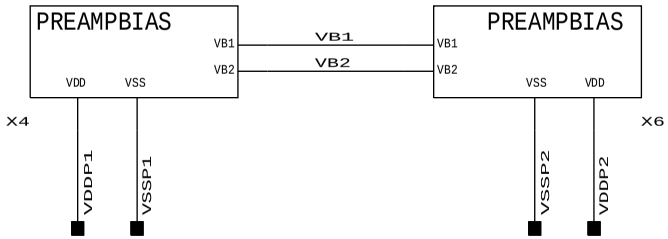
68 Pin LDCC Package:

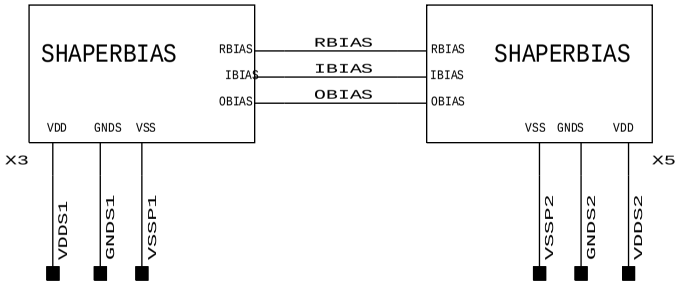




DIM	in mm.
A	25.15
B	20.52
C	24.1
D	0.50
E	1.27
F	2.03







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Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	
SCALE	

TOP Level
Schematic of IC31a Die

8-22-1996_12:13

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516-344-5486
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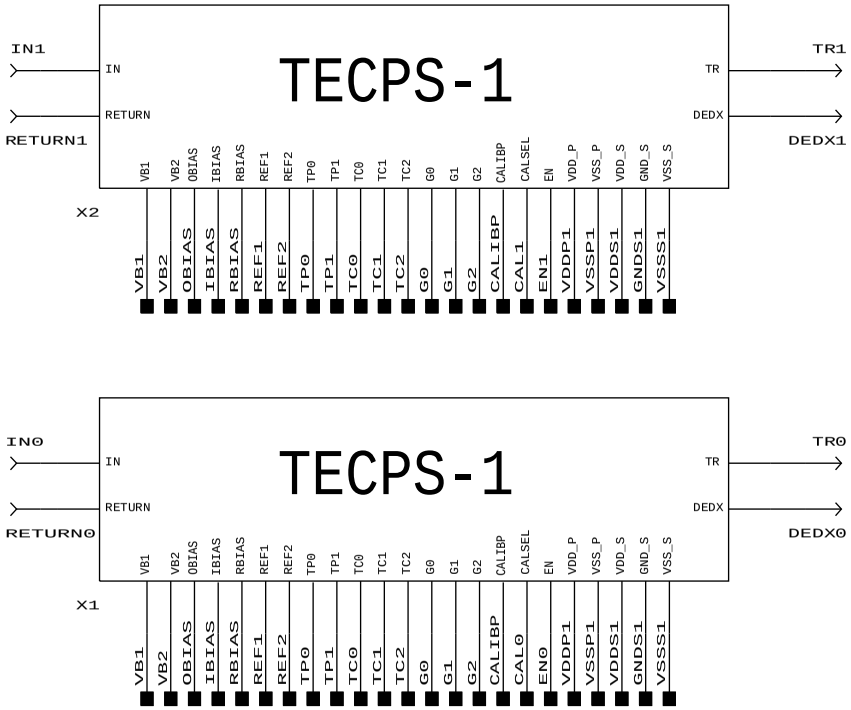
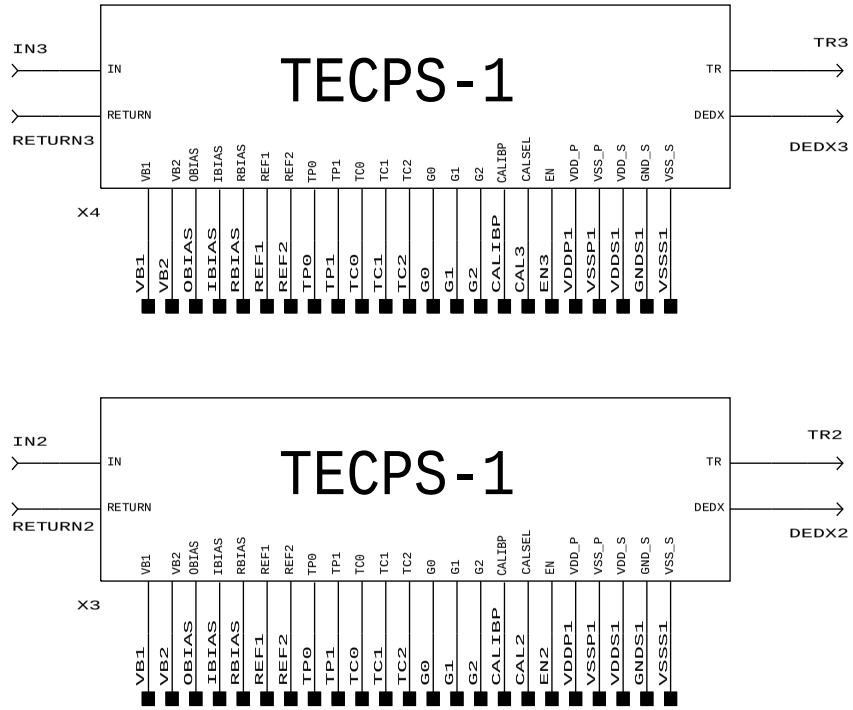
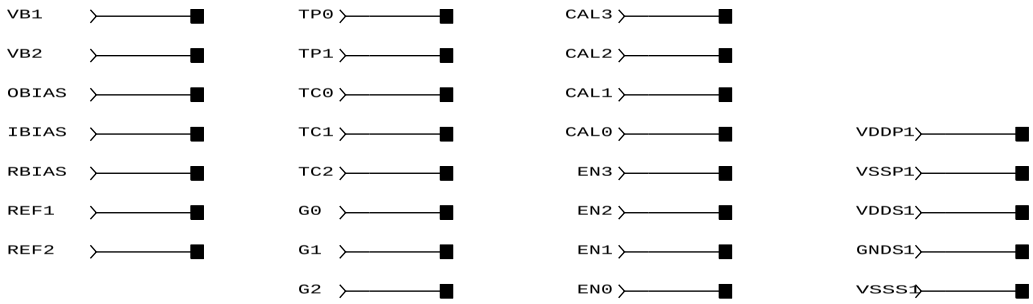
Sheet: 1 OF 1







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Approvals	Date	Drawing: PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
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SIZE	B	TOP Level Schematic of 8 Channel TECPS
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REV NO:		
SCALE		8-22-1996_9:23

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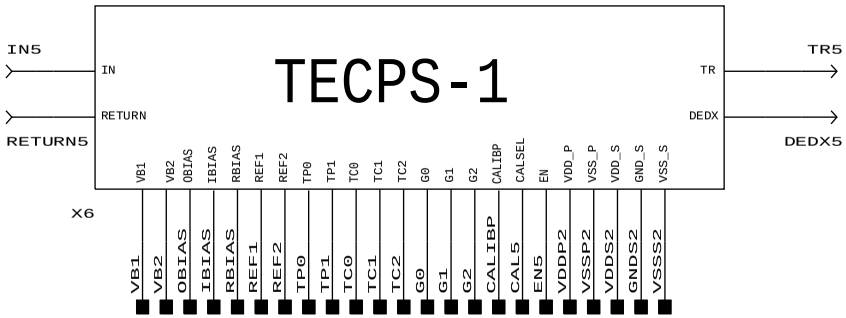

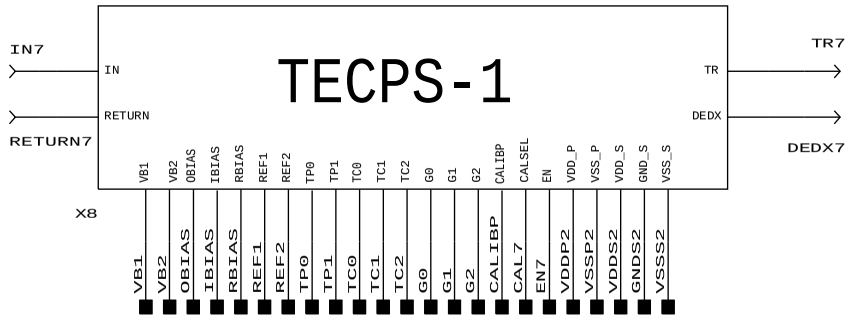

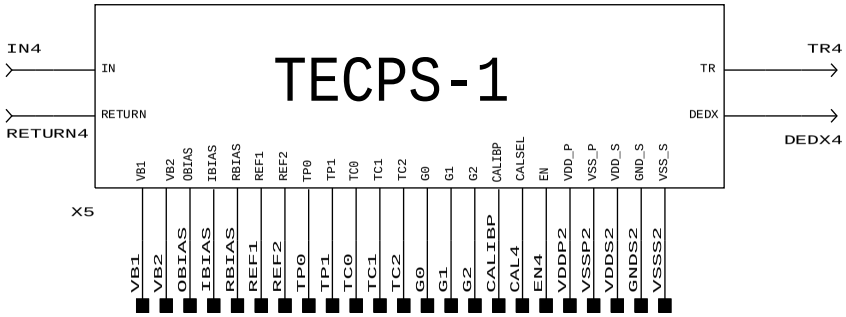

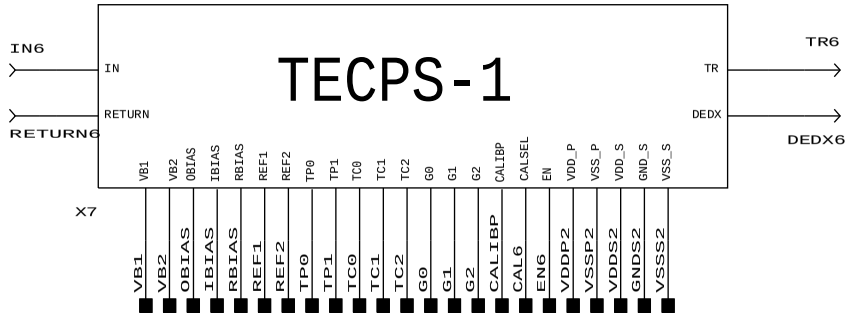

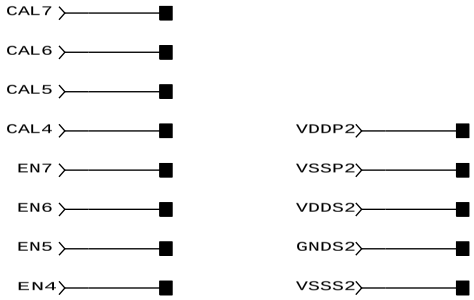

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Approvals	Date	Drawing:
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SIZE	B	TOP Level Schematic of 8 Channel TECPS	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
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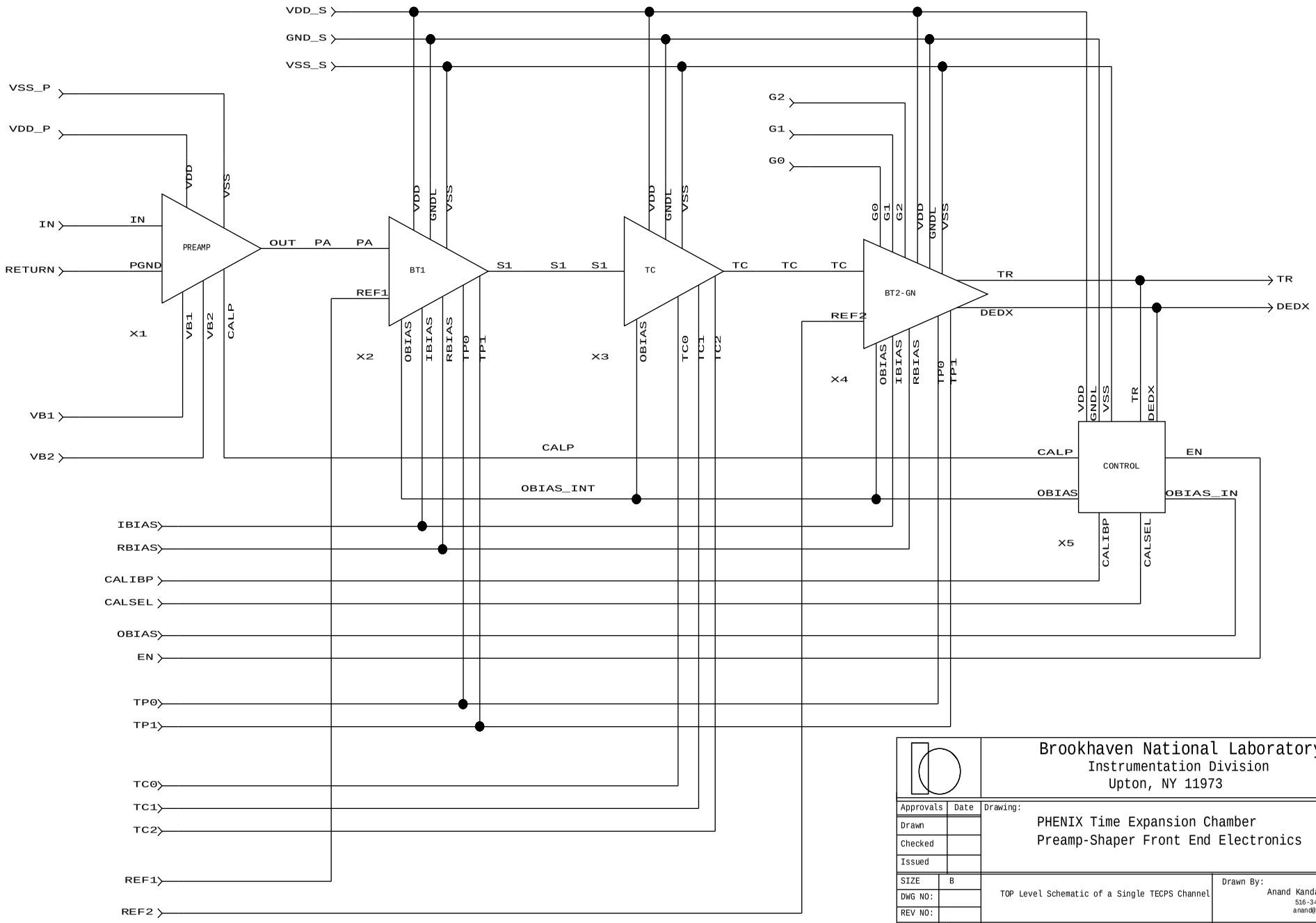

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

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TOP Level Schematic of a Single TECPS Channel

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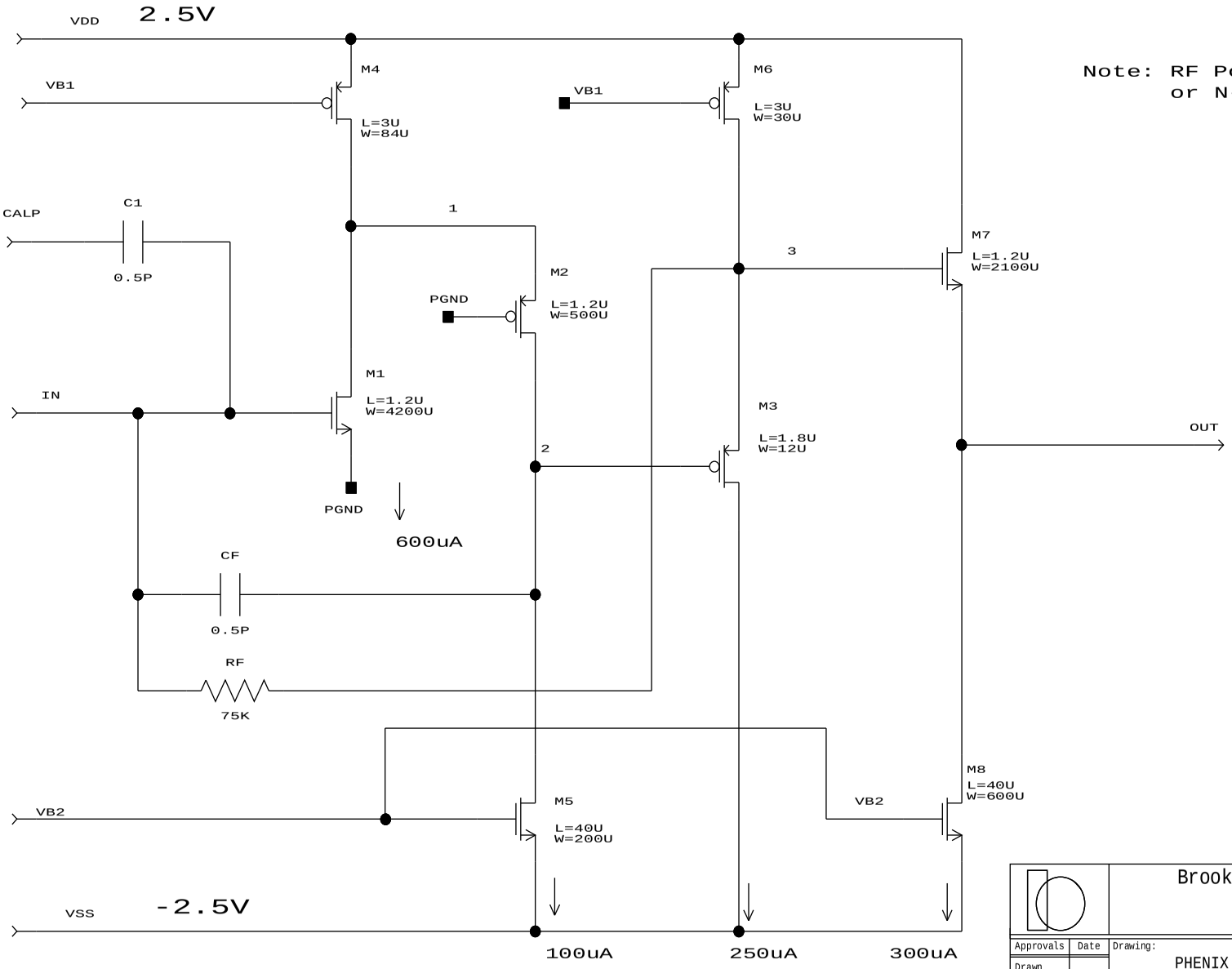

Note: RF Polysilicon, w=1.2 um
or N-well

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

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SCALE	

Preamplifier for PHENIX TEC

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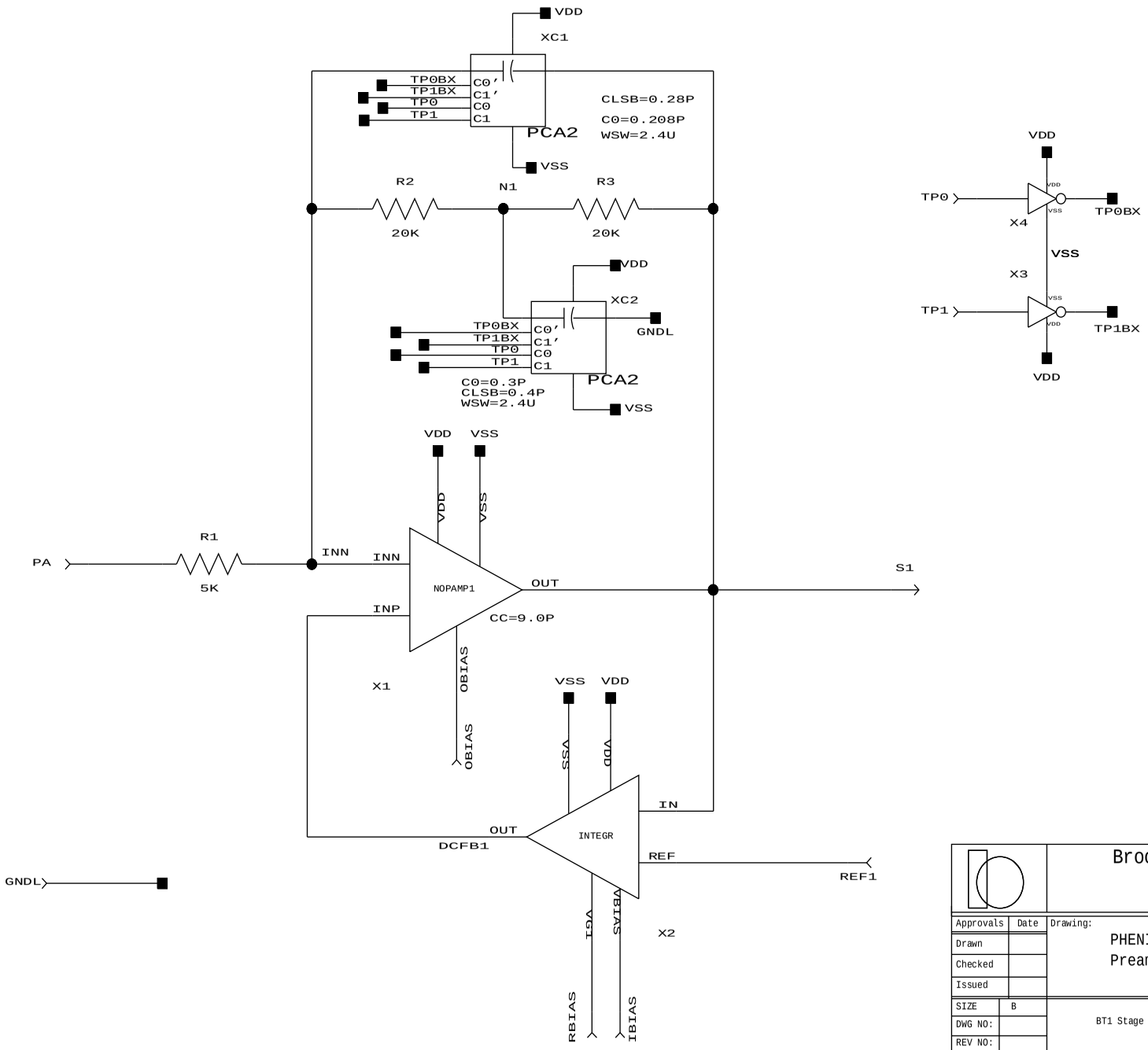

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Checked		Preamp-Shaper Front End Electronics
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SIZE	B	BT1 Stage of TEC-Shaper	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
DWG NO:			
REV NO:			
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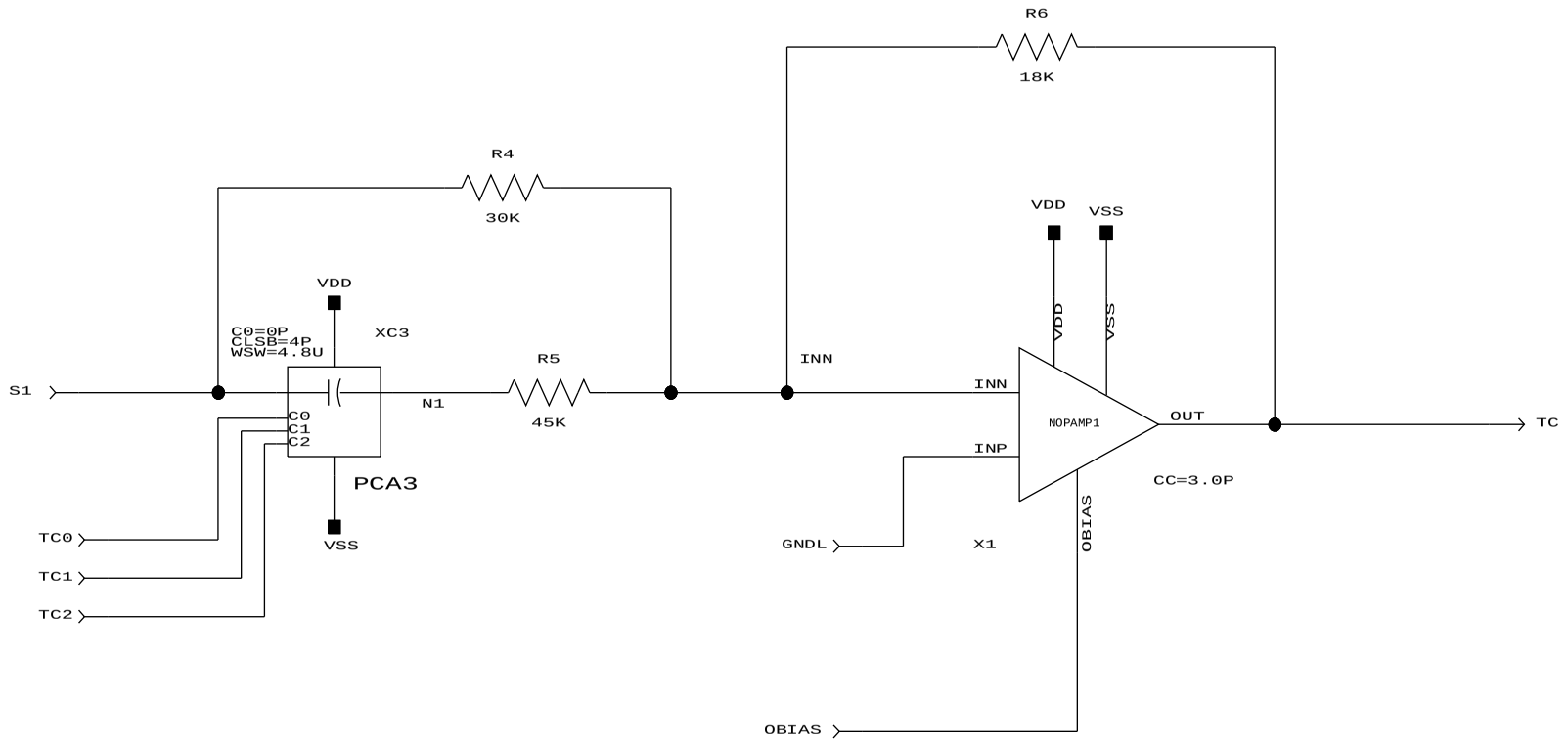

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Approvals	Date	Drawing:
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SIZE	B	Tail Cancellation Stage for TEC shaper
DWG NO:		
REV NO:		
SCALE		8-22-1996_12:39

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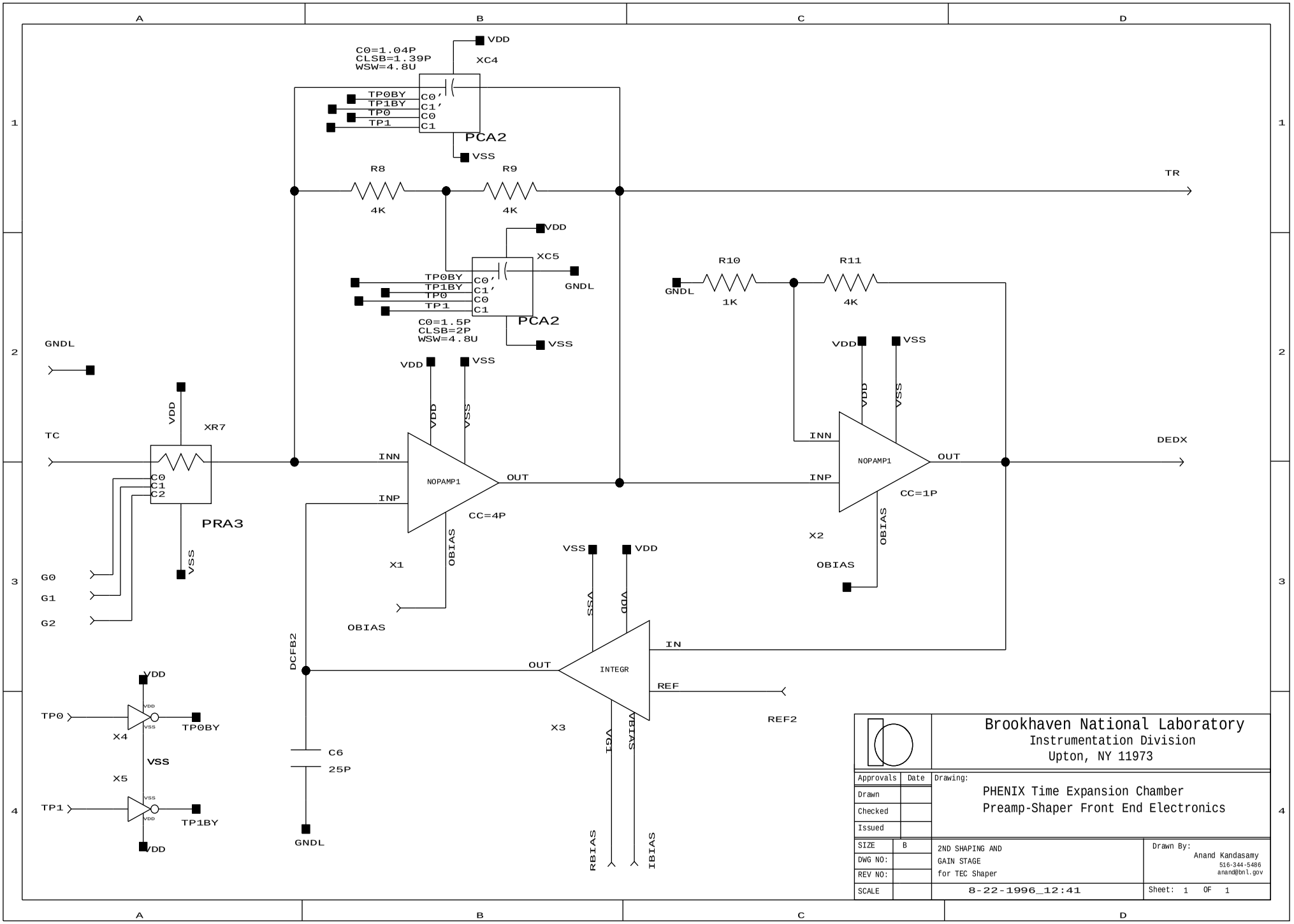
C0=1.04P
CLSB=1.39P
WSW=4.8U
VDD
XC4
TP0BY
TP1BY
TP0
TP1
C0'
C1'
C0
C1
PCA2
VSS
R8
4K
R9
4K
TR
VDD
XC5
GNDL
TP0BY
TP1BY
TP0
TP1
C0'
C1'
C0
C1
PCA2
C0=1.5P
CLSB=2P
WSW=4.8U
VSS
R10
1K
R11
4K
GNDL
GNDL
VDD
VSS
VDD
VSS
VDD
XR7
TC
C0
C1
C2
PRA3
VSS
G0
G1
G2
INN
INP
NOPAMP1
OUT
CC=4P
X1
OBIAS
OBIAS
VDD
VSS
VDD
VSS
INN
INP
NOPAMP1
OUT
CC=1P
X2
OBIAS
OBIAS
DEDX
VSS
VDD
VSS
VDD
IN
OUT
INTEGR
REF
REF2
X3
VG1
VBIAS
RBIAS
IBIAS
DCFB2
C6
25P
GNDL
VDD
TP0
X4
TP0BY
VSS
X5
TP1
TP1BY
VDD
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Date
Drawing:
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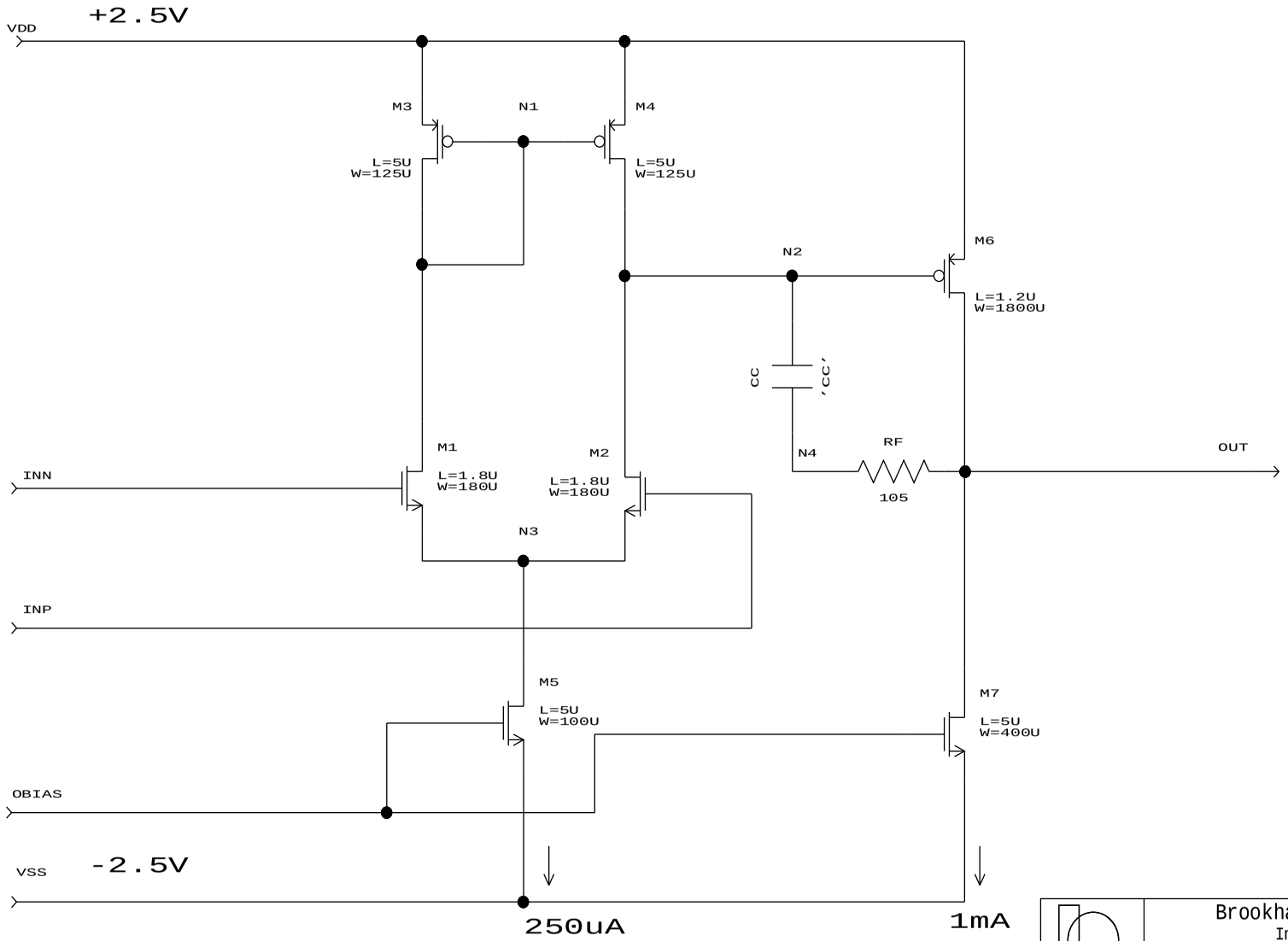
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics
SIZE
B
DWG NO:
REV NO:
SCALE
2ND SHAPING AND
GAIN STAGE
for TEC Shaper
8-22-1996_12:41
Drawn By:
Anand Kandasamy
516-344-5486
anand@bnl.gov
Sheet: 1 OF 1



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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B	Opamp for TEC Shaper
DWG NO:		
REV NO:		
SCALE		8-22-1996_9:43

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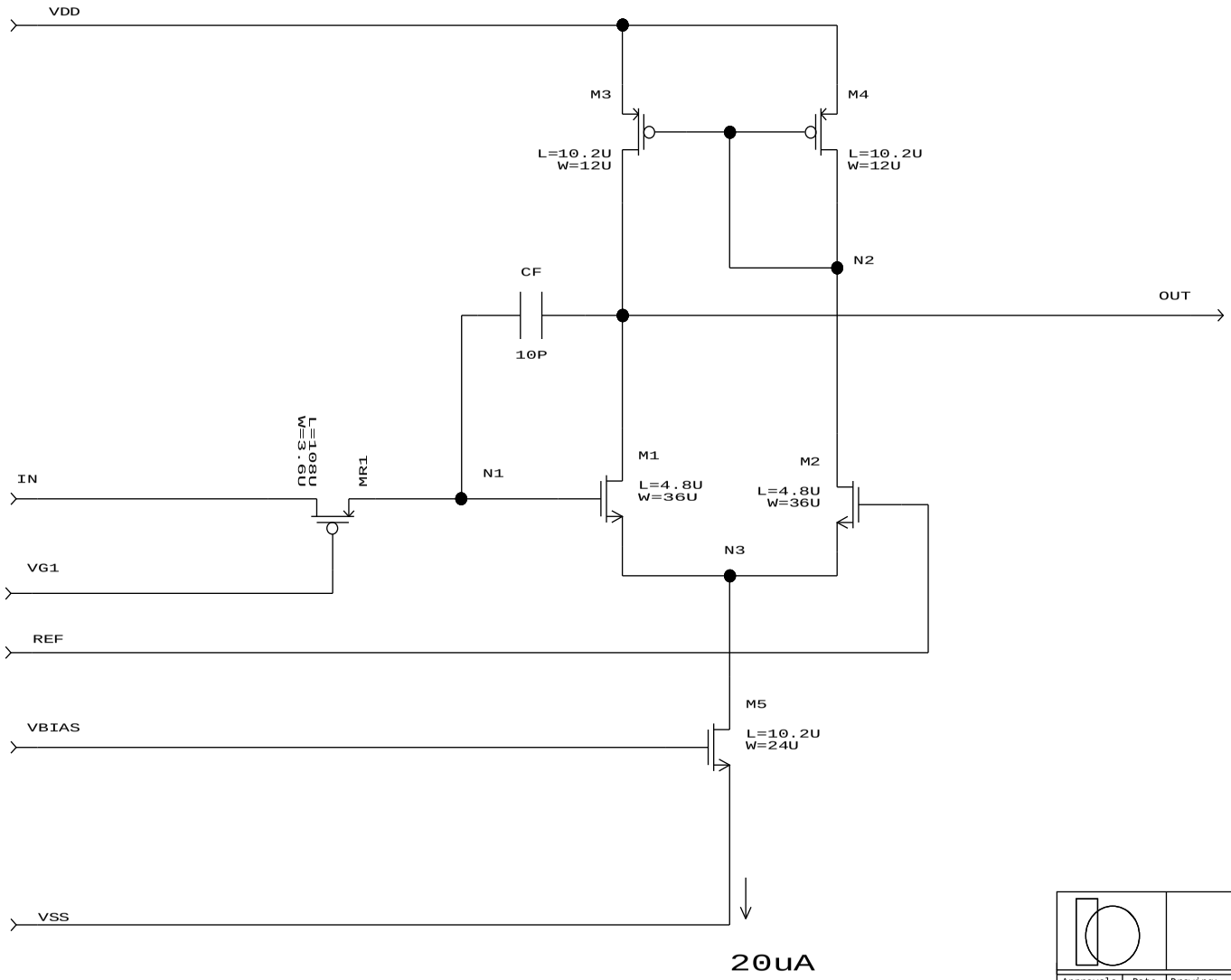

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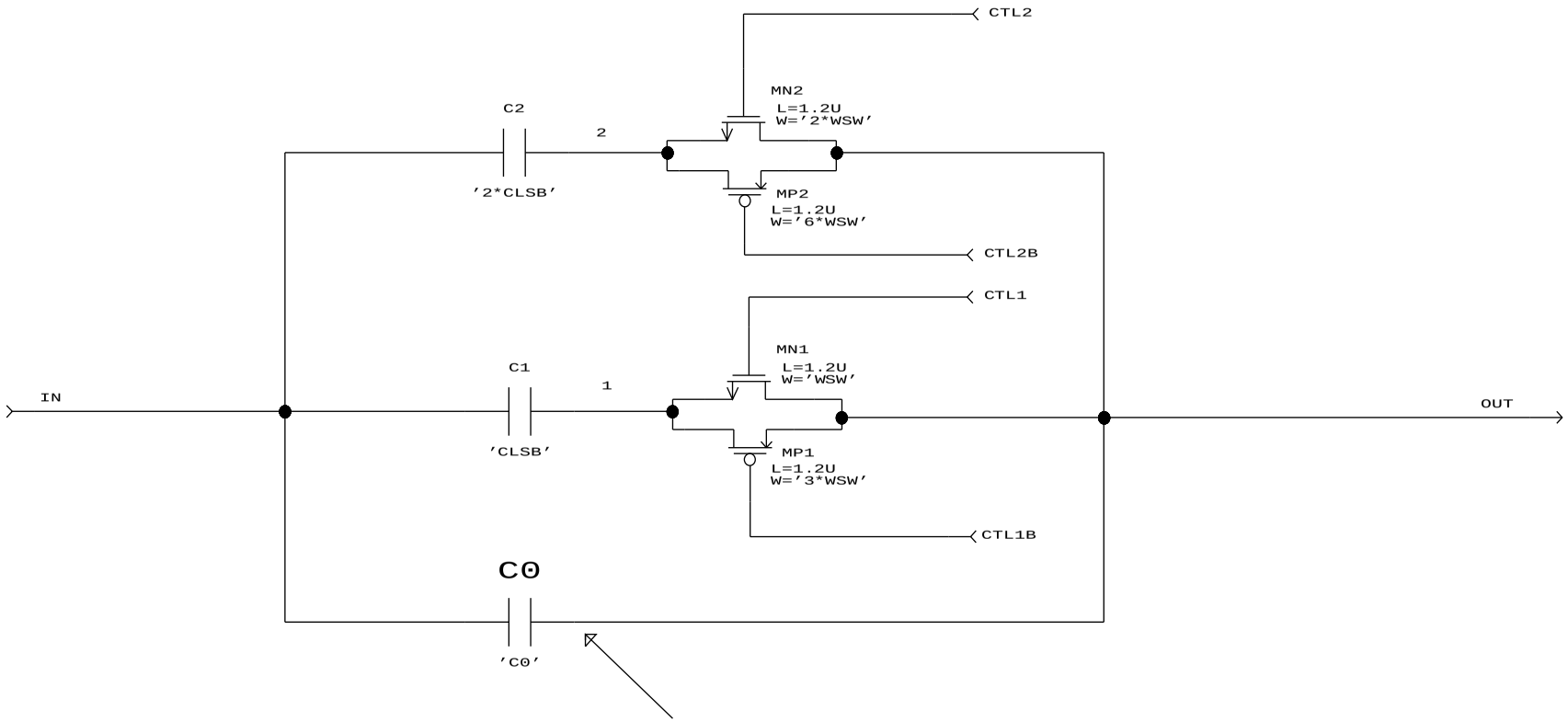
Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B	Integrator for TEC Shaper	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
DWG NO:			
REV NO:			
SCALE		8-22-1996_12:36	Sheet: 1 OF 1



NOTE: BOTTOM PLATE (PARASITIC) TOWARDS NODE OUT

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	
SCALE	

2 Bit Programmable
Capacitor Array
for TEC Shaper

8-22-1996_12:38

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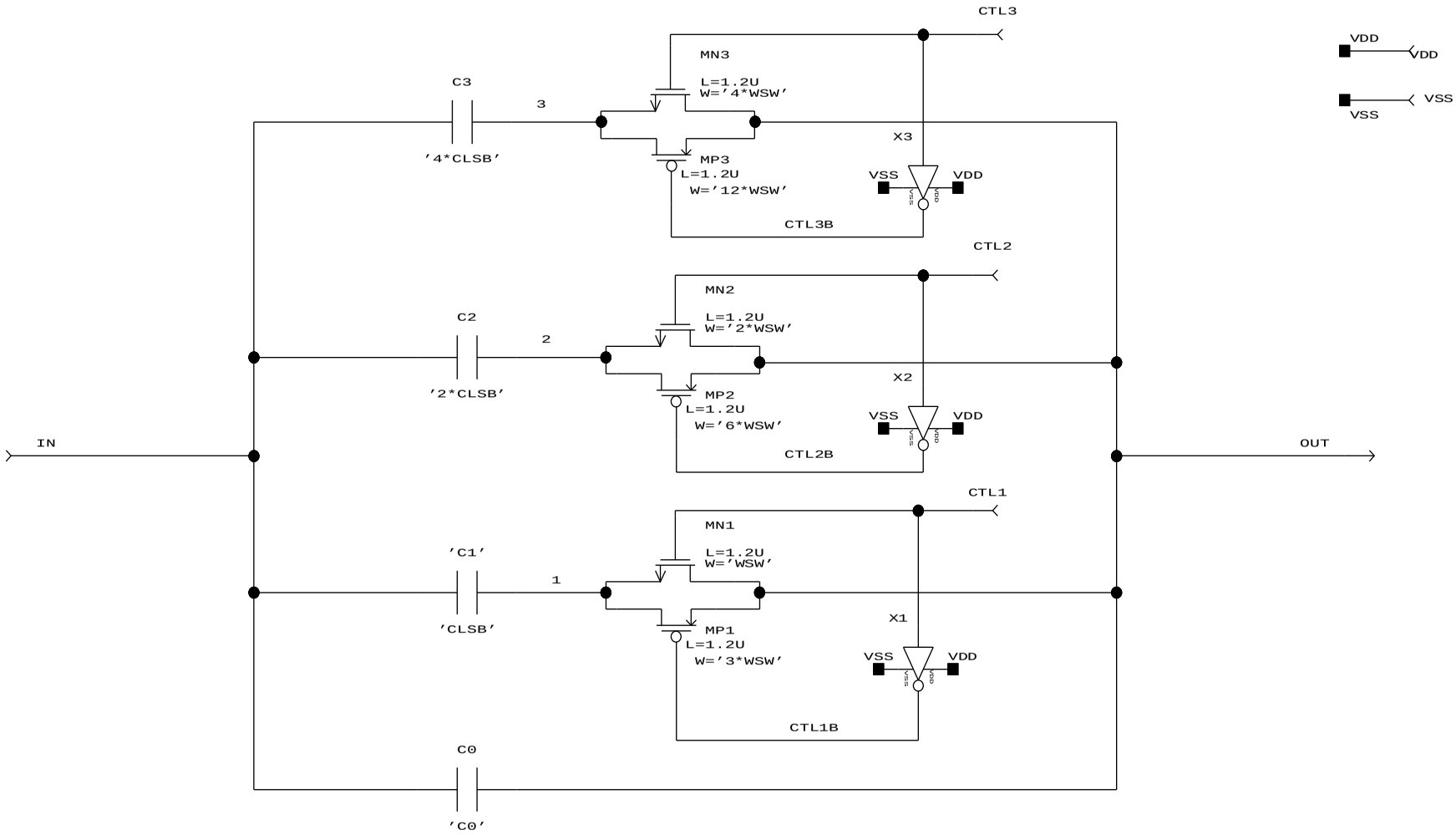

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Drawn		PHENIX Time Expansion Chamber
Checked		Preamp-Shaper Front End Electronics
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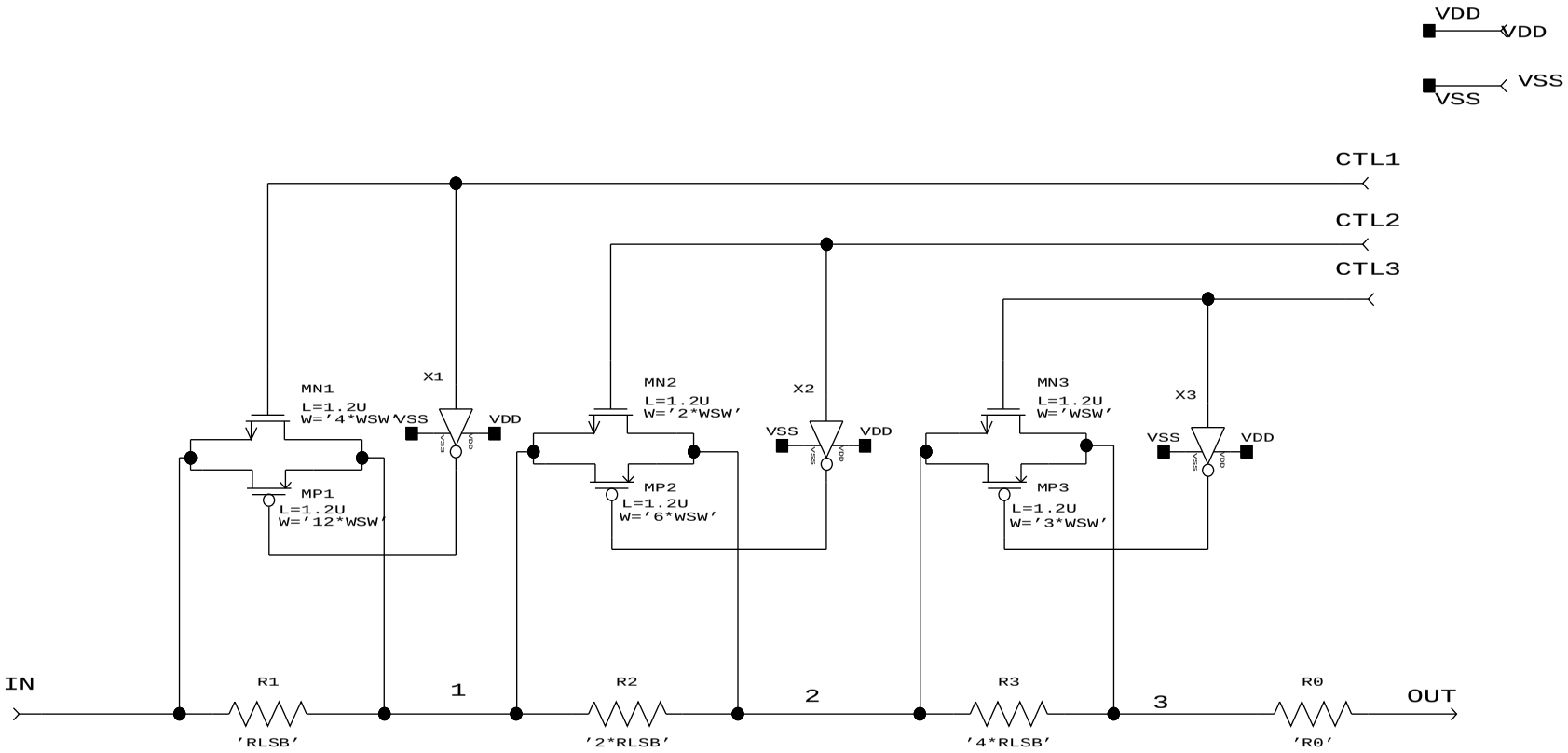
SIZE	B	3 Bit Programmable Capacitor Array for TEC Shaper	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
DWG NO:			
REV NO:			
SCALE		8-22-1996_12:40	Sheet: 1 OF 1



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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	
SCALE	

3 Bit Programmable
Resistor Array
for TEC Shaper

8-22-1996_12:42

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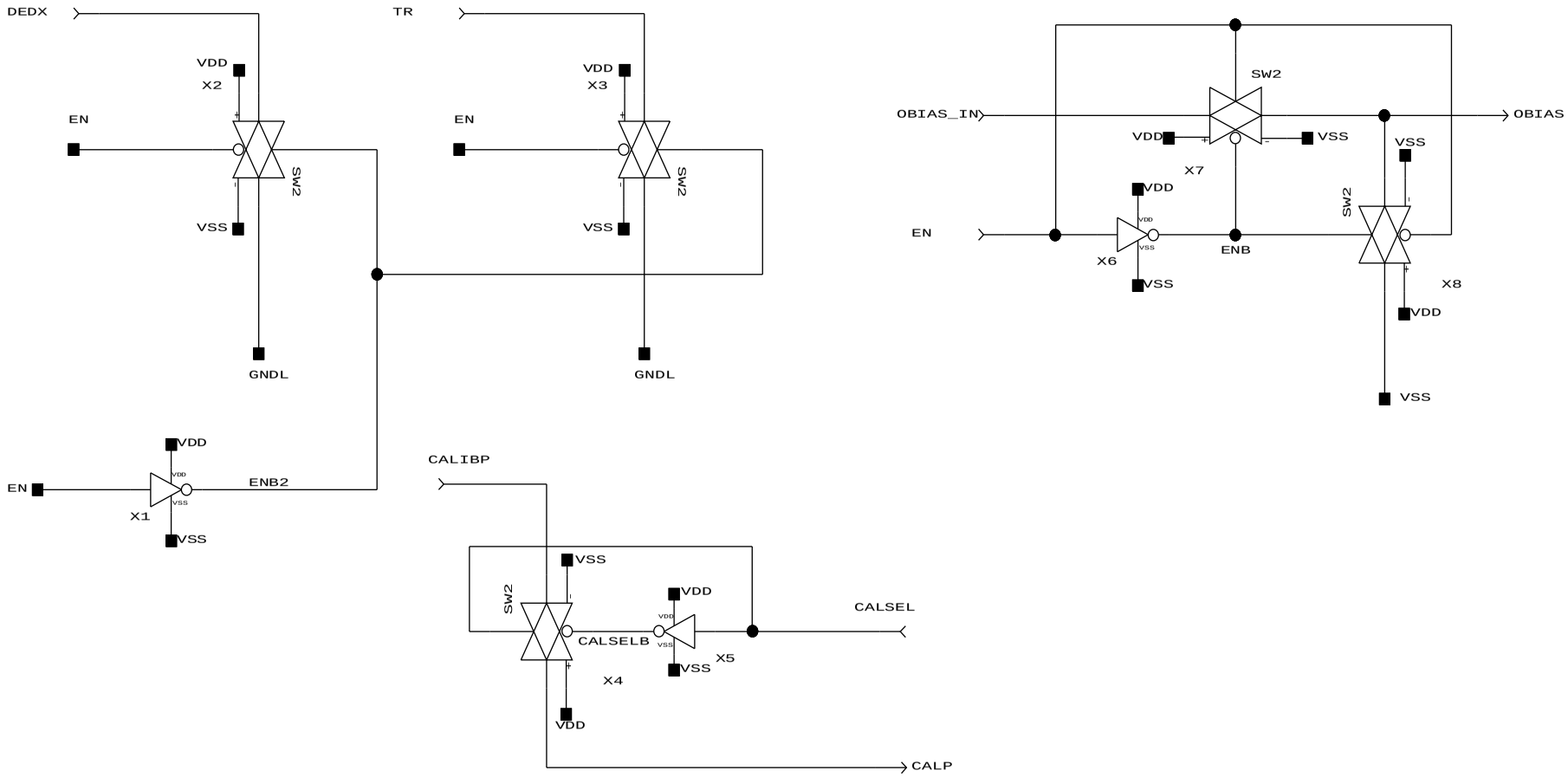

VDD

GNDL

VSS

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Approvals	Date	Drawing:
Drawn		PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Checked		
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SIZE	B	Control Module for Enable and Calibration
DWG NO:		
REV NO:		
SCALE		8-22-1996_12:43

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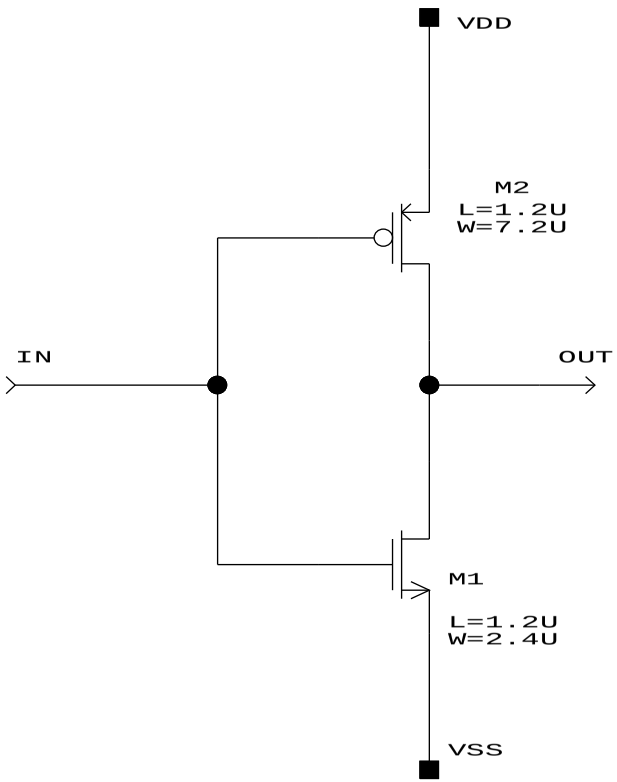
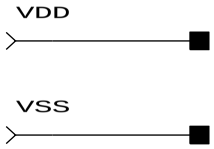
Sheet: 1 OF 1





		Brookhaven National Laboratory Instrumentation Division Upton, NY 11973
Approvals	Date	Drawing: PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Drawn		
Checked		
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SIZE	A	Inverter inv108
DWG NO:		
REV NO:		
SCALE		8-22-1996_10:08

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516-344-5486
anand@bnl.gov

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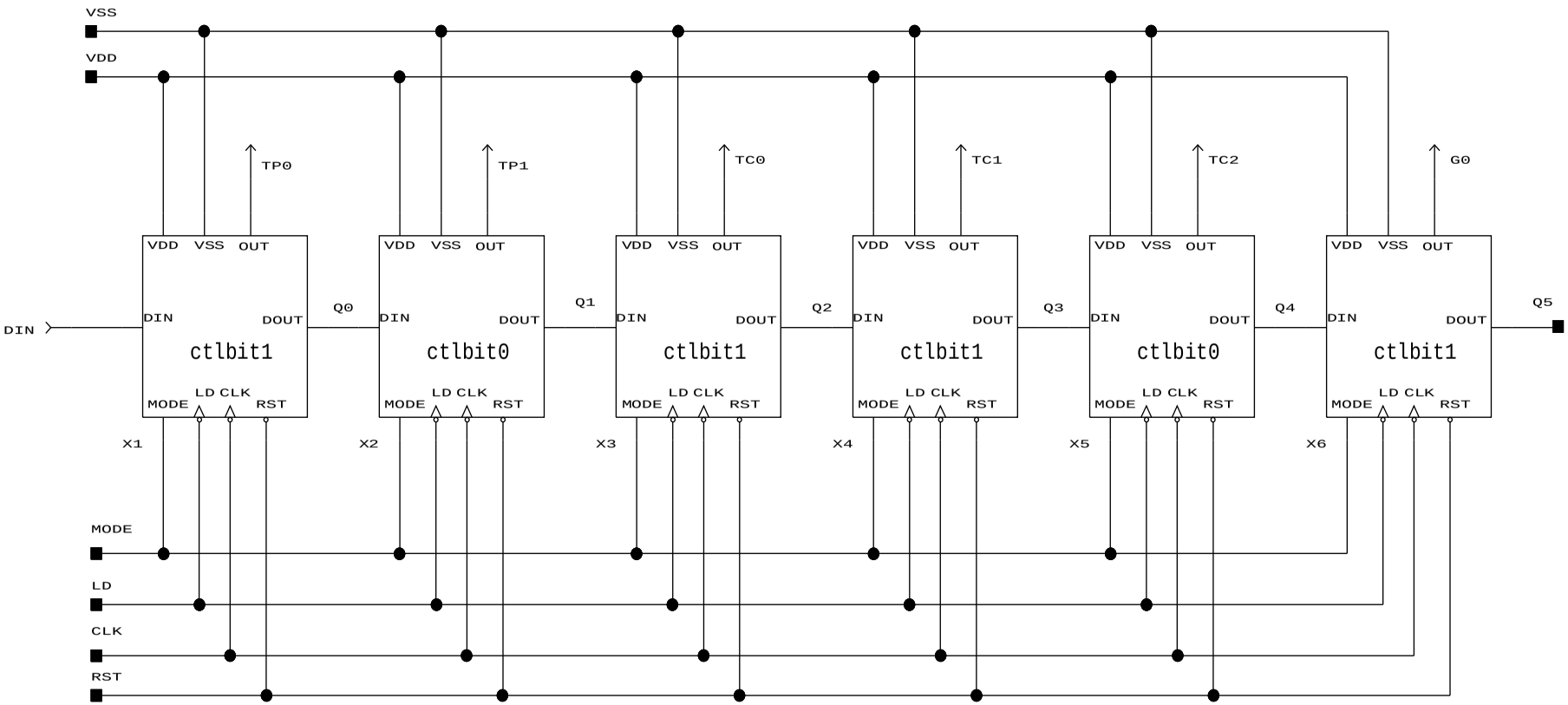

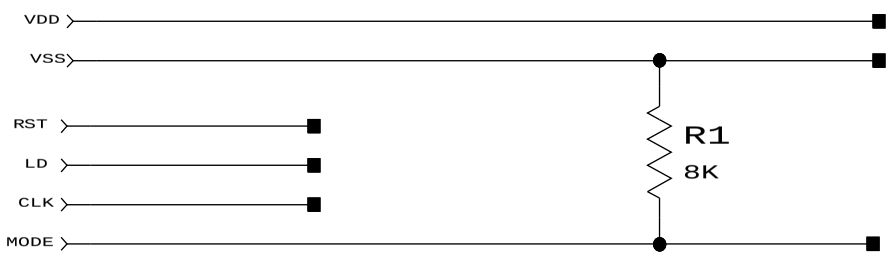

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	
SCALE	

Serial Interface for TEC-PS

8-22-1996_11:18

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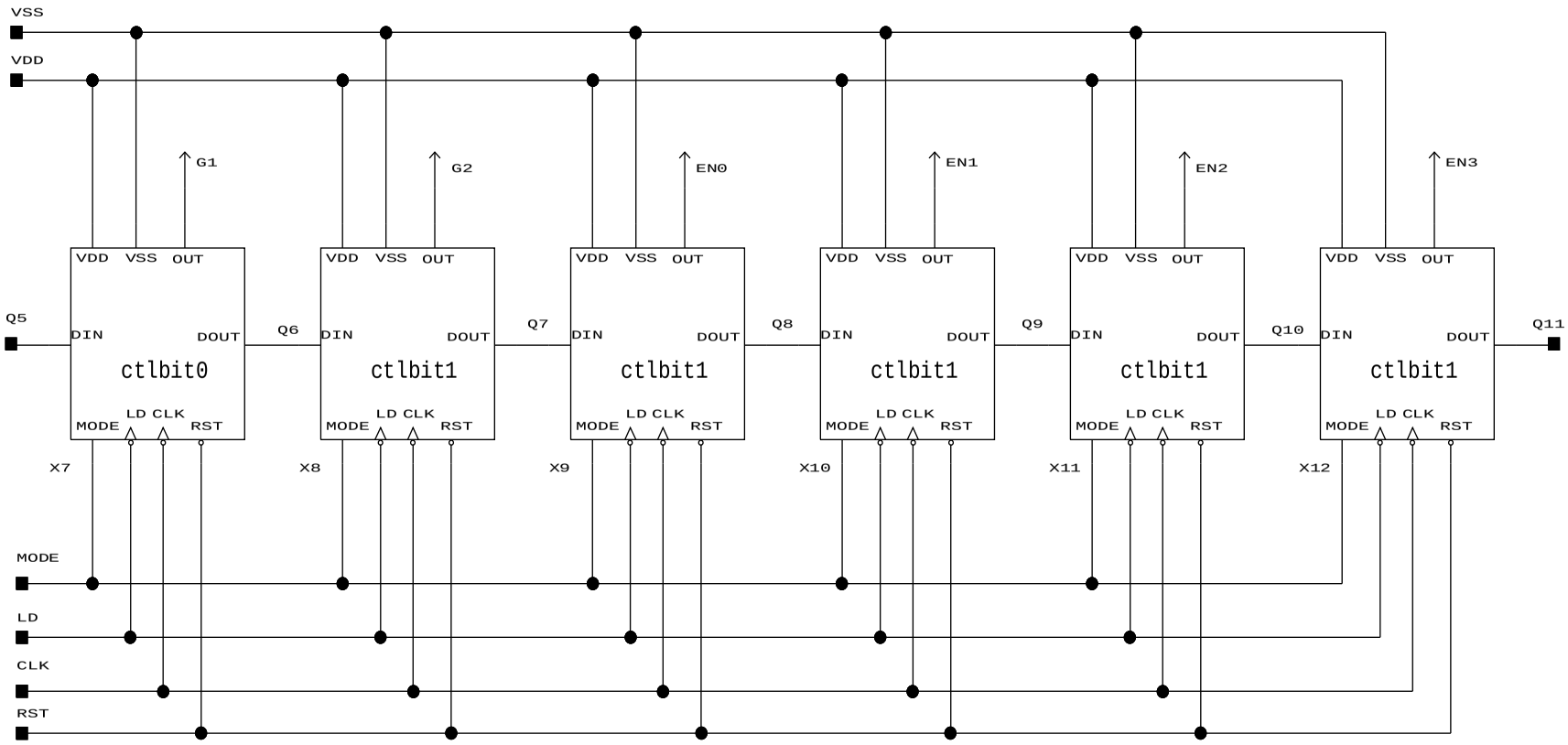

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

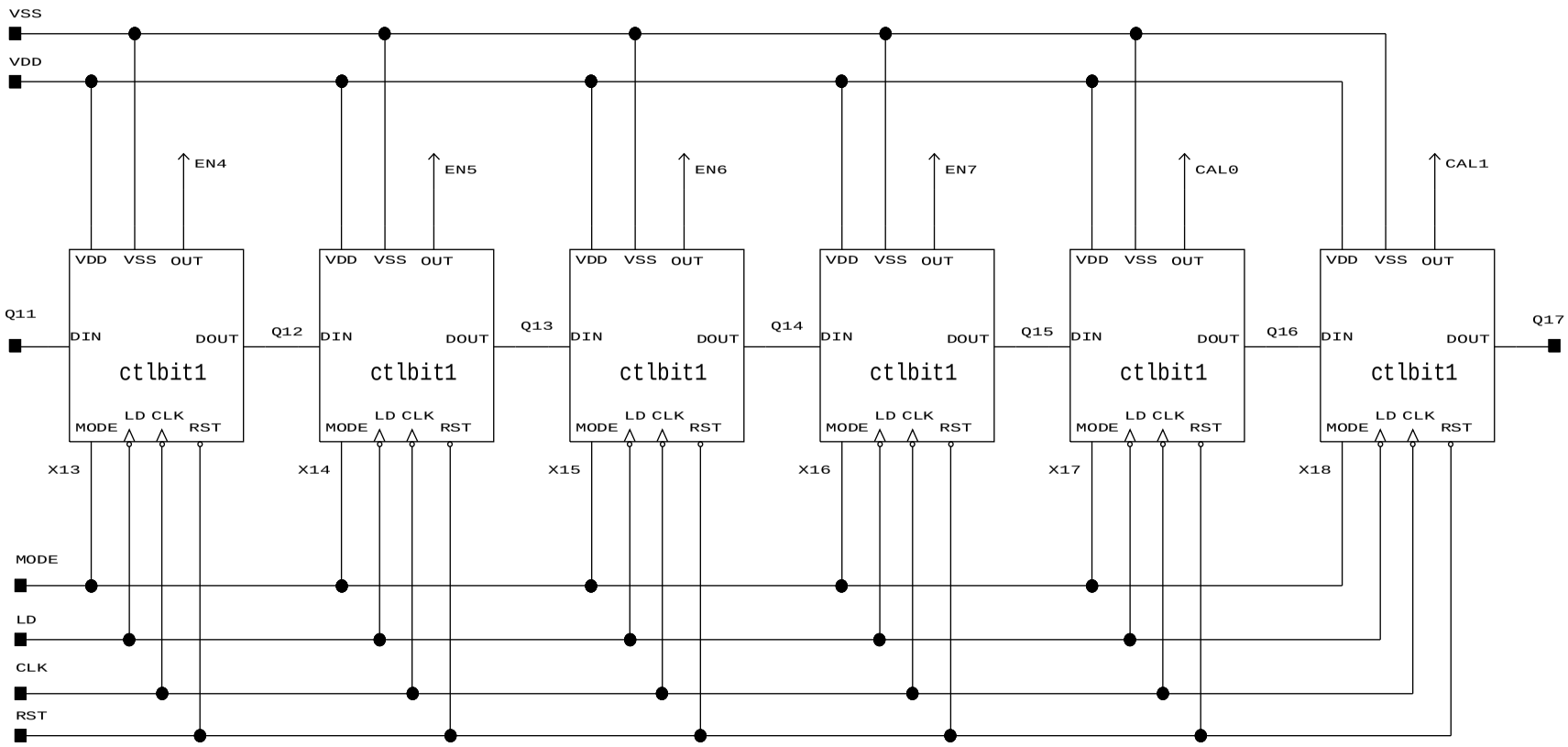
SIZE	B
DWG NO:	
REV NO:	
SCALE	

Serial Interface for TEC-PS

8-22-1996_10:14

Drawn By:
Anand Kandasamy
516-344-5486
anand@bnl.gov

Sheet: 2 OF 4



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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	
SCALE	

Serial Interface for TEC-PS

8-22-1996_10:15

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Anand Kandasamy
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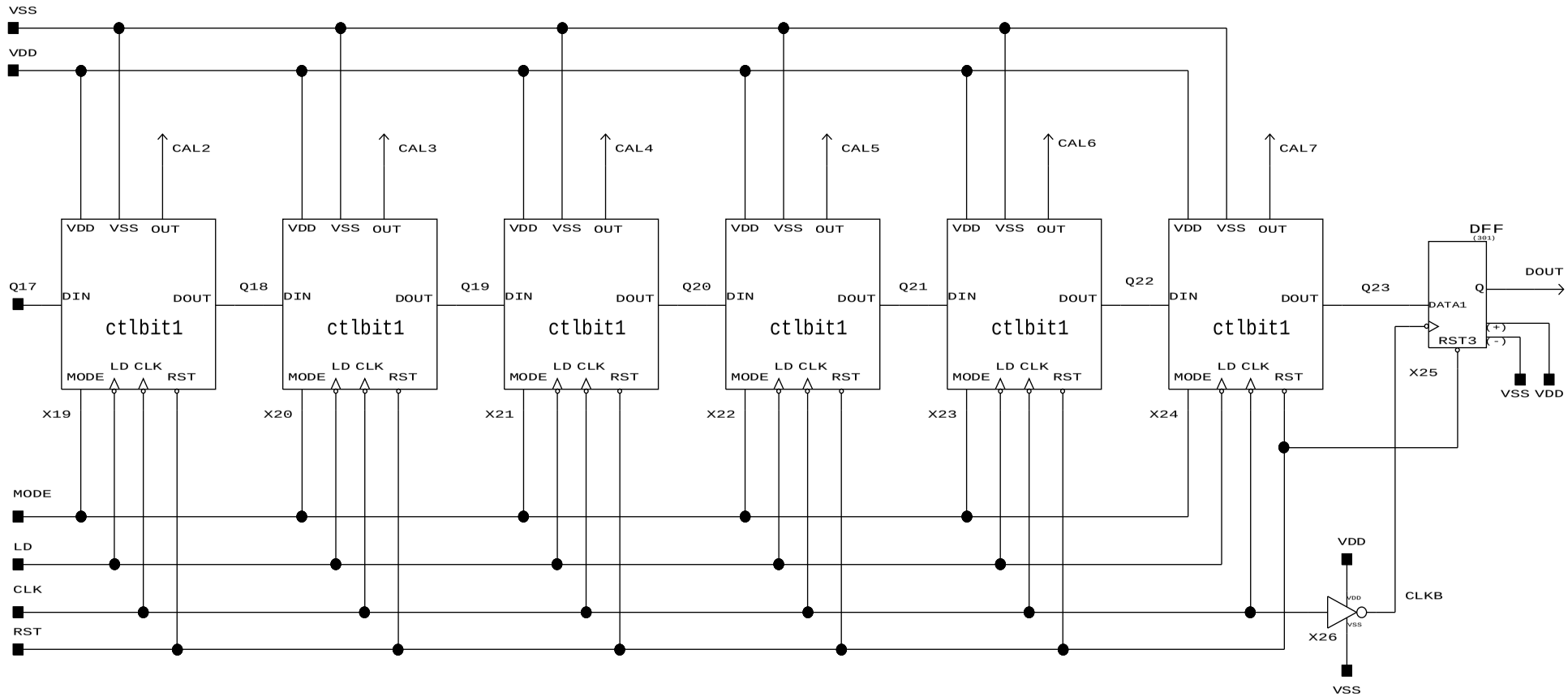
Sheet: 3 OF 4



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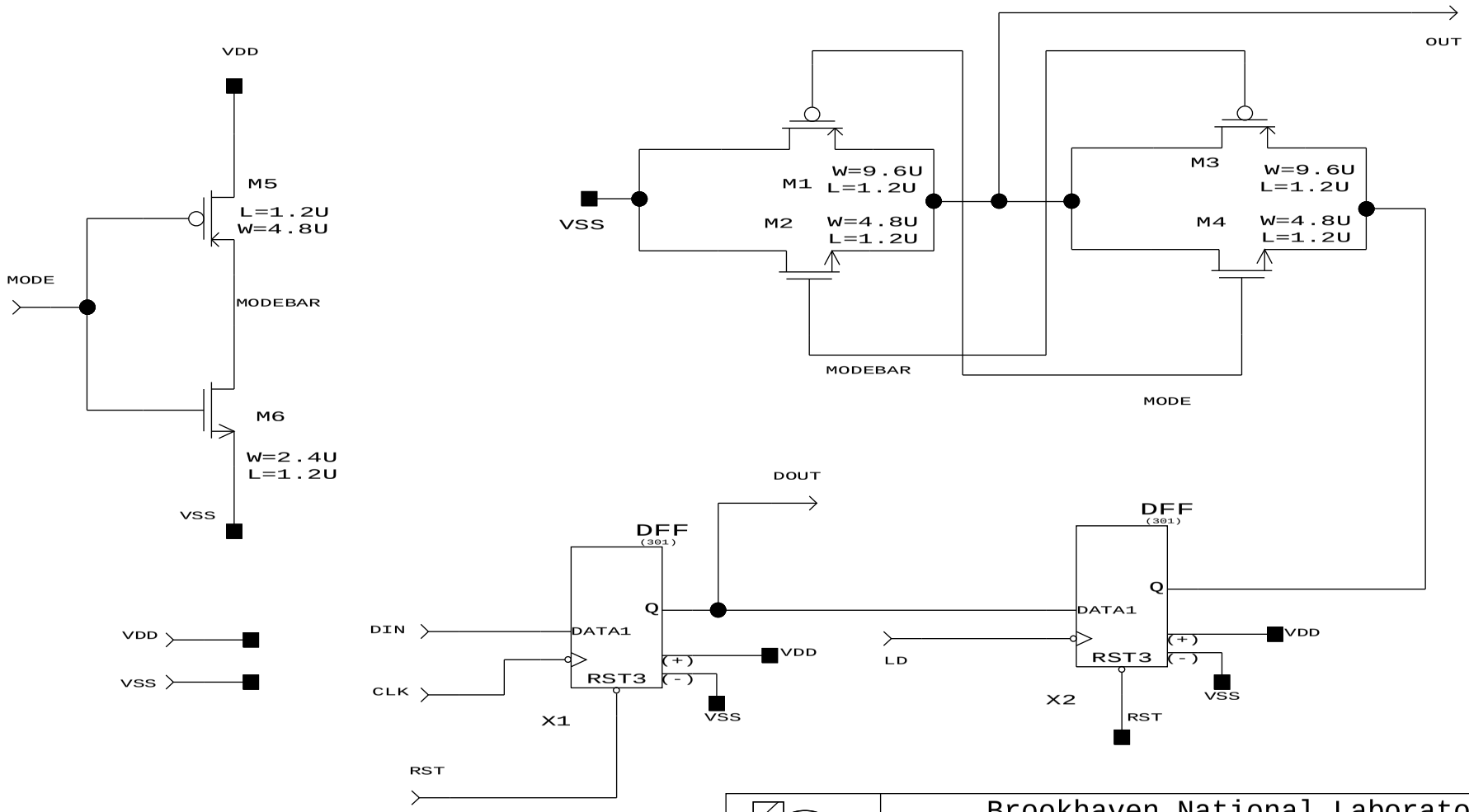
Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B	Serial Interface for TEC-PS	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
DWG NO:			
REV NO:			
SCALE		8-22-1996_10:40	Sheet: 4 OF 4



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Drawing:

PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	A
DWG NO:	
REV NO:	
SCALE	

Control Bit [Default = 0]

8-22-1996_10:19

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Anand Kandasamy
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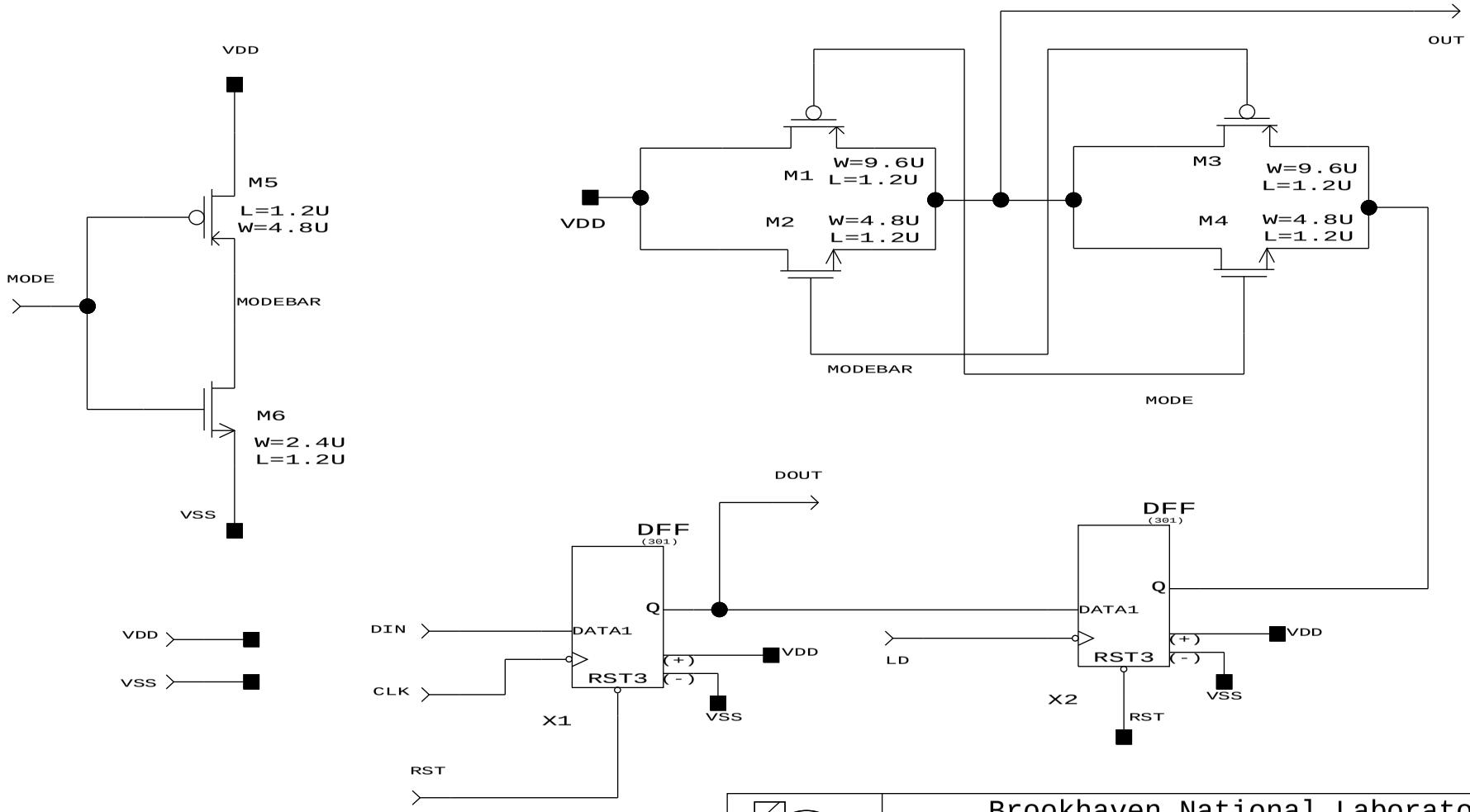

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Drawing:

PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	A
DWG NO:	
REV NO:	
SCALE	

Control Bit [Default = 1]

8-22-1996_10:20

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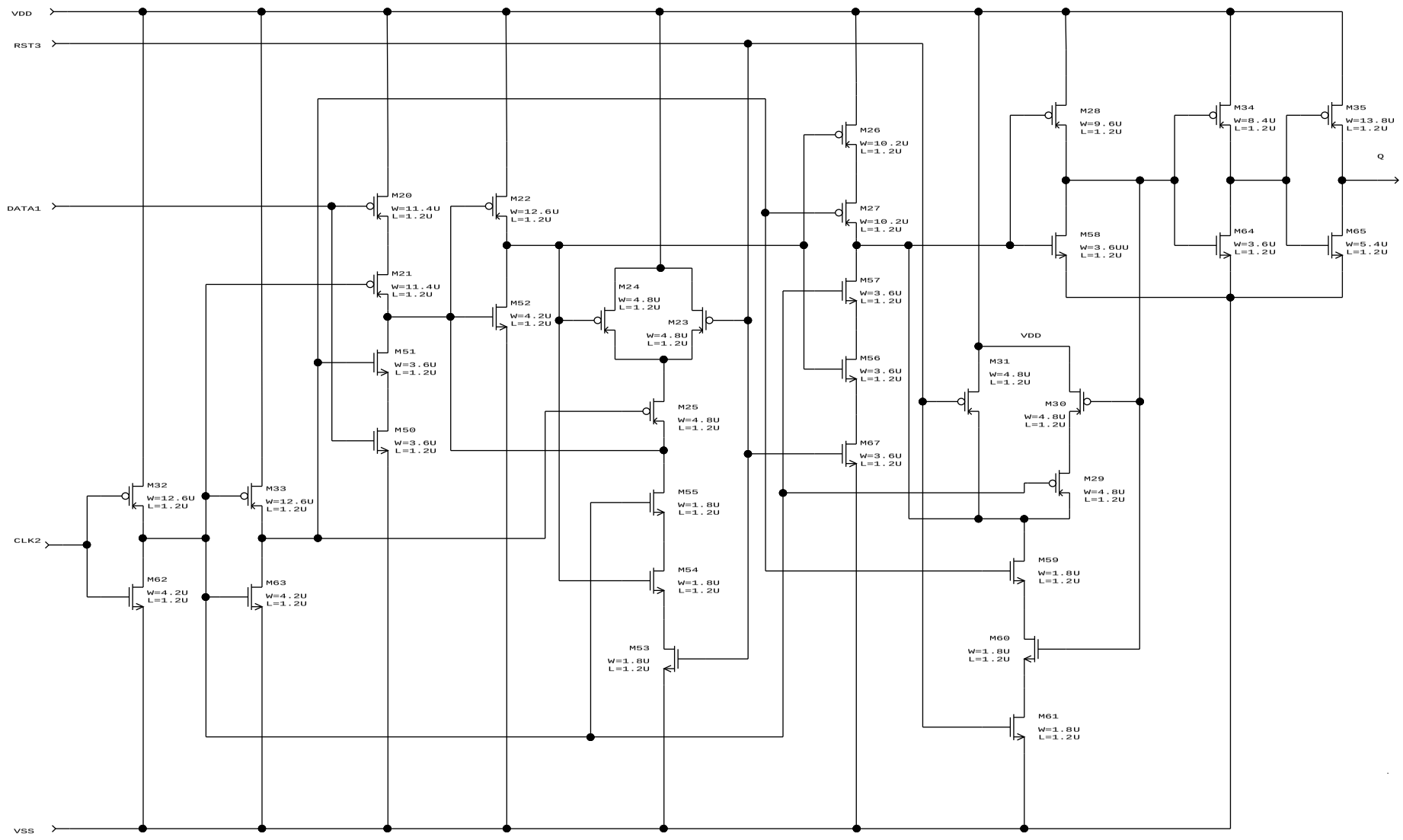
anand@bnl.gov

Sheet: 1 OF 1



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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	C
DWG NO:	
REV NO:	
SCALE	

D- Flip Flop for Control Bit

8-22-1996_10:40

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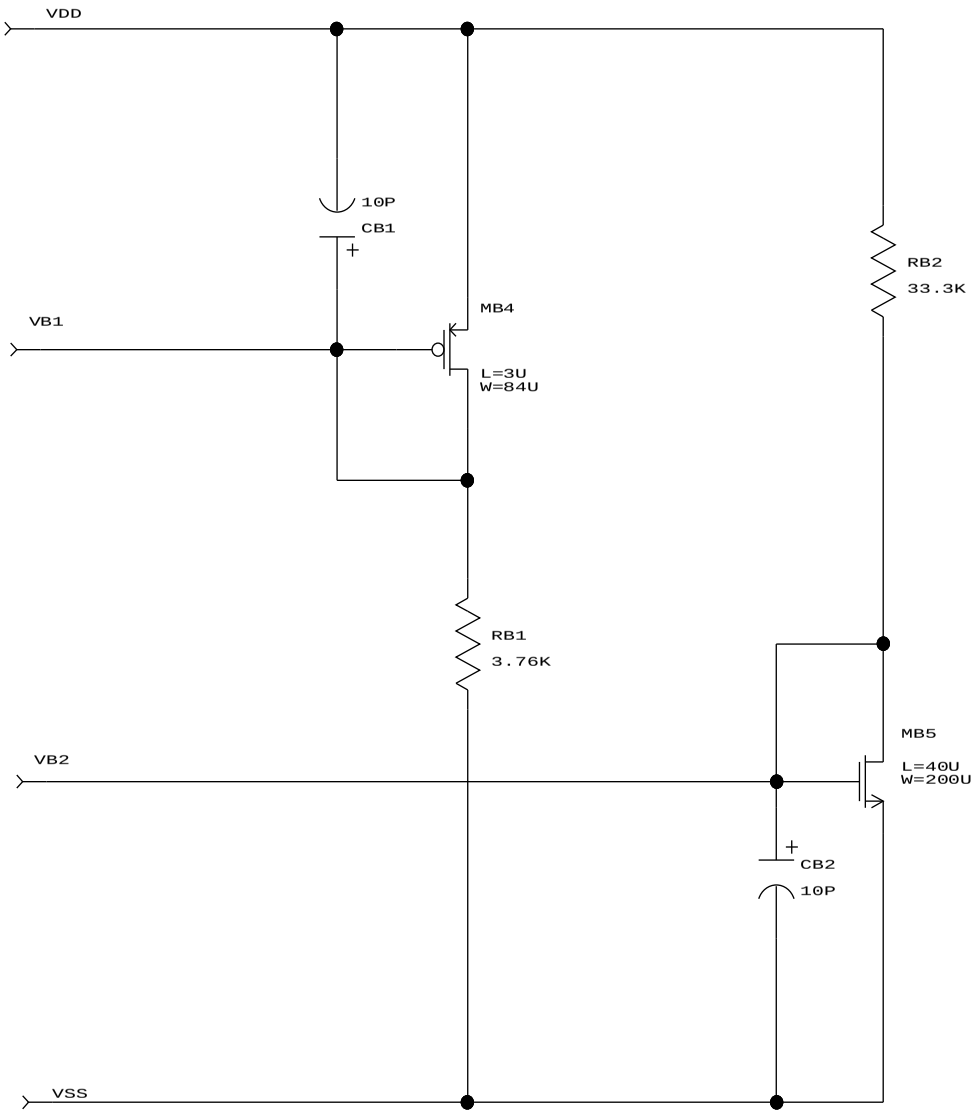
anand@bnl.gov

Sheet: 1 OF 1



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Drawn		PHENIX Time Expansion Chamber
Checked		Preamp-Shaper Front End Electronics
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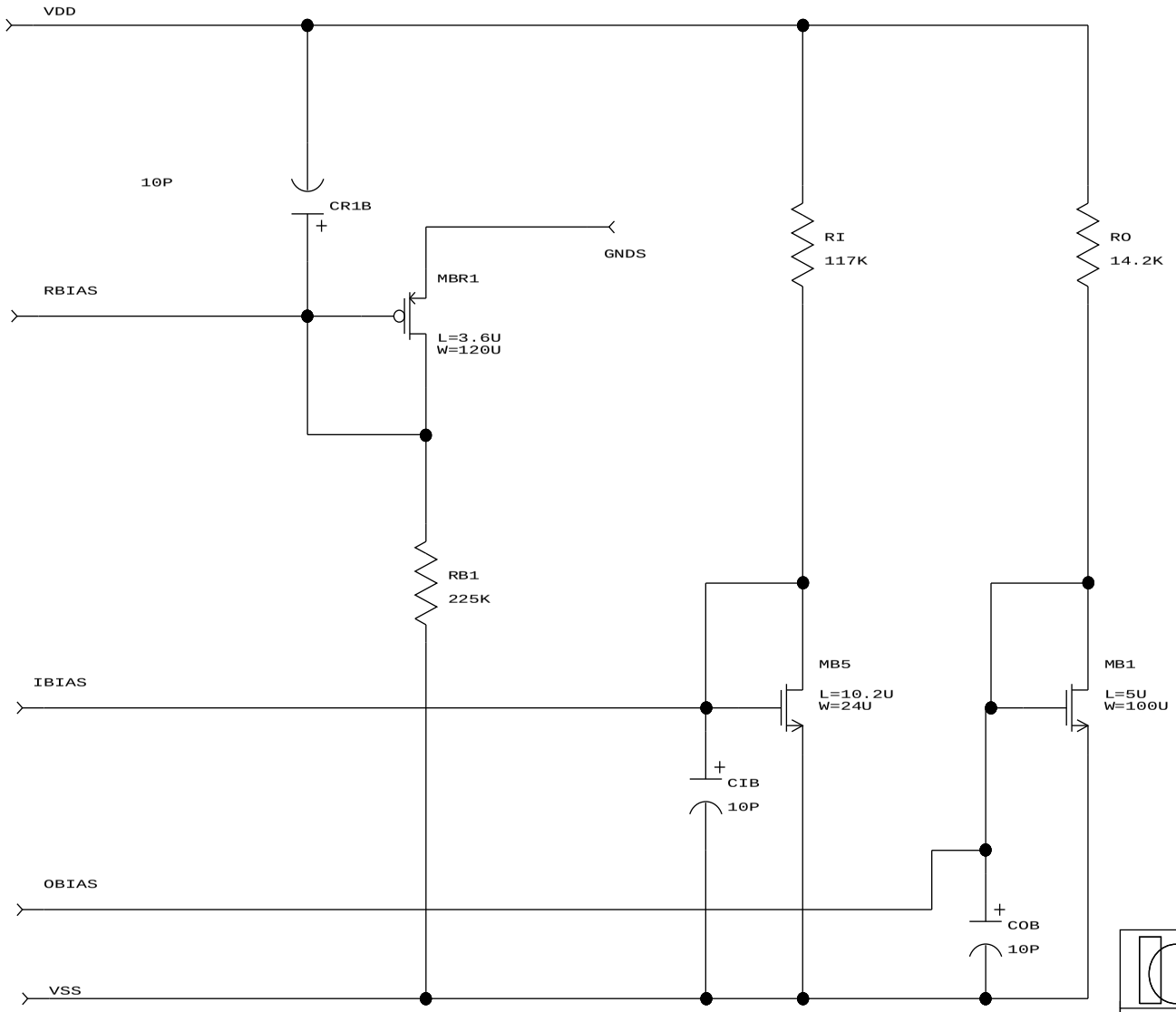
SIZE	B	Preamplifier Bias for TEC Preamp	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
DWG NO:			
REV NO:			
SCALE		8-22-1996_10:12	Sheet: 1 OF 1



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Checked		Preamp-Shaper Front End Electronics
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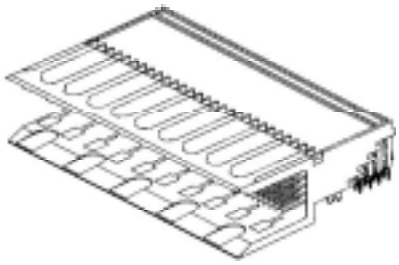
SIZE	B	Shaper Bias for TEC Shaper	Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov
DWG NO:			
REV NO:			
SCALE		8-22-1996_10:11	Sheet: 1 OF 1

Anand Kandasamy
04/02/97

PHENIX
Time Expansion Chamber
Preamp-Shaper Electronics and Interfacing specifications

I. Interface to the TEC Anode Board:

- Interface between the TEC-PS and the TEC Anode Board using AMP Z-PACK[i] 2mm Future Bus connectors.



- ♦ Four 24 Pin connectors per TEC-PS board
- ♦ Male Z-PACK connectors on the TEC-PS board.
- ♦ Connectors are mounted on the Bottom[ii] side of the printed circuit board.

- External ESD protection on the Input lines for the TEC-PS Integrated circuits.

II. Power and Ground:

- Unregulated Power Supply feed from the Anode boards, through the Z-PACK connectors. The following unregulated supplies are required from the Anode board for local regulation.

    1. +3.0 Volts [minimum] for +2.5 Volts regulation.
    2. +6.0 Volts [minimum] for +5.0 Volts regulation.
    3. -6.0 Volts [minimum] for -5.0 Volts and -2.5 Volts regulation.
    4. 0 Volts, Power Supply Ground and Preamp/Shaper Return.

- Power supply for the TEC-PS board electronic components are regulated locally on every board. The following regulated voltages are available on the TEC-PS board along with Ground.

    1. +2.5 Volts.
    2. -2.5 Volts.
    3. +5.0 Volts.
    4. -5.0 Volts.

- Power Consumption[iii] per TEC-Preamp-Shaper board.[Quiescent current]

    1. +3.0 Volts: 400mA [1.2 Watts]
    2. +6.0 Volts: 220mA [1.32 Watts]
    3. -6.0 Volts: 550mA [3.3 Watts]

    - Total Power consumption: 5.82 Watts/32 channels.

- TEC-PS Preamp returns are ganged together to the ground plane of the Printed circuit board.

III. Geographical Addressing for TEC-PS Boards:

- Geographical Addressing from each PS board on every TEC plane:

  - 15 boards/plane requiring 4 ID bits.
  - ID bits are routed into the PS board through the Anode Interface Z-PACK connectors.
  - Logic Levels of ID bits from the Anode Board: +3.0 Volts : "ONE"
    0 Volts : "ZERO"
  - ID bits are level translated into RS-422 Signals and shipped to the FEM through the output connectors.

IV. Mechanical specifications of the TEC-PS Board:

- Mechanical Dimension and Board Clearances of the TEC-PS board.

Board width	: 3.75"	maximum
Board Edge to Component clearance	: 0.1875"	minimum
Board Thickness	: 0.0625"	maximum
Board Length	: ***Layout imposed***	
Component height on the Solder side	: 0.236"	maximum
Component height on the component side	: 1.00"	maximum

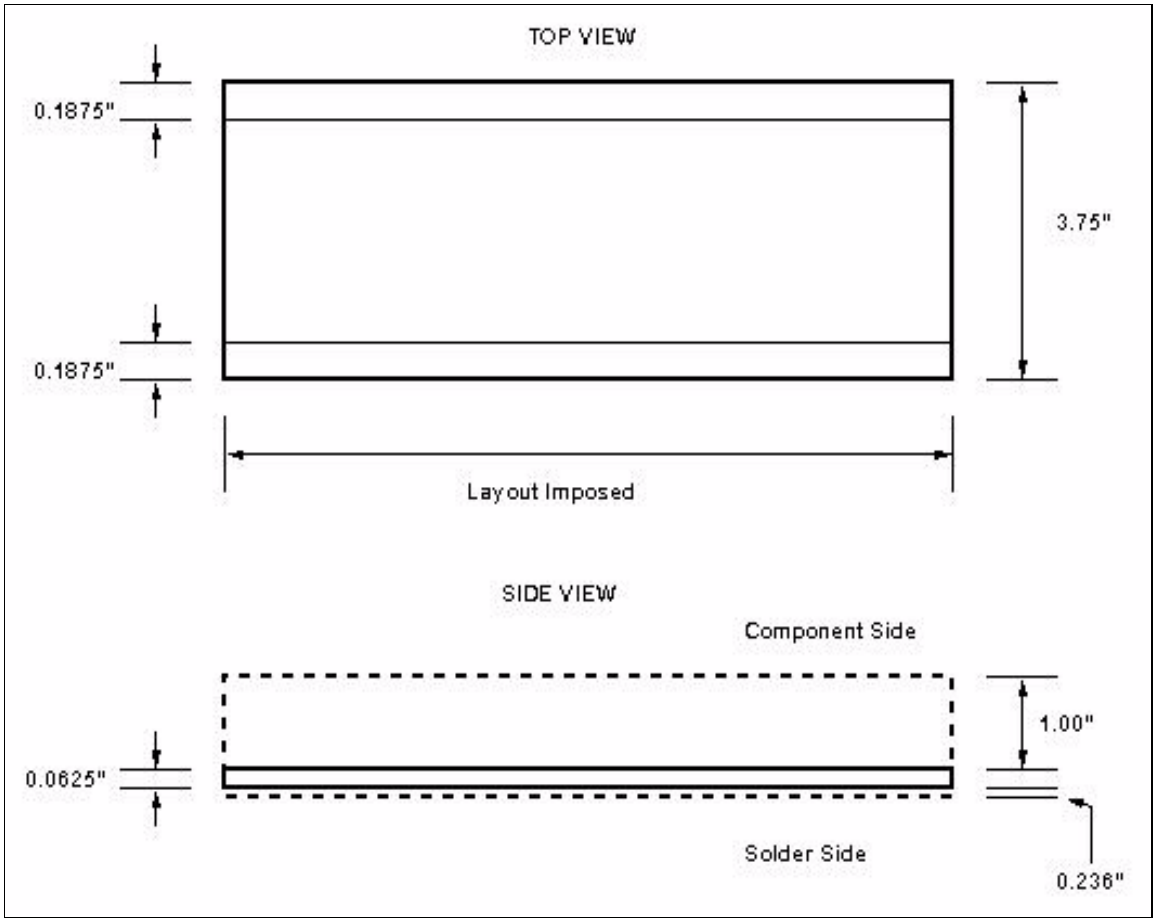


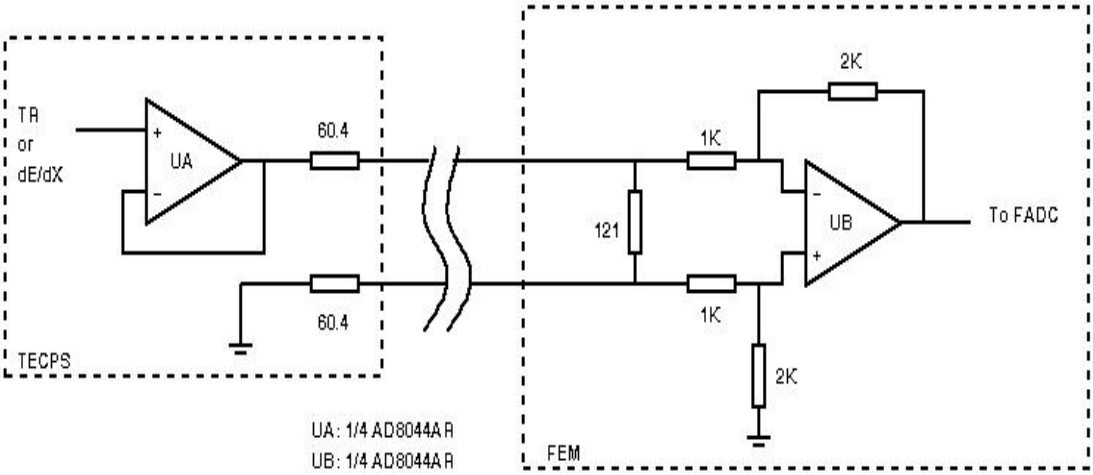
Figure 1

V. Interface to the FEM Board:

a. Preamp-Shaper:

- 32 Preamp-Shaper Channels per TEC PS board.
    1. 32 dE/dX outputs.
    2. 32 TR outputs.

- Pseudo Differential output Line drivers for TR and dE/dX signals to the FEM.



- TEC-PS to TEC-FEM interface using Amphenol 0.025" Twist 'N' Flat planar cable[iv], 40 twisted pairs.
- Amphenol 0.025" High-Density connectors for output cable interface.
    - Amphenol's Cable mount High density IDC sockets[v].
    - Amphenol's Board mounted High density straight IDC headers[vi].
- Output connectors are mounted on the bottom[vii] side of the TEC-PS board and should be within the maximum clearance allowed (1.00").

b. Control, Calibration, Read-back and Monitoring:

- TEC-PS configuration [Gain, Calibration mask and Channel Mask] are set using serial stream downloaded from the FEM.
    - All control lines given below are fully differential using RS-422 protocol.
        1. Serial Data Input.
        2. Serial Clock.
        3. Serial Data Load.
        4. Serial Data Output [Read-back].

- Onboard Calibration circuit.
    - On Board DAC and switching circuitry for Preamp/Shaper Calibration.
    - Maximum Calibration charge : 200fC.
    - Calibration Strobe signal from the FEM as differential RS-422 signal.
    - DAC programmed from the FEM using the same serial stream used for configuring the TEC-PS Integrated circuits.

- Onboard PLD is used for converting part of the serial stream [12 bits] to parallel data for the DAC. The PLD is a feed through for the entire serial stream which consists of data to configure 4 TEC-PS integrated circuits.

- No ground connection to exist between the FEM and the TEC-PS boards. All control and data signal [Calibration strobe, Serial and Analog] are differential, Analog signal output to the FEM are pseudo differential. The serial link, calibration strobe and address bits are fully differential using RS-422 protocol.

- Two 40 pair cables for output and control signals to and from the FEM and TEC-PS board.
    - dE/dX and TR signals interleaved on two output connectors.

- Input connector for pulsing the TEC-PS integrated circuits for diagnostics purposes, circumventing the onboard calibration circuitry. [A 2 pin SIP header is sufficient].

- Input connector for diagnosing the serial link. [This connector is separate from the output connector].
    - This diagnostic serial link has to be RS-422 signals.

VI. <u>Serial Link Specifications:</u>

- Data is latched into the shift register flip-flops on the falling edge of the clock.
- Total number of bits per TEC-Preamp-Shaper Integrated circuit:

1.	Control:			
	♦ Peaking Time	:	2	bits
	♦ Tail Cancellation	:	3	bits
	♦ Gain	:	3	bits
2.	Calibration	:	8	bits
3.	Channel Mask	:	8	bits
	Total	:	24	bits

- Total number of bits per TEC-Preamp Shaper Board:

♦	DAC	:	12	bits
♦	TEC-PS (4 x 24 bits)	:	96	bits
	Total	:	108	bits

- Serial Protocol:

    1. The entire serial stream (108 bits) are shifted in, on the negative edge of the serial clock.
    2. A falling edge on the LOAD line latches the serially shifted data onto the configuration registers of the TEC-PS integrated circuits and the output bits of the PLD for the DAC.
    3. The data-out of each chip in the chain is delayed by ½ a clock cycle to eliminate any flip-flop setup violations.

- The entire Serial stream for the TEC-PS board is as shown in Figure 2:

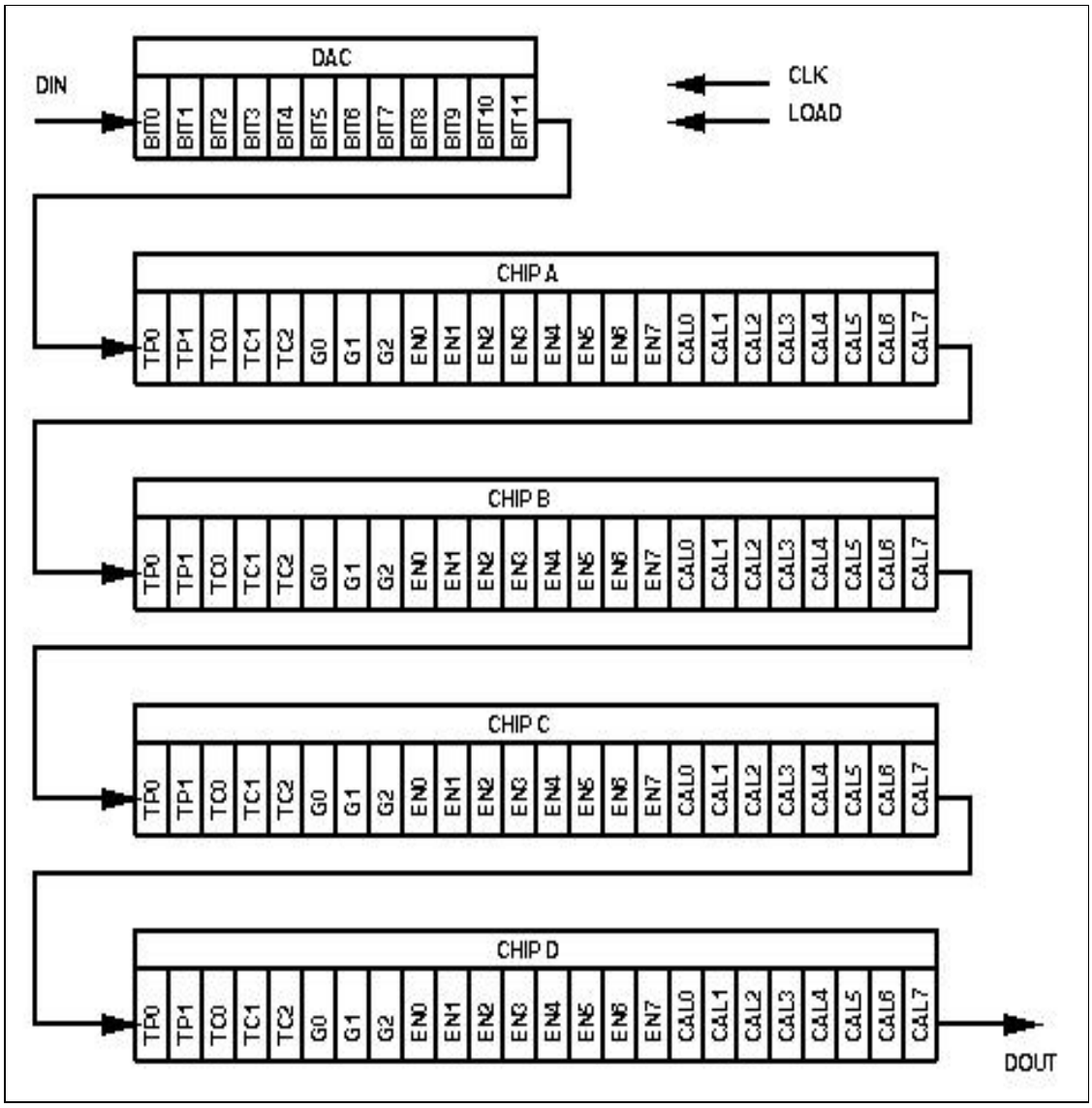


Figure 2

VII. <u>Thermal Management:</u>

- The Packages chosen for the Local Power regulators does not impose the need for any additional heat sinks for the regulators for any power dissipation considerations and thermal runaway of the regulators.

- Overall Thermal management method for the TEC-PS board has to be discussed and finalized.

IX. <u>TEC-PS Printed Circuit Board Assembly and Connector details:</u>

- All components with the exception of capacitors and resistors can be mounted on the bottom side [Solder side].

BNL-IO

- Input Connector Pin count:

1.	Anode wire inputs	:	32	
2.	Ground [Preamp Returns + Power Ground]	:	48	
3.	Power +3.0 Volts	:	3	
4.	Power +6.0 Volts	:	3	
5.	Power -6.0 Volts	:	6	
6.	ID Bits [Geographical Addressing Bits]	:	4	
	Total Used	:	96	
	Used/Total	:	96/96	[100% Utilized]

- Output Connector Pin count [in pairs]:

1.	dE/dX outputs	:	32	
2.	TR outputs	:	32	
3.	Serial Download	:	3	
4.	Serial Read back	:	1	
5.	Calibration Strobe	:	1	
6.	ID Bits [Geographical Addressing Bits]	:	4	
	Total Used	:	73	
	Used/Total	:	73/80	[91.2% Utilized]

a. Input Connector Pin assignment scheme for the TEC-PS board:

The TEC-PS board is designed the right side up and its inverted and interfaced to the TEC anode boards. This requires extensive mapping of the pins from the Anode board to the TEC-PS board. The figure and the pin numbers give below are for the right side up [Good only for layout needs and Test bench]. Only on inverting and interfacing it to the anode boards, the pins and the signal correspond to the correct mapping.

Figure 3 shown below is the 4 Z-PACK connectors on the TEC-PS board along with the naming scheme followed:

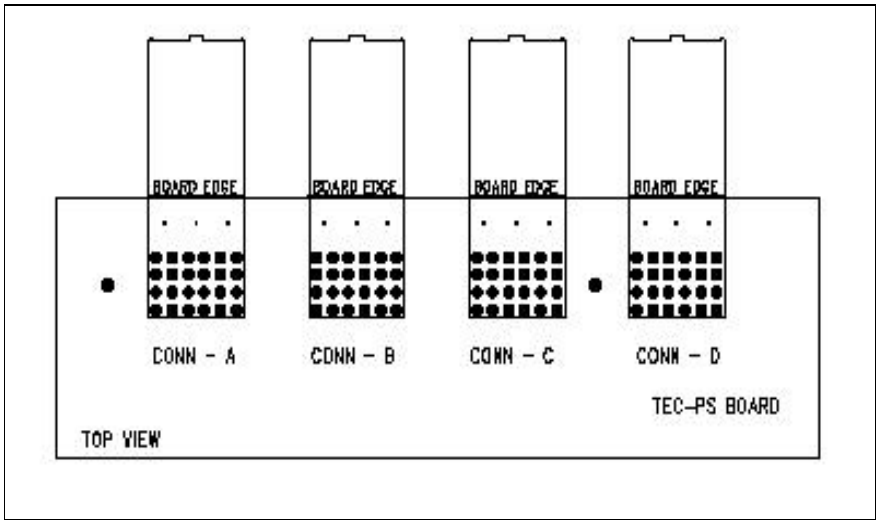


Figure 3

The TEC-PS board layout is approached in the following manner, since the TEC-PS board has to be interfaced to the TEC-Anode board inverted. Since the CAD software's work on the top-down topology, the board is designed as a 180 degree flipped. The scheme is illustrated in figure 4 and 5.

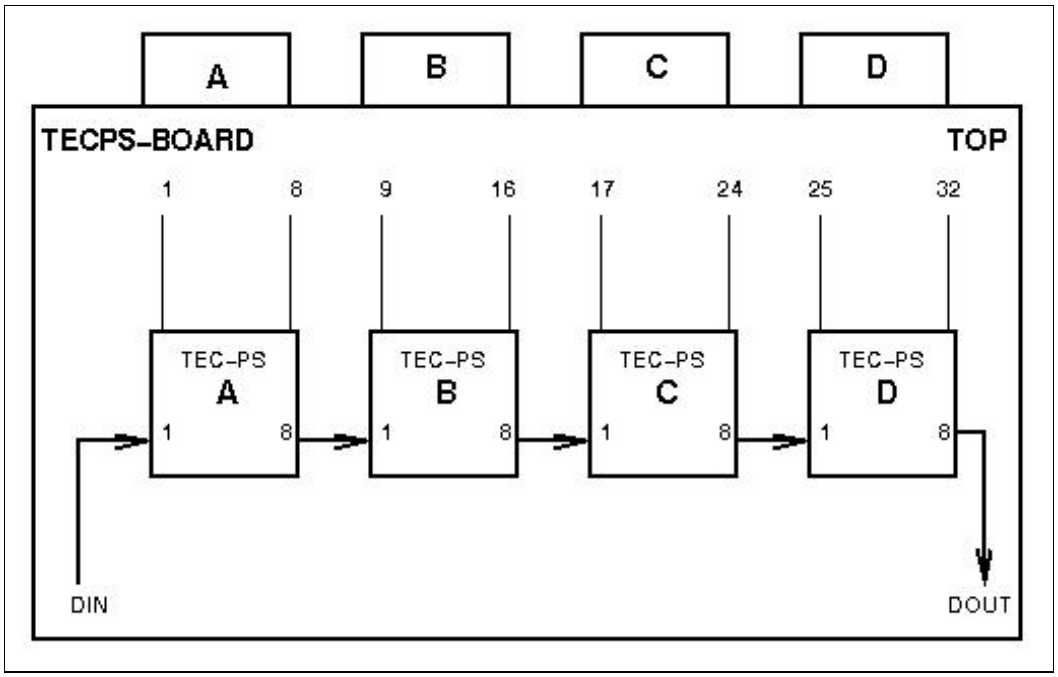


Figure 4

Figure 4 illustrates how the layout designer and the test bench engineer interprets the TEC-PS board. The channels are number from Left to right as Anode 0 to Anode 31. Note only partial modules are shown in these figures. This figure is the only figure of use for pin assignment for layout of the TEC-PS board.

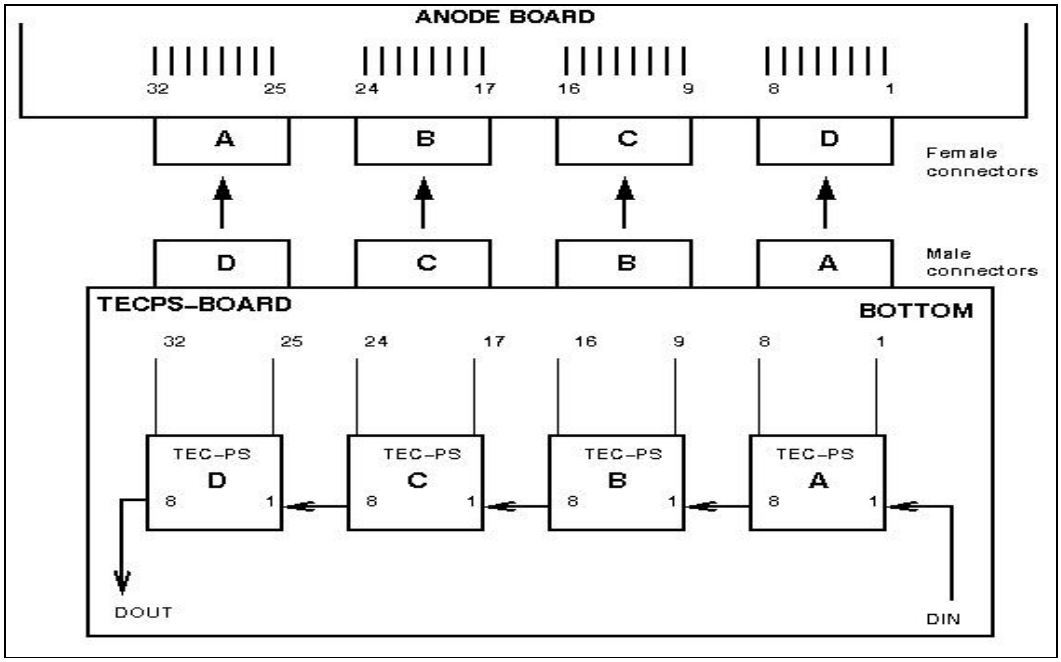


Figure 5

Figure 5 depicts how the TEC-PS board will be flipped and interfaced to the TEC Anode board. This figure is looking through the TEC-PS printed circuit board and the components are on the bottom side.

Input connector pin assignment:

- Anode signal assignments:

Anode	CHIP	Connector	Pin Number
0	A	B	2
1	A	B	4
2	A	B	5
3	A	B	7
4	A	B	10
5	A	B	12
6	A	B	13
7	A	B	15
8	B	B	18
9	B	B	20
10	B	B	21
11	B	B	23
12	B	C	2
13	B	C	4
14	B	C	5
15	B	C	7

Anode	CHIP	Connector	Pin Number
16	C	C	10
17	C	C	12
18	C	C	13
19	C	C	15
20	C	C	18
21	C	C	20
22	C	C	21
23	C	C	23
24	D	D	2
25	D	D	4
26	D	D	5
27	D	D	7
28	D	D	10
29	D	D	12
30	D	D	13
31	D	D	15

- Ground pin assignments:

Connector	Pin Number
A	2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 22 and 23
B	1, 3, 6, 8, 9, 11, 14, 16, 17, 19, 22 and 24
C	1, 3, 6, 8, 9, 11, 14, 16, 17, 19, 22 and 24
D	1, 3, 6, 8, 9, 11, 14, 16, 17, 19, 22 and 24

- Unregulated power supply pin assignments:

Connector	Unregulated Supply	Pin Number
A	+ 6.0 Volts	13, 17 and 21
A	- 6.0 Volts	4, 8, 12, 16, 20 and 24
A	+ 3.0 Volts	1, 5 and 9

- Geographical address bits pin assignment:

ID Bit	Connector	Pin Number
S1	D	24
S2	D	23
S3	D	22
S4	D	21

b. Output connector pin assignment scheme:

Connector 1:

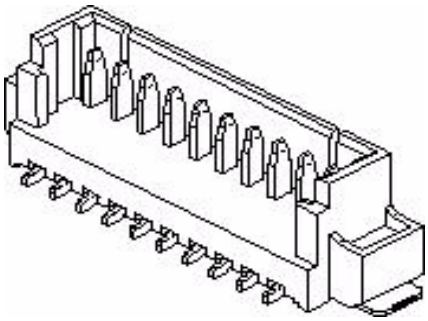
Signal	Pin Number	Signal	Pin Number
dE/dX 0	1	**R_dE/dX 0**	2
TR 0	3	**R_TR 0**	4
dE/dX 1	5	**R_dE/dX 1**	6
TR 1	7	**R_TR 1**	8
dE/dX 2	9	**R_dE/dX 2**	10
TR 2	11	**R_TR 2**	12
dE/dX 3	13	**R_dE/dX 3**	14
TR 3	15	**R_TR 3**	16
dE/dX 4	17	**R_dE/dX 4**	18
TR 4	19	**R_TR 4**	20
dE/dX 5	21	**R_dE/dX 5**	22
TR 5	23	**R_TR 5**	24
dE/dX 6	25	**R_dE/dX 6**	26
TR 6	27	**R_TR 6**	28
dE/dX 7	29	**R_dE/dX 7**	30
TR 7	31	**R_TR 7**	32
dE/dX 8	33	**R_dE/dX 8**	34
TR 8	35	**R_TR 8**	36
dE/dX 9	37	**R_dE/dX 9**	38
TR 9	39	**R_TR 9**	40
dE/dX 10	41	**R_dE/dX 10**	42
TR 10	43	**R_TR 10**	44
dE/dX 11	45	**R_dE/dX 11**	46
TR 11	47	**R_TR 11**	48
dE/dX 12	49	**R_dE/dX 12**	50
TR 12	51	**R_TR 12**	52
dE/dX 13	53	**R_dE/dX 13**	54
TR 13	55	**R_TR 13**	56
dE/dX 14	57	**R_dE/dX 14**	58
TR 14	59	**R_TR 14**	60
dE/dX 15	61	**R_dE/dX 15**	62
TR 15	63	**R_TR 15**	64
reserved	65	**reserved**	66
Rdbk_P	67	**Rdbk_N**	68
reserved	69	**reserved**	70
DATA_P	71	**DATA_N**	72
reserved	73	**reserved**	74
CLK_P	75	**CLK_N**	76
reserved	77	**reserved**	78
LD_P	79	**LD_N**	80

Connector 2:

Signal	Pin Number	Signal	Pin Number
dE/dX 16	1	**R_dE/dX 16**	2
TR 16	3	**R_TR 16**	4
dE/dX 17	5	**R_dE/dX 17**	6
TR 17	7	**R_TR 17**	8
dE/dX 18	9	**R_dE/dX 18**	10
TR 18	11	**R_TR 18**	12
dE/dX 19	13	**R_dE/dX 19**	14
TR 19	15	**R_TR 19**	16
dE/dX 20	17	**R_dE/dX 20**	18
TR 20	19	**R_TR 20**	20
dE/dX 21	21	**R_dE/dX 21**	22
TR 21	23	**R_TR 21**	24
dE/dX 22	25	**R_dE/dX 22**	26
TR 22	27	**R_TR 22**	28
dE/dX 23	29	**R_dE/dX 23**	30
TR 23	31	**R_TR 23**	32
dE/dX 24	33	**R_dE/dX 24**	34
TR 24	35	**R_TR 24**	36
dE/dX 25	37	**R_dE/dX 25**	38
TR 25	39	**R_TR 25**	40
dE/dX 26	41	**R_dE/dX 26**	42
TR 26	43	**R_TR 26**	44
dE/dX 27	45	**R_dE/dX 27**	46
TR 27	47	**R_TR 27**	48
dE/dX 28	49	**R_dE/dX 28**	50
TR 28	51	**R_TR 28**	52
dE/dX 29	53	**R_dE/dX 28**	54
TR 29	55	**R_TR 29**	56
dE/dX 30	57	**R_dE/dX 30**	58
TR 30	59	**R_TR 30**	60
dE/dX 31	61	**R_dE/dX 31**	62
TR 31	63	**R_TR 31**	64
reserved	65	**reserved**	66
reserved	67	**reserved**	68
Strobe_P	69	**Strobe_N**	70
reserved	71	**reserved**	72
S1_P	73	**S1_N**	74
S2_P	75	**S2_N**	76
S3_P	77	**S3_N**	78
S4_P	79	**S4_N**	80

c. Serial link diagnostic connector pin assignment:

Connector 3:



- The serial link diagnostic connector[viii] is an 8 contact wire to board header.

The pin assignment is as follows:

Signal	Pin Number
Rdbk_P	1
Rdbk_N	2
DATA_P	3
DATA_N	4
CLK_P	5
CLK_N	6
LD_P	7
LD_N	8

---

[i] AMP Z-PACK 2mm future bus Male connector. AMP Part number: 223513-1
[ii] In TEC, the PS board components are mounted on to the PC board such that they are facing the core of the detector.
[iii] Final Power consumption numbers will be made available when the design of Revision 2 of the Preamp shaper board is finalized. For detailed information refer to TEC-Preamp Shaper Power consumption document [Oct-07-1996].
[iv] Amphenol, 0.025" TWIST 'N' Flat planar cable 425 series, 80 conductors [40 twisted pairs]. Amphenol part number: 425-3006-080
[v] Amphenol 0.025" High Density cable mount IDC sockets. Amphenol Part number: 845-C080S-ALA55.
[vi] Amphenol 0.025" High Density board mounted straight IDC sockets. Amphenol Part number: 845-A080P-ALA55.
[vii] Same as endnote ii.
[viii] Molex 1.25mm wire to board header; Molex part number: 53398-0890

Anand Kandasamy/tec_ps_specs4/Pages 10/02/20/97 2:09 PM

TEC Preamp Shaper Power$_i$ Consumption: Oct 07,1996

Specifications:

Inputs: 32
Outputs: 64 [1 De/Dx and 1 TR output per input]
Number of TEC-PS Chips / board : 4
Number of Line Drivers / board : 64

Power Numbers:

TEC-PS:
Current consumption per TEC-PS chip:

Vdd : 57 mA
Vss_{ii} : 52 mA

Current consumption per TEC-PS board:

Vdd : 228 mA
Vss_{ii} : 208 mA

Line Drivers:

Quiescent Current per driver : 2.75 mA
Total quiescent current per board : 176 mA

The Transmission Line is a 100 ohm system:

Case A: DeDx at its maximum output and TR at 1/5th of the DeDx output:
1 channel:
DeDx @ MAX[+2.5 or -2.5] : 25 mA
TR @ 1/5th of DeDx : 5 mA
32 Channel:
DeDx : 800 mA
TR : 160 mA

Total current consumption in case A: $I_{DeDx} + I_{TR} + I_q$

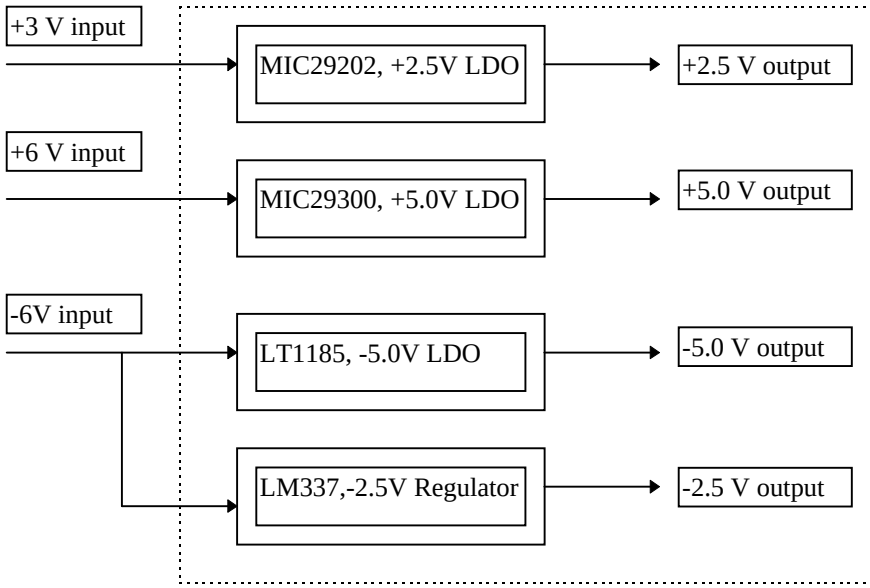
800 + 160 + 176
Total Case A: 1136mA

Case B: DeDx at its maximum output and TR at its maximum$_{iii}$:
1 channel:
DeDx @ MAX[+2.5 or -2.5] : 25 mA
TR @ MAX[+2.5 or -2.5] : 25 mA
32 Channel:
DeDx : 800 mA
TR : 800 mA

Total current consumption in case A: $I_{DeDx} + I_{TR} + I_q$

800 + 800 + 176
Total Case A: 1776mA

Regulation Scheme:



Current required from the Unregulated supply[iv]:

+3 Volts : 228 mA + 15 mA	=	243 mA
+6 Volts : 2 (800 mA) + 176mA + 35 mA	=	1811 mA
-6 Volts : 2 (800 mA) + 176 mA + 208 mA + 5mA	=	1989 mA

TEC-PS Front End current requirement:

Unregulated Supply	I peak	Iquiescent	Units
+3V	243	243	mA
+6V	1811	211	mA
-6V	1989	389	mA

Notes:

i) This power consumption numbers is not complete, as components like DAC and serial interface logic are not included.

ii) Actual current flow is I_{vdd} = 56.74 mA
I_{vss} = 52.19 mA
I_{gnd} = 4.55 mA
Ground current was neglected for simplicity:

iii) DeDx has a gain of 5 over the TR output, when TR goes to its maximum, DeDx will be clamped to its saturation output voltage.

iv) This Current includes the regulator current,
+3V : $I_{vdd,TECPS} + I_{reg}$
+6V: $I_{vcc,driver,DeDx} + I_{vcc,driver,TR} + I_{drivers,quiescent} + I_{reg}$
-6V: $I_{vee,driver,DeDx} + I_{vee,driver,TR} + I_{drivers,quiescent} + I_{vss,TECPS} + I_{reg}$

Quad 150 MHz Rail-to-Rail Amplifier

AD8044

FEATURES

Fully Specified for +3 V, +5 V, and ±5 V Supplies
Output Swings Rail to Rail
Input Voltage Range Extends 200 mV Below Ground
No Phase Reversal with Inputs 1 V Beyond Supplies
Low Power of 2.75 mA/Amp
High Speed and Fast Settling on +5 V:
- **150 MHz –3 dB Bandwidth (G = +1)**
- **170 V/µs Slew Rate**
- **45 ns Settling Time to 0.1%**

Good Video Specifications (R_L = 150 Ω, G = +2)
- **Gain Flatness of 0.1 dB to 12 MHz**
- **0.06% Differential Gain Error**
- **0.15° Differential Phase Error**

Low Distortion
- **–58 dBc Worst Harmonic @ 5 MHz**

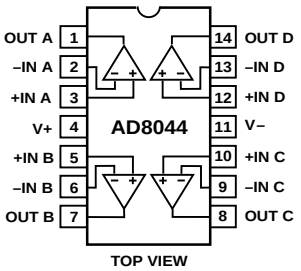
Outstanding Load Drive Capability
- **Drives 50 mA 0.5 V from Supply Rails**

Cap Load Drive of 45 pF

APPLICATIONS

Active Filters
Power Sensitive High Speed Systems
Video Switchers
Distribution Amplifiers
A/D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)

CONNECTION DIAGRAM
14-Pin Plastic Mini-DIP and SOIC



PRODUCT DESCRIPTION

The AD8044 is a quad low power, voltage feedback, high speed amplifier designed to operate on +3 V, +5 V or ±5 V supplies. It has true single-supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

The output voltage swing extends to within 25 mV of each rail, providing the maximum output dynamic range. Additionally, it features gain flatness of 0.1 dB to 12 MHz while offering differential gain and phase error of 0.05% and 0.25° on a single +5 V supply. This makes the AD8044 ideal for video electronics such as cameras, video switchers or any high speed portable equipment. The AD8044's low distortion and fast settling make it ideal for active filter applications.

The AD8044 offers low power supply current of 13 mA max and can run on a single +3 V power supply. These features are ideally suited for portable and battery powered applications where size and power are critical.

The wide bandwidth of 150 MHz along with 170 V/µs of slew rate on a single +5 V supply make the AD8044 useful in many general purpose, high speed applications where dual power supplies of up to ±6 V and single supplies from +3 V to +12 V are needed. The AD8044 is available in 14-pin plastic DIP and SOIC.

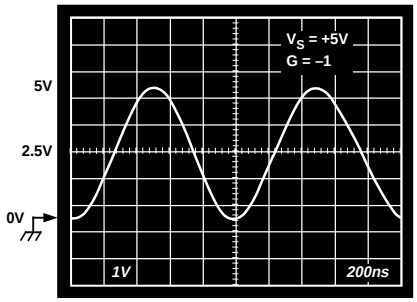


Figure 1. Output Swing: Gain = –1, V_S = +5 V

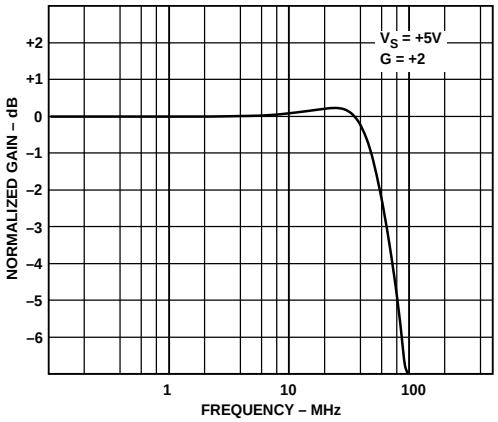


Figure 2. Frequency Response: Gain = +2, V_S = +5 V

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AD8044–SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	130	150		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		12		MHz
Slew Rate	G = –1, V_O = 2 V Step	140	170		V/µs
Full Power Response	V_O = 2 V p-p		26		MHz
Settling Time to 1%	G = –1, V_O = 2 V Step		30		ns
Settling Time to 0.1%			40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–75		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		850		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.04		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.22		Degrees
Crosstalk	f = 5 MHz, R_L = 1 kΩ, G = +2		60		dB
DC PERFORMANCE					
Input Offset Voltage			1.0	4	mV
	T_{MIN}–T_{MAX}			6.2	mV
Offset Drift			8		µV/°C
Input Bias Current			2	3.0	µA
	T_{MIN}–T_{MAX}			4	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	86	94		dB
	T_{MIN}–T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–0.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	80	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			0.03 to 4.975		V
R_L = 1 kΩ		0.17 to 4.83	0.075 to 4.91		V
R_L = 50 Ω		1.4 to 3.6	0.68 to 4.1		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = 0.5 V to 4.5 V		30		mA
Short Circuit Current	Sourcing		50		mA
	Sinking		90		mA
Capacitive Load Drive	G = +2		40		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			11	13	mA
Power Supply Rejection Ratio	V_S = 0, +5 V, ±1 V	72	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = +25°C, V_S = +3 V, R_L = 2 kΩ to 1.5 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	120	135		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		10		MHz
Slew Rate	G = –1, V_O = 2 V Step	125	150		V/µs
Full Power Response	V_O = 2 V p-p		22		MHz
Settling Time to 1%	G = –1, V_O = 2 V Step		35		ns
Settling Time to 0.1%			55		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = –1, R_L = 100 Ω		–54		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		600		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 1.5 V, Input V_{CM} = 0.5 V		0.13		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 1.5 V, Input V_{CM} = 0.5 V		0.3		Degrees
Crosstalk	f = 5 MHz		60		dB
DC PERFORMANCE					
Input Offset Voltage			1.5	4	mV
	T_{MIN}–T_{MAX}			6.2	mV
Offset Drift			8		µV/°C
Input Bias Current			2	3.5	µA
	T_{MIN}–T_{MAX}			3.5	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	86	92		dB
	T_{MIN}–T_{MAX}		89		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–0.2 to 2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	76	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			0.025 to 2.98		V
R_L = 1 kΩ		0.15 to 2.85	0.06 to 2.93		V
R_L = 50 Ω		1.0 to 2.0	0.4 to 2.4		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = 0.5 V to 2.5 V		25		mA
Short Circuit Current	Sourcing		35		mA
	Sinking		50		mA
Capacitive Load Drive	G = +2		35		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			10.5	12.2	mA
Power Supply Rejection Ratio	V_S = 0, +3 V, ±0.5 V	72	80		dB
OPERATING TEMPERATURE RANGE		0		+70	°C

Specifications subject to change without notice.

AD8044–SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 2 kΩ to 0 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	140	160		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		15		MHz
Slew Rate	G = –1, V_O = 2 V Step	150	190		V/µs
Full Power Response	V_O = 2 V p-p		29		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		30		ns
Settling Time to 0.01%			40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–77		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		900		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω		0.06		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω		0.15		Degrees
Crosstalk	f = 5 MHz		60		dB
DC PERFORMANCE					
Input Offset Voltage			1.4	4.5	mV
	T_{MIN}–T_{MAX}			6.8	mV
Offset Drift			10		µV/°C
Input Bias Current			2	3.5	µA
	T_{MIN}–T_{MAX}			3.5	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	90	96		dB
	T_{MIN}–T_{MAX}		95		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–5.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = –5 V to 3.5 V	76	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			–4.97 to +4.97		V
R_L = 1 kΩ		–4.75 to +4.75	–4.85 to +4.85		V
R_L = 50 Ω		–1.5 to +1.5	–2.5 to +2.5		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = –4.5 V to +4.5 V		30		mA
Short Circuit Current	Sourcing		60		mA
	Sinking		110		mA
Capacitive Load Drive	G = +2		40		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			11.5	13.5	mA
Power Supply Rejection Ratio	V_S = –5, +5 V, ±1 V	72	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +12.6 V
Internal Power Dissipation[2]
  Plastic Package (N) . . . . . 1.6 Watts
  Small Outline Package (R) . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±3.4 V
Output Short Circuit Duration
  . . . . . Observe Power Derating Curves
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for the device in free air:
14-Pin Plastic Package: θ_{JA} = 75°C/Watt
14-Pin SOIC Package: θ_{JA} = 120°C/Watt.

ORDERING GUIDE

Model	Supply Voltage	Temperature Range	Package Description
AD8044AN	+5, ±5	–40°C to +85°C	14-Pin Plastic DIP (N-14)
AD8044AN	+3	0°C to +70°C	14-Pin Plastic DIP (N-14)
AD8044AR	+5, ±5	–40°C to +85°C	14-Pin Plastic SOIC (R-14)
AD8044AR	+3	0°C to +70°C	14-Pin Plastic SOIC (R-14)
AD8044AR-REEL			REEL-SOIC (R-14)

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8044 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8044 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

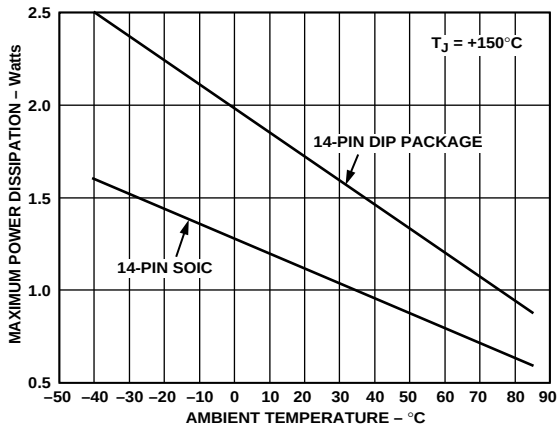


Figure 3. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8044 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8044–Typical Performance Characteristics

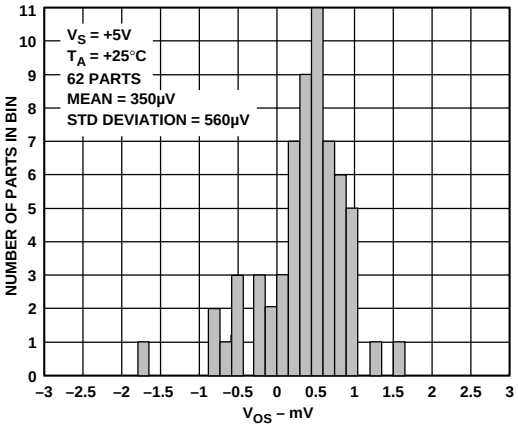


Figure 4. Typical Distribution of V_{OS}

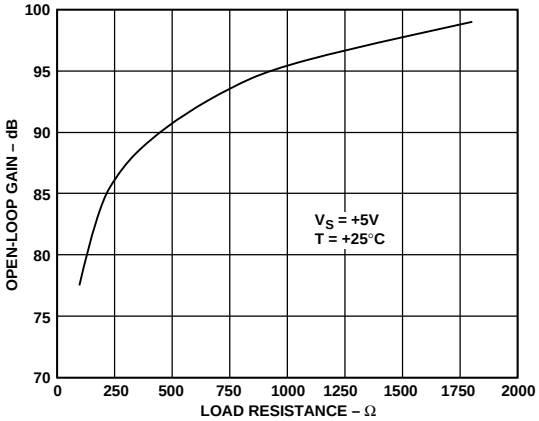


Figure 7. Open-Loop Gain vs. R_L to +2.5 V

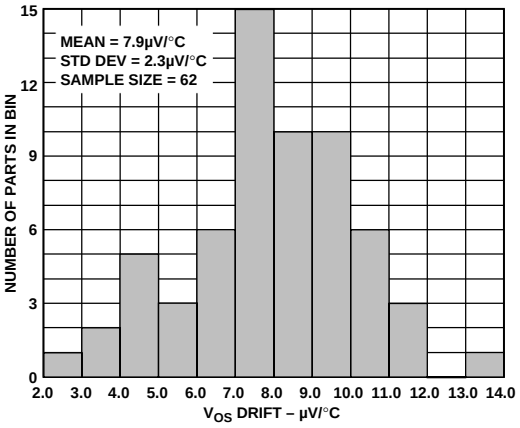


Figure 5. V_{OS} Drift Over –40°C to +85°C

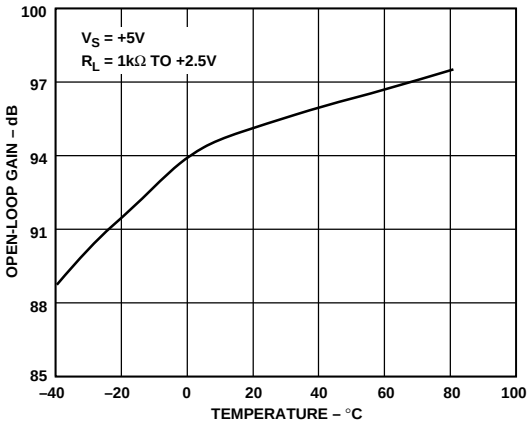


Figure 8. Open-Loop Gain vs. Temperature

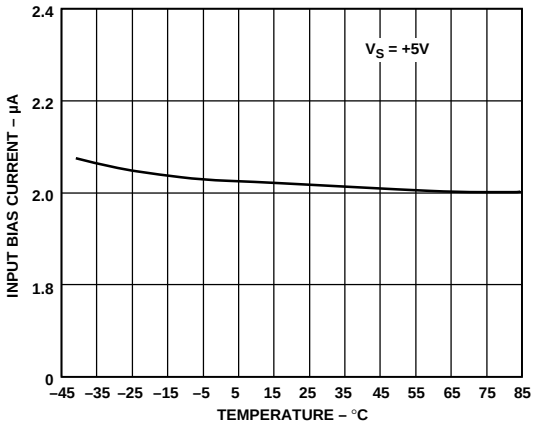


Figure 6. I_B vs. Temperature

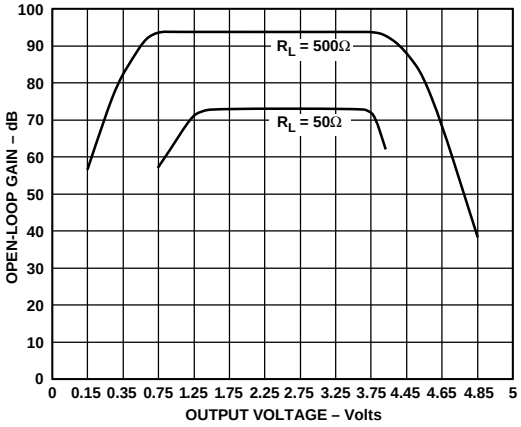


Figure 9. Open-Loop Gain vs. Output Voltage

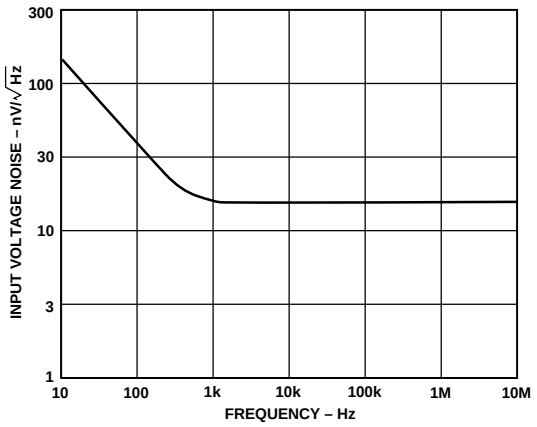


Figure 10. Input Voltage Noise vs. Frequency

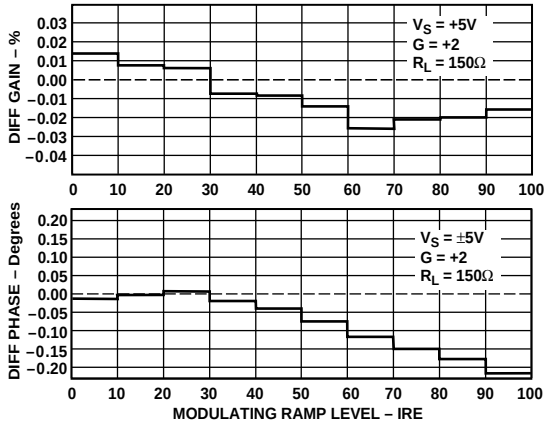


Figure 13. Differential Gain and Phase Errors

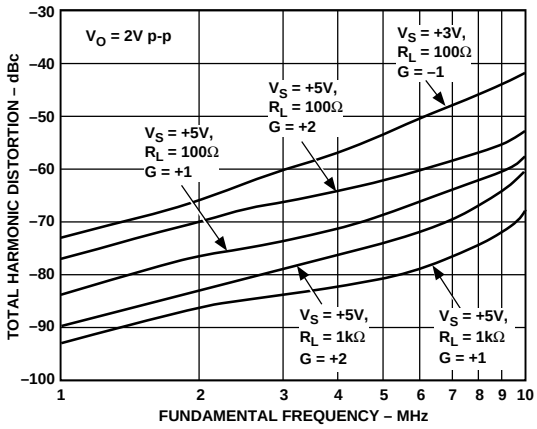


Figure 11. Total Harmonic Distortion

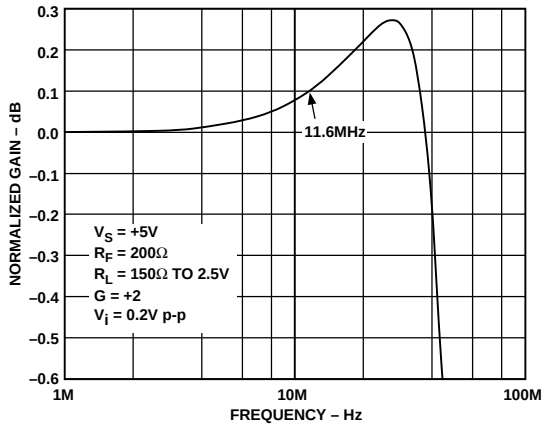


Figure 14. 0.1 dB Gain Flatness

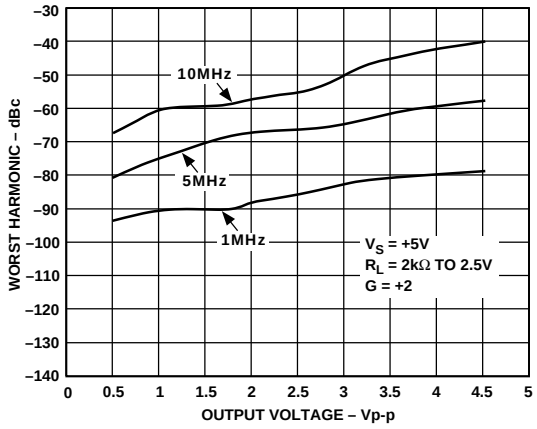


Figure 12. Worst Harmonic vs. Output Voltage

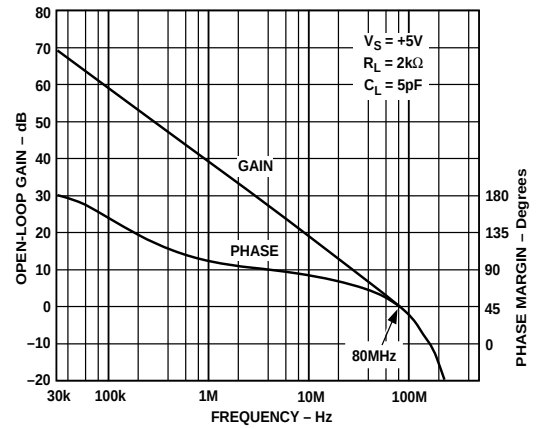


Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

AD8044–Typical Performance Characteristics

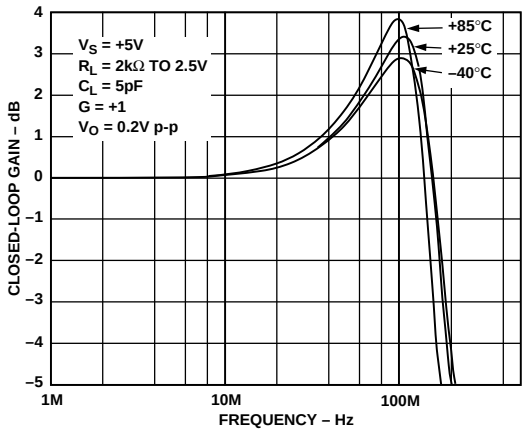


Figure 16. Closed-Loop Frequency Response vs. Temperature

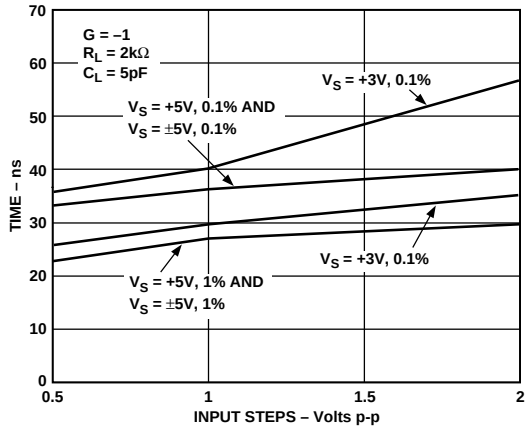


Figure 19. Settling Time vs. Input Step

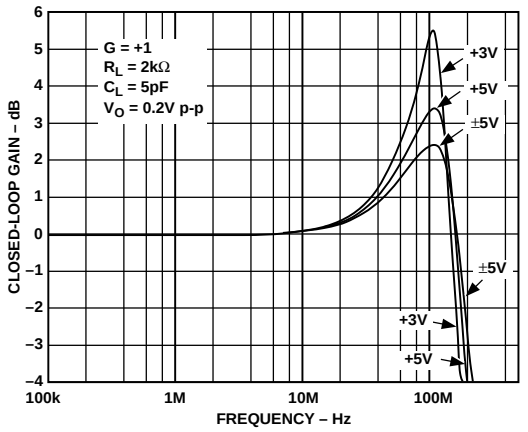


Figure 17. Closed-Loop Frequency Response vs. Supply

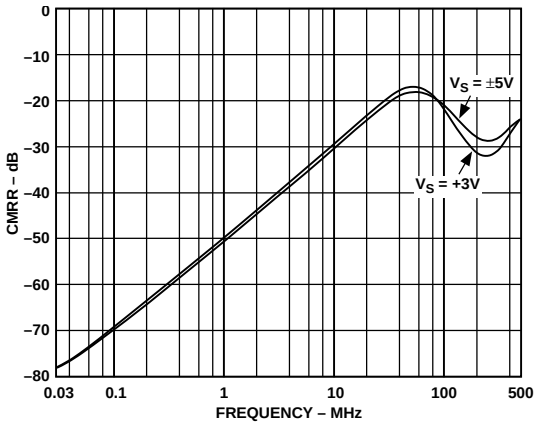


Figure 20. CMRR vs. Frequency

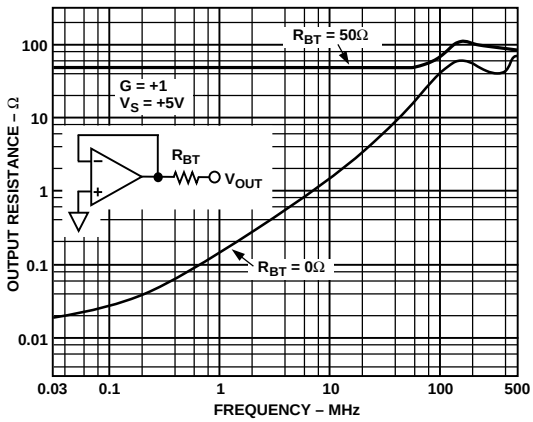


Figure 18. Output Resistance vs. Frequency

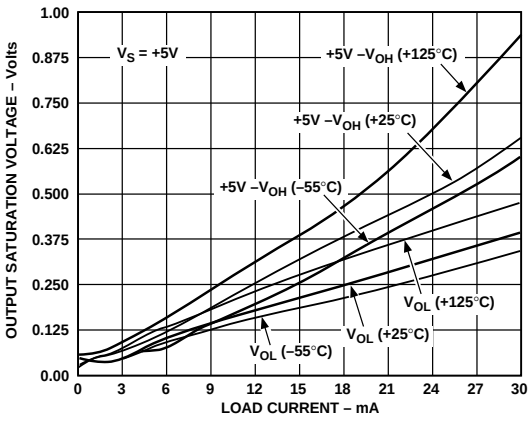


Figure 21. Output Saturation Voltage vs. Load Current

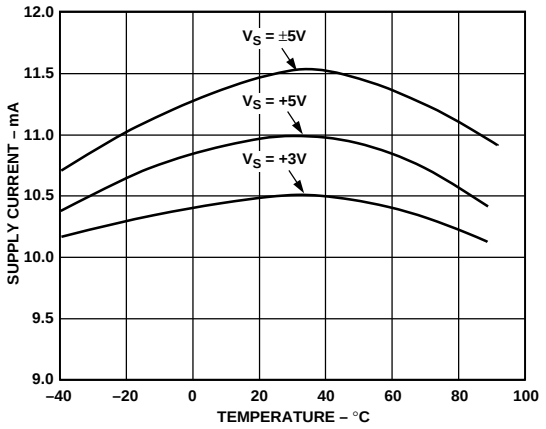


Figure 22. Supply Current vs. Temperature

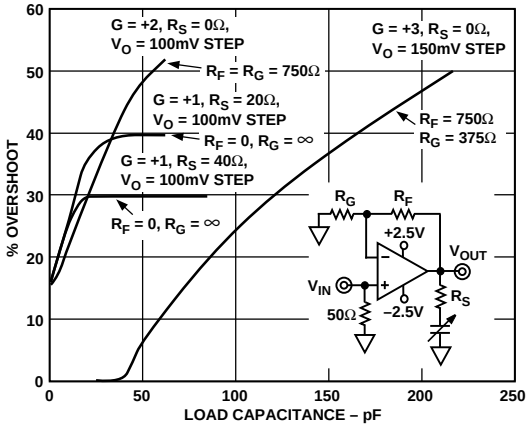


Figure 25. % Overshoot vs. Capacitive Load

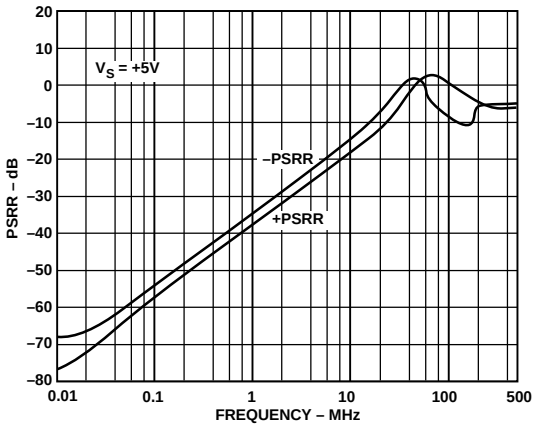


Figure 23. PSRR vs. Frequency

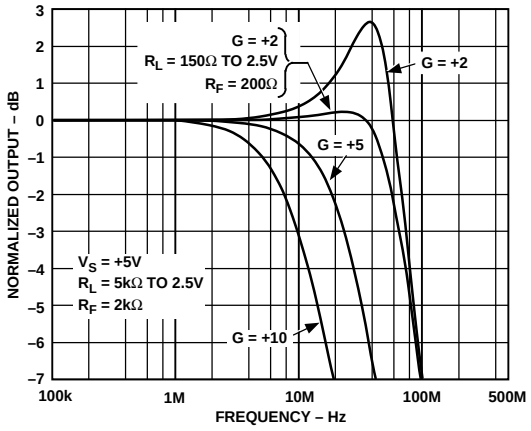


Figure 26. Frequency Response vs. Closed-Loop Gain

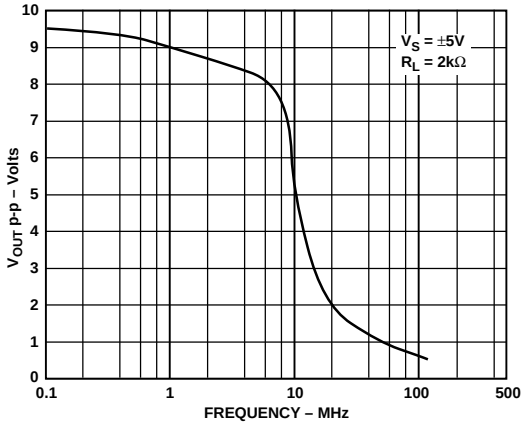


Figure 24. Output Voltage Swing vs. Frequency

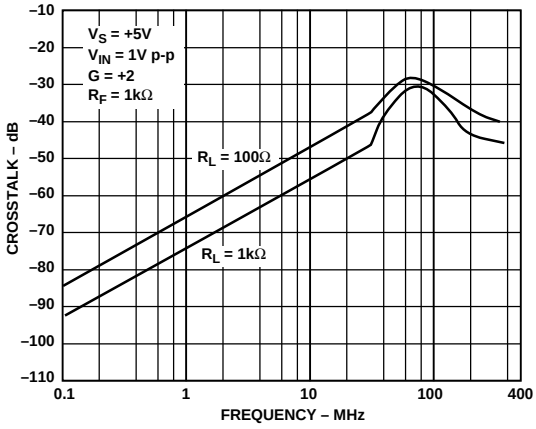
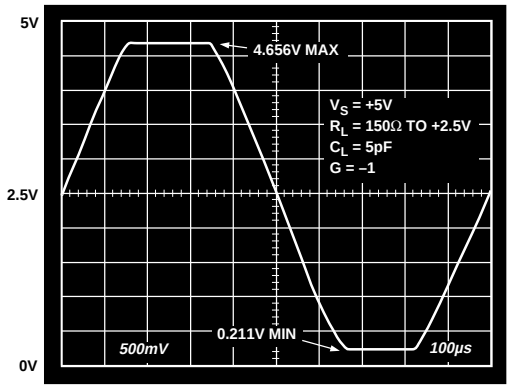
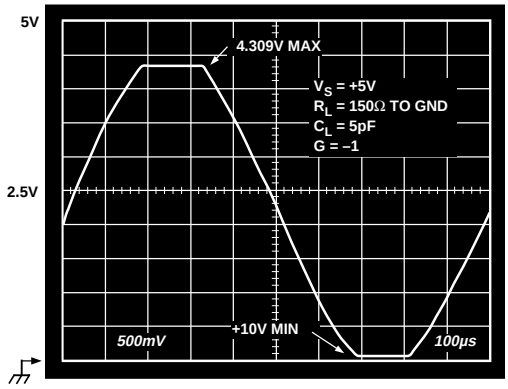


Figure 27. Crosstalk (Output to Output) vs. Frequency

AD8044–Typical Performance Characteristics



a.



b.

Figure 28. Output Swing vs. Load Reference Voltage, V_S = +5 V, G = –1

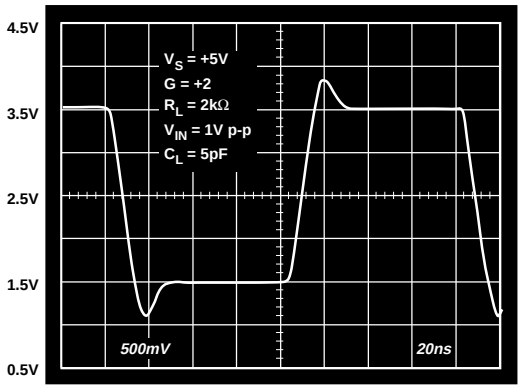


Figure 29. One Volt Step Response, V_S = +5 V, G = +2

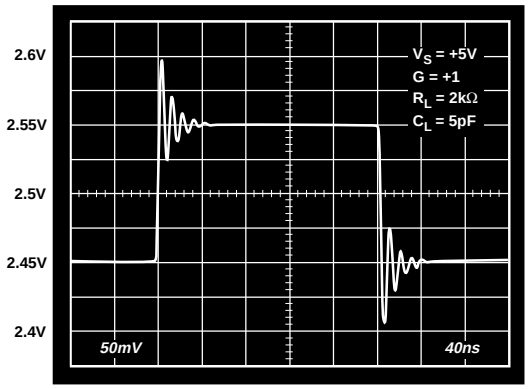


Figure 30. 100 mV Step Response, V_S = +5 V, G = +1

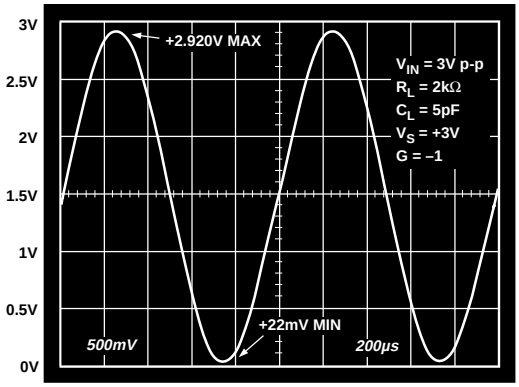


Figure 31. Output Swing, V_S = +3 V

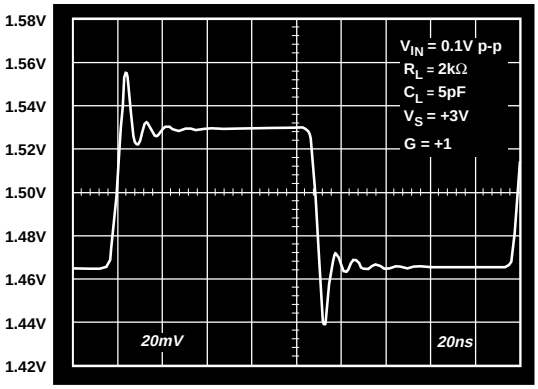


Figure 32. Step Response, G = +1, V_{IN} = 100 mV

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 33, the AD8044 recovers within 50 ns from negative overdrive and within 25 ns from positive overdrive.

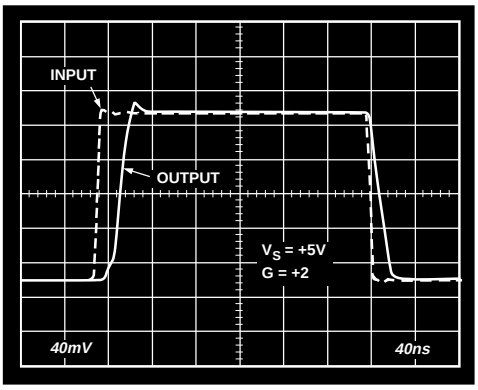


Figure 33. Overdrive Recovery

Circuit Description

The AD8044 is fabricated on Analog Devices' proprietary eXtra-Fast Complementary Bipolar (XFCB) process which enables the construction of PNP and NPN transistors with similar f_Ts in the 2 GHz–4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features allow the construction of high frequency, low distortion amplifiers with low supply currents. This design uses a differential output input stage to maximize bandwidth and headroom (see Figure 34). The smaller signal swings required on the first stage outputs (nodes S1P, S1N) reduce the effect of nonlinear currents due to junction capacitances and improve the distortion performance. With this design harmonic distortion of better than –85 dB @ 1 MHz into 100 Ω with V_{OUT} = 2 V p-p (Gain = +2) on a single 5 volt supply is achieved.

The AD8044's rail to rail output range is provided by a complementary common-emitter output stage. High output drive capability is provided by injecting all output stage predriver currents directly into the bases of the output devices Q8 and Q36. Biasing of Q8 and Q36 is accomplished by I8 and I5, along with a common-mode feedback loop (not shown). This circuit topology allows the AD8044 to drive 50 mA of output current with the outputs within 0.5 V of the supply rails.

On the input side, the device can handle voltages from –0.2 V below the negative rail to within 1.2 V of the positive rail. Exceeding these values will not cause phase reversal; however, the input ESD devices will begin to conduct if the input voltages exceed the rails by greater than 0.5 V.

Output Impedance and Capacitance Drive

The AD8044's common-emitter output stage is very different than a typical emitter follower topology. Nonetheless, the amplifier's output impedance behaves the same way as traditional designs in a typical feedback application. The 110 dB loop gain reduces it to less than 0.1 Ω at low frequencies. At higher frequencies, the output impedance rises as the loop gain of the circuit drops (Figure 18). The output impedance eventually becomes capacitive due to integrator transistors C3 and C9.

Capacitive loads interact with the circuit output impedance to create an extra delay in the feedback path. This reduces circuit stability, and can cause unwanted ringing and oscillation. A given value of capacitance causes much less of an effect when the amplifier is used in a higher noise gain. This is illustrated in Figure 25, which plots the percent overshoot of the amplifier's step response when used in gains of +1, +2 and +3.

If greater phase margin is desired, a small resistor in series with the output can be used to isolate the loop from the effect of the load capacitance. Figure 25 shows the effect of this strategy with G = 4.

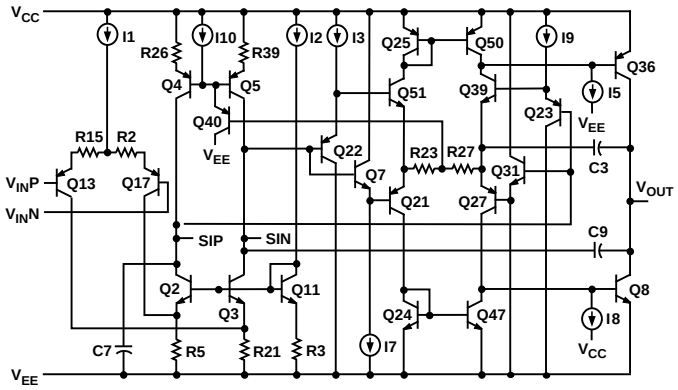


Figure 34. AD8044 Simplified Schematic

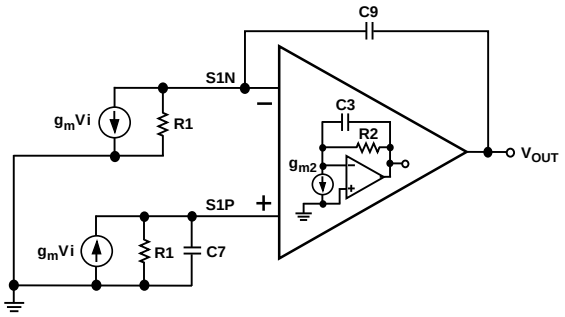


Figure 35. Small Signal Schematic

APPLICATIONS

RGB Buffer

The AD8044 can provide buffering of RGB signals that include ground while operating from a single +3 V or +5 V supply.

When driving two monitors from the same RGB video source it is necessary to provide an additional driver for one of the monitors to prevent the double termination situation that the second monitor presents. This has usually required a dual supply op amp, because the level of the input signal from the video driver goes all the way to ground during horizontal blanking. In single supply systems it can be a major inconvenience and expense to add an additional negative supply.

A single AD8044 can provide the necessary drive capability and yet does not require a negative supply in this application. Figure ?? is a schematic that uses three amplifiers out of a single AD8044 to provide buffering for a second monitor.

The source of the RGB signals is shown to be from a set of three current output DACs that are within a single supply graphics IC. This is typically the situation in most PCs and workstations which might use either a stand-alone triple DAC or the DACs could be integrated into a larger graphics chip.

During horizontal blanking, the current output from the DACs is turned off and the RGB outputs are pulled to ground by the termination resistors. If voltage sources were used for the RGB signals, then the termination resistors near the graphics IC would be in series and the rest of the circuit would remain the same. This is because a voltage source is an ac short circuit, so a series resistor is required to make the drive end of the line see 75 Ω to ac ground. On the other hand, a current source has a very high output impedance, so a shunt resistor is required to make the drive end of the line see 75 Ω to ground. In either case, the monitor terminates its end of the line with 75 Ω.

The circuit of Figure 36 shows minimum signal degradation when using a single supply for the AD8044. The circuit performs equally well on either a +3 V or +5 V supply.

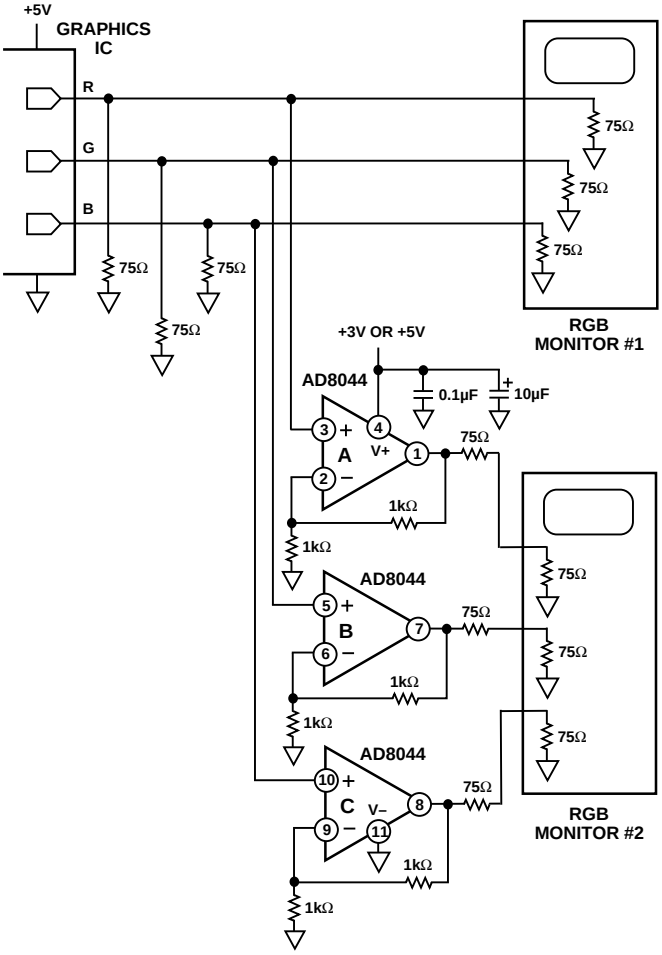


Figure 36. Single Supply RGB Video Driver

Figure 37 is an oscilloscope photo of the circuit in Figure 36 operating from a +3 V supply and driven by the Blue signal of a color bar pattern. Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700 mV peak. The output of the AD8044 is 1.4 V with the termination resistors providing a divide-by-two.

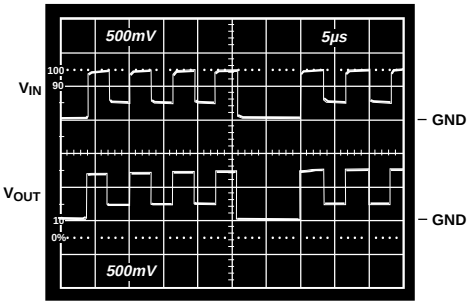


Figure 37. +3 V, RGB Buffer

HDSL Line Driver

HDSL or high-bit-rate digital subscriber line is becoming popular as a means to provide data communication at DS1 rates (1.544 MBPS) over moderate distances via conventional telephone twisted pair wires. In these systems, the transceiver at the customer's end is sometimes powered via the twisted pair from a power source at the central office. It is sometimes required to raise the dc voltage of the power source to compensate for IR drops in long lines or lines with narrow gauge wires.

Because of this, it is highly desirable to keep the power consumption of the customer's transceiver as low as possible. One means to realize significant power savings is to run the transceiver from a ±5 V supply instead of the more conventional ±12 V. This has not

The high output swing and current drive capability of the AD8042 make it ideally suited to this application. Figure 41 shows a circuit for the analog portion of an HDSL transceiver using the AD8042 as the line driver.

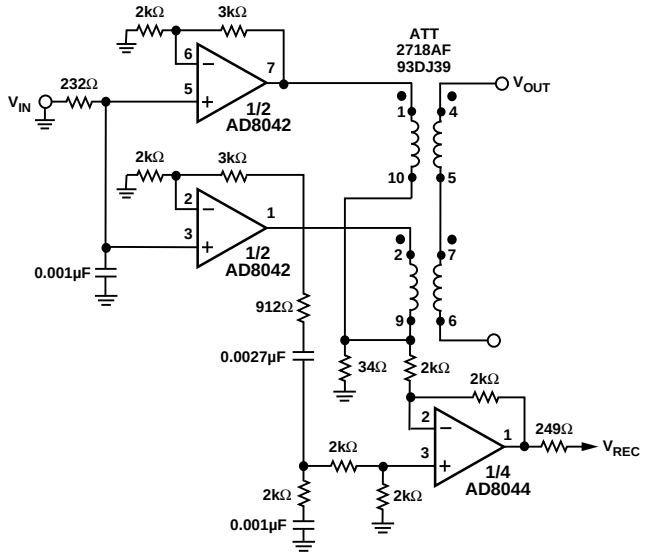


Figure 38. Twisted Pair Driver

Active Filters

Active filters at higher frequencies require wider bandwidth op amps to work effectively. Excessive phase shift produced by lower frequency op amps can significantly impact active filter performance.

Figure 39 shows an example of a 2 MHz biquad bandwidth filter that uses three op amps of an AD8044 package. Such circuits are sometimes used in medical ultrasound systems to lower the noise bandwidth of the analog signal before A/D conversion.

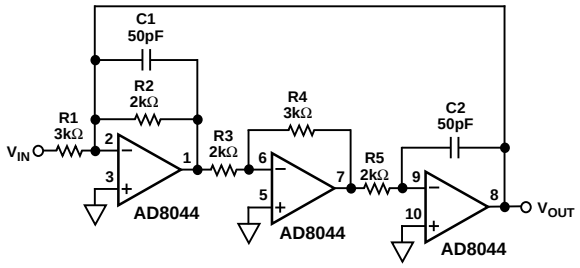


Figure 39. 2 MHz Biquad Bandpass Filter Using AD8044

The frequency response of the circuit is shown in Figure 40.

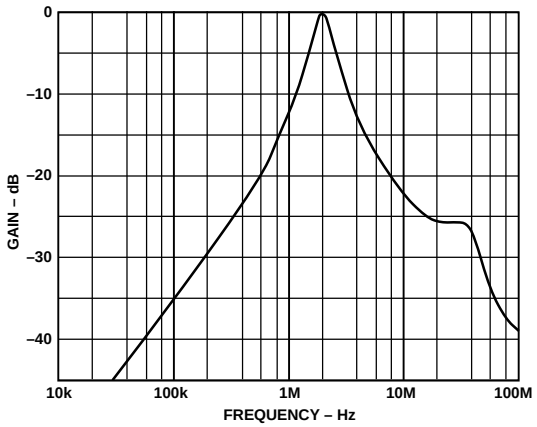


Figure 40. Frequency Response of 2 MHz Bandpass Biquad Filter

Layout Considerations

The specified high speed performance of the AD8044 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are necessary.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce the stray capacitance.

Chip capacitors should be used for the supply bypassing. One end should be connected to the ground plane and the other within 1/8 inch of each power pin. An additional large (0.47 μF – 10 μF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large signal changes at the output.

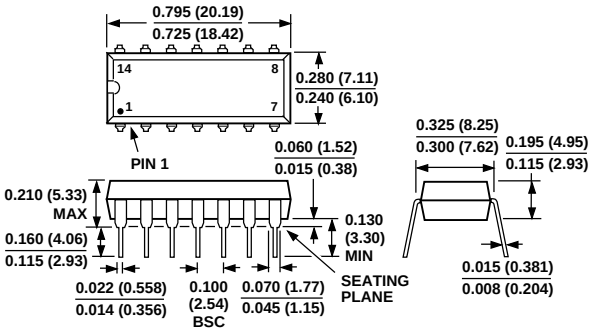
The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

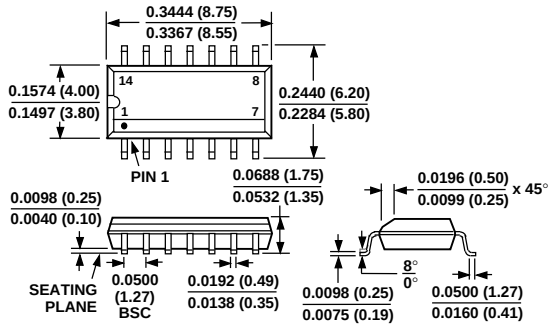
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP (N-14)



14-Lead SOIC (R-14)

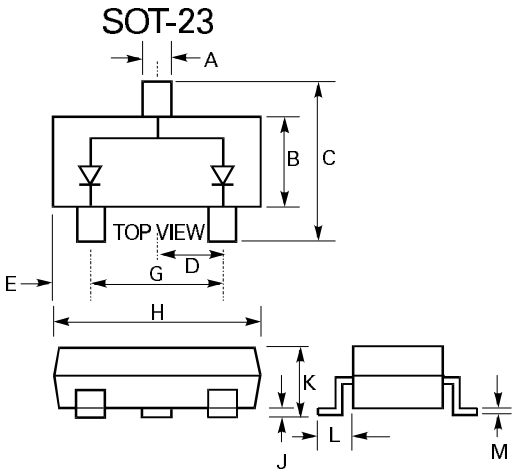


BAW56

SURFACE MOUNT SWITCHING DIODE

Features

- High Conductance
- Ultra Fast Switching Time
- Dual Diode with Common Anode Connection



Mechanical Data

- TERMINALS: Solderable per MIL-STD-202, Method 208
- CASE: SOT-23 Molded Plastic
- MOUNTING POSITION: Any
- POLARITY: See Diagram
- WEIGHT: 0.008 gram

Alternate Marking Codes:
A1, JD, RA1, P

	Min	Max
A	0.37	0.50
B	1.19	1.40
C	2.10	2.50
D	0.89	1.05
E	0.45	0.61
G	1.78	2.05
H	2.79	3.05
J	0.013	0.150
K	0.89	1.10
L	0.45	0.61
M	0.076	0.130
All Dimensions in mm		

Maximum Ratings Single Diode

Characteristic	Symbol	Value	Unit
Power Dissipation @ T_A = 25°C for Total Package (Mounted)	P_d	300	mW
Reverse Voltage, Peak Reverse Voltage	V_R, V_{RM}	70	V
Peak Forward Current	I_{FM}	300	mA
Average Rectified Current	I_{AV}	100	mA
Peak Forward Surge Current —Pulse Width = 1μSec —Pulse Width = 1 Second	I_{FSM}	2.0 0.5	A A
Storage & Operating Temperature	T_j, T_{STG}	-55 to +150	°C

Electrical Characteristics Single Diode @ T_A = 25°C Unless otherwise specified

Characteristic	Test Conditions	Symbol	Min	Max	Unit
Breakdown Voltage	I_R = 100μA	$V_{(BR)}$	70		V
Reverse Current	V_R = 70V V_R = 25V, T_A = 150°C V_R = 70V, T_A = 150°C	I_R	—	5 30 100	μA
Forward Voltage	I_F = 1.0mA I_F = 10mA I_F = 50mA I_F = 150mA	V_F	—	715 0.855 1.0 1.25	mV V V V
Reverse Recovery Time	I_F = I_R = 10mA I_{RR} = 1.0mA R_L = 100Ω	T_{rr}	—	6.0	nSec
Diode Capacitance	V_F = V_R = 0 f = 1MHz	C_T	—	4.0	pF

To order/reorder this document please request Data Sheet BAW56 Rev. C 8/13/96 or current revision.

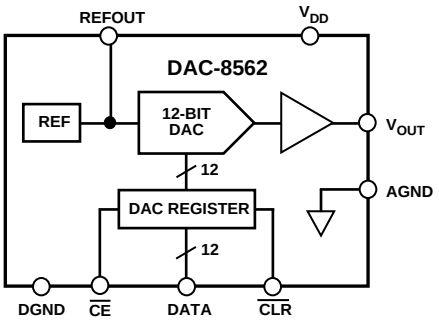
+5 Volt, Parallel Input Complete 12-Bit DAC

DAC8562

FEATURES
Complete 12-Bit DAC
No External Components
Single +5 Volt Operation
1 mV/Bit with 4.095 V Full Scale
True Voltage Output, ±5 mA Drive
Very Low Power –3 mW

APPLICATIONS
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC8562 is a complete, parallel input, 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DAC, is a rail-to-rail amplifier, latch and reference. The reference (REFOUT) is trimmed to 2.5 volts, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The DAC8562 is coded straight binary. The op amp output swings from 0 to +4.095 volts for a one millivolt per bit resolution, and is capable of driving ±5 mA. Built using low temperature-coefficient silicon-chrome thin-film resistors, excellent linearity error over temperature has been achieved as shown below in the linearity error versus digital input code plot.

Digital interface is parallel and high speed to interface to the fastest processors without wait states. The interface is very simple requiring only a single $\overline{CE}$ signal. An asynchronous $\overline{CLR}$ input sets the output to zero scale.

The DAC8562 is available in two different 20-pin packages, plastic DIP and SOL-20. Each part is fully specified for operation over –40°C to +85°C, and the full +5 V ± 5% power supply range.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8562/883 data sheet which specifies operation over the –55°C to +125°C temperature range.

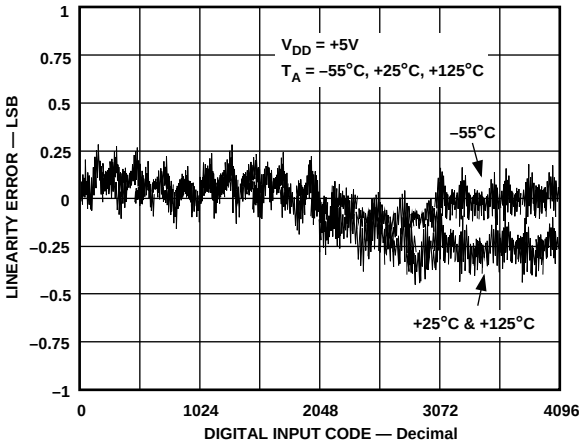


Figure 1. Linearity Error vs. Digital Input Code Plot

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

DAC8562–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 ± 5%, R_S = No Load, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 2	12			Bits
Relative Accuracy	INL	E Grade	–1/2	±1/4	+1/2	LSB
		F Grade	–1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data - FFF_H[3]				
		E Grade	4.087	4.095	4.103	V
		F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4		±16		ppm/°C
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H	±5	±7		mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[4]		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 5	5	7		mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA			0.1	%/mA
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 4			10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]						
Chip Enable Pulse Width	t_{CEW}		30			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Clear Pulse Width	t_{CLRW}		20			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough				35		nV sec
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB = 1 mV for 0 to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]Very little sink current is available at the REFOUT pin. Use external buffer if setting up a virtual ground.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{DD} = +5.0 V ± 5%, R_L = No Load, T_A = +25°C, applies to part number DAC8562GBC only, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Relative Accuracy	INL		–1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	–1	±3/4	+ 1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H	4.085	4.095	4.105	V
Reference Output Voltage	V_{REF}		2.490	2.500	2.510	V
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5 V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTE
[1]Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND and AGND . . . . . –0.3 V, +10 V
Logic Inputs to DGND . . . . . –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . –0.3 V, V_{DD} + 0.3 V
V_{REFOUT} to AGND . . . . . –0.3 V, V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V, V_{DD}
I_{OUT} Short Circuit to GND . . . . . 50 mA
Package Power Dissipation . . . . . (T_J max – T_A)/θ_{JA}
Thermal Resistance θ_{JA}
20-Pin Plastic DIP Package (P) . . . . . 74°C/W
20-Lead SOIC Package (S) . . . . . 89°C/W
Maximum Junction Temperature (T_J max) . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

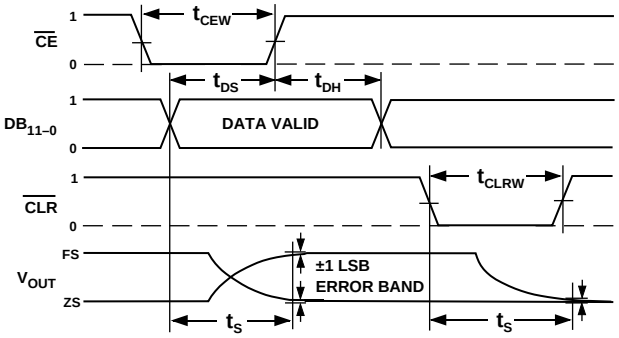


Figure 2. Timing Diagram

Table I. Control Logic Truth Table

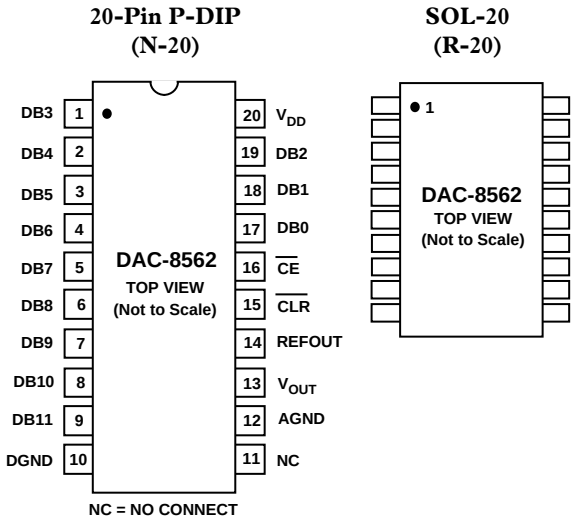
$\overline{CE}$	$\overline{CLR}$	DAC Register Function
H	H	Latched
L	H	Transparent
↑ +	H	Latched with New Data
X	L	Loaded with All Zeros
H	↑ +	Latched All Zeros

↑ + Positive Logic Transition; X Don't Care.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

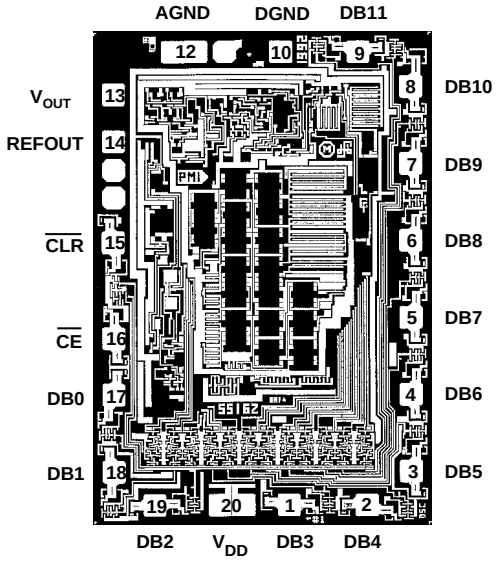
PIN CONFIGURATIONS



ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Option
DAC8562EP	±1/2	–40°C to +85°C	N-20
DAC8562FP	±1	–40°C to +85°C	N-20
DAC8562FS	±1	–40°C to +85°C	R-20
DAC8562GBC	±1	+25°C	Dice

DICE CHARACTERISTICS



SUBSTRATE IS COMMON WITH V_{DD}.

TRANSISTOR COUNT: 524

DIE SIZE: 0.70 X 0.105 INCH; 7350 SQ MILS

Table II. Nominal Output Voltage vs. Input Code

Binary	Hex	Decimal	Output (V)
0000 0000 0000	000	0	0.000 Zero Scale
0000 0000 0001	001	1	0.001
0000 0000 0010	002	2	0.002
0000 0000 1111	00F	15	0.015
0000 0001 0000	010	16	0.016
0000 1111 1111	0FF	255	0.255
0001 0000 0000	100	256	0.256
0001 1111 1111	1FF	511	0.511
0010 0000 0000	200	512	0.512
0011 1111 1111	3FF	1023	1.023
0100 0000 0000	400	1024	1.024
0111 1111 1111	7FF	2047	2.047
1000 0000 0000	800	2048	2.048 Half Scale
1100 0000 0000	C00	3072	3.072
1111 1111 1111	FFF	4095	4.095 Full Scale

PIN DESCRIPTIONS

Pin	Name	Description
20	V_{DD}	Positive supply. Nominal value +5 volts, ±5%.
1-9 17-19	DB0-DB11	Twelve Binary Data Bit inputs. DB11 is the MSB and DB0 is the LSB.
16	$\overline{CE}$	Chip Enable. Active low input.
15	$\overline{CLR}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale.
8	DGND	Digital ground for input logic.
12	AGND	Analog Ground. Ground reference for the internal bandgap reference voltage, the DAC, and the output buffer.
13	V_{OUT}	Voltage output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.
14	REFOUT	Nominal 2.5 V reference output voltage. This node must be buffered if required to drive external loads.
11	NC	No Connection. Leave pin floating.

OPERATION

The DAC8562 is a complete ready to use 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains a voltage-switched, 12-bit, laser-trimmed digital-to-analog converter, a curvature-corrected bandgap reference, a rail-to-rail output op amp, and a DAC register. The parallel data interface consists of 12 data bits, DB0–DB11, and a active low $\overline{CE}$ strobe. In addition, an asynchronous $\overline{CLR}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output (not available to the user) is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

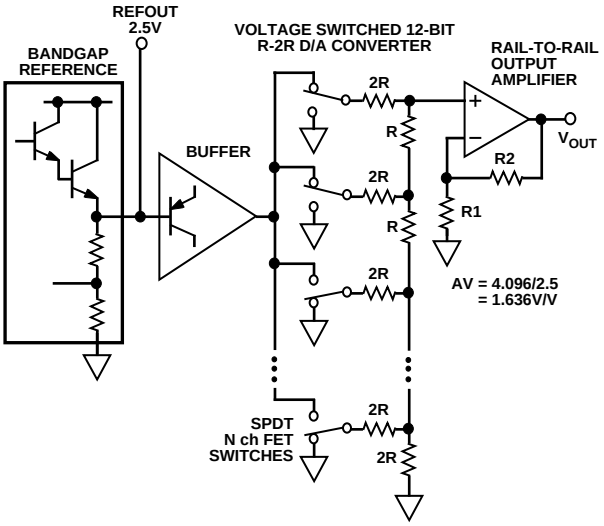


Figure 3. Equivalent DAC8562 Schematic of Analog Portion

The op amp has a 16 µs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the Typical Performances section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the –5% supply tolerance value of 4.75 volts.

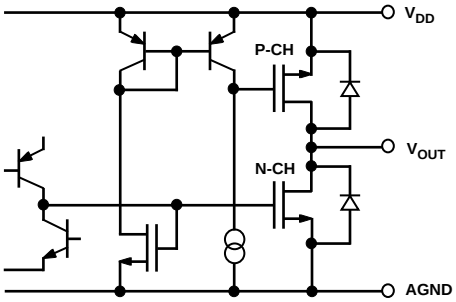


Figure 4. Equivalent Analog Output Circuit

Figures 5 and 6 in the typical performance characteristics section provide information on output swing performance near ground and full scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the REFOUT pin. Since REFOUT is not intended to drive external loads, it must be buffered–refer to the applications section for more information. The equivalent emitter follower output circuit of the REFOUT pin is shown in Figure 3.

Bypassing the REFOUT pin is not required for proper operation. Figure 7 shows broadband noise performance.

POWER SUPPLY

The very low power consumption of the DAC8562 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the DAC8562 is strongly dependent on the actual logic-input voltage-levels present on the DB0–DB11, $\overline{CE}$ and $\overline{CLR}$ pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total DAC8562 supply current as a function of the actual value of input logic voltage. Consequently for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the DB0–DB11 pins provides the lowest standby dissipation of 600 µA with a +5 V power supply.

As with any analog system, it is recommended that the DAC8562 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the DAC8562 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the DAC8562 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 11, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The DAC8562 has a 12-bit DAC register that simplifies interface to a 12-bit (or wider) data bus. The latch is controlled by the Chip Enable ($\overline{CE}$) input. If the application does not involve a data bus, wiring $\overline{CE}$ low allows direct operation of the DAC.

The data latch is level triggered and acquires data from the data bus during the time period when $\overline{CE}$ is low. When $\overline{CE}$ goes high, the data is latched into the register and held until $\overline{CE}$ returns low. The minimum time required for the data to be present on the bus before $\overline{CE}$ returns high is called the data setup time (t_{DS}) as seen in Figure 2. The data hold time (t_{DH}) is the amount of time that the data has to remain on the bus after $\overline{CE}$ goes high. The high speed timing offered by the DAC8562 provides for direct interface with no wait states in all but the fastest microprocessors.

Typical Performance Characteristics

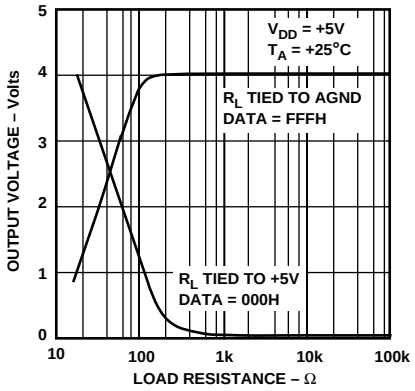


Figure 5. Output Swing vs. Load

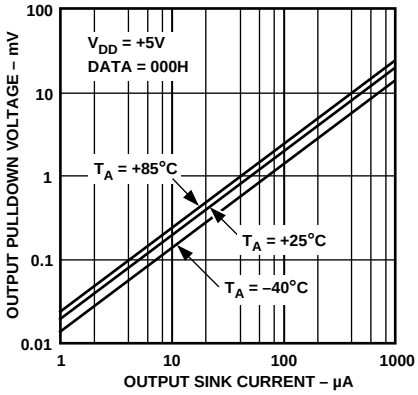


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

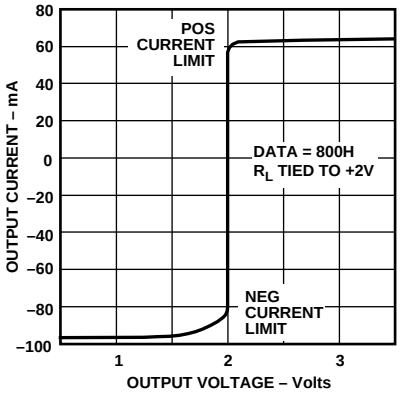


Figure 7. I_{OUT} vs. V_{OUT}

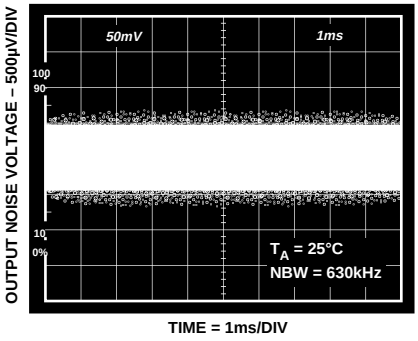


Figure 8. Broadband Noise

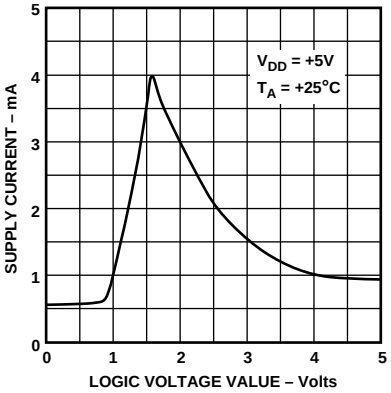


Figure 9. Supply Current vs. Logic Input Voltage

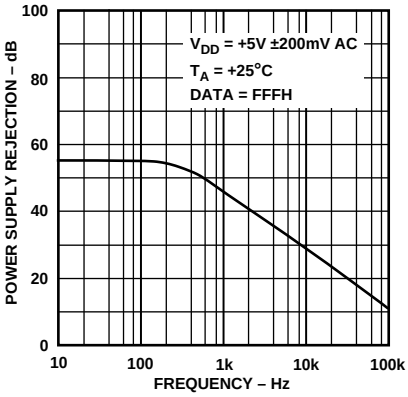


Figure 10. Power Supply Rejection vs. Frequency

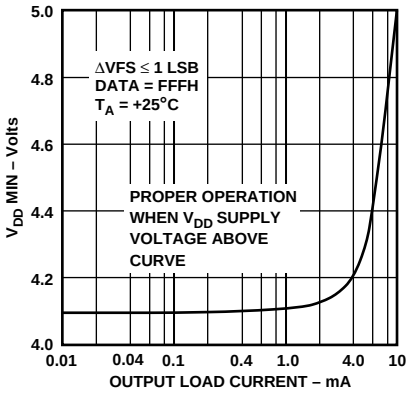


Figure 11. Minimum Supply Voltage vs. Load

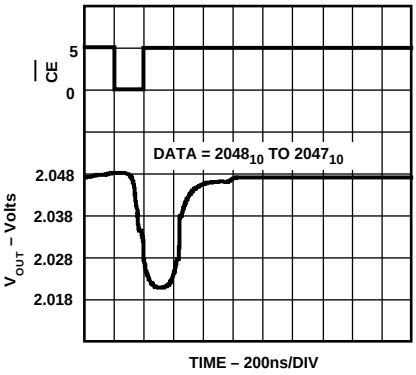


Figure 12. Midscale Transition Performance

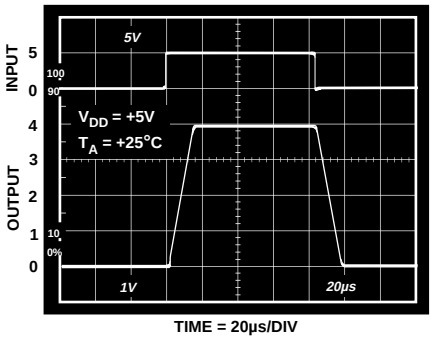


Figure 13. Large Signal Settling Time

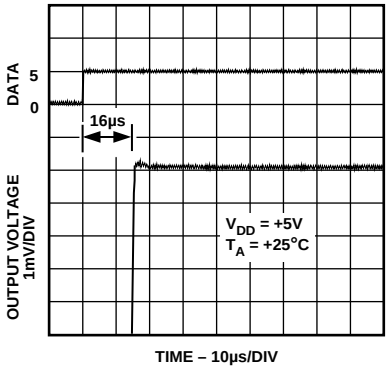


Figure 14. Output Voltage Rise Time Detail

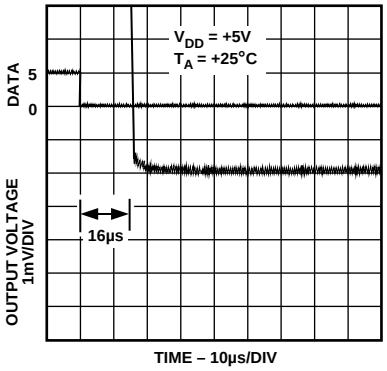


Figure 15. Output Voltage Fall Time Detail

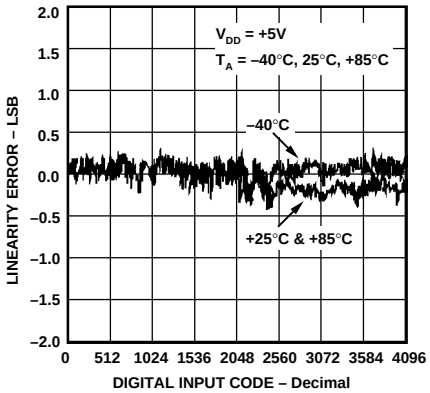


Figure 16. Linearity Error vs. Digital Code

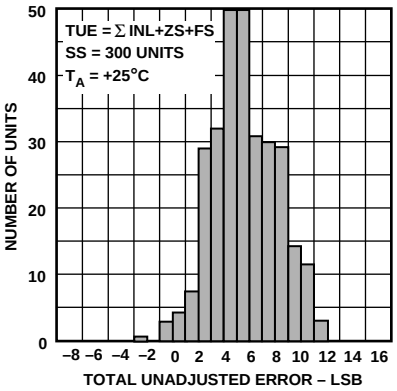


Figure 17. Total Unadjusted Error Histogram

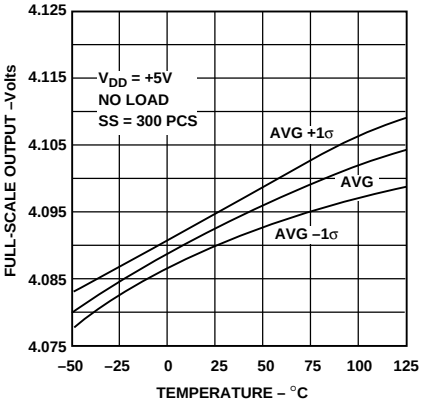


Figure 18. Full-Scale Voltage vs. Temperature

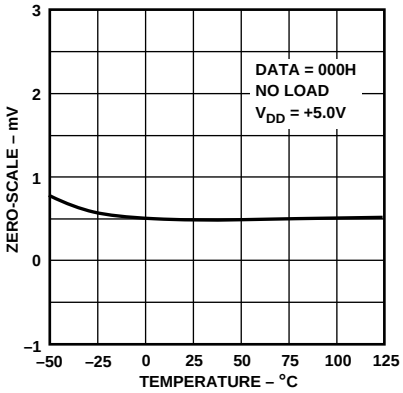


Figure 19. Zero-Scale Voltage vs. Temperature

DAC8562–Typical Performance Characteristics

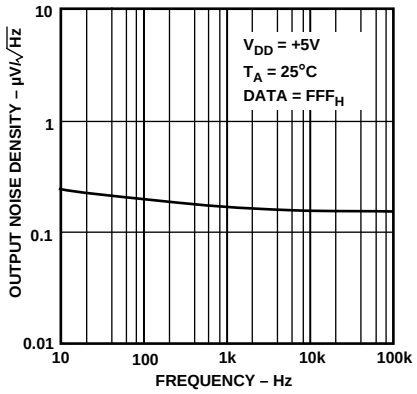


Figure 20. Output Voltage Noise Density vs. Frequency

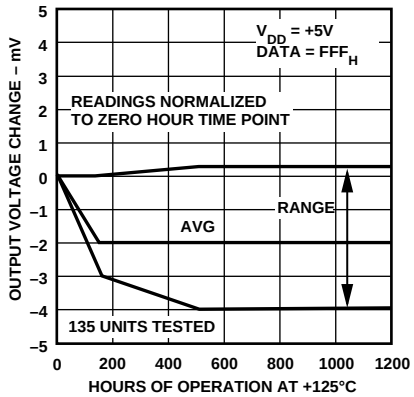


Figure 21. Long-Term Drift Accelerated by Burn-In

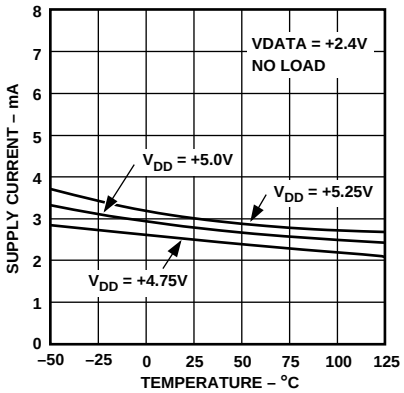


Figure 22. Supply Current vs. Temperature

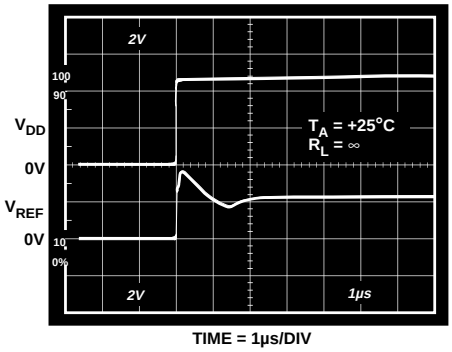


Figure 23. Reference Startup vs. Time

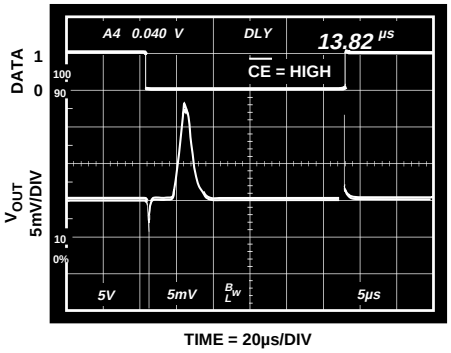


Figure 24. Digital Feedthrough vs. Time

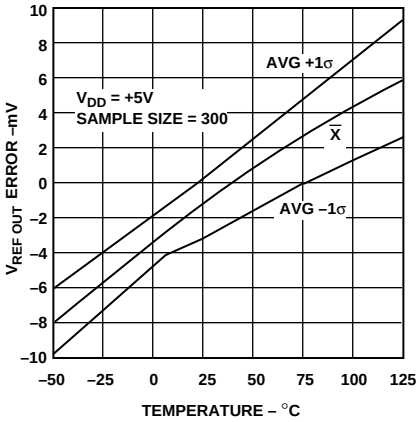


Figure 25. Reference Error vs. Temperature

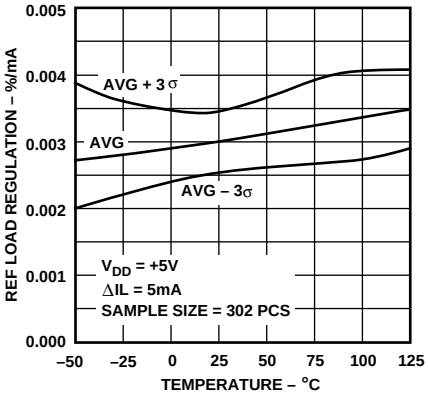


Figure 26. Reference Load Regulation vs. Temperature

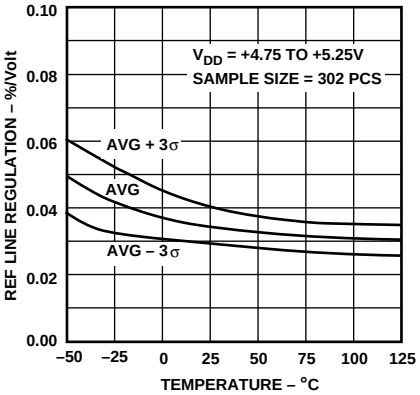


Figure 27. Reference Line Regulation vs. Temperature

APPLICATIONS SECTION

Power Supplies, Bypassing, and Grounding

All precision converter products require careful application of good grounding practices to maintain full-rated performance. Because the DAC8562 has been designed for +5 V applications, it is ideal for those applications under microprocessor or microcomputer control. In these applications, digital noise is prevalent; therefore, special care must be taken to assure that its inherent precision is maintained. This means that particularly good engineering judgment should be exercised when addressing the power supply, grounding, and bypassing issues using the DAC8562.

The power supply used for the DAC8562 should be well filtered and regulated. The device has been completely characterized for a +5 V supply with a tolerance of ±5%. Since a +5 V logic supply is almost universally available, it is not recommended to connect the DAC directly to an unfiltered logic supply without careful filtering. Because it is convenient, a designer might be inclined to tap a logic circuit s supply for the DAC's supply. Unfortunately, this is not wise because fast logic with nanosecond transition edges induces high current pulses. The high transient current pulses can generate glitches hundreds of millivolts in amplitude due to wiring resistances and inductances. This high frequency noise will corrupt the analog circuits internal to the DAC and cause errors. Even though their spike noise is lower in amplitude, directly tapping the output of a +5 V system supplies can cause errors because these supplies are of the switching regulator type that can and do generate a great deal of high frequency noise. Therefore, the DAC and any associated analog circuitry should be powered directly from the system power supply outputs using appropriate filtering. Figure 28 illustrates how a clean, analog-grade supply can be generated from a +5 V logic supply using a differential LC filter with separate power supply and return lines. With the values shown, this filter can easily handle 100 mA of load current without saturating the ferrite cores. Higher current capacity can be achieved with larger ferrite cores. For lowest noise, all electrolytic capacitors should be low ESR (Equivalent Series Resistance) type.

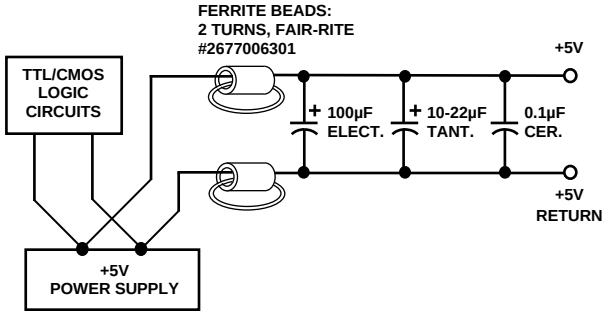


Figure 28. Properly Filtering a +5 V Logic Supply Can Yield a High Quality Analog Supply

The DAC8562 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (Pin 10) and AGND (Pin 12). The DGND pin is the return for the digital circuit sections of the DAC and serves as their input threshold reference point. Thus DGND should be connected to the same ground as the circuitry that drives the digital inputs.

Pin 12, AGND, serves as the supply rail for the internal voltage reference and the output amplifier. This pin should also serve as the reference point for all analog circuitry associated with the DAC8562. Therefore, to minimize any errors, it is recommended that the AGND connection of the DAC8562 be connected to a high quality analog ground. If the system contains any analog signal path carrying a significant amount of current, then that path should have its own return connection to Pin 12.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common to one place only. If the common tie point is remote and an accidental disconnection of that one common tie point were to occur due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the DAC8562, it is recommended that the common ground tie points be provided at each such device. If only one system ground can be connected directly to the DAC8562, it recommended that the analog common be used. If the system's AGND has suitably low impedance, then the digital signal currents flowing in it should not seriously affect the ground noise. The amount of digital noise introduced by connecting the two grounds together at the device will not adversely affect system performance due to loss of digital noise immunity.

Generous bypassing of the DAC's supply goes a long way in reducing supply line-induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic is recommended. The decoupling capacitors should be connected between the DAC's supply pin (Pin 20) and the analog ground (Pin 12). Figure 29 shows how the DGND, AGND, and bypass connections should be made to the DAC8562.

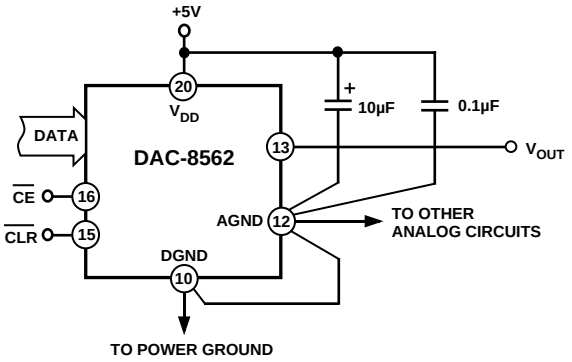


Figure 29. Recommended Grounding and Bypassing Scheme for the DAC-8562

Unipolar Output Operation

This is the basic mode of operation for the DAC8562. As shown in Figure 30, the DAC8562 has been designed to drive loads as low as 820 Ω in parallel with 500 pF. The code table for this operation is shown in Table III.

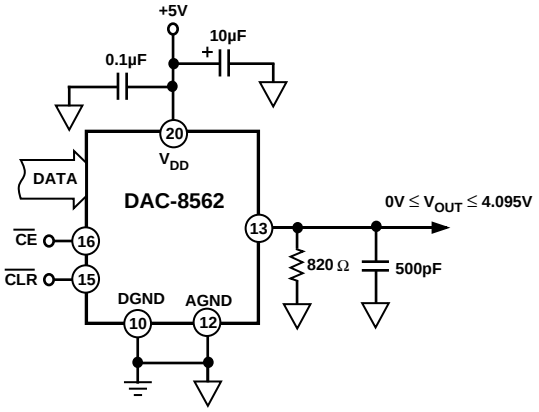


Figure 30. Unipolar Output Operation

Table III. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

Operating the DAC8562 on +12 V or +15 V Supplies Only

Although the DAC8562 has been specified to operate on a single, +5 V supply, a single +5 V supply may not be available in many applications. Since the DAC8562 consumes no more than 6 mA, maximum, then an integrated voltage reference, such as the REF02, can be used as the DAC8562 +5 V supply. The configuration of the circuit is shown in Figure 31. Notice that the reference's output voltage requires no trimming because of the REF02's excellent load regulation and tight initial output voltage tolerance. Although the maximum supply current of the DAC8562 is 6 mA, local bypassing of the REF02's output with at least 0. 1 µF at the DAC's voltage supply pin is recommended to prevent the DAC's internal digital circuits from affecting the DAC's internal voltage reference.

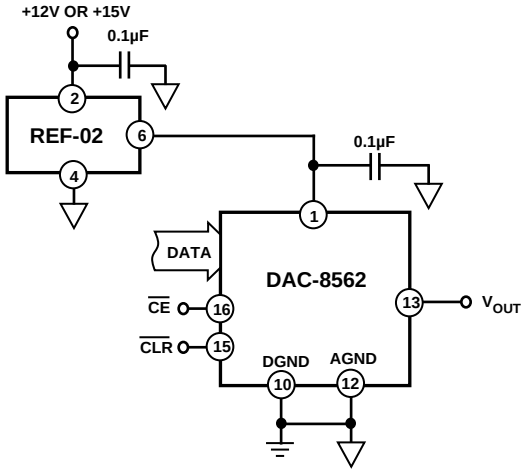


Figure 31. Operating the DAC8562 on +12 V or +15 V Supplies Using a REF02 Voltage Reference

Measuring Offset Error

One of the most commonly specified endpoint errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volt. There are some DACs where offset errors may be present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the DAC8562, for example, the zero-scale error is specified to be +3 LSBs. Since zero scale coincides with zero volt, it is not possible to measure negative offset error.

By adding a pull-down resistor from the output of the DAC8562 to a negative supply as shown in Figure 32, offset errors can now be read at zero code. This configuration forces the output P-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 µA maximum.

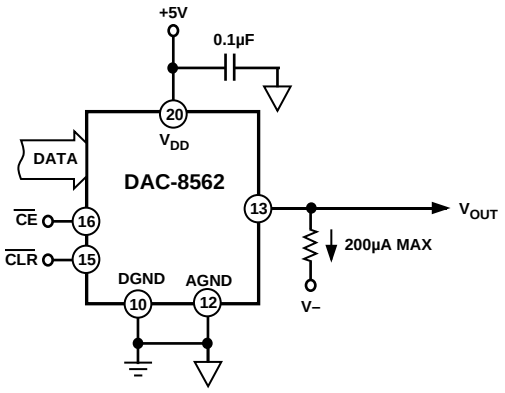


Figure 32. Measuring Zero-Scale or Offset Error

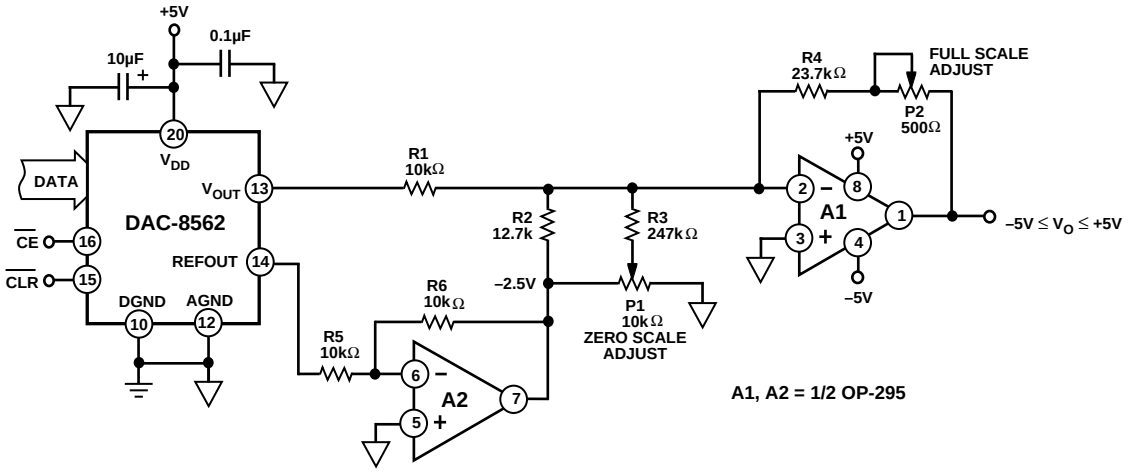


Figure 33. Bipolar Output Operation

Bipolar Output Operation

Although the DAC8562 has been designed for single supply operation, bipolar operation is achievable using the circuit illustrated in Figure 33. The circuit uses a single supply, rail-to-rail OP295 op amp and the DAC's internal +2.5 V reference to generate the –2.5 V reference required to level-shift the DAC output voltage. The circuit has been configured to provide an output voltage in the range $-5\ V \le V_{OUT} \le +5\ V$ and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table IV provides the relationship between the digital codes and output voltage.

The transfer function of the circuit is given by:

$$V_O = -1\,mV \times Digital\ Code \times \left(\frac{R4}{R1}\right) + 2.5 \times \left(\frac{R4}{R2}\right)$$

and, for the circuit values shown, becomes:

$$V_O = -2.44\ mV \times Digital\ Code + 5\ V$$

Table IV. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	–4 9976
801	2049	–2.44E–3
800	2048	0
7FF	2047	+2.44E–3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, R4, R5, and R6 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors while an R4 to R1 and R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 34 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim The output voltage is coded in offset binary and is given by:

$$V_O = 1\,mV \times Digital\ Code \times \left(\frac{R4}{R3+R4}\right) \times \left(1 + \frac{R2}{R1}\right)$$

$$-REFOUT \times \left(\frac{R2}{R1}\right)$$

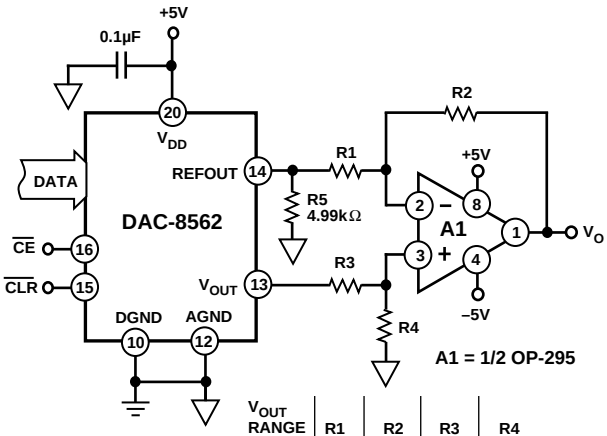
For the ±2 5 V output range and the circuit values shown in the table, the transfer equation becomes:

$$V_O = 1.22\ mV \times Digital\ Code - 2.5\ V$$

Similarly, for the ±5 V output range, the transfer equation becomes:

$$V_O = 2.44\ mV \times Digital\ Code - 5\ V$$

Note that, for ±5 V output voltage operation, R5 is required as a pull-down for REFOUT. Or, REFOUT can be buffered by an op amp configured as a follower that can source and sink current.



VOUT RANGE	R1	R2	R3	R4
±2.5V	10k	10k	10k	15.4k + 274
±5V	10k	20k	10k	43.2k + 499

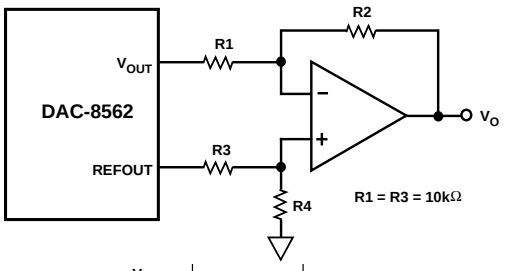
Figure 34. Bipolar Output Operation Without Trim Version 1

Alternatively, the output voltage can be coded in complementary offset binary using the circuit in Figure 35. This configuration eliminates the need for a pull-down resistor or an op amp for REFOUT The transfer equation of the circuit is given by:

$$V_O = -1\,mV \times Digital\ Code \times \left(\frac{R2}{R1}\right) + REFOUT \times \left(\frac{R4}{R3+R4}\right) \times \left(1+\frac{R2}{R1}\right)$$

and, for the values shown, becomes:

$$V_O = -2.44\,mV \times Digital\ Code + 5\,V$$



V_O RANGE	R2	R4
±5V	23.7k + 715	13.7k + 169Ω

Figure 35 Bipolar Output Operation Without Trim Version 2

Generating a Negative Supply Voltage

Some applications may require bipolar output configuration, but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, only +12 V, +15 V, and/or +5 V are available. Shown in Figure 36 is a method of generating a negative supply voltage using one CD4049, a CMOS hex inverter, operating on +12 V or +15 V. The circuit is essentially a charge pump where two of the six are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2. The remaining four inverters are wired in parallel for higher output current. The square-wave output is level translated by C2 to a negative-going signal, rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump will provide an output voltage of –5 V for current loading in the range 0.5 mA ≤ I_{OUT} ≤ 10 mA with a +15 V supply and 0.5 mA ≤ I_{OUT} ≤ 7 mA with a +12 V supply.

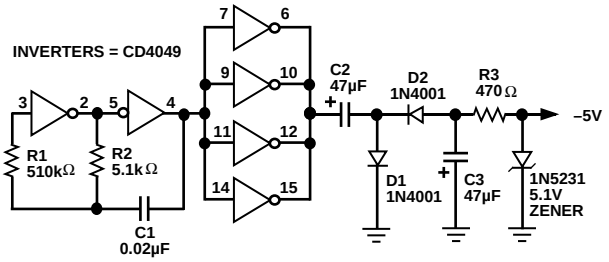


Figure 36. Generating a –5 V Supply When Only +12 V or +15 V Are Available

Audio Volume Control

The DAC8562 is well suited to control digitally the gain or attenuation of a voltage controlled amplifiers. In professional audio mixing consoles, music synthesizers, and other audio processors, VCAs, such as the SSM2018, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of the audio level when the slew rate of the analog input control voltage, V_C, is properly chosen. The circuit in Figure 37 illustrates a volume control application using the DAC8562 to control the attenuation of the SSM2018.

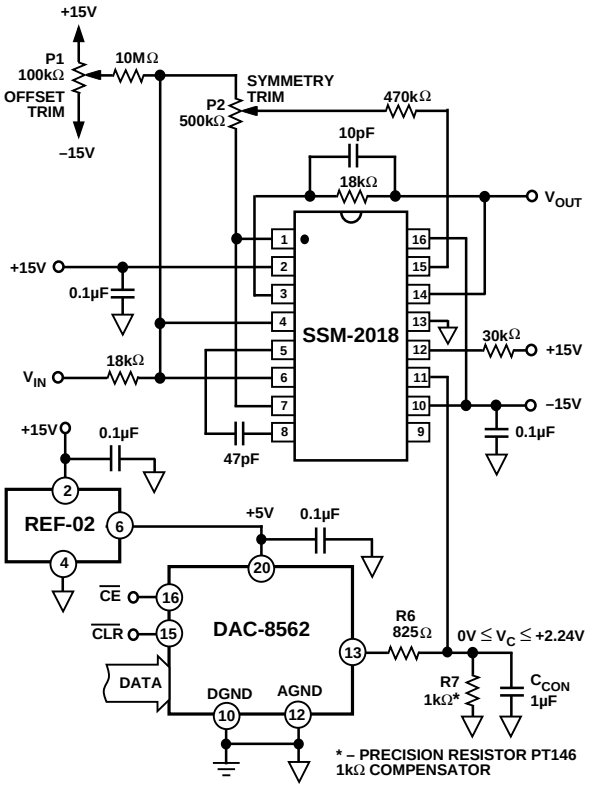


Figure 37. Audio Volume Control

Since the supply voltage available in these systems is typically ±15 V or ±18 V, a REF02 is used to supply the +5 V required to power the DAC. No trimming of the reference is required because of the reference's tight initial tolerance and low supply current consumption of the DAC8562. The SSM2018 is configured as a unity-gain buffer when its control voltage equals 0 volt. This corresponds to a 000_H code from the DAC8562. Since the SSM2018 exhibits a gain constant of –28 mV/dB (typical), the DAC's full-scale output voltage has to be scaled down by R6 and R7 to provide 80 dB of attenuation when the digital code equals FFF_H. Therefore, every DAC LSB corresponds to 0.02 dB of attenuation. Table V illustrates the attenuation versus digital code of the volume control circuit.

Table V. SSM2018 VCA Attenuation vs. DAC8562 Input Code

Hexadecimal Number in DAC Register	Control Voltage (V)	VCA Attenuation (dB)
000	0	0
400	+0.56	20
800	+1.12	40
C00	+1.68	60
FFF	+2.24	80

To compensate for the SSM2018's gain constant temperature coefficient of –3300 ppm/°C, a 1 kΩ, temperature-sensitive resistor (R7) manufactured by the Precision Resistor Company with a temperature coefficient of +3500 ppm/°C is used. A C_{CON} of 1 µF provides a control transition time of 1 ms which yields a click-free change in the audio channel attenuation. Symmetry and offset trimming details of the VCA can be found in the SSM2018 data sheet.

Information regarding the PT146 1 kΩ "Compensator" can be obtained by contacting:

Precision Resistor Company, Incorporated
10601 75th Street North
Largo, FL 34647
(813) 541-5771

A High-Compliance, Digitally Controlled Precision Current Source

The circuit in Figure 38 shows the DAC8562 controlling a high-compliance, precision current source using an AMP05 instrumentation amplifier. The AMP05's reference pin becomes the input, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS}. Voltage gain is set to unity, so the transfer function is given by the following equation:

$$I_{OUT} = \frac{V_{IN}}{R_{CS}}$$

If R_{CS} equals 100 Ω, the output current is limited to +10 mA with a 1 V input. Therefore, each DAC LSB corresponds to 2.4 µA. If a bipolar output current is required, then the circuit in Figure 33 can be modified to drive the AMP05's reference pin with a ±1 V input signal.

Potentiometer P1 trims the output current to zero with the input at 0 V. Fine gain adjustment can be accomplished by adjusting R1 or R2.

A Digitally Programmable Window Detector

A digitally programmable, upper/lower limit detector using two DAC8562s is shown in Figure 39. The required upper and lower limits for the test are loaded into each DAC individually by controlling HDAC/$\overline{\text{LDAC}}$. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero which will turn the red LED on.

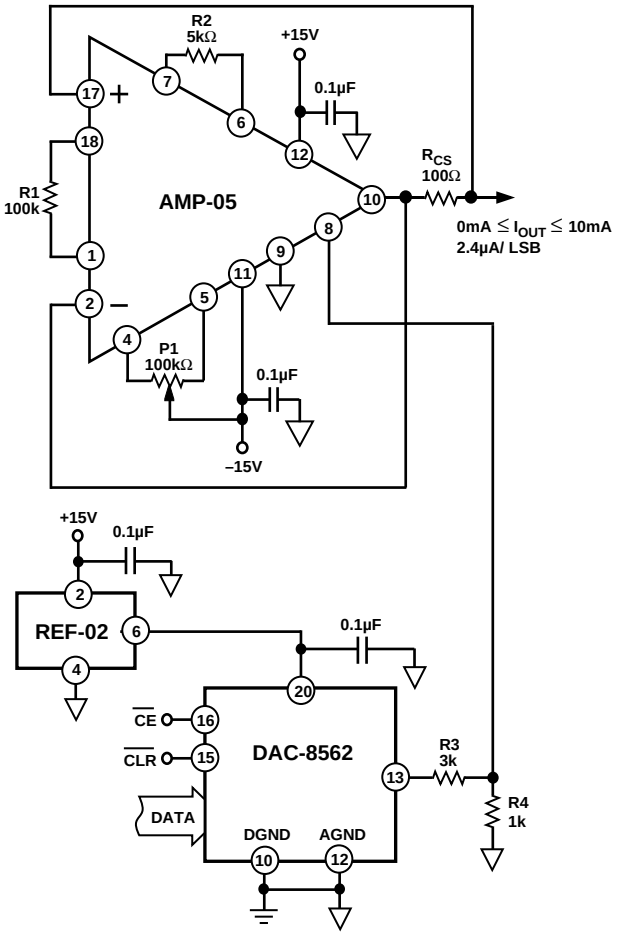


Figure 38. A High-Compliance, Digitally Controlled Precision Current Source

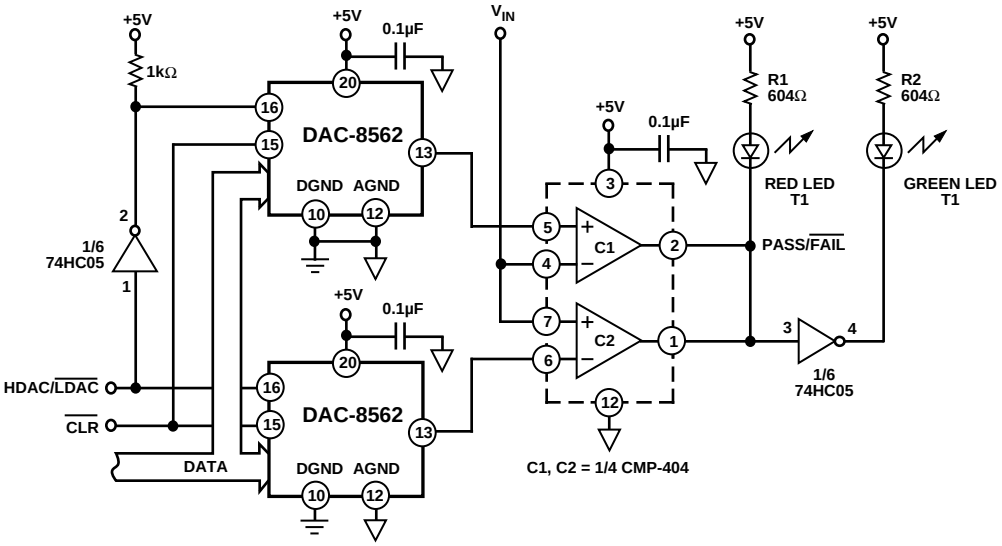


Figure 39. A Digitally Programmable Window Detector

Decoding Multiple DAC8562s

The $\overline{CE}$ function of the DAC8562 can be used in applications to decode a number of DACs. In this application, all DACs receive the same input data; however, only one of the DACs' $\overline{CE}$ input is asserted to transfer its parallel input register contents into the DAC. In this circuit, shown in Figure 40, the $\overline{CE}$ timing is generated by a 74HC139 decoder and should follow the DAC8562's standard timing requirements. To prevent timing errors, the 74HC139 should not be activated by its $\overline{ENABLE}$ input while the coded address inputs are changing. A simple timing circuit, R1 and C1, connected to the DACs' $\overline{CLR}$ pins resets all DAC outputs to zero during power-up.

MICROPROCESSOR INTERFACING

DAC-8562–MC68HC11 INTERFACE

The circuit illustrated in Figure 41 shows a parallel interface between the DAC8562 and a popular 8-bit microcontroller, the M68HC11, which is configured in a single-chip operating mode. The interface circuit consists of a pair of 74ACT11373 transparent latches and an inverter. The data is loaded into the latches in two 8-bit bytes; the first byte contains the four most significant bits, and the lower 8 bits are in the second byte. Data is taken from the microcontroller's port B output lines, and three interface control lines, $\overline{CLR}$, $\overline{CE}$, and MSB/$\overline{LSB}$, are controlled by the M68HC11's PC2, PC1, and PC0 output lines, respectively. To transfer data into the DAC, PC0 is set, enabling U1's outputs. The first data byte is loaded into U1 where the four least significant bits of the byte are connected to MSB–DB8. PC0 is then cleared; this latches U1's inputs and enables U2's outputs. U2s outputs now become DB7–DB0. The DAC output is updated with the contents of U1 and U2 when PC1 is cleared. The DAC's $\overline{CLR}$ input, controlled by the M68HC11's PC2 output line, provides an asynchronous clear function that sets the DAC's output to zero. Included in this section is the source code for operating the DAC-8562–M68HC11 interface.

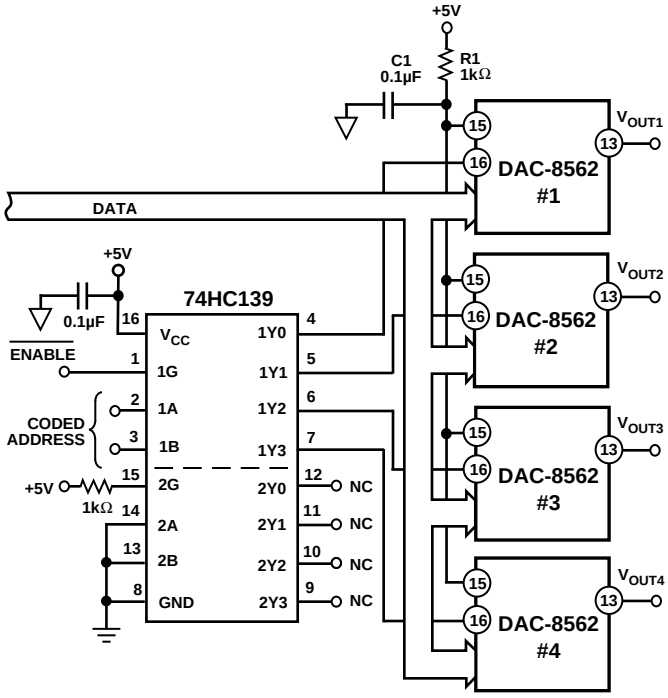


Figure 40. Decoding Multiple DAC8562s Using the $\overline{CE}$ Pin

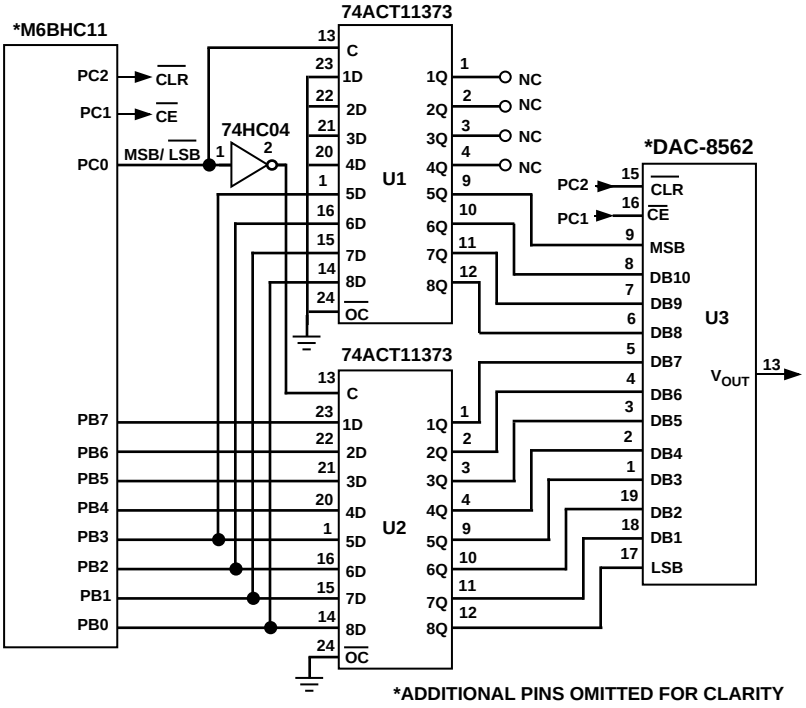


Figure 41. DAC8562 to MC68HC11 Interface

DAC8562 – M68HC11 Interface Program Source Code

```
*
* DAC8562 to M68HC11 Interface Assembly Program
* Adolfo A. Garcia
* September 14, 1992
*
* M68HC11 Register definitions
*
PORTB   EQU   $1004
PORTC   EQU   $1003          Port C control register
*                            "0,0,0,0;0,CLR/,CE/,MSB-LSB/"
DDRC    EQU   $1007          Port C data direction
*
* RAM variables:             MSBS are encoded from 0 (Hex) to F (Hex)
*                            LSBS are encoded from 00 (Hex) to F (Hex)
*                            DAC requires two 8-bit loads
*
MSBS    EQU   $00            Hi-byte: "0,0,0,0;MSB,DB10,DB9,DB8"
LSBS    EQU   $01            Lo-byte: "DB7,DB6,DB5,DB4;DB3,DB2,
                             DB1,DB0"
*
* Main Program
*
        ORG   $C000          Start of user's RAM in EVB
INIT    LDS   #$CFFF         Top of C page RAM
*
* Initialize Port C Outputs
*
        LDAA  #$07           0,0,0,0;0,1,1,1
        STAA  DDRC           CLR/,CE/, and MSB-LSB/ are now enabled
                             as outputs
        LDAA  #$06           0,0.0,0;0,1,1,0
*                            CLR/-Hi, CE/-Hi, MSB-LSB/-Lo
        STAA  PORTC          Initialize Port C Outputs
*
* Call update subroutine
*
        BSR   UPDATE         Xfer 2 8-bit words to DAC8562
        JMP   $E000          Restart BUFFALO
*
* Subroutine UPDATE
*
UPDATE  PSHX                 Save registers X, Y, and A
        PSHY
        PSHA
*
* Enter contents of the Hi-byte input register
*
        LDAA  #$0A           0,0,0,0;1,0,1,0
        STAA  MSBS           MSBS are set to 0A (Hex)
*
* Enter Contents of' Lo-byte input register
*
        LDAA  #$AA           1,0,1,0;1,0,1,0
        STAA  LSBS           LSBS are set to AA (Hex)
*
        LDX   #MSBS          Stack pointer at 1st byte to send via Port B
        LDY   #$1000         Stack pointer at on-chip registers
*
* Clear DAC output to zero
*
        BCLR  PORTC,Y $04    Assert CLR/
        BSET  PORTC,Y $04    De-assert CLR/
*
* Loading input buffer latches
*
        BSET  PORTC,Y $01    Set hi-byte register load
TFRLP   LDAA  0,X            Get a byte to transfer via Port B
        STAA  PORTB          Write data to input register
        INX                  Increment counter to next byte for transfer
        CPX   #LSBS+1        Are we done yet ?
        BEQ   DUMP           If yes, update DAC output
        BCLR  PORTC,Y $01    Latch hi-byte register and set lo-byte register
                             load
        BRA   TFRLP
*
```

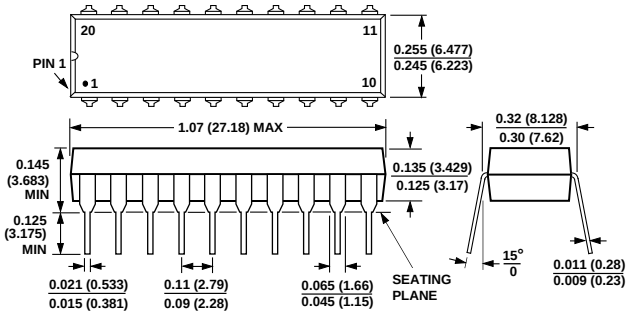
DAC8562–M68HC11 Interface Program Source Code (Continued)

```
* Update DAC output with contents of input registers
*
DUMP    BCLR  PORTC,Y $02    Assert CE/
        BSET  PORTC,Y $02    Latch DAC register
*
        PULA                 When done, restore registers X, Y & A
        PULY
        PULX
        RTS                  ** Return to Main Program **
```

OUTLINE DIMENSIONS

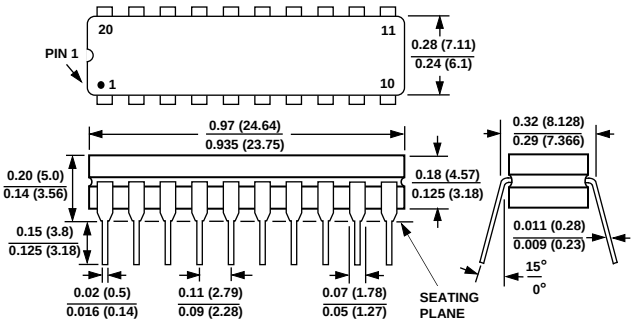
Dimensions shown in inches and (mm).

20-Pin Plastic DIP (P-Suffix)



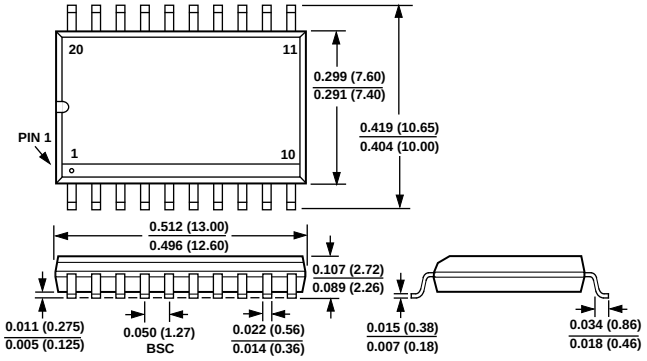
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42.

20-Pin Cerdip (R-Suffix)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42.

20-Lead SOIC (S-Suffix)



C1713–24–10/92

PRINTED IN U.S.A.

TEMIC

Siliconix

SD211DE/SST211 Series

N-Channel Lateral DMOS FETs

SD211DE SST211
SD213DE SST213
SD215DE SST215

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ V_{GS} = 10 V	0.5	2
SD213DE	10	1.5	45 @ V_{GS} = 10 V	0.5	2
SD215DE	20	1.5	45 @ V_{GS} = 10 V	0.5	2
SST211	30	1.5	50 @ V_{GS} = 10 V	0.5	2
SST213	10	1.5	50 @ V_{GS} = 10 V	0.5	2
SST215	20	1.5	50 @ V_{GS} = 10 V	0.5	2

For applications information see AN301, page 33.

Features

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

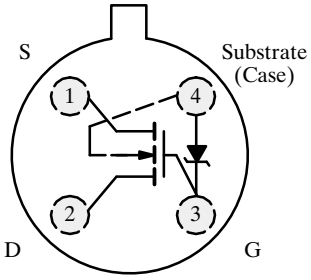
- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD211 may be used for ±5-V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated Zener diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series and non-Zener protection—SD210DE/214DE.

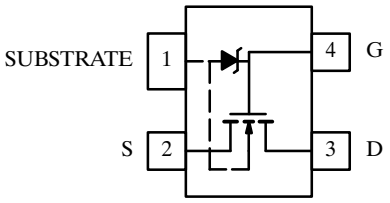
TO-206AF
(TO-72)



Top View

SD211DE, SD213DE, SD215DE

TO-253
(SOT-143)



Top View

SST211 (D1)*, SST213 (D3)*, SST215 (D5)*

*Marking Code for TO-253

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage	(SD211DE/SST211)	−30/25 V
	(SD213DE/SST213)	−15/25 V
	(SD215DE/SST215)	−25/30 V
Gate-Substrate Voltage[a]	(SD211DE/SST211)	−0.3/25 V
	(SD213DE/SST213)	−0.3/25 V
	(SD215DE/SST215)	−0.3/30 V
Drain-Source Voltage	(SD211DE/SST211)	30 V
	(SD213DE/SST213)	10 V
	(SD215DE/SST215)	20 V
Source-Drain Voltage	(SD211DE/SST211)	10 V
	(SD213DE/SST213)	10 V
	(SD215DE/SST215)	20 V
Drain-Substrate Voltage	(SD211DE/SST211)	30 V
	(SD213DE/SST213)	15 V
	(SD215DE/SST215)	25 V
Source-Substrate Voltage	(SD211DE/SST211)	15 V
	(SD213DE/SST213)	15 V
	(SD215DE/SST215)	25 V
Drain Current		50 mA
Lead Temperature ($^1/_{16}$" from case for 10 seconds)		300°C
Storage Temperature		−65 to 150°C
Operating Junction Temperature		−55 to 125°C
Power Dissipation[a]		300 mW

Notes:
a. Derate 3 mW/°C above 25°C

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211 Series Min	Limits 211 Series Max	Limits 213 Series Min	Limits 213 Series Max	Limits 215 Series Min	Limits 215 Series Max	Unit
Static											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source Open		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain Open		35	15		15		25		
Drain-Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$V		0.01		100		100		100	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V (SD Series)	58		70		70		70	Ω
			$V_{GS} = 5$ V (SST Series)	60		75		75		75	
			$V_{GS} = 10$ V (SD Series)	38		45		45		45	
			$V_{GS} = 10$ V (SST Series)	40		50		50		50	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							

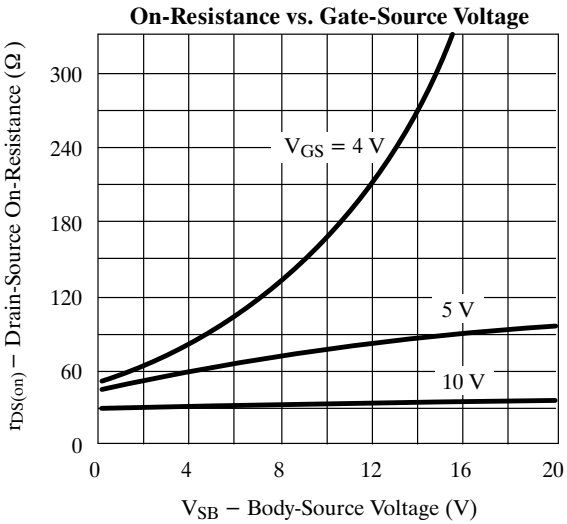
Specifications[a]

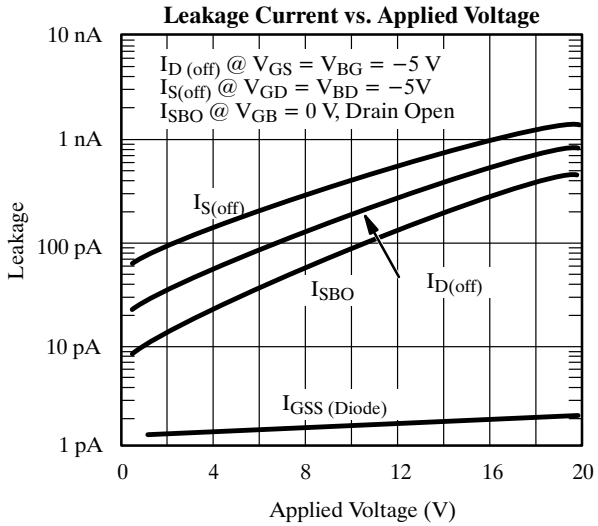
Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211 Series Min	Limits 211 Series Max	Limits 213 Series Min	Limits 213 Series Max	Limits 215 Series Min	Limits 215 Series Max	Unit
Dynamic											
Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{SB} = 0 V, I_D = 20 mA, f = 1 kHz	SD Series	11	10		10		10		mS
			SST Series	10.5	9		9		9		
	g_{os}		A11	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10 V, f = 1 MHz, V_{GS} = V_{BS} = −15 V	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
			SST Series	4.2							
Reverse Transfer Capacitance	C_{rss}		SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{d(on)}$	SD Series Only, V_{SB} = 0 V, V_{IN} 0 to 5 V, R_G = 25 Ω, V_{DD} = 5 V, R_L = 680 Ω		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{d(off)}$			2							
	t_f			6							

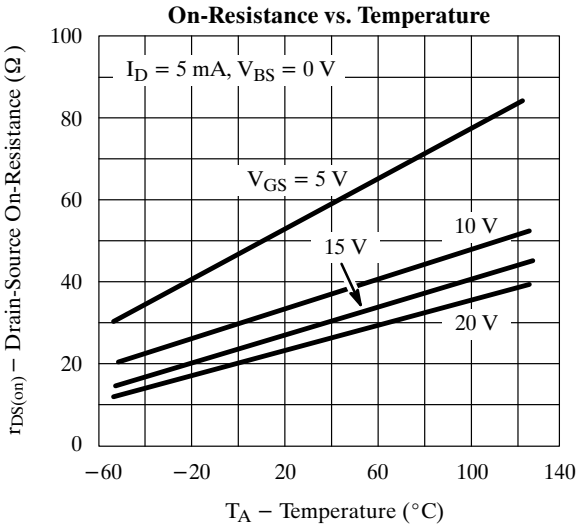
Notes:
a. T_A = 25°C unless otherwise noted.
b. B is the body (substrate), and (BR) is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

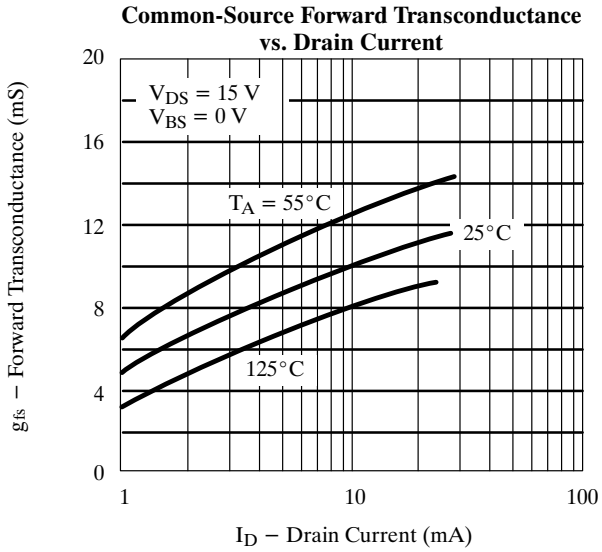
DMCBA

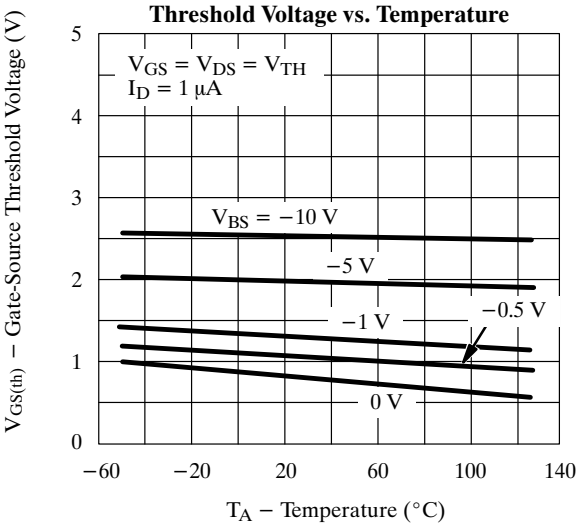
Typical Characteristics

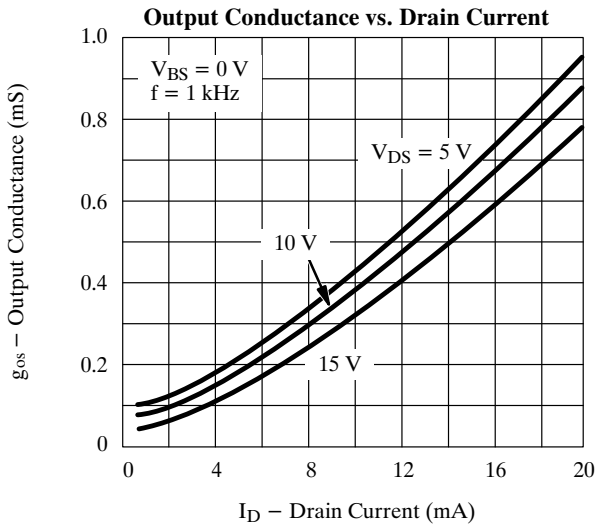




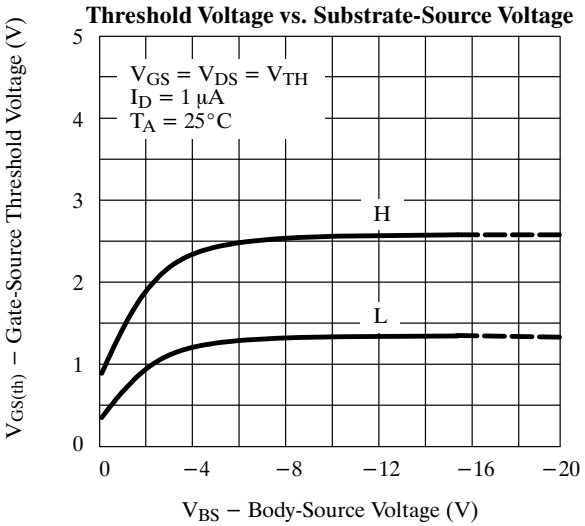


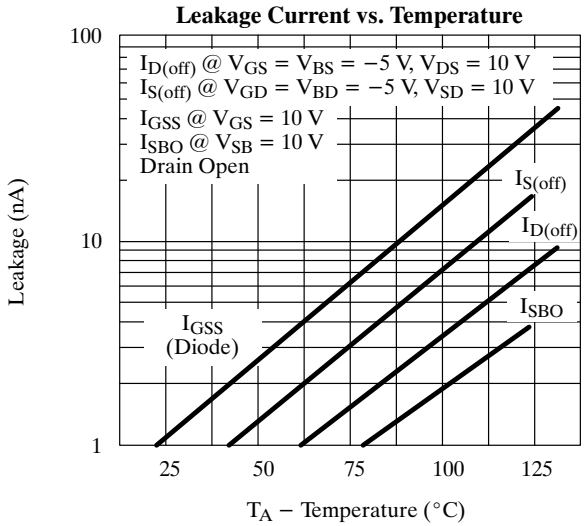


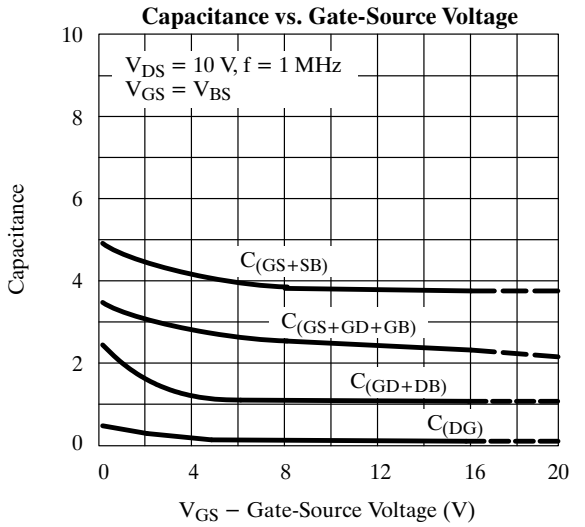


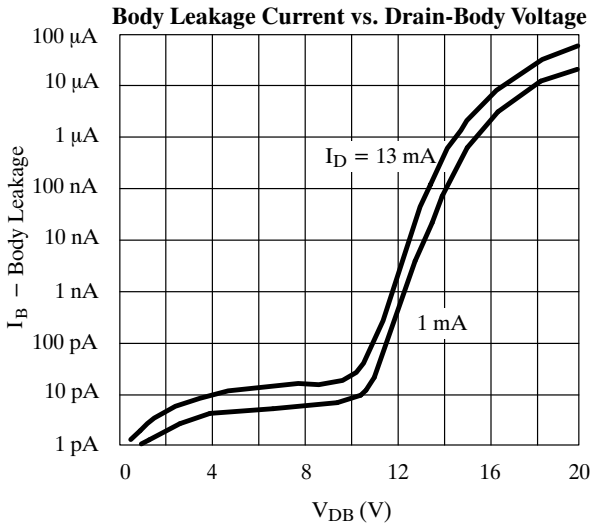


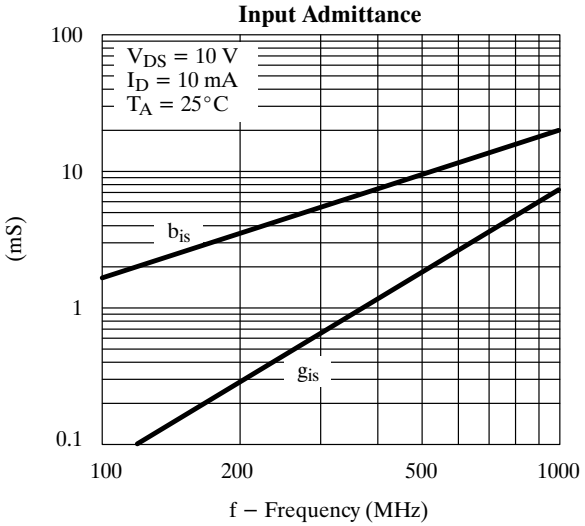
Typical Characteristics (Cont'd)

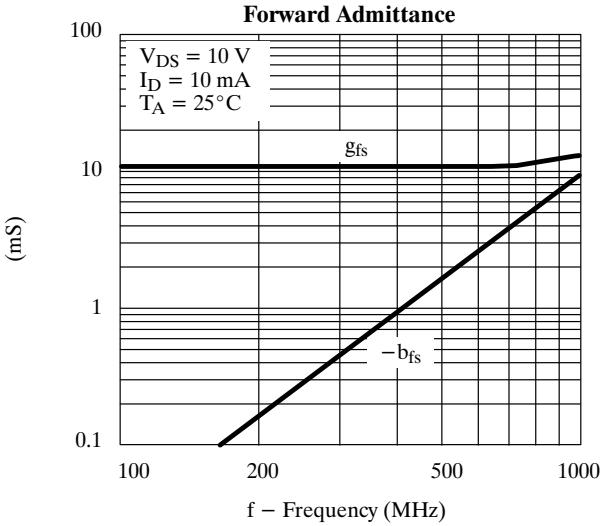




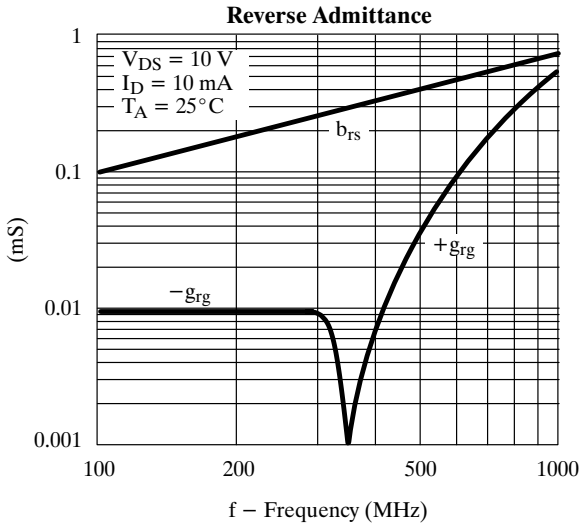


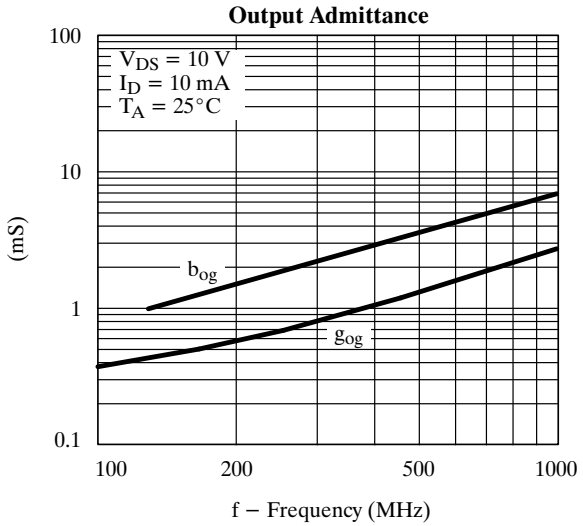


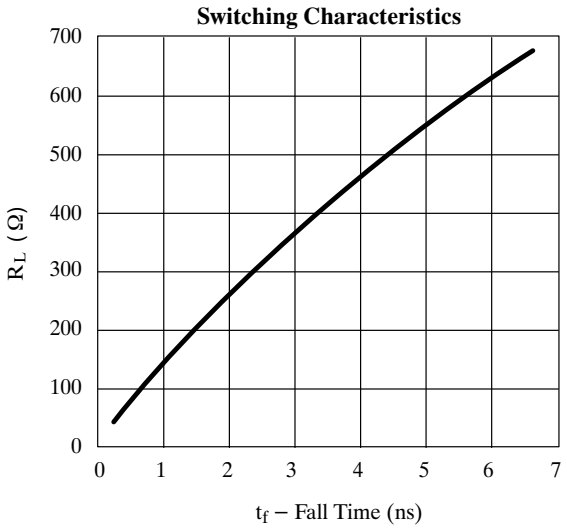


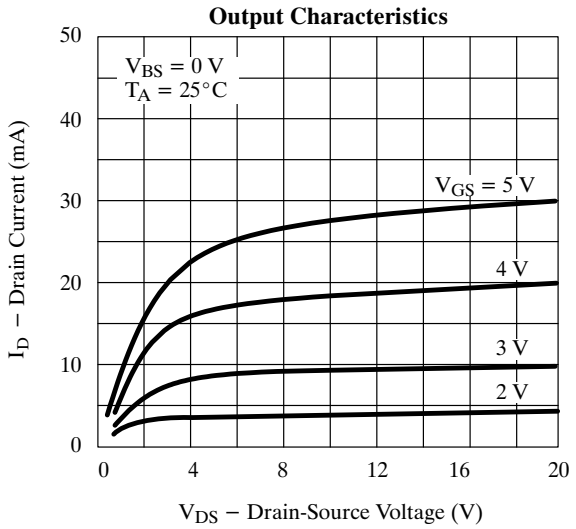


Typical Characteristics

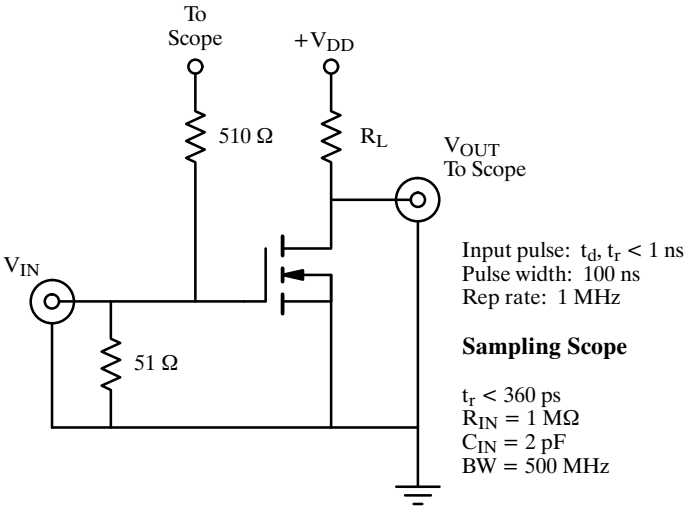


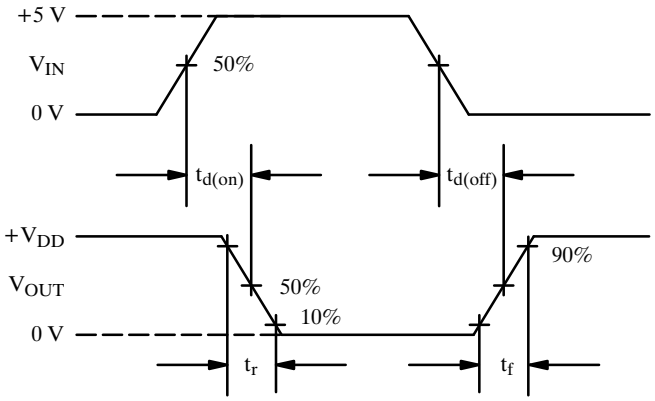






Switching Time Test Circuit





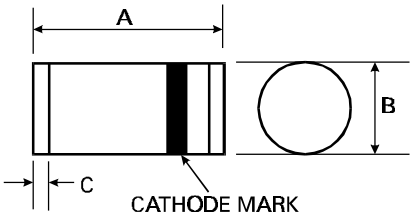
DL4001 - DL4007

1.0 AMPERE GLASS PASSIVATED SURFACE MOUNT RECTIFIER

Features

- Glass passivated junction
- Plastic material has Underwriters Lab flammability Classfication 94V-0
- High current capability
- Low forward voltage drop
- High reliability and low leakage
- For surface mounted application

MELF



	Min	Max
A	4.8	5.2
B	2.4	2.5
C	0.55∅ Nominal	
All dimensions in mm		

Mechanical Data

- TERMINALS: Solderable per MIL-STD-202, Method 208
- CASE: MELF, Molded Plastic
- MOUNTING POSITION: Any
- POLARITY: Cathode band

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60Hz, resistive or inductive load.

Characteristic	Symbol	DL4001	DL4002	DL4003	DL4004	DL4005	DL4006	DL4007	Unit
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	V_{RSM}	35	70	140	280	420	560	700	V
Maximum DC Blocking Voltage	V_{DC}	50	100	200	400	600	800	1000	V
Maximum Average Forward Rectified Current @ Terminal Temp (T_T) = 75°C	$I_{(AV)}$	1.0							A
Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	30							A
Maximum Forward Voltage at 1.0A	V_F	1.1							V
Maximum dc Reverse Current at Rated dc Blocking Voltage T_A = 25°C T_A = 100°C	I_R	5.0 50							μA μA
Typical Thermal Resistance (Note 1)	$R_{\theta JA}$	50							°C/W
Typical Junction Capacitance (Note 2)	C_J	15							pF
Storage and Operating Temperature Range	T_J, T_{STG}	-65 to +175							°C

NOTE: 1. Thermal resistance from junction to ambient.
2. Measured at 1MHz and applied reverse voltage of 4.0 volts.

To order/reorder this document please request Data Sheet DL4001 Rev. B 5/8/96 or Data Sheet DL4001 (Current Revision).

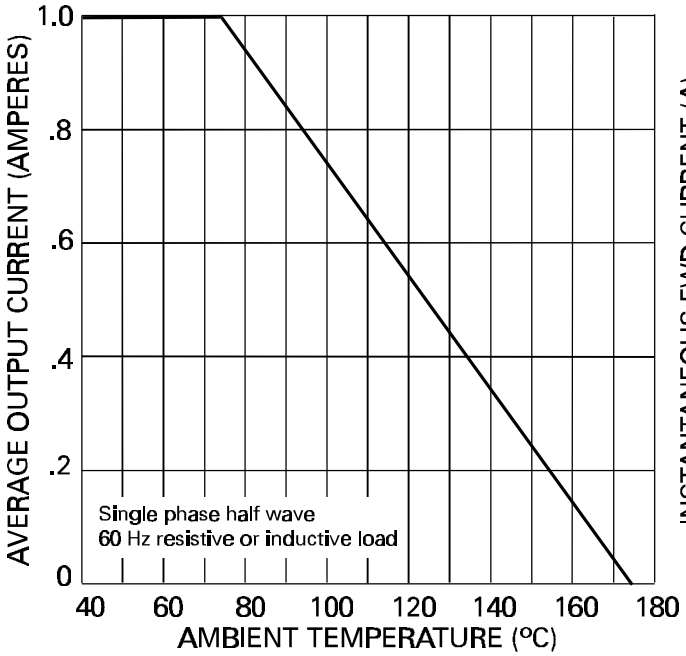


Fig. 1 Forward Current Derating Curve

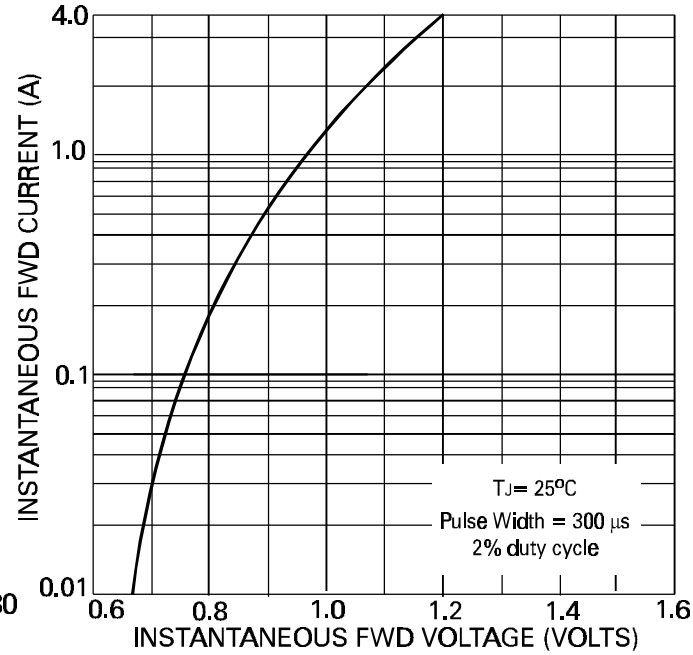


Fig. 2 Typical Forward Characteristics

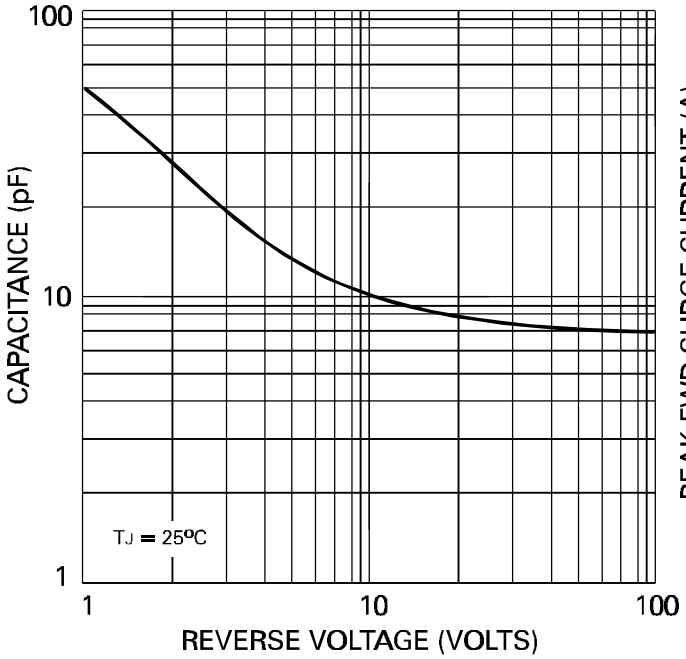


Fig. 3 Typical Junction Capacitance

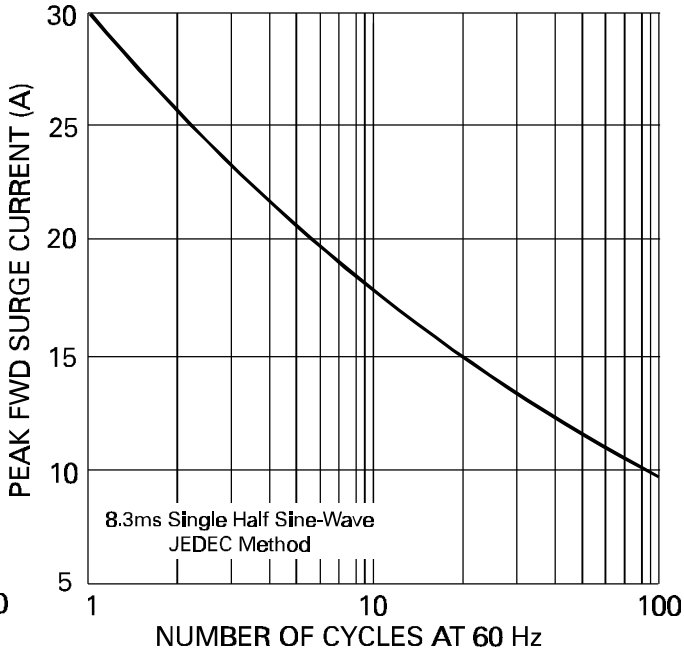


Fig. 4 Max Non-Repetitive Peak Fwd Surge Current

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PRELIMINARY

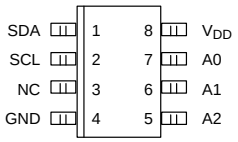
DALLAS SEMICONDUCTOR

DS1624
Digital Thermometer and Memory

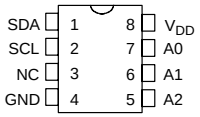
FEATURES

- Temperature measurements require no external components
- Measures temperatures from –55°C to +125°C in 0.03125°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.05625°F increments
- Temperature is read as a 13–bit value (two byte transfer)
- Converts temperature to digital word in 200 ms, typical
- 256 bytes of E^2 memory on board for storing information such as frequency compensation coefficients
- Data is read/written via a 2–wire serial interface (open drain I/O lines)
- Applications include temperature–compensated crystal oscillators for test equipment and radio systems
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1624S
8–PIN SOIC (208 MIL)
See Mech. Drawings Section



DS1624
8–PIN DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

SDA	–	2–Wire Serial Data Input/Output
SCL	–	2–Wire Serial Clock
GND	–	Ground
A0	–	Chip Address Input
A1	–	Chip Address Input
A2	–	Chip Address Input
V_{DD}	–	Digital Power Supply (+3V– +5V)
NC	–	No Connection

DESCRIPTION

The DS1624 consists of a digital thermometer and 256 bytes of E^2 memory. The thermometer provides 13–bit temperature readings which indicate the temperature of the device. The E^2 memory allows a user to store frequency compensation coefficients for digital correction of crystal frequency due to temperature. Any other type of information may also reside in this user space.

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DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	SDA	**Data input/output pin** for 2–wire serial communication port.
2	SCL	**Clock input/output pin** for 2–wire serial communication port.
3	NC	**No Connect**. No Internal Connection.
4	GND	**Ground pin.**
5	A2	**Address input pin.**
6	A1	**Address input pin.**
7	A0	**Address input pin.**
8	V_{DD}	**Supply Voltage** 3V to 5V input power pin.

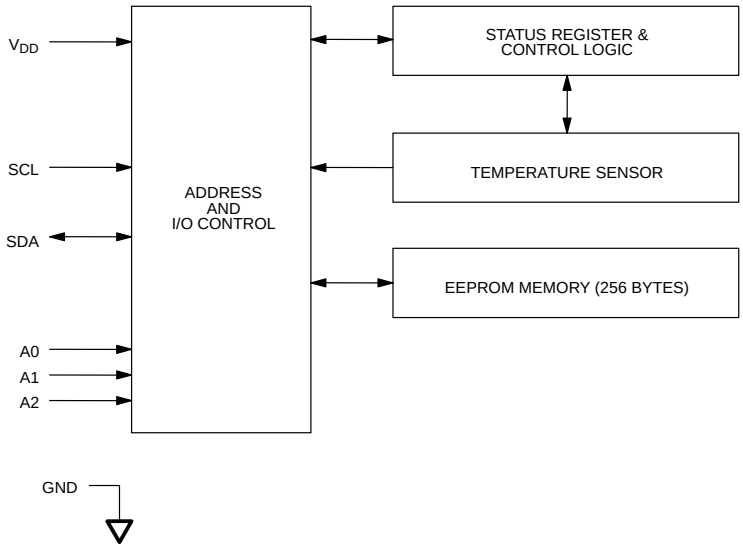
OVERVIEW

A block diagram of the DS1624 is shown in Figure 1. The DS1624 consists of two separate functional units: 1) a 256–byte nonvolatile E^2 memory, and 2) a direct–to–digital temperature sensor.

The nonvolatile memory is made up of 256 bytes of E^2 memory. This memory may be used to store any type of information the user wishes; for example, frequency compensation coefficients may be placed in this memory to allow for compensation of measured frequency depending upon the temperature at which the measurement is made. These memory locations are accessed through the 2–wire serial bus.

The direct to digital temperature sensor allows the DS1624 to measure the ambient temperature and report the temperature value in a 13–bit word, with 0.03125°C resolution. The temperature sensor and its related registers are accessed through the 2–wire serial interface.

DS1624 FUNCTIONAL BLOCK DIAGRAM Figure 1



2–WIRE SERIAL DATA BUS

The DS1624 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master”. The devices that are controlled by the master are “slaves”. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START an d STOP conditions. The DS1624 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL. The following bus protocol has been defined (See Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 KHz clock rate) and a fast mode (400 KHz clock rate) are defined. The DS1624 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 2

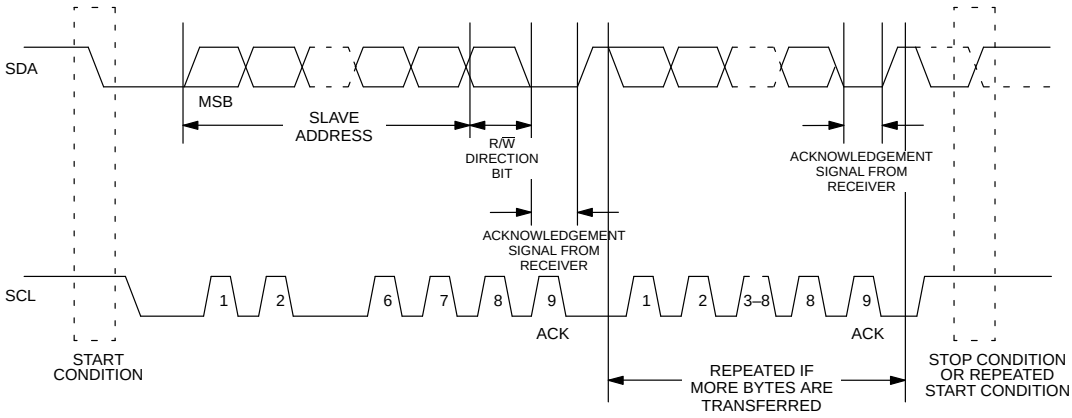


Figure 2 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1624 may operate in the following two modes:

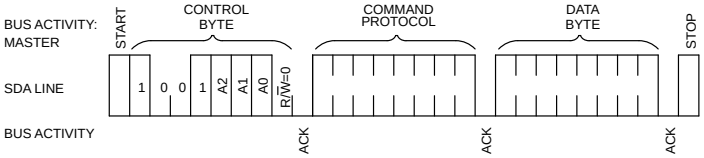
1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1624 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

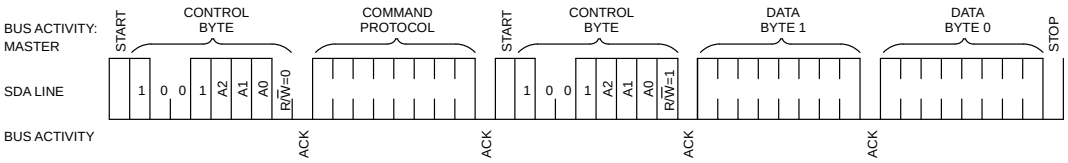
A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1624, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. These bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1624 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2–WIRE SERIAL COMMUNICATION WITH DS1624 Figure 3

Write to DS1624



Read from DS1624



OPERATION–MEASURING TEMPERATURE

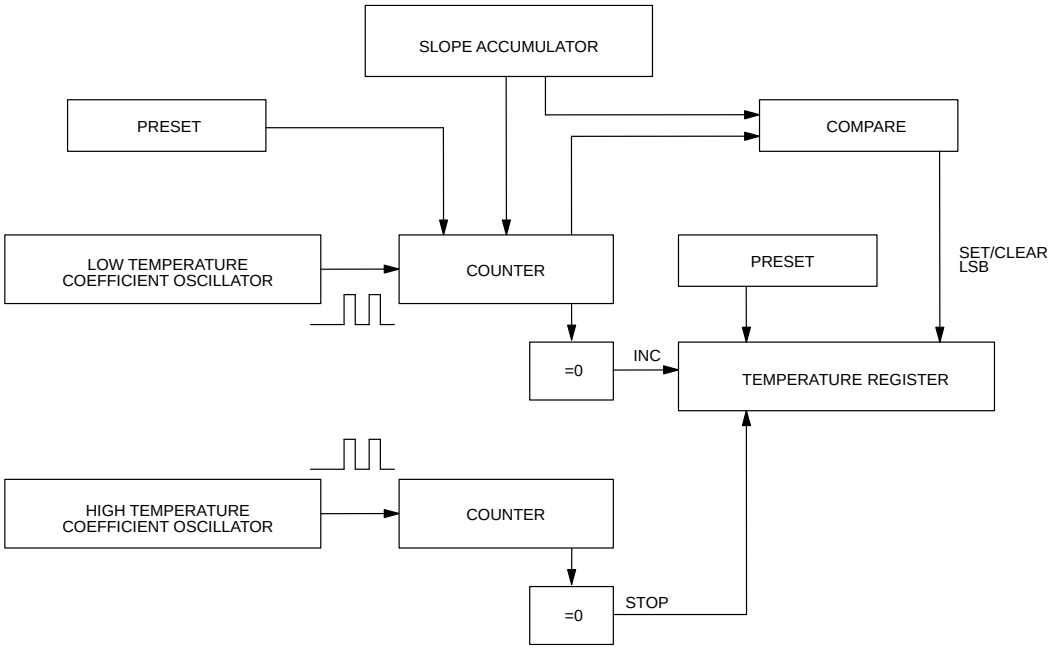
A block diagram of the DS1624 is shown in Figure 1.The DS1624 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 4.

The DS1624 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator is used to compensate for the nonlinear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

TEMPERATURE MEASURING CIRCUITRY Figure 4



Internally, this calculation is performed by the DS1624 to provide 0.03125°C resolution. The temperature reading is provided in a 13–bit, two's complement reading by issuing READ TEMPERATURE command. Table 2 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 2–wire serial interface, MSB first. The DS1624 can measure temperature over the range of –55°C to +125°C in 0.03125°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

TEMPERATURE/DATA RELATIONSHIPS

Table 2

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7D00h
+25.0625°C	00011001 00010000	1910h
+$^1/_2$°C	00000000 10000000	0080h
+0°C	00000000 00000000	0070h
–$^1/_2$°C	11111111 10000000	FF80h
–25.0625°C	11100110 11110000	E6F0h
–55°C	11001001 00000000	C900h

Since data is transmitted over the 2–wire bus MSB first, temperature data may be written to/read from the DS1624 as either a single byte (with temperature resolution of 1°C), or as two bytes, the second byte containing the value of the 5 least significant bits of the temperature reading, as shown in Table 1. Note that the remaining three bits of this byte are set to all 0's.

Note that temperature is represented in the DS1624 in terms of a 0.03125°C LSB, yielding the following 13–bit format:

MSB								LSB							
0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0

= –25.0625°C

OPERATION AND CONTROL

A configuration/status register is used to determine the method of operation that the DS1624 will use in a particular application, as well as indicating the status of the temperature conversion operation.

The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	1	0	0	1	0	1	1SHOT

where

DONE= Conversion Done bit. "1" = Conversion complete, "0" = conversion in progress.

1SHOT= One Shot Mode. If 1SHOT is "1", the DS1624 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is "0", the DS1624 will continuously perform temperature conversions. This bit is nonvolatile.

Since the configuration register is implemented in E^2, writes to the register require 10 ms to complete. After issuing a command to write to the configuration register, no further accesses to the DS1624 should be made for at least 10 ms.

OPERATION – MEMORY

BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the DS1624.

Following a START condition, the device code (4–bit), the slave address (3 bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. The master then sends the Access Memory protocol. This indicates to the addressed DS1624 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the DS1624. After receiving the acknowledge of the DS1624, the master device transmits the data word to be written into the addressed memory location. The DS1624 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the DS1624. A repeated START condition, instead of a STOP condition, will abort the programming operation.

During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms.)

PAGE PROGRAM MODE

To program the DS1624, the master sends addresses and data to the DS1624 which is the slave. This is done by supplying a START condition followed by the 4–bit device code, the 3–bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. The master then sends the Access Memory protocol. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the DS1624, it is placed in the address pointer defining which memory location is to be written. The DS1624 will generate an acknowledge after every 8–bits received and store them consecutively in an 8–byte RAM until a STOP condition is detected which initiates the internal programming cycle.

A repeated START condition, instead of a STOP condition, will abort the programming operation.During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms).

If more than eight bytes are transmitted by the master, the DS1624 will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address register's bottom three bits to increment while the upper five bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word, byte programming mode is entered.

READ MODE

In this mode, the master is reading data from the DS1624 E^2 memory. The master first provides the slave address to the device, with R/$\overline{W}$ set to 0. The master then sends the Access Memory protocol, and, after receiving an acknowledge, then provides the word address, which is the address of the memory location at which it wishes to begin reading. Note that while this is a read operation, the address pointer must first be written. During this period the DS1624 generates acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the R/$\overline{W}$ bit is set to 1, to put the DS1624 in read mode. After the DS1624 generates the acknowledge bit, it then outputs the data from the addressed location on the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge. When the address pointer reaches the end of the 256–byte memory space (address FFh), it will increment from the end of the memory back to the first location of the memory (address 00h).

COMMAND SET

Data and control information is read from and written to the DS1624 in the format shown in Figure 3. To write to the DS1624, the master will issue the slave address of the DS1624, and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1624 will issue an acknowledge, and then the master may send data to the DS1624. If the DS1624 is to be read, the master must send the command protocol as before, and then issue a repeated START condition and the control byte again, this time with the R/$\overline{W}$ bit set to 1 to allow reading of the data from the DS1624. The command set for the DS1624 as shown in Table 3 is as follows:

Access Memory [17h]

This command instructs the DS1624 to access its E^2 memory. After issuing this command, the next data byte is the value of the word address to be accessed. See OPERATION–MEMORY section for detailed explanations of the use of this protocol and data format following it.

Access Config [ACh]

If R/$\overline{W}$ is 0, this command writes to the configuration register. After issuing this command, the next data byte is value to be written into the configuration register. If R/$\overline{W}$ is 1, the next data byte read is the value store d in the configuration register.

Read Temperature [AAh]

This command reads the last temperature conversion result. The DS1624 will send two bytes, in the format described earlier, which are the contents of this register.

Start Convert T [EEh]

This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1624 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]

This command stops temperature conversion. No further data is required. This command may be used to halt a DS1624 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1624 will remain idle until a Start Convert T is issued to resume continuous operation.

DS1624 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	2–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Read last converted temperature value from temperature register.	AAh	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
MEMORY COMMANDS				
Access Memory	Reads or writes to 256–byte EEPROM memory.	17h	<write data>	2
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.

2. Writing to the E^2 typically requires 10 ms at room temperature. After issuing a write command, no further reads or writes should be requested for at least 10 ms.

   During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms).

MEMORY FUNCTION EXAMPLE

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
{Command protocol for configuration register} {Start here}				
TX	RX	START	Bus Master Initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	ACh	Bus Master sends Access Config command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	00h	Bus Master sets up DS1624 for continuous conversion.	
RX	TX	ACK	DS1624 generates acknowledge bit.	2
{Command protocol for Start Convert T} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	EEh	Bus Master sends Start Convert T command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	STOP	Bus Master initiates the STOP condition.	
{Command protocol for reading the Temperature} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr, 0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	AAh	Bus Master sends Read Temp command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,1>	Bus Master sends DS1624 address: R/$\overline{W}$=1;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the MSB byte of Temperature.	
TX	RX	ACK	Bus Master generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the LSB byte of Temperature.	
TX	RX	STOP	Bus Master Initiates the STOP condition.	

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
{Command protocol for writing to EEPROM} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	17h	Bus Master sends Access Memory command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	<madr>	Bus Master sends the starting memory address.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	<data>	Bus Master sends the first byte of data.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	<data>	Bus Master sends the second byte of data.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
TX	RX	<data>	Bus Master sends the n-th byte of data.	3
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	STOP	Bus Master initiates the STOP condition.	4
{Command protocol for reading from EEPROM} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	17h	Bus Master sends Access Memory command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	<madr>	Bus Master sends the starting memory address.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,1>	Bus Master sends DS1624 address: R/$\overline{W}$=1;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the first byte of data.	

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
TX	RX	ACK	Bus Master generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the second byte of data.	
TX	RX	ACK	Bus Master generates acknowledge bit.	
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
RX	TX	<data>	DS1624 sends the n-th byte of data.	5
TX	RX	STOP	Bus Master initiates the STOP condition.	

NOTES:

1. If this protocol follows a write and the DS1624 does not acknowledge here, restart the protocol at the Start here. If it does acknowledge, continue on.
2. Wait for write to complete (10 ms typ. 50 ms max). If DS1624 does not acknowledge the command protocol immediately following a configure register or write mem protocol, the DS1624 has not finished writing. Restart the new command protocol until the DS1624 acknowledges.
3. If n is greater than eight, the last eight bytes are the only bytes saved in memory. If the starting address is 00 and the incoming data is 00 11 22 33 44 55 66 77 88 99, the result will be mem00=88 mem01=99 mem02=22 mem03=33 mem04=44 mem05=55 mem06=66 mem07=77. The data wraps around and overwrites itself.
4. The STOP condition causes the DS1624 to initiate the write to EEPROM sequence. If a START condition comes instead of the STOP condition, the write is aborted. The data is not saved.
5. For reading, the address is incremented. If the starting address is 04h and 30 bytes of data are read out, 21h is the final address read.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	2.97	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.97V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to 70°C –55°C to +0°C and +70°C to +125°C	See Typical Curve		$\pm^1/_2$	°C	11
Low Level Input Voltage	V_{IL}		–0.5		$0.3V_{DD}$	V	
High Level Input Voltage	V_{IH}		$0.7V_{DD}$		V_{DD}+0.5	V	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	
Low Level Output Voltage	V_{OL1}	3 mA sink current	0		0.4	V	
	V_{OL2}	6 mA sink current	0		0.6	V	
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{DD}$	–10		10	µA	2
I/O Capacitance	$C_{I/O}$				10	pF	
Active Supply Current	I_{CC}	Temperature Conversion			1000		
		E^2 Write			400	µA	3, 4
		Communication Only			100		
Standby Supply Current	I_{STBY}			1	3	µA	3, 4

AC ELECTRICAL CHARACTERISTICS (–55°C to +125°C; V_{DD}=2.97V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}			200	500	ms	
NV Write Cycle Time	t_{WR}	0°C to 70°C		10	50	ms	10
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	KHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6, 7
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20+0.1C_B$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20+0.1C_B$		300 300	ns	9
Setup time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_b				400	pF	

All values referred to V_{IH}=0.9 V_{DD} and V_{IL}=0.1 V_{DD}.

AC ELECTRICAL CHARACTERISTICS (–55°C to +125°C; V_{DD}=2.97V to 5.5V)

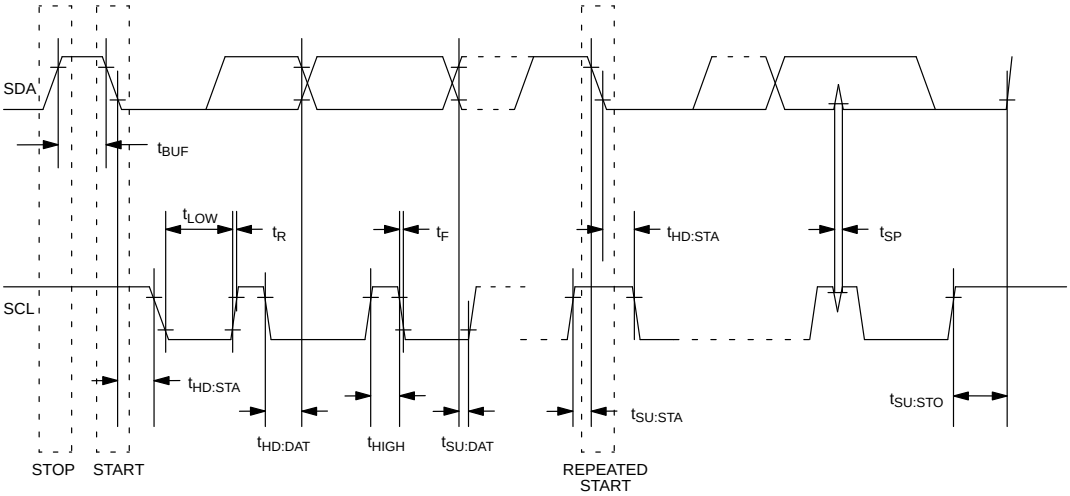
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with SDA pin open.
4. I_{CC} specified with V_{CC} at 5.0V and SDA, SCL = 5.0V, 0°C to +70°C.

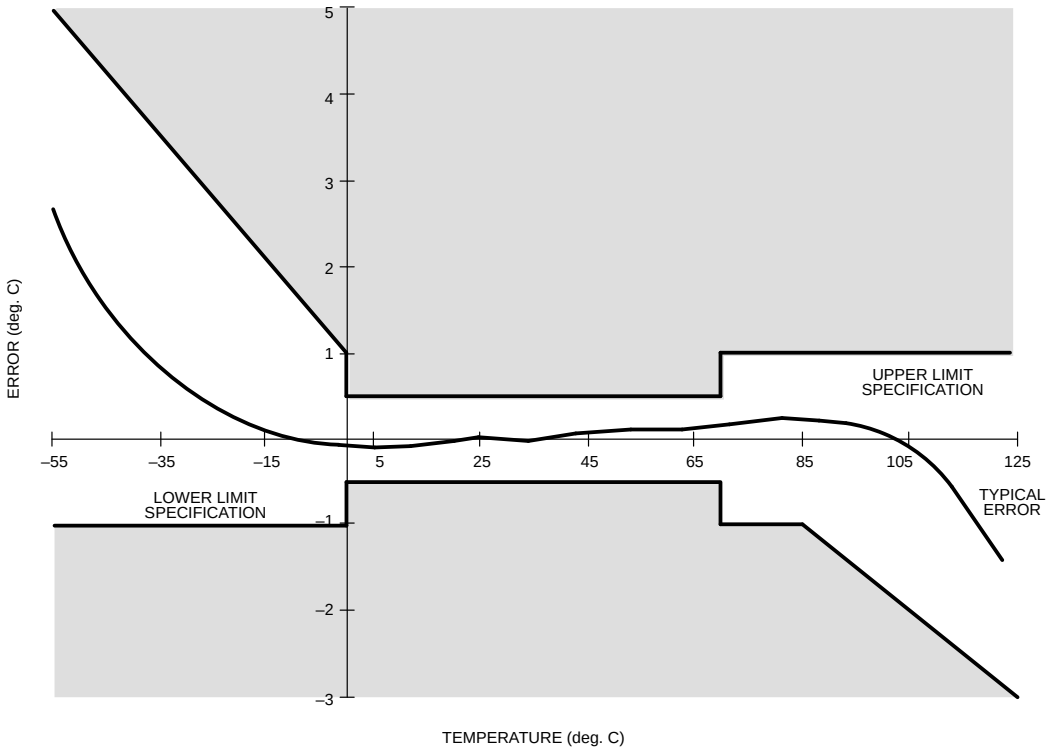
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX}+t_{SU:DAT}$ = 1000+250 = 1250 ns before the SCL line is released.
9. C_b – total capacitance of one bus line in pF.
10. Writing to the nonvolatile memory should only take place in the 0°C to +70°C temperature range.
11. See Typical Curve for specification limits outside the 0°C to 70°C temperature range.

TIMING DIAGRAMS



TYPICAL PERFORMANCE CURVE

DS1624 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



National Semiconductor

January 1996

DS26C31T/DS26C31M CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (see Note 8). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

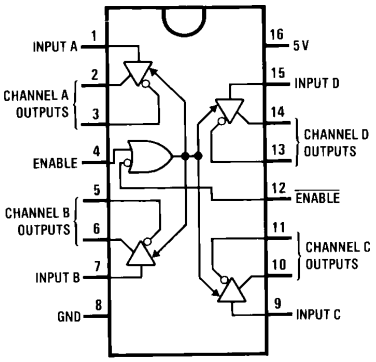
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs will not load line when V_{CC} = 0V
- DS26C31T meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount
- Mil-Std-883C compliant

Connection Diagrams

Dual-In-Line Package



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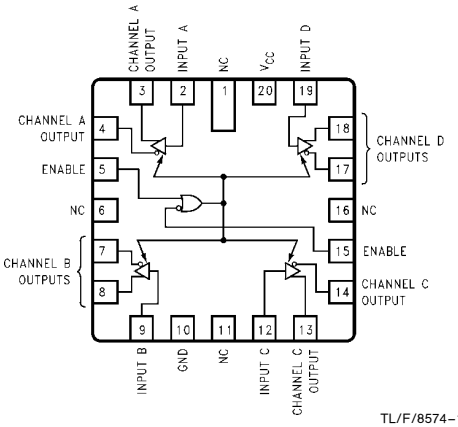
Top View

Order Number DS26C31TJ, DS26C31TM or DS26C31TN
See NS Package Number J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet

Order Number DS26C31ME/883, DS26C31MJ/883 or DS26C31MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier (E)



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max. Power Dissipation (P_D) @25°C (Note 3)	
Ceramic "J" Pkg.	2419 mW
Plastic "N" Pkg.	1736 mW
SOIC "M" Pkg.	1226 mW
Ceramic "W" Pkg.	1182 mW
Ceramic "E" Pkg.	2134 mW
Lead Temperature (T_L) (Soldering, 4 sec.)	260°C

This device does not meet 2000V ESD Rating. (Note 13)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS26C31T	−40	+85	°C
DS26C31M	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = -20$ mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 20$ mA			0.3	0.5	V
V_T	Differential Output Voltage	$R_L = 100\Omega$ (Note 5)		2.0	3.1		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference In Differential Output	$R_L = 100\Omega$ (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	$R_L = 100\Omega$ (Note 5)			1.8	3.0	V
$\lvert V_{OS} - \overline{V_{OS}}\rvert$	Difference In Common Mode Output	$R_L = 100\Omega$ (Note 5)				0.4	V
I_{IN}	Input Current	$V_{IN} = V_{CC}$, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current (Note 6)	DS26C31T $I_{OUT} = 0$ μA	$V_{IN} = V_{CC}$ or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.0	mA
		DS26C31M $I_{OUT} = 0$ μA	$V_{IN} = V_{CC}$ or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.1	mA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}} = V_{IH}$			±0.5	±5.0	μA

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND (Notes 5, 7)		−30		−150	mA
I_{OFF}	Output Leakage Current Power Off (Note 5)	DS26C31T $V_{CC} = 0V$	$V_{OUT} = 6V$			100	μA
			$V_{OUT} = -0.25V$			−100	μA
		DS26C31M $V_{CC} = 0V$	$V_{OUT} = 6V$			100	μA
			$V_{OUT} = 0V$ (Note 8)			−100	μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of ''Electrical Characteristics'' provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N package at 13.89 mW/°C, J package 16.13 mW/°C, M package 9.80 mW/°C, E package 12.20 mW/°C, and W package 6.75 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Note 8: The DS26C31M (−55°C to +125°C) is tested with V_{OUT} between +6V and 0V while RS-422A condition is +6V and −0.25V.

Switching Characteristics $V_{CC} = 5V \pm 10\%$, $t_r \leq 6$ ns, $t_f \leq 6$ ns (*Figures 1, 2, 3* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	S1 Open	2	6	11	14	ns
Skew	(Note 9)	S1 Open		0.5	2.0	3.0	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
t_{PZH}	Output Enable Time	S1 Closed		11	19	22	ns
t_{PZL}	Output Enable Time	S1 Closed		13	21	28	ns
t_{PHZ}	Output Disable Time (Note 10)	S1 Closed		5	9	12	ns
t_{PLZ}	Output Disable Time (Note 10)	S1 Closed		7	11	14	ns
C_{PD}	Power Dissipation Capacitance (Note 11)			50			pF
C_{IN}	Input Capacitance			6			pF

Note 9: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 10: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 11: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

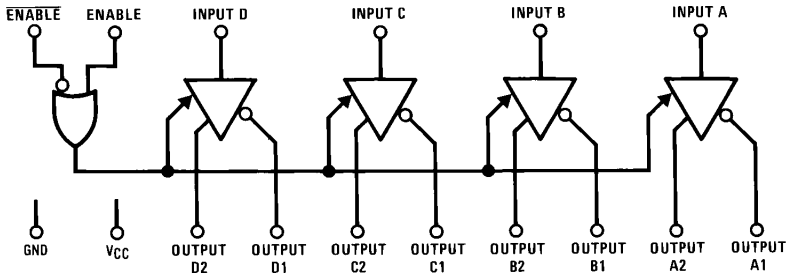
V_{CC} = 5V, T_A = 25°C, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns (*Figures 2, 4, 5* and *6*) (Note 12)

Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	C_L = 30 pF S1 Closed S2 Closed	6	8	10	15	ns
Skew	(Note 9)	C_L = 30 pF S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times	C_L = 30 pF S1 Closed S2 Closed	4	6			ns
t_{PLZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Closed S2 Open	6	9	15	35	ns
t_{PHZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Open S2 Closed	4	7	15	25	ns
t_{PZL}	Output Enable Time	C_L = 30 pF S1 Closed S2 Open	14	20	20	30	ns
t_{PZH}	Output Enable Time	C_L = 30 pF S1 Open S2 Closed	11	17	20	30	ns

Note 12: This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or guaranteed.

Note 13: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥ 1500V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Logic Diagram



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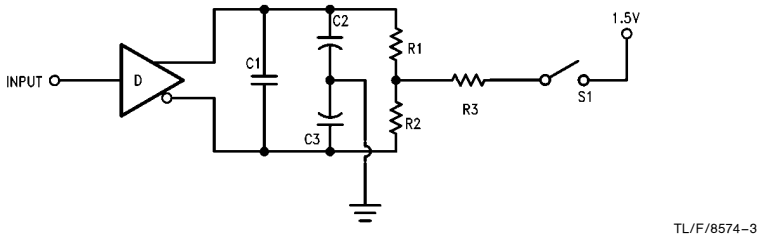
AC Test Circuit and Switching Time Waveforms



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

FIGURE 1. AC Test Circuit

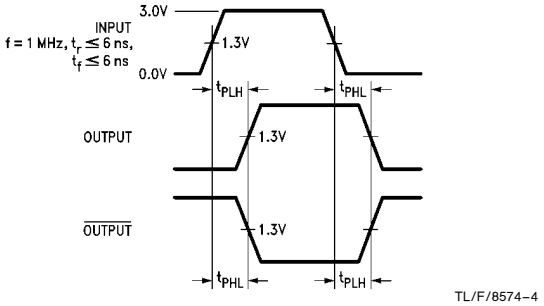


FIGURE 2. Propagation Delays

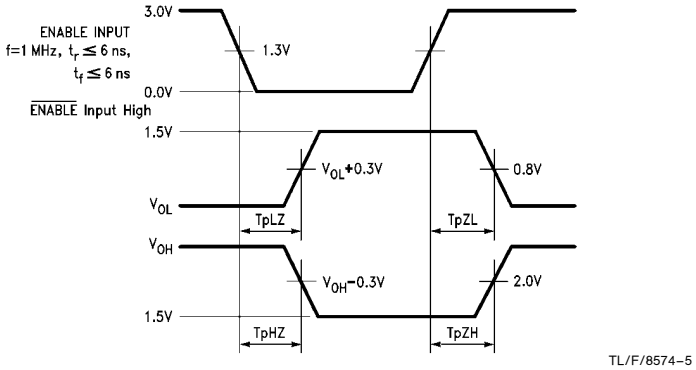
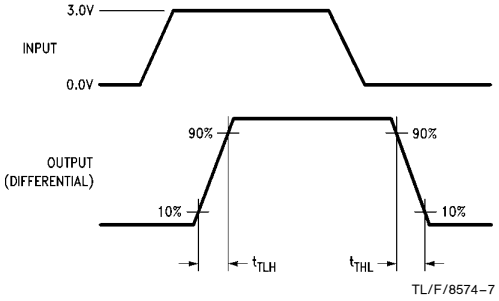


FIGURE 3. Enable and Disable Times



Input pulse; f = 1 MHz, 50%; $t_r \leq$ 6 ns, $t_f \leq$ 6 ns

FIGURE 4. Differential Rise and Fall Times

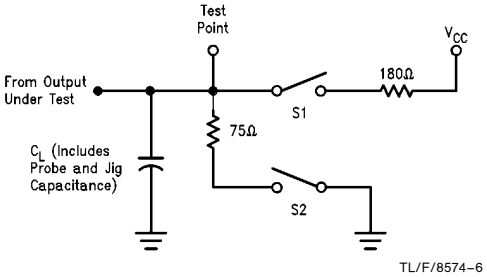


FIGURE 5. Load AC Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)

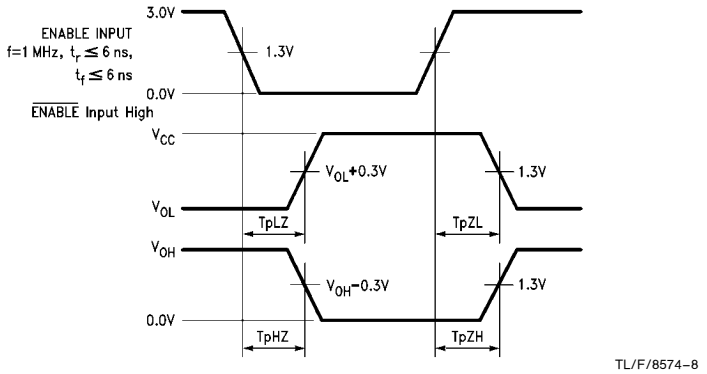
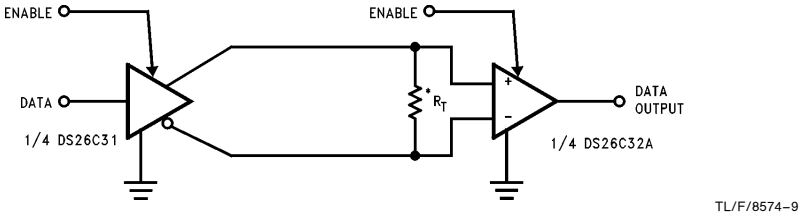


FIGURE 6. Enable and Disable Times for "LS-Type" Load

Typical Applications

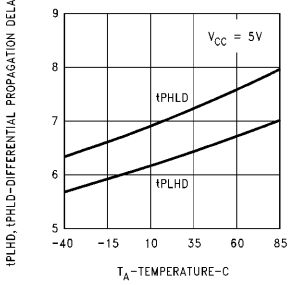
Two-Wire Balanced System, RS-422



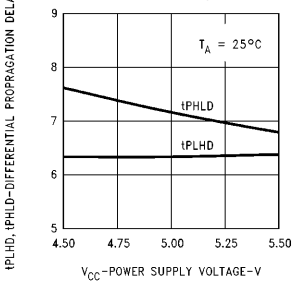
*R_T is optional although highly recommended to reduce reflection.

Typical Performance Characteristics

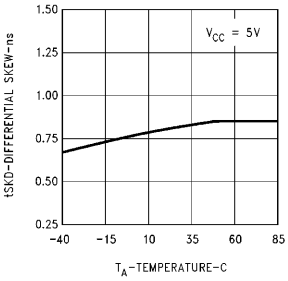
Differential Propagation Delay vs Temperature



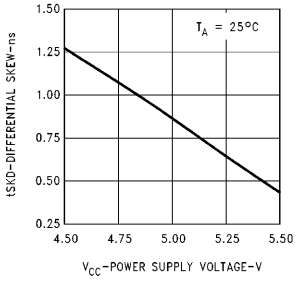
Differential Propagation Delay vs Power Supply Voltage



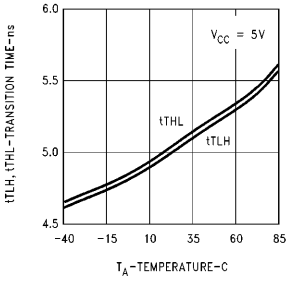
Differential Skew vs Temperature



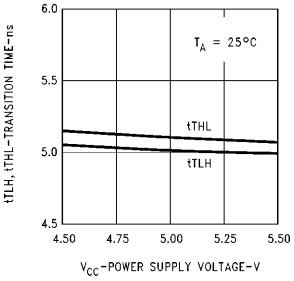
Differential Skew vs Power Supply Voltage



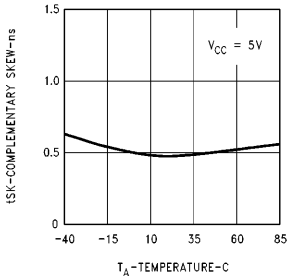
Differential Transition Time vs Temperature



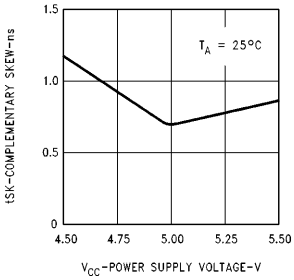
Differential Transition Time vs Power Supply Voltage



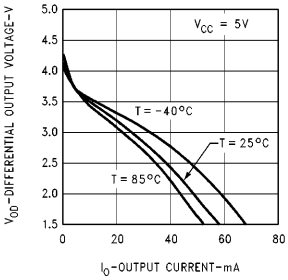
Complementary Skew vs Temperature



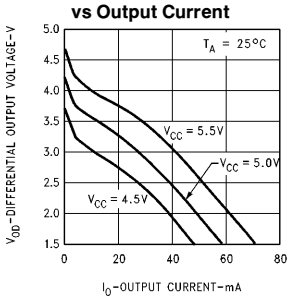
Complementary Skew vs Power Supply Voltage



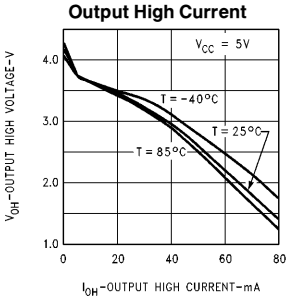
Differential Output Voltage vs Output Current



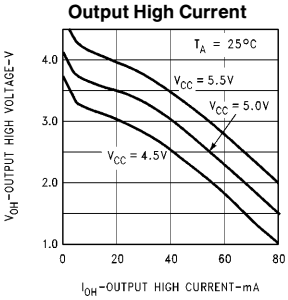
Differential Output Voltage vs Output Current



Output High Voltage vs Output High Current



Output High Voltage vs Output High Current



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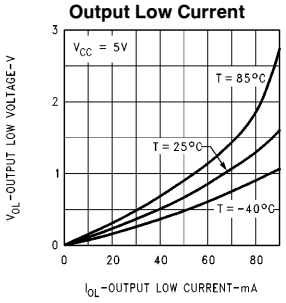
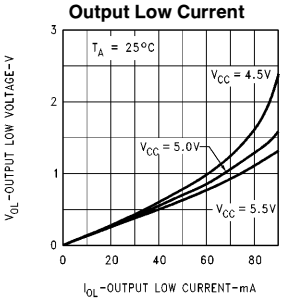
Typical Performance Characteristics (Continued)

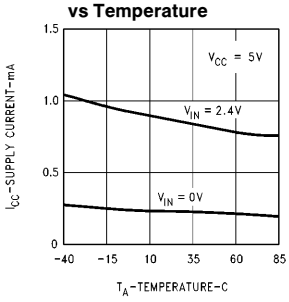
Output Low Voltage vs Output Low Current



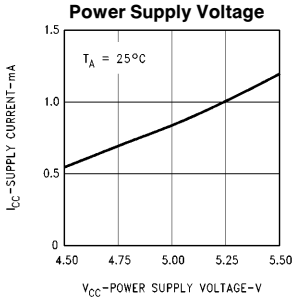
Output Low Voltage vs Output Low Current



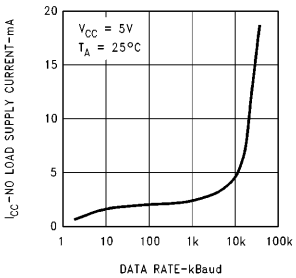
Supply Current vs Temperature



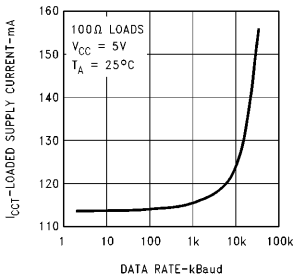
Supply Current vs Power Supply Voltage



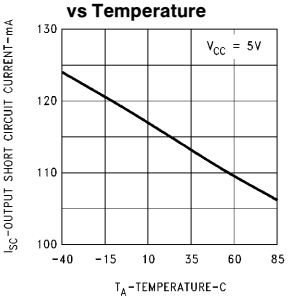
No Load Supply Current vs Data Rate



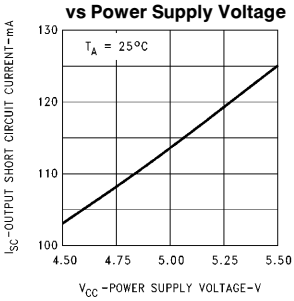
Loaded Supply Current vs Data Rate



Output Short Circuit Current vs Temperature



Output Short Circuit Current vs Power Supply Voltage



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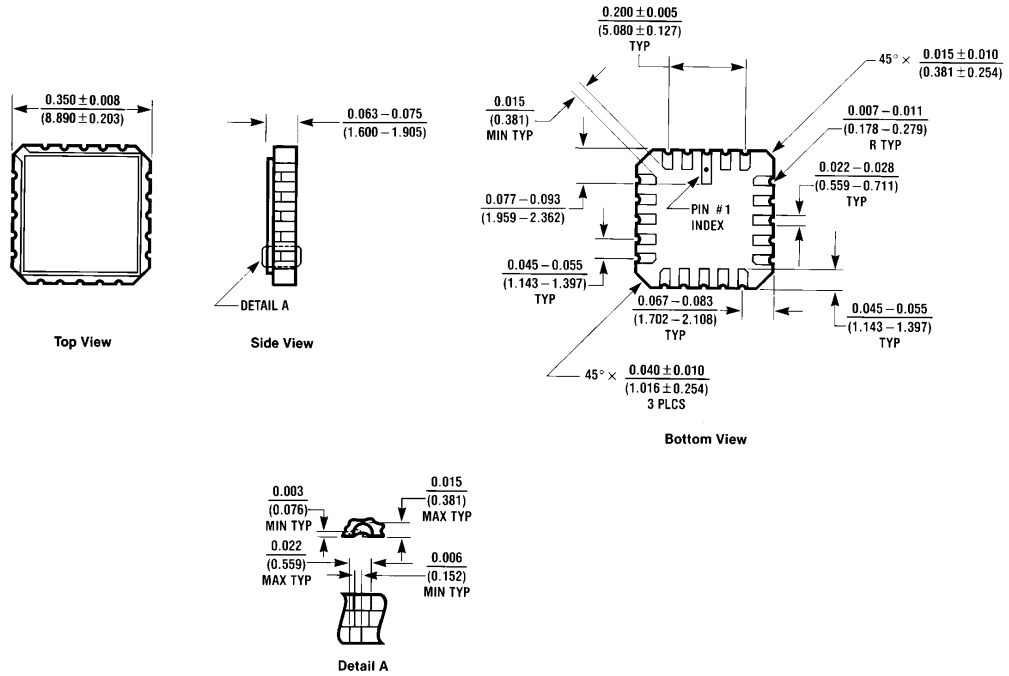
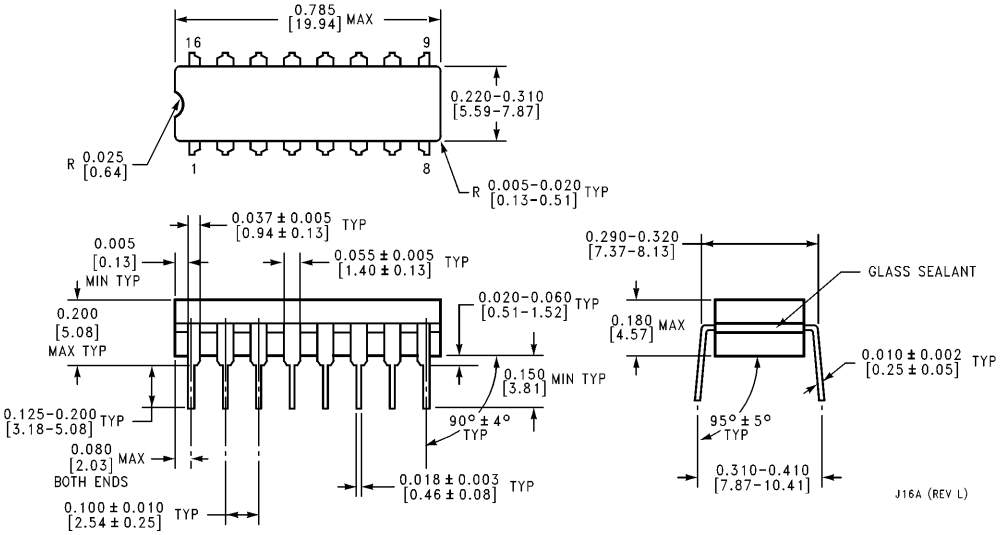
Physical Dimensions inches (millimeters)

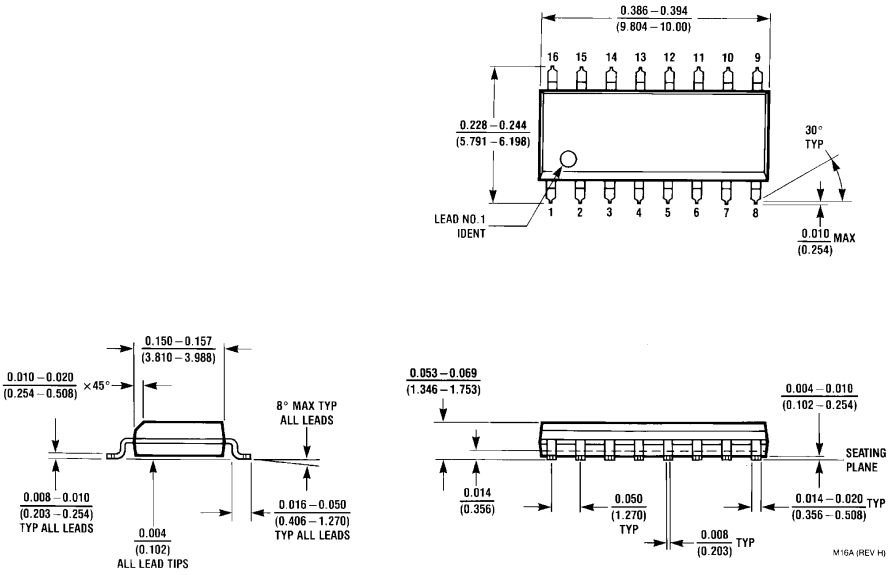


20-Lead Ceramic Leadless Chip Carrier (E)
Order Number DS26C31ME/883
NS Package Number E20A

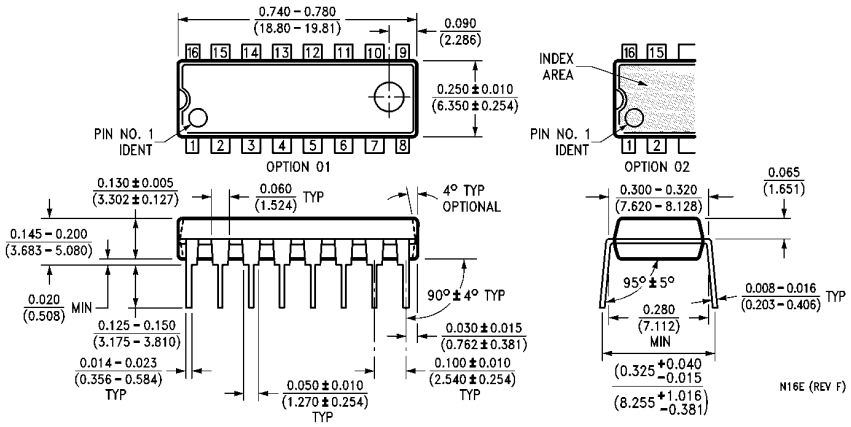


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DS26C31TJ or DS26C31MJ/883
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

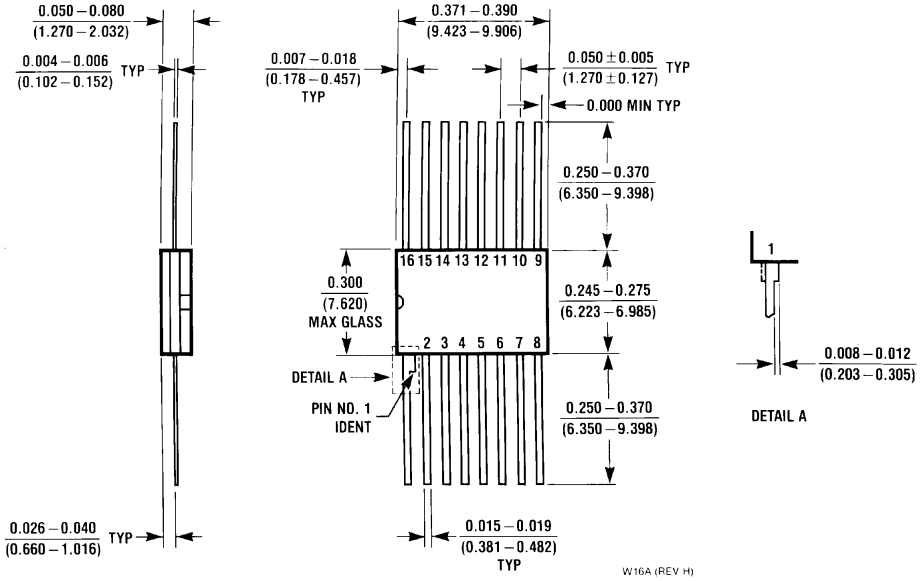


Molded Package Small Outline (M)
Order Number DS26C31TM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DS26C31TN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak Package (W)
Order Number DS26C31MW/883
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

January 1996

DS26C32AT/DS26C32AM Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

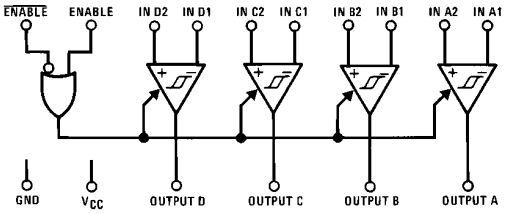
The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- CMOS design for low power
- ±0.2V sensitivity over input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses
- Available in Surface Mount
- Mil-Std-883C compliant

Logic Diagram



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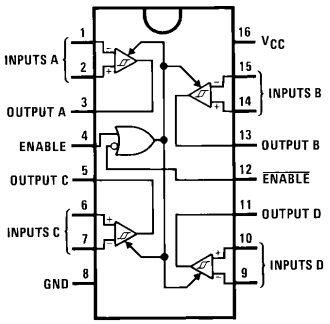
Connection Diagrams

Dual-In-Line Package



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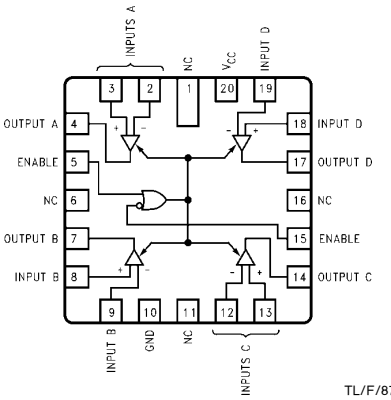
Top View

Order Number DS26C32ATJ, DS26C32ATM or DS26C32ATN
See NS Package J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet.

Order Number DS26C32AME/883, DS26C32AMJ/883 or DS26C32AMW/883
See NS Package E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



TL/F/8764–12

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH}$ (Max)	H
		$V_{ID} \leq V_{TH}$ (Min)	L
		Open	H

Z = TRI-STATE

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Pkg.	2308 mW
Plastic "N" Pkg.	1645 mW
SOIC "M" Pkg.	1190 mW
Ceramic "E" Pkg.	2108 mW
Ceramic "W" Pkg.	1215 mW
Maximum Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	−40	+85	°C
DS26C32AM	−55	+125	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$		−200	35	+200	mV
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	DS26C32AT	5.0	6.8	10	kΩ
			DS26C32AM	4.5	6.8	11	kΩ
I_{IN}	Input Current	$V_{IN} = +10V$, Other Input = GND	DS26C32AT		+1.1	+1.5	mA
			DS26C32AM		+1.1	+1.8	mA
		$V_{IN} = -10V$, Other Input = GND	DS26C32AT		−2.0	−2.5	mA
			DS26C32AM		−2.0	−2.7	mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, $V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA		3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, $V_{DIFF} = -1V$ $I_{OUT} = 6.0$ mA			0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage			2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage					0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, ENABLE = V_{IL}, $\overline{ENABLE} = V_{IH}$			±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND				±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, $V_{DIF} = +1V$	DS26C32AT		16	23	mA
			DS26C32AM		16	25	mA
V_{HYST}	Input Hysteresis	$V_{CM} = 0V$			60		mV

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C32AT	DS26C32AM	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	$C_L = 50$ pF $V_{DIFF} = 2.5V$ $V_{CM} = 0V$	10	19	30	35	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	$C_L = 50$ pF $V_{DIFF} = 2.5V$ $V_{CM} = 0V$		4	9	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	22	29	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	23	29	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of ''Electrical Characteristics'' provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥2000V
All other pins ≥1000V
EIAJ (0Ω, 200 pF) ≥350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C, M Package 9.52 mW/°C, E Package 12.04 mW/°C, and W package 6.94 mW/°C.

Comparison Table of Switching Characteristics into ''LS-Type'' Load

(*Figures 4, 5,* and *6*) (Note 6)

Symbol	Parameter	Conditions	DS26C32A	DS26LS32A	Units
			Typ	Typ	
t_{PLH} t_{PHL}	Input to Output	$C_L = 15$ pF	17 19	23 23	ns ns
t_{LZ} t_{HZ}	ENABLE to Output	$C_L = 5$ pF	13 12	15 20	ns ns
t_{ZL} t_{ZH}	ENABLE to Output	$C_L = 15$ pF	13 13	14 15	ns ns

Note 6: This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested or guaranteed.

Test and Switching Waveforms

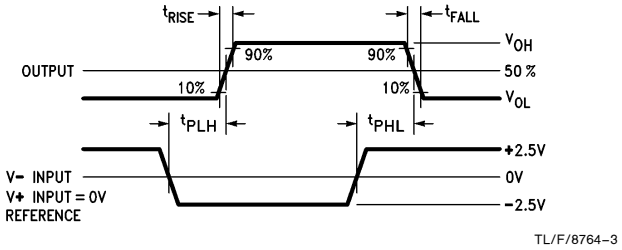
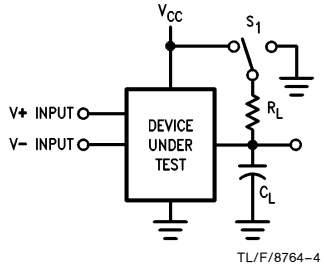


FIGURE 1. Propagation Delay



C_L includes load and test jig capacitance.

S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

S_1 = Gnd for t_{PZH} and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

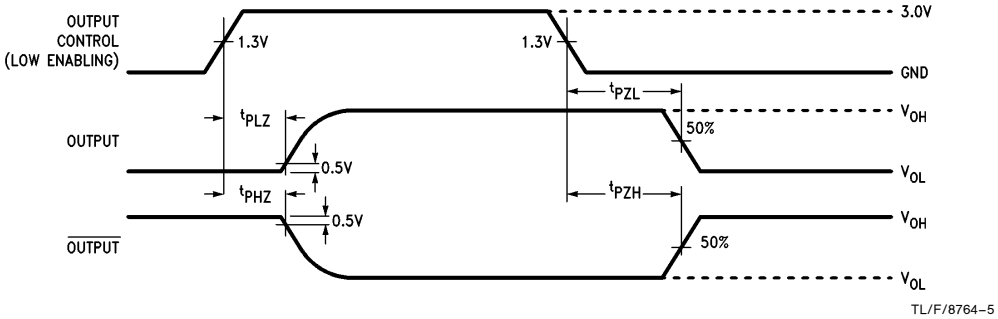


FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuit and Switching Time Waveforms

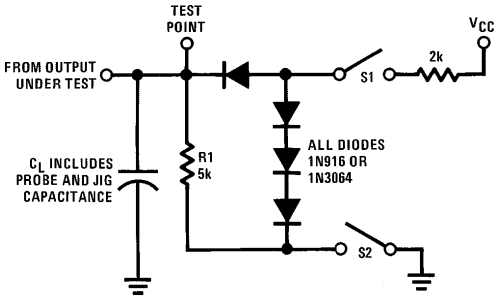


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FIGURE 4. Load Test Circuit for TRI-STATE Outputs for "LS-Type" Load

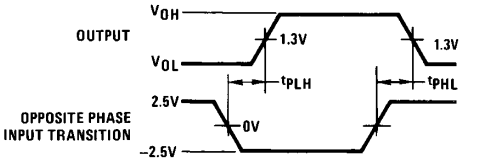

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FIGURE 5. Propagation Delay for "LS-Type" Load (Notes 7, 9)

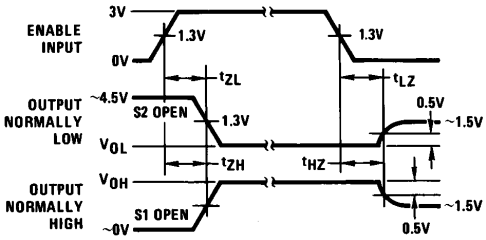

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FIGURE 6. Enable and Disable Times for "LS-Type" Load (Notes 8, 9)

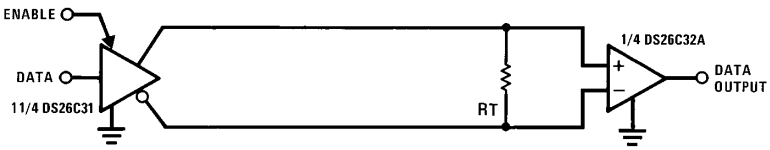
Note 7: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 8: S1 and S2 of load circuit are closed except where shown.

Note 9: Pulse generator for all pulses: Rate $\leq$ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced Systems, RS-422



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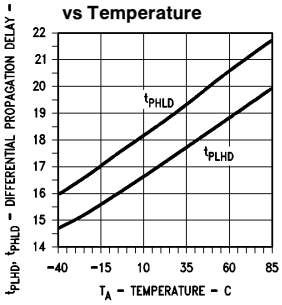
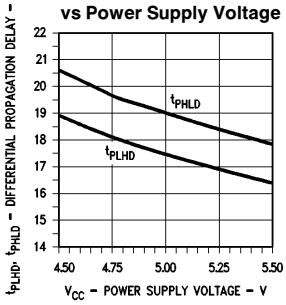
Typical Performance Characteristics

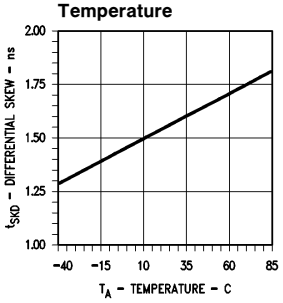
Differential Propagation Delay vs Temperature



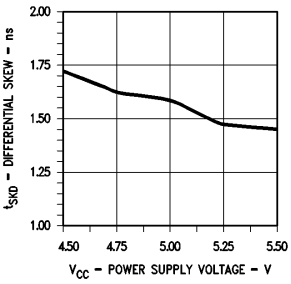
Differential Propagation Delay vs Power Supply Voltage



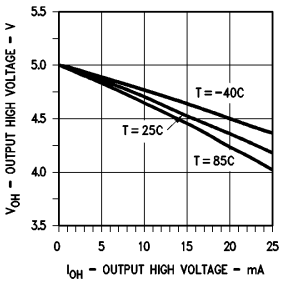
Differential Skew vs Temperature



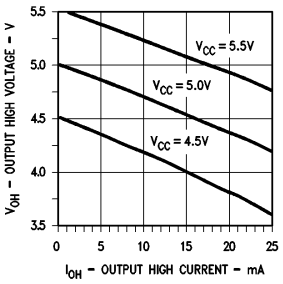
Differential Skew vs Power Supply Voltage



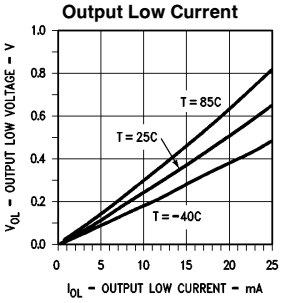
Output High Voltage vs Output High Current



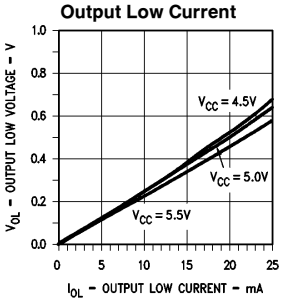
Output High Voltage vs Output High Current



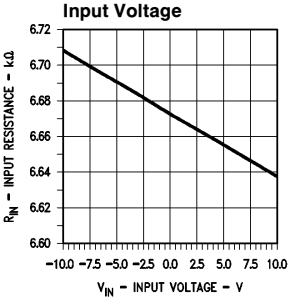
Output Low Voltage vs Output Low Current



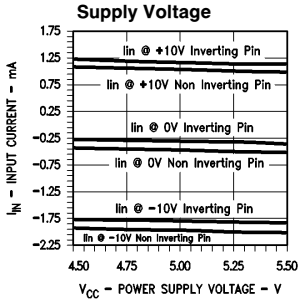
Output Low Voltage vs Output Low Current



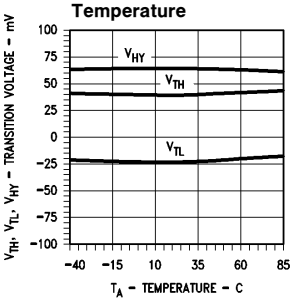
Input Resistance vs Input Voltage



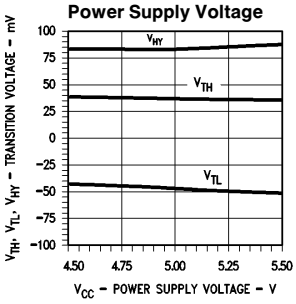
Input Current vs Power Supply Voltage



Hysteresis & Differential Transition Voltage vs Temperature



Hysteresis & Differential Transition Voltage vs Power Supply Voltage



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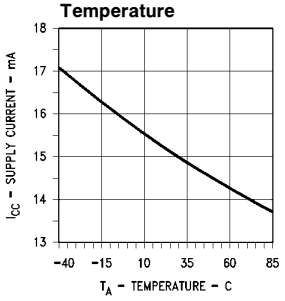
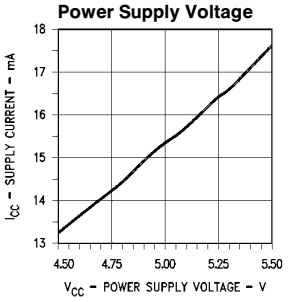
Typical Performance Characteristics (Continued)

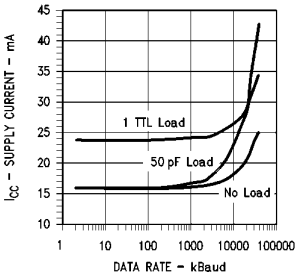
Supply Current vs Temperature



Disabled Supply Current vs Power Supply Voltage

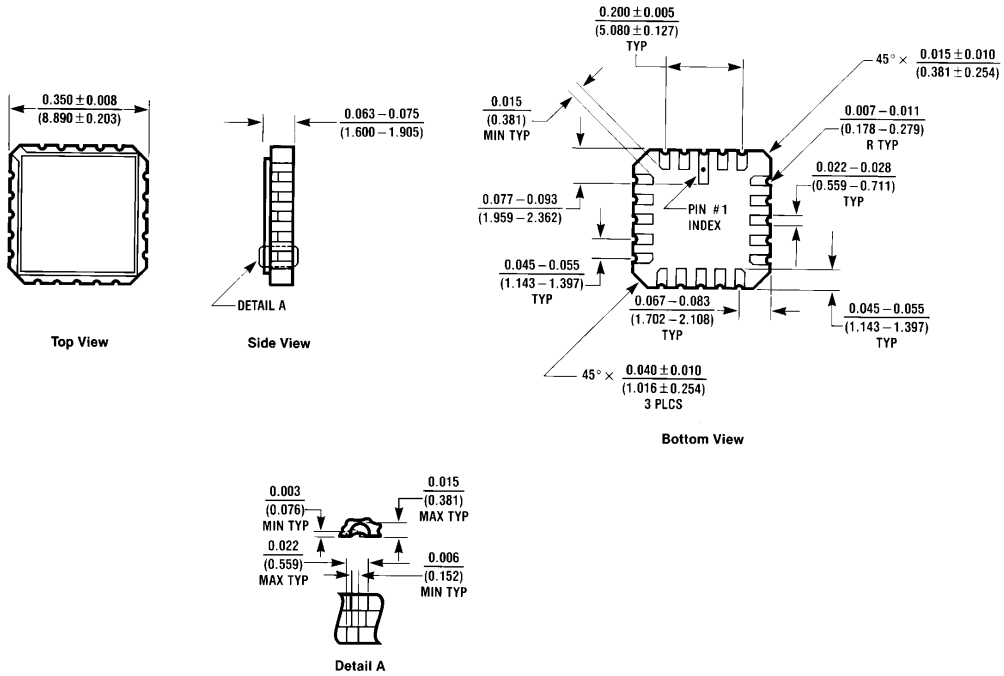


Supply Current vs Data Rate

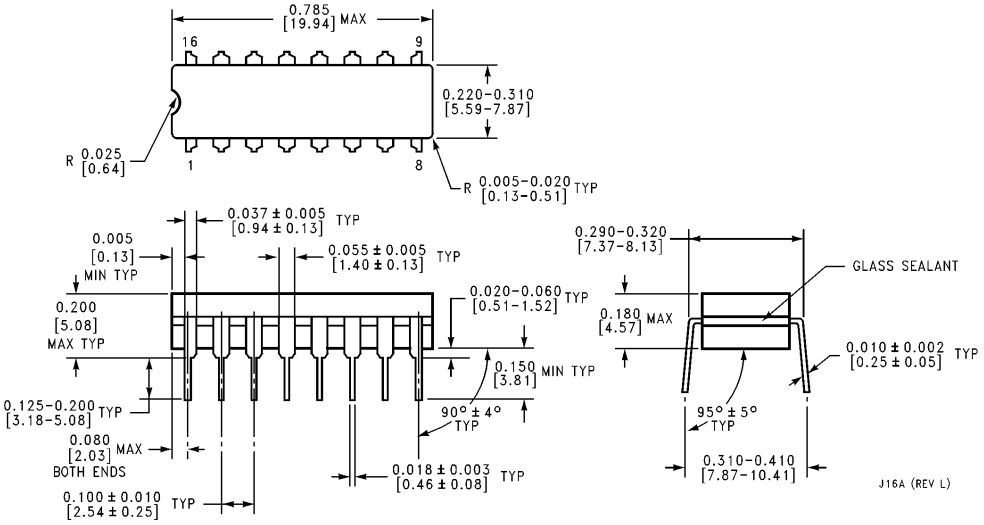


TL/F/8764–11

Physical Dimensions inches (millimeters)

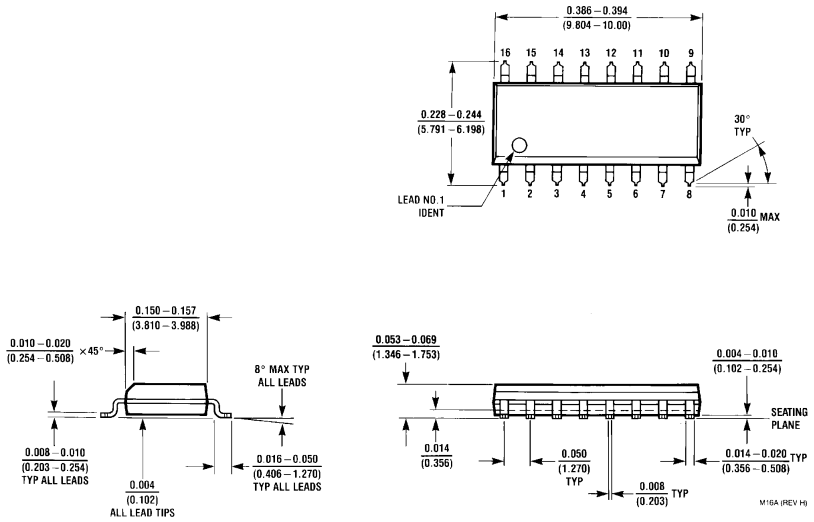


20-Lead Ceramic Leadless Chip Carrier (E)
Order Number DS26C32AME/883
NS Package Number E20A

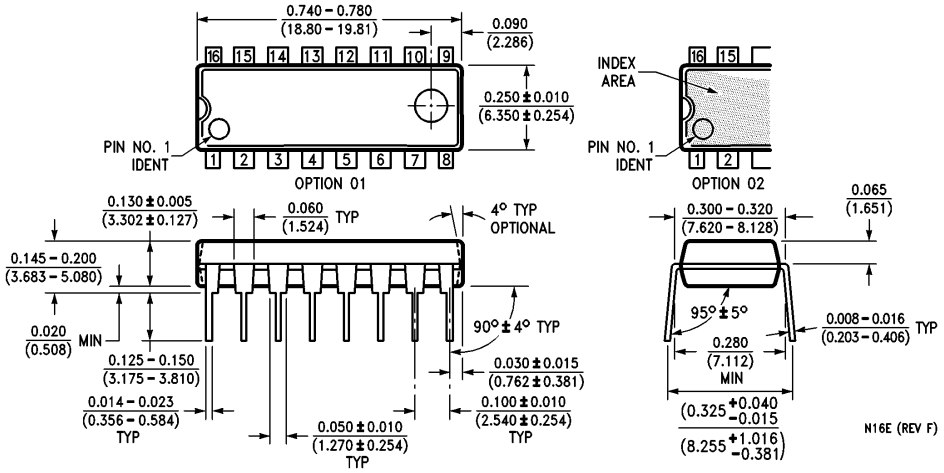


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DS26C32ATJ or DS26C32AMJ/883
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



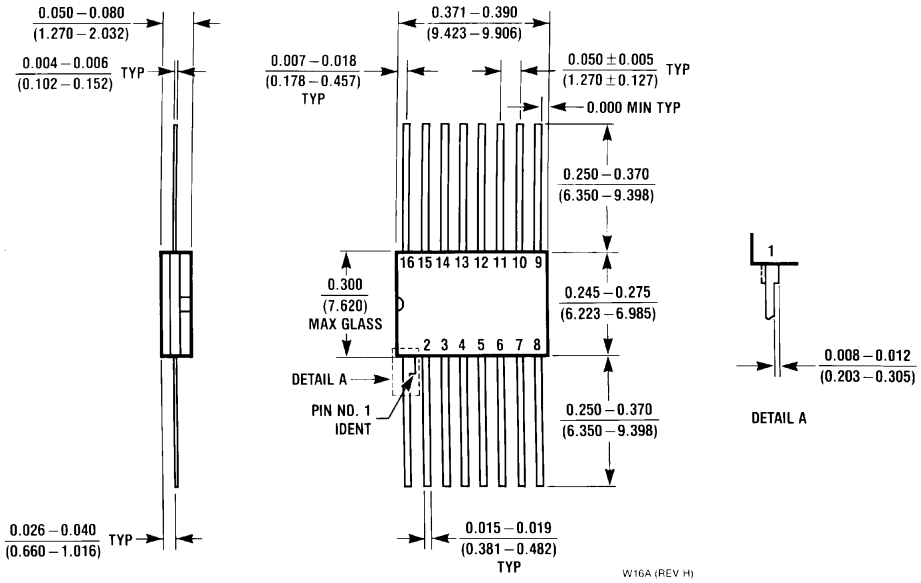
16-Lead Molded Small Outline Package (M)
Order Number DS26C32ATM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DS26C32ATN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)

Lit. # 103324



16-Lead Ceramic FlatPak (W)
Order Number DS26C32AMW/883
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

January 1995

LM137/LM337
3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM337 are ideal complements to the LM117/LM317 adjustable positive regulators.

Features

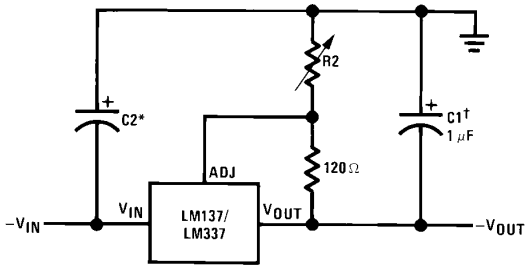
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- P+ Product Enhancement tested
- Standard 3-lead transistor package
- Output is short circuit protected

LM137 Series Packages and Power Capability

Device	Package	Rated Power Dissipation	Design Load Current
LM137/337	TO-3 (K) TO-39 (H)	20W 2W	1.5A 0.5A
LM337	TO-220 (T)	15W	1.5A

Typical Applications

Adjustable Negative Voltage Regulator



TL/H/9067–1

Full output current not available at high input-output voltages

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4″ from power-supply filter capacitor

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	−55°C to +150°C
LM337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic Package (Soldering, 4 sec.)	260°C
ESD Rating	2k Volts

Electrical Characteristics (Note 1)

Parameter	Conditions	LM137			LM337			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_j = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ (Note 2) $I_L = 10$ mA		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_j = 25°C$, $10\ mA \le I_{OUT} \le I_{MAX}$		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\ mA \le I_L \le I_{MAX}$ $3.0V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $T_A = 25°C$		2	5		2	5	μA
Reference Voltage	$T_j = 25°C$ (Note 3) $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3) $10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	−1.225 −1.200	−1.250 −1.250	−1.275 −1.300	−1.213 −1.200	−1.250 −1.250	−1.287 −1.300	V V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 40V$ $\lvert V_{IN} - V_{OUT} \rvert \le 10V$		2.5 1.2	5 3		2.5 1.5	10 6	mA mA
Current Limit	$\lvert V_{IN} - V_{OUT} \rvert \le 15V$ K and T Package H Package $\lvert V_{IN} - V_{OUT} \rvert = 40V$, $T_j = 25°C$ K and T Package H Package	 1.5 0.5 0.24 0.15	 2.2 0.8 0.4 0.17	 3.5 1.8 	 1.5 0.5 0.15 0.10	 2.2 0.8 0.4 0.17	 3.7 1.9 	 A A A A
RMS Output Noise, % of V_{OUT}	$T_j = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz $C_{ADJ} = 10\ \mu F$	 66	60 77		 66	60 77		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package K Package T Package		12 2.3	15 3		12 2.3 4	15 3	°C/W °C/W °C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	H Package K Package T Package		140 35			140 35 50		°C/W °C/W °C/W

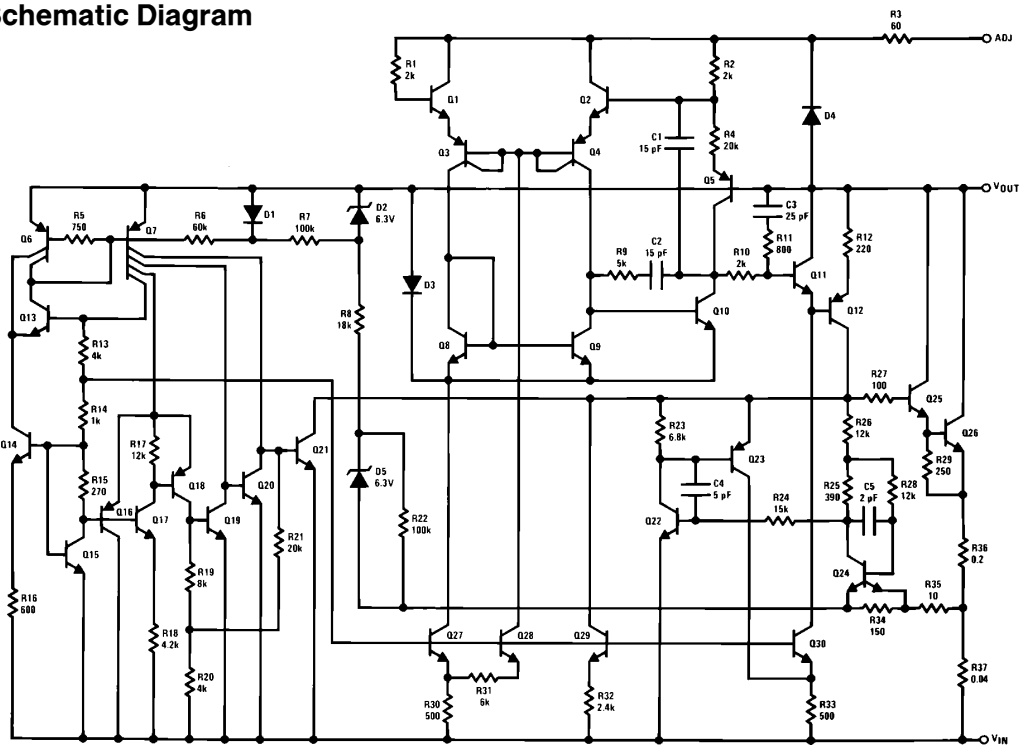
Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages, and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point ⅛″ below the base of the TO-3 and TO-39 packages.

Note 3: Selected devices with tightened tolerance reference voltage available.

Note 4: Refer to RETS137H drawing for LM137H or RETS137K drawing for LM137K military specifications.

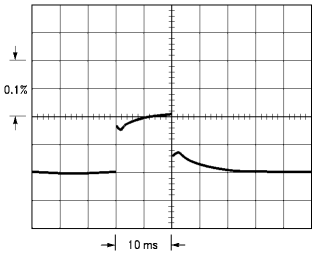
Schematic Diagram



TL/H/9067–2

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

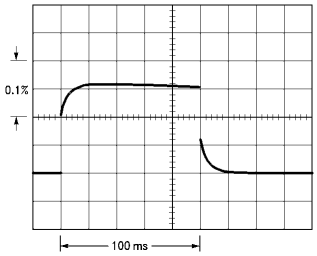


TL/H/9067–3

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_{IL} = 0A \rightarrow 0.25A \rightarrow 0A$
Vertical sensitivity, 5 mV/div

FIGURE 1

In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W × 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step at the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



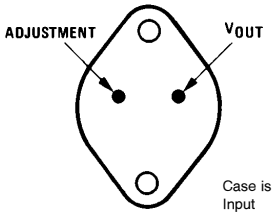
TL/H/9067–4

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Horizontal sensitivity, 20 ms/div

FIGURE 2

Connection Diagrams

TO-3
Metal Can Package

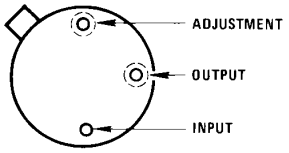


TL/H/9067–5

Bottom View
Order Number LM137K/883
See NS Package Number K02C

Order Number LM337K STEEL
See NS Package Number K02A

TO-39
Metal Can Package



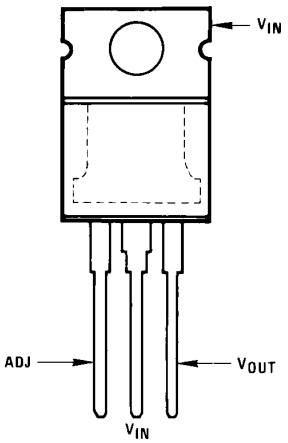
Case Is Input

TL/H/9067–6

Bottom View

Order Number LM137H, LM137H/883 or LM337H
See NS Package Number H03A

TO-220
Plastic Package



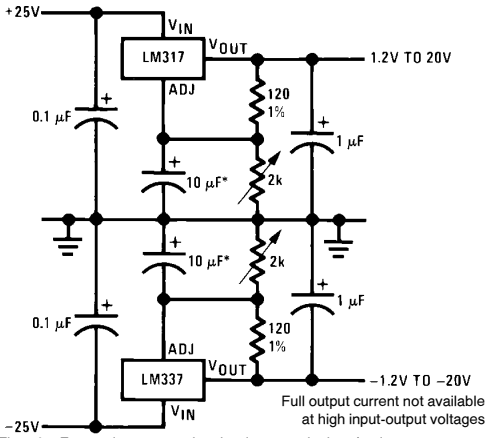
TL/H/9067–7

Front View

Order Number LM337T
See NS Package Number T03B

Typical Applications (Continued)

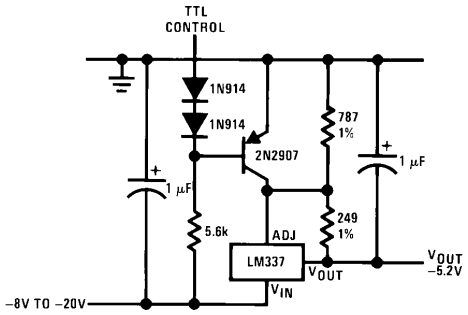
Adjustable Lab Voltage Regulator



*The 10 μF capacitors are optional to improve ripple rejection

TL/H/9067–9

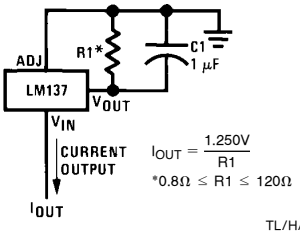
−5.2V Regulator with Electronic Shutdown*



TL/H/9067–10

*Minimum output ≅ −1.3V when control input is low

Current Regulator

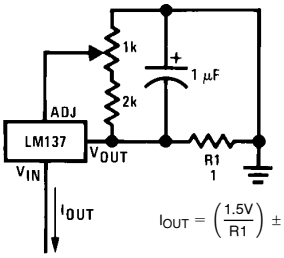


$I_{OUT} = \frac{1.250V}{R1}$

*0.8Ω ≤ R1 ≤ 120Ω

TL/H/9067–11

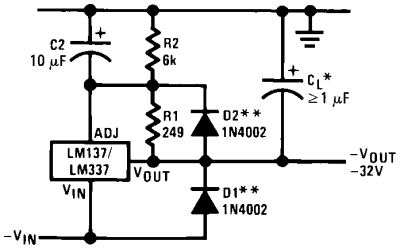
Adjustable Current Regulator



$I_{OUT} = \left(\frac{1.5V}{R1}\right) \pm 15\%$ adjustable

TL/H/9067–12

Negative Regulator with Protection Diodes

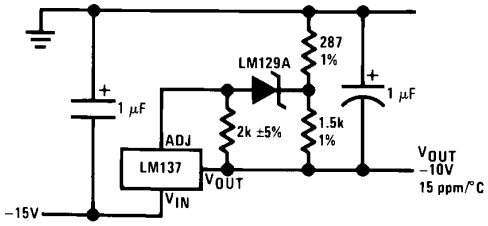


TL/H/9067–13

*When C_L is larger than 20 μF, D1 protects the LM137 in case the input supply is shorted

**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

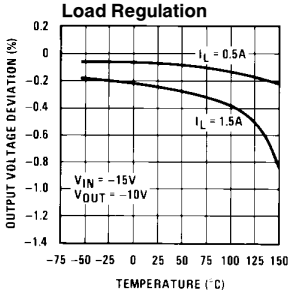
High Stability −10V Regulator



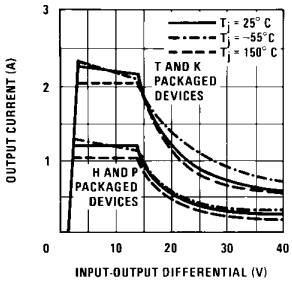
TL/H/9067–14

Typical Performance Characteristics (K Steel and T Packages)

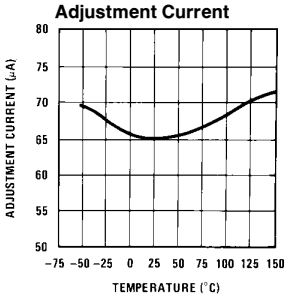
Load Regulation



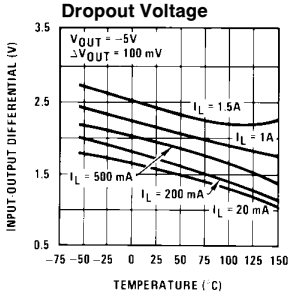
Current Limit



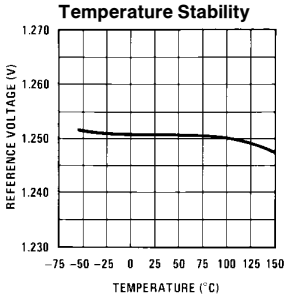
Adjustment Current



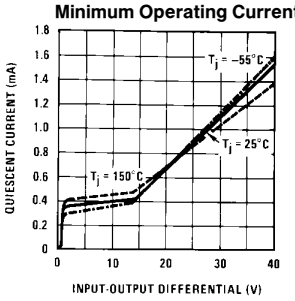
Dropout Voltage



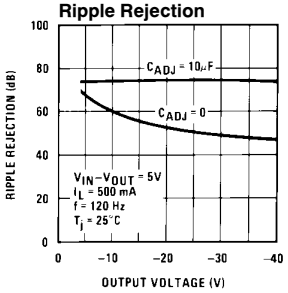
Temperature Stability



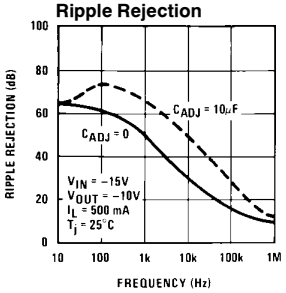
Minimum Operating Current



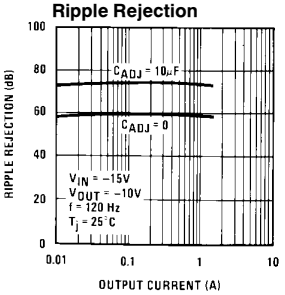
Ripple Rejection



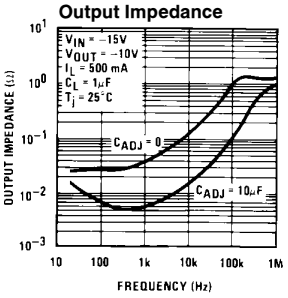
Ripple Rejection



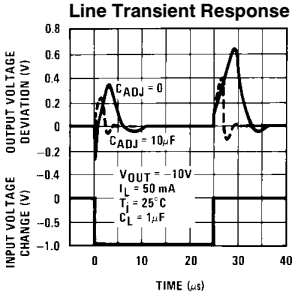
Ripple Rejection



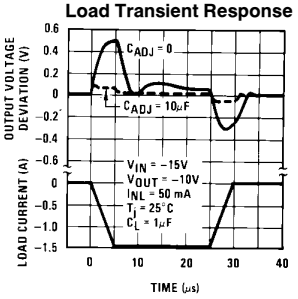
Output Impedance



Line Transient Response

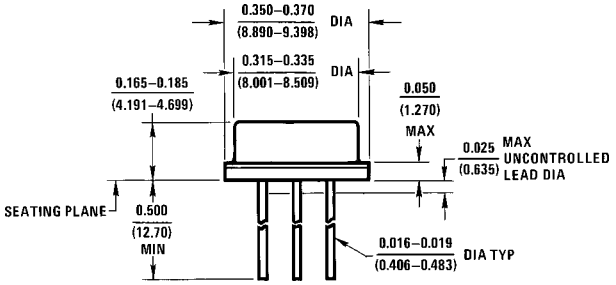


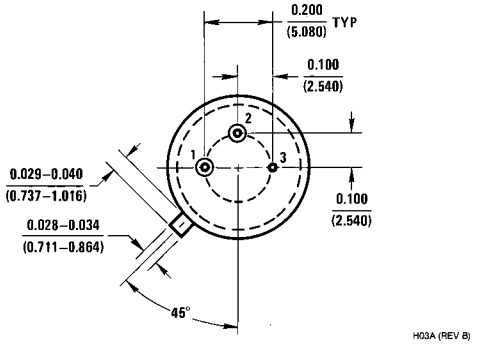
Load Transient Response



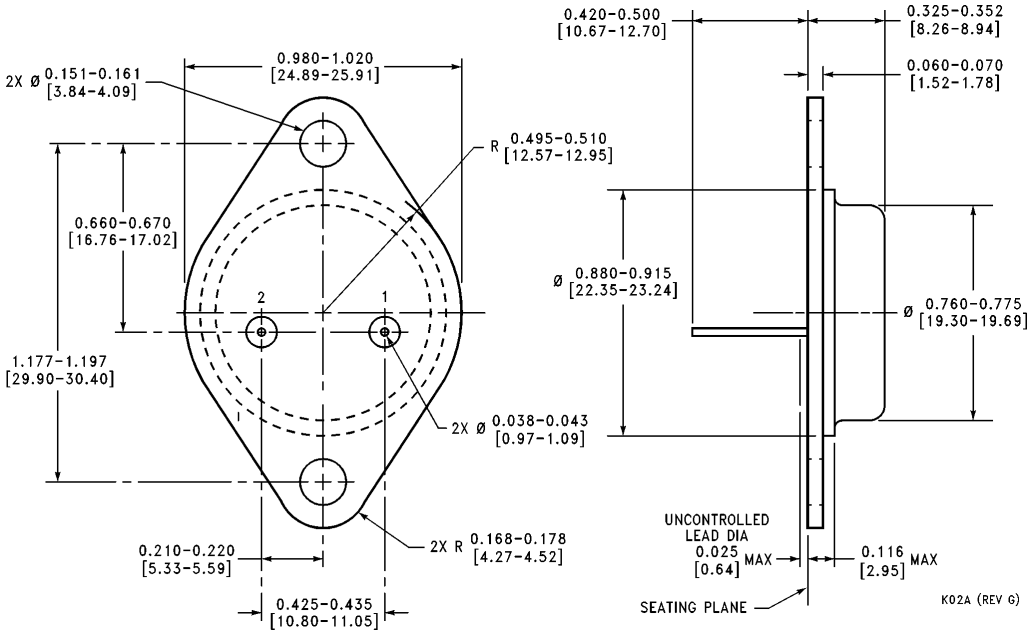
TL/H/9067–15

Physical Dimensions inches (millimeters)



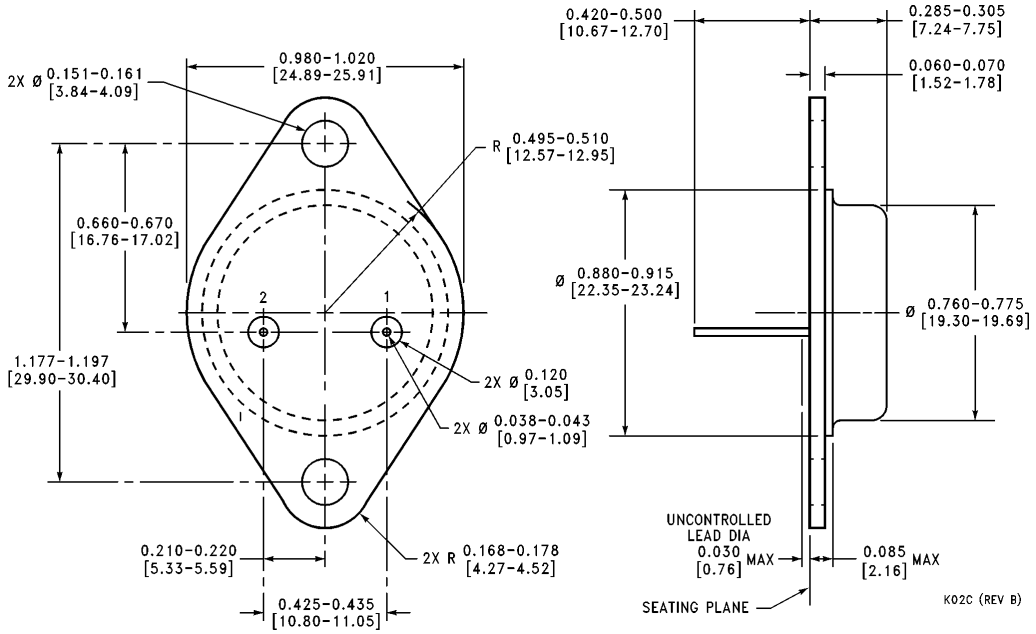


Metal Can Package (H)
Order Number LM137H, LM137H/883 or LM337H
NS Package Number H03A



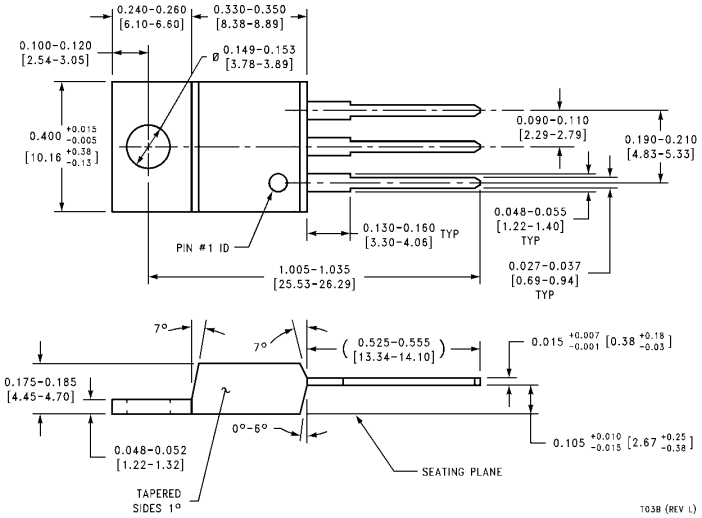
Metal Can Package (K)
Order Number LM337K STEEL
NS Package Number K02A

Physical Dimensions inches (millimeters) (Continued)



Mil-Aero Metal Can Package (K)
Order Number LM137K/883
NS Package Number K02C

Physical Dimensions inches (millimeters) (Continued)



TO-220 Plastic Package (T)
Order Number LM337T
NS Package Number T03B

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FEATURES

- Low Resistance Pass Transistor: 0.25Ω
- Dropout Voltage: 0.75V at 3A
- ±1% Reference Voltage
- **Accurate** Programmable Current Limit
- Shutdown Capability
- Internal Reference Available
- Standard 5-Lead Packages
- Full Remote Sense
- Low Quiescent Current: ≈2.5mA
- Good High Frequency Ripple Rejection

DESCRIPTION

The LT1185 is a 3A low dropout regulator with adjustable current limit and remote sense capability. It can be used as a positive output regulator with floating input or as a standard negative regulator with grounded input. The output voltage range is 2.5V to 25V, with ±1% accuracy on the internal reference voltage.

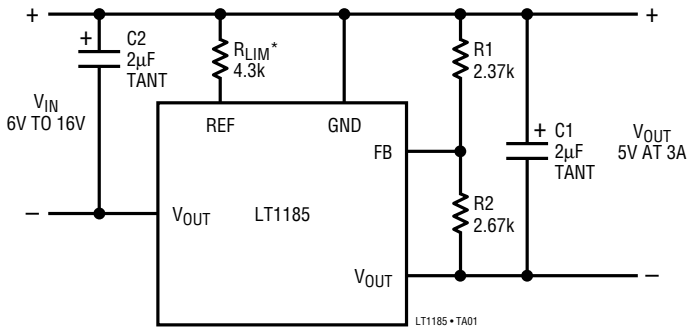
The LT1185 uses a saturation-limited NPN transistor as the pass element. This device gives the linear dropout characteristics of an FET pass element with significantly less die area. High efficiency is maintained by using special anti-saturation circuitry that adjusts base drive to track load current. The "on resistance" is typically 0.25Ω.

Accurate current limit is programmed with a single 1/8W external resistor, with a range of zero to three amperes. A second, fixed internal limit circuit prevents destructive currents if the programming current is accidentally over-ranged. Shutdown of the regulator output is guaranteed when the program current is less than 1μA, allowing external logic control of output voltage.

The LT1185 has all the protection features of previous LTC regulators, including power limiting and thermal shut-down. The 4-lead TO-3 package is specified for –55°C to 150°C operation and the 5-lead TO-220 is specified over 0°C to 125°C.

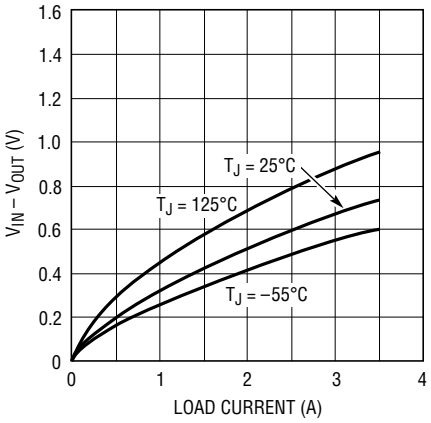
TYPICAL APPLICATION

5V, 3A Regulator with 3.5A Current Limit



*CURRENT LIMIT = 15k/R_{LIM} = 3.5A

Dropout Voltage

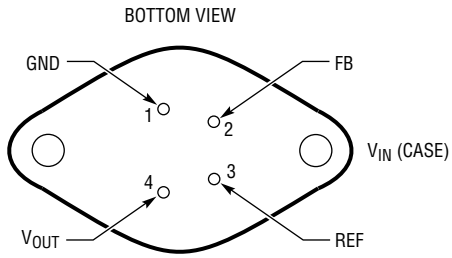


ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V
Input-Output Differential 30V
FB Voltage 7V
REF Voltage 7V
Output Voltage 30V
Output Reverse Voltage 2V
Operating Ambient Temperature Range
  LT1185C ..... 0°C to 70°C
  LT1185M ..... –55°C to 125°C
Operating Junction Temperature Range*
Control Section
  LT1185C ..... 0°C to 125°C
  LT1185I ..... –40°C to 125°C
  LT1185M ..... –55°C to 150°C
Power Transistor Section
  LT1185C ..... 0°C to 150°C
  LT1185I ..... –40°C to 150°C
  LT1185M ..... –55°C to 175°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

*See Application Section for details on calculating Operation Junction Temperature

PACKAGE/ORDER INFORMATION

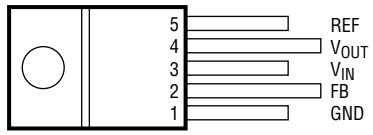


K PACKAGE
4-LEAD TO-3 METAL CAN

$\theta_{JC\ MAX}$ = 2.5°C/W, θ_{JA} = 35°C/W

ORDER PART NUMBER

LT1185MK



T PACKAGE
5-LEAD TO-220

$\theta_{JC\ MAX}$ = 2.5°C/W, θ_{JA} = 50°C/W

ORDER PART NUMBER

LT1185CT
LT1185IT

ELECTRICAL CHARACTERISTICS

Adjustable Version, V_{IN} = 7.4V, V_{OUT} = V_{REF}, I_{OUT} = 1mA, R_{LIM} = 4.02k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage (At FB Pin)				2.37		V
Reference Voltage Tolerance (At FB Pin) (Note 1)	$V_{IN} – V_{OUT}$ = 5V			0.3	±1	%
	1mA ≤ I_{OUT} ≤ 3A $V_{IN} – V_{OUT}$ = 1.2V to V_{IN} = 30V P ≤ 25W (Note 5), V_{OUT} = 5V $T_{MIN} ≤ T_J ≤ T_{MAX}$ (Note 8)	●		1	±2.5	%
Feedback Pin Bias Current		●		0.7	2	μA
Droput Voltage (Note 2)	I_{OUT} = 0.5A, V_{OUT} = 5V I_{OUT} = 3A, V_{OUT} = 5V			0.20 0.67	0.37 1.00	V V
Load Regulation (Note 6)	I_{OUT} = 5mA to 3A $V_{IN} – V_{OUT}$ = 1.5V to 10V, V_{OUT} = 5V			0.05	0.3	%
Line Regulation (Note 6)	$V_{IN} – V_{OUT}$ = 1V to 20V, V_{OUT} = 5V			0.002	0.01	%/V
Minimum Input Voltage	I_{OUT} = 1A (Note 3) I_{OUT} = 3A			4.0 4.3		V V
Internal Current Limit (See Graph for Guaranteed Curve) (Note 11)	1.5V ≤ $V_{IN} – V_{OUT}$ ≤ 10V		3.3	3.6	4.0	A
		●	3.1		4.2	A
	$V_{IN} – V_{OUT}$ = 15V	●	2.0	3.0	4.0	A
	$V_{IN} – V_{OUT}$ = 20V	●	1.0	1.7	2.6	A
	$V_{IN} – V_{OUT}$ = 30V	●	0.2	0.4	1.0	A

ELECTRICAL CHARACTERISTICS

Adjustable Version, V_{IN} = 7.4V, V_{OUT} = V_{REF}, I_{OUT} = 1mA, R_{LIM} = 4.02k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External Current Limit Programming Constant	$5k \le R_{LIM} \le 15k$, V_{OUT} = 1V (Note 10)	●		15k		A•Ω
External Current Limit Error	$1A \le I_{LIM} \le 3A$			0.02 I_{LIM}	0.06 I_{LIM} + 0.03	A
	$R_{LIM} = 15k \times A/I_{LIM}$	●		0.04 I_{LIM}	0.09 I_{LIM} + 0.05	A
Quiescent Supply Current	I_{OUT} = 5mV $4V \le V_{IN} \le 25V$ (Note 4)	●		2.5	3.5	mA
Supply Current Change with Load	$V_{IN} - V_{OUT} = V_{SAT}$ (Note 9)	●		25	40	mA/A
	$V_{IN} - V_{OUT} \ge 2V$	●		10	25	mA/A
REF Pin Shutoff Current		●	0.4	2	7	μA
Thermal Regulation (See Applications Information)	$V_{IN} - V_{OUT}$ = 10V I_{OUT} = 5mA to 2A			0.005	0.014	%/W
Reference Voltage Temperature Coefficient	(Note 7)			0.003	0.01	%/°C
Thermal Resistance Junction to Case	TO-3 Control Area				1	°C/W
	Power Transistor				3	°C/W
	TO-220 Control Area				1	°C/W
	Power Transistor				3	°C/W

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Reference voltage is guaranteed both at nominal conditions (no load, 25°C) and at worst case conditions of load, line, power and temperature. An intermediate value can be calculated by adding the effects of these variables in the actual application. See the Applications Information section of this data sheet.

Note 2: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \times I_{OUT}$. For load current less than 0.5A, see graph.

Note 3: "Minimum input voltage" is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 2. For output voltages below 4V, "minimum input voltage" specification may limit dropout voltage before transistor saturation limitation.

Note 4: Supply current is measured on the ground pin, and does not include load current, R_{LIM}, or output divider current.

Note 5: The 25W power level is guaranteed for an input-output voltage of 8.3V to 17V. At lower voltages the 3A limit applies, and at higher voltages the internal power limiting may restrict regulator power below 25W. See graphs.

Note 6: Line and load regulation are measured on a pulse basis with a pulse width of ≈2ms, to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See Application Section for details.

Note 7: Guaranteed by design and correlation to other tests, but not tested.

Note 8: T_{JMIN} = 0°C for the LT1185C, –40°C for LT1185I, and –55°C for the LT1185M. Power transistor area and control circuit area have different maximum junction temperatures. Control area limits are T_{JMAX} = 125°C for the LT1185C and LT1185I and 150°C for the LT1185M. Power area limits are 150°C for LT1185C and LT1185I and 175°C for LT1185M.

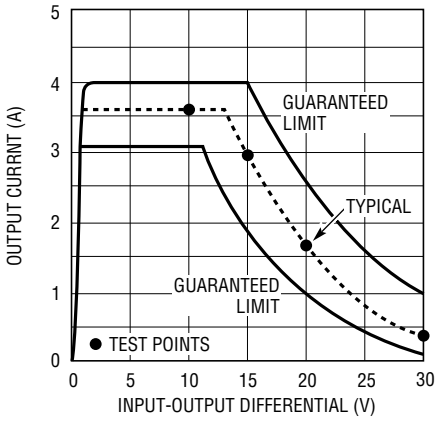
Note 9: V_{SAT} is the maximum specified dropout voltage; $0.25V + 0.25 \times I_{OUT}$.

Note 10: Current limit is programmed with a resistor from REF pin to GND pin. The value is $15k/I_{LIM}$.

Note 11: For $V_{IN} - V_{OUT}$ = 1.5V; V_{IN} = 5V, V_{OUT} = 3.5V. V_{OUT} = 1V for all other current limit tests.

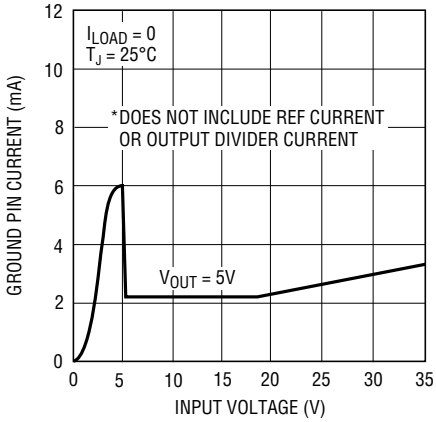
TYPICAL PERFORMANCE CHARACTERISTICS

Internal Current Limit



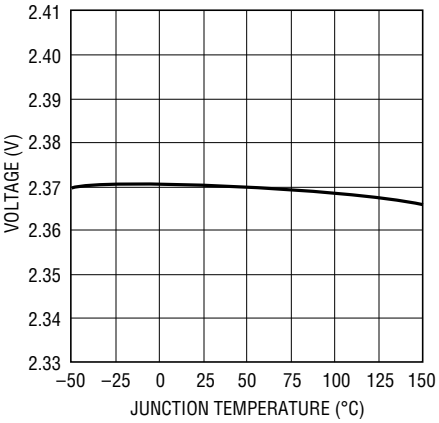
LT1185 • TPC01

Quiescent Ground Pin Current*



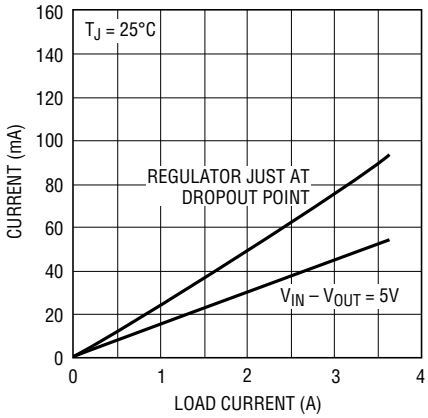
LT1185 • TPC02

Feedback Pin Voltage Temperature Drift



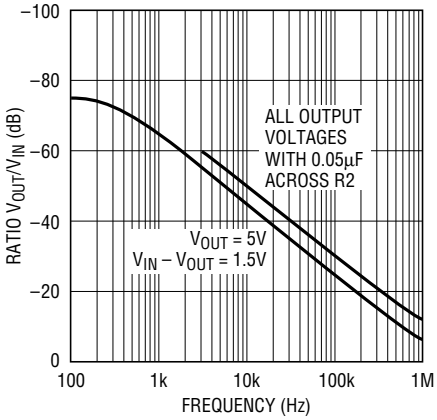
LT1185 • TPC03

Ground Pin Current



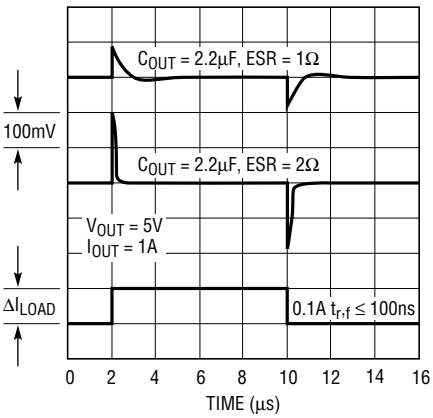
LT1185 • TPC04

Ripple Rejection vs Frequency



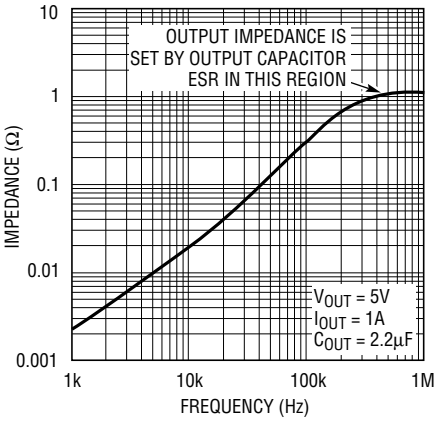
LT1185 • TPC05

Load Transient Response



LT1185 • TPC06

Output Impedance



LT1183 • TPC07

APPLICATIONS INFORMATION

Block Diagram

A simplified block diagram of the LT1185 is shown in Figure 1. A 2.37V bandgap reference is used to bias the input of the error amplifier A1, and the reference amplifier A2. A1 feeds a triple NPN pass transistor stage which has the two driver collectors tied to ground so that the main pass transistor can completely saturate. This topology normally has a problem with unlimited current in Q1 and Q2 when the input voltage is less than the minimum required to create a regulated output. The standard "fix" for this problem is to insert a resistor in series with Q1 and Q2 collectors, but this resistor must be low enough in value to supply full base current for Q3 under worst case conditions, resulting in very high supply current when the input voltage is low. To avoid this situation, the LT1185 uses an auxiliary emitter on Q3 to create a drive limiting feedback loop which automatically adjusts the drive to Q1 so that the base drive to Q3 is just enough to saturate Q3, but no more. Under saturation conditions, the auxiliary emitter is acting like a collector to shunt away the output current of A1. When the input voltage is high enough to keep Q3 out of saturation, the auxiliary emitter current drops to zero even when Q3 is conducting full load current.

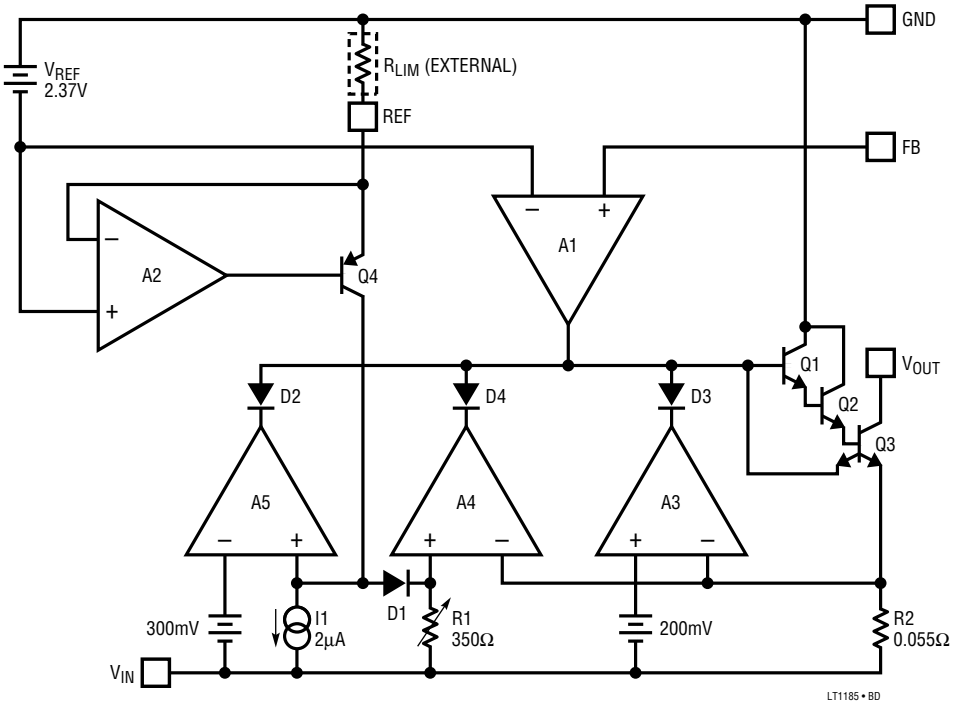


Figure 1. Block Diagram

APPLICATIONS INFORMATION

Amplifier A2 is used to generate an internal current through Q4 when an external resistor is connected from the REF pin to ground. This current is equal to 2.37V divided by R_{LIM}. It generates a current limit sense voltage across R1. The regulator will current limit via A4 when the voltage across R2 is equal to the voltage across R1. These two resistors essentially form a current "amplifier" with a gain of 350/0.055 = 6,360. Good temperature drift is inherent because R1 and R2 are made from the same diffusions. Their ratio, not absolute value, determines current limit. Initial accuracy is enhanced by trimming R1 slightly at wafer level. Current limit is equal to $15k\Omega/R_{LIM}$.

D1 and I1 are used to guarantee regulator shutdown when REF pin current drops below 2μA. A current less than 2μA through Q4 causes the + input of A5 to go low and shut down the regulator via D2.

A3 is an internal current limit amplifier which can override the external current limit. It provides "goof proof" protection for the pass transistor. Although not shown, A3 has a nonlinear foldback characteristic at input-output voltages above 12V to guarantee safe area protection for Q3. See the graph, Internal Current Limit in the Typical Performance Characteristics of this data sheet.

Setting Output Voltage

The LT1185 output voltage is set by two external resistors (see Figure 2). Internal reference voltage is trimmed to 2.37V so that a standard 1% 2.37k resistor (R1) can be used to set divider current at 1mA. R2 is then selected from:

$$R2 = \frac{(V_{OUT} - 2.37)\ R1}{V_{REF}}$$

for R1 = 2.37k and V_{REF} = 2.37V, this reduces to:

$$R2 = V_{OUT} - 2.37k$$

suggested values of 1% resistors are shown.

V_{OUT}	R2 WHEN R1 = 2.37k
5V	2.67k
5.2V	2.87k
6V	3.65k
12V	9.76k
15V	12.7k

Output Capacitor

The LT1185 has a collector output NPN pass transistor, which makes the open-loop output impedance much higher than an emitter follower. Open-loop gain is a direct function of load impedance, and causes a main-loop "pole" to be created by the output capacitor, in addition to an internal pole in the error amplifier. To ensure loop stability, the output capacitor must have an ESR (effective series resistance) which has an upper limit of 2Ω, and a lower limit of 0.2 divided by the capacitance in μF. A 2μF output capacitor, for instance, should have a maximum ESR of 2Ω, and a minimum of 0.2/2 = 0.1Ω. These values are easily encompassed by standard solid tantalum capacitors, but occasionally a solid tantalum unit will have abnormally high ESR, especially at very low temperatures. The suggested 2μF value shown in the circuit applications should be increased to 4.7μF for –40°C and –55°C designs if the 2μF units cannot be guaranteed to stay below 2Ω at these temperatures.

Although solid tantalum capacitors are suggested, other types can be used if they meet the ESR requirements. Standard aluminum electrolytic capacitors need to be upward of 25μF in general to hold 2Ω maximum ESR, especially at low temperatures. Ceramic, plastic film, and monolithic capacitors have a problem with ESR being too *low*. These types should have a 1Ω carbon resistor in series to guarantee loop stability.

The output capacitor should be located close to the regulator (≤3") to avoid excessive impedance due to lead inductance. A six inch lead length (2 × 3") will generate an extra 0.8Ω inductive reactance at 1MHz, and unity-gain frequency can be up to that value.

For remote sense applications, the capacitor should still be located close to the regulator. Additional capacitance can be added at the remote sense point, but the remote capacitor must be at least 2μF solid tantalum. It cannot be a low ESR type like ceramic or mylar unless a 0.5Ω to 1Ω carbon resistor is added in series with the capacitor. Logic boards with multiple low ESR bypass capacitors should have a solid tantalum unit added in parallel whose value is approximately five times the combined value of low ESR capacitors.

APPLICATIONS INFORMATION

Large output capacitors (electrolytic or solid tantalum) will not cause the LT1185 to oscillate, but they will cause a damped "ringing" at light load currents where the ESR of the capacitor is several orders of magnitude lower than the load resistance. This ringing only occurs as a result of transient load or line conditions and normally causes no problems because of its low amplitude (≤25mV).

Heat Sinking

The LT1185 will normally be used with a heat sink. The size of the heat sink is determined by load current, input and output voltage, ambient temperature, and the thermal resistance of the regulator, junction-to-case (θ_{JC}). The LT1185 has two separate values for θ_{JC}: one for the power transistor section, and a second, lower value for the control section. The reason for two values is that the power transistor is capable of operating at higher continuous temperature than the control circuitry. At low power levels, the two areas are at nearly the same temperature, and maximum temperature is limited by the control area. At high power levels, the power transistor will be at a significantly higher temperature than the control area and its maximum operating temperature will be the limiting factor.

To calculate heat sink requirements, you must solve a thermal resistance formula twice, one for the power transistor and one for the control area. The *lowest* value obtained for heat sink thermal resistance must be used. In these equations, two values for maximum junction temperature and junction-to-case thermal resistance are used, as given in Electrical Specifications.

$$\theta_{HS} = \frac{(T_{JMAX} - T_{AMAX})}{P} - \theta_{JC} - \theta_{CHS}.$$

θ_{HS} = Maximum heat sink thermal resistance.

θ_{JC} = LT1185 junction-to-case thermal resistance.

θ_{CHS} = Case-to-heat sink (interface) thermal resistance, including any insulating washers.

T_{JMAX} = LT1185 maximum operating junction temperature.

T_{AMAX} = Maximum ambient temperature in customers application.

$$P = \text{Device dissipaton} = (V_{IN} - V_{OUT})(I_{OUT}) + \frac{I_{OUT}}{40}(V_{IN}).$$

Example: A commercial version of the LT1185 in the TO-220 package is to be used with a maximum ambient temperature of 60°C. Output voltage is 5V at 2A. Input voltage can vary from 6V to 10V. Assume an interface resistance of 1°C/W.

First solve for control area, where the maximum junction temperature is 125°C for the TO-220 package, and θ_{JC} = 1°C/W:

$$P = (10V - 5V)(2A) + \frac{2A}{40}(10V) = 10.5W$$

$$\theta_{HS} = \frac{125°C - 60°C}{10.5W} - 1°C/W - 1°C/W = 4.2°C/W$$

Next, solve for power transistor limitation, with T_{JMAX} = 150°C, θ_{JC} = 3°C/W:

$$\theta_{HS} = \frac{150 - 60}{10.5} - 3 - 1 = 4.6°C/W$$

The lowest number must be used, so heat sink resistance must be less than 4.2°C/W.

Some heat sink data sheets show graphs of heat sink temperature rise vs power dissipation instead of listing a value for thermal resistance. The formula for θ_{HS} can be rearranged to solve for maximum heat sink temperature rise:

$$\Delta T_{HS} = T_{JMAX} - T_{AMAX} - P(\theta_{JC} + \theta_{CHS})$$

Using numbers from the previous example:

ΔT_{HS} = 125°C – 60 – 10.5(1 + 1) = 44°C control section

ΔT_{HS} = 150°C – 60 – 10.5(3 + 1) = 48°C power transistor

The smallest rise must be used, so heat sink temperature rise must be less than 44°C at a power level of 10.5W.

For board level applications, where heat sink size may be critical, one is often tempted to use a heat sink which barely meets the requirements. This is permissible *if* correct assumptions were made concerning maximum ambient temperature and power levels. One complicating

APPLICATIONS INFORMATION

factor is that local ambient temperature may be somewhat higher because of the point source of heat. The consequences of excess junction temperature include poor reliability, especially for plastic packages, and the possibility of thermal shutdown or degraded electrical characteristics. The final design should be checked *in situ* with a thermocouple attached to the regulator case under worst case conditions of high ambient, high input voltage, and full load.

What About Overloads?

IC regulators with thermal shutdown, like the LT1185, allow heat sink designs which concentrate on worst case "normal" conditions and ignore "fault" conditions. An output overload or short may force the regulator to exceed its maximum junction temperature rating, but thermal shutdown is designed to prevent regulator failure under these conditions. A word of caution however; thermal shutdown temperatures are typically 175°C in the control portion of the die and 180°C to 225°C in the power transistor section. Extended operation at these temperatures can cause permanent degradation of plastic encapsulation. Designs which may be subjected to extended periods of overload should either use the hermetic TO-3 package or increase heat sink size. Foldback current limiting can be implemented to minimize power levels under fault conditions.

External Current Limit

The LT1185 requires a resistor to set current limit. The value of this resistor is 15k divided by the desired current limit (in amps). The resistor for 2A current limit would be 15k/2A = 7.5k. Tolerance over temperature is ±10%, so current limit is normally set 15% above maximum load current. Foldback limiting can be employed if short-circuit current must be lower than full load current (see Typical Applications).

The LT1185 has internal current limiting which will override external current limit if power in the pass transistor is excessive. The internal limit is ≈3.6A with a foldback characteristic which is dependent on input-output voltage, not output voltage *per se* (see Typical Performace Characteristics).

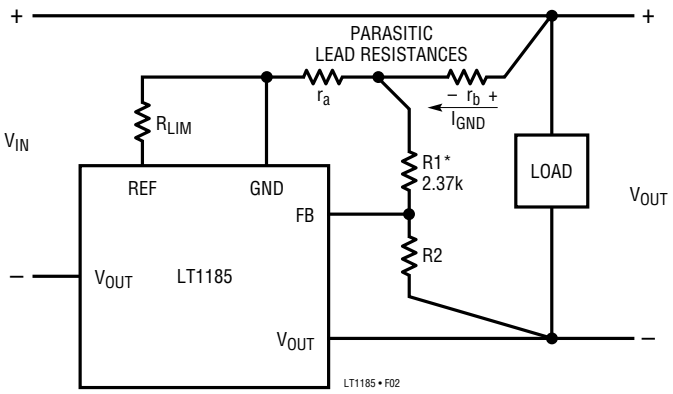
Ground Pin Current

Ground pin current for the LT1185 is approximately 2mA plus $I_{OUT}/40$. At I_{OUT} = 3A, ground pin current is typically 2mA + 3/40 = 77mA. Worst case guarantees on the ratio of I_{OUT} to ground pin current are contained in the Electrical Specifications.

Ground pin current can be important for two reasons. It adds to power dissipation in the regulator and it can affect load/line regulation if a long line is run from the ground pin to load ground. The additional power dissipation is found by multiplying ground pin current by input voltage. In a typical example, with V_{IN} = 8V, V_{OUT} = 5V and I_{OUT} = 2A, the LT1185 will dissipate (8V – 5V)(2A) = 6W in the pass transistor and (2A/40)(8V) = 0.4W in the internal drive circuitry. This is only a 1.5% efficiency loss, and a 6.7% increase in regulator power dissipation, but these values will increase at higher output voltages.

Ground pin current can affect regulation as shown in Figure 2. Parasitic resistance in the ground pin lead will create a voltage drop which *increases* output voltage as load current is increased. Similarly, output voltage can *decrease* as input voltage increases because the "$I_{OUT}/40$" component of ground pin current drops significantly at higher input-output differentials. These effects are small enough to be ignored for local regulation applications, but for remote sense applications, they may need to be considered. Ground lead resistance of 0.4Ω would cause an output voltage error of up to (3A/40)(0.4Ω) = 30mV, or 0.6% at V_{OUT} = 5V. Note that if the sense leads are connected as shown in Figure 2, with $r_a \approx 0\Omega$, this error is a fixed number of millivolts, and does not increase as a function of DC output voltage.

APPLICATIONS INFORMATION



*R1 SHOULD BE CONNECTED DIRECTLY TO GROUND LEAD, NOT TO THE LOAD, SO THAT $r_a \approx 0\Omega$. THIS LIMITS THE OUTPUT VOLTAGE ERROR TO $(I_{GND})(r_b)$. ERRORS CREATED BY r_a ARE MULTIPLIED BY (1 + R2/R1). NOTE THAT V_{OUT} *INCREASES* WITH INCREASING GROUND PIN CURRENT. R2 SHOULD BE CONNECTED DIRECTLY TO LOAD FOR REMOTE SENSING.

Figure 2. Proper Connection of Positive Sense Lead

Shutdown Techniques

The LT1185 can be shut down by open-circuiting the REF pin. The current flowing into this pin must be less than 0.4μA to guarantee shutdown. Figure 3 details several ways to create the "open" condition, with various logic levels. For variations on these schemes, simply remember that the voltage on the REF pin is 2.4V negative with respect to the ground pin.

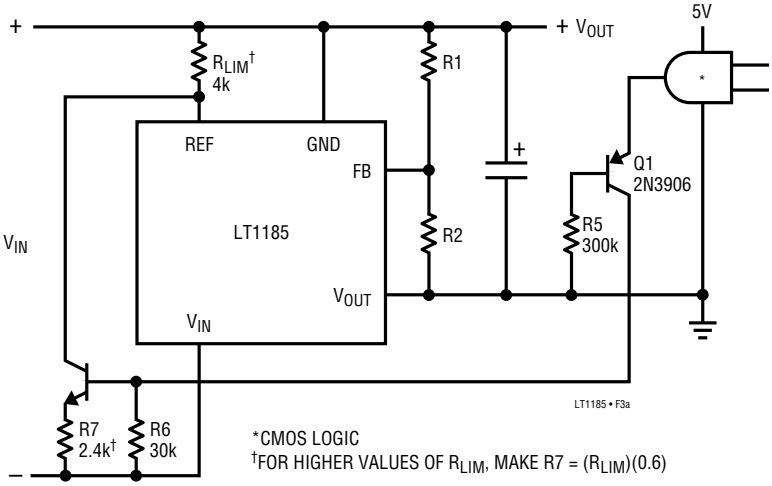
Output Overshoot

Very high input voltage slew rate during start-up may cause the LT1185 output to overshoot. Up to 20% overshoot could occur with input voltage ramp-up rate exceeding 1V/μs. This condition cannot occur with normal 50Hz to 400Hz rectified AC inputs because parasitic resistance and inductance will limit rate of rise even if the power switch is closed at the peak of the AC line voltage. This assumes that the switch is in the AC portion of the circuit. If instead, a switch is placed directly in the regulator input so that a large filter capacitor is precharged, fast input slew rates will occur on switch closure. The output of the regulator will slew at a rate set by current limit and output capacitor size; $dVdt = I_{LIM}/C_{OUT}$. With $I_{LIM} = 3.6A$ and $C_{OUT} = 2.2\mu F$, the output will slew at 1.6V/μs and overshoot can occur. This overshoot can be reduced to a few hundred millivolts or less by increasing the output capacitor to 10μF and/or reducing current limit so that output slew rate is held below 0.5V/μs.

A second possibility for creating output overshoot is recovery from an output short. Again, the output slews at a rate set by current limit and output capacitance. To avoid overshoot, the ratio I_{LIM}/C_{OUT} should be less than 0.5×10^6. Remember that load capacitance can be added to C_{OUT} for this calculation. Many loads will have multiple supply bypass capacitors that total more than C_{OUT}.

APPLICATIONS INFORMATION

5V Logic, Positive Regulated Output



5V Logic, Negative Regulated Output

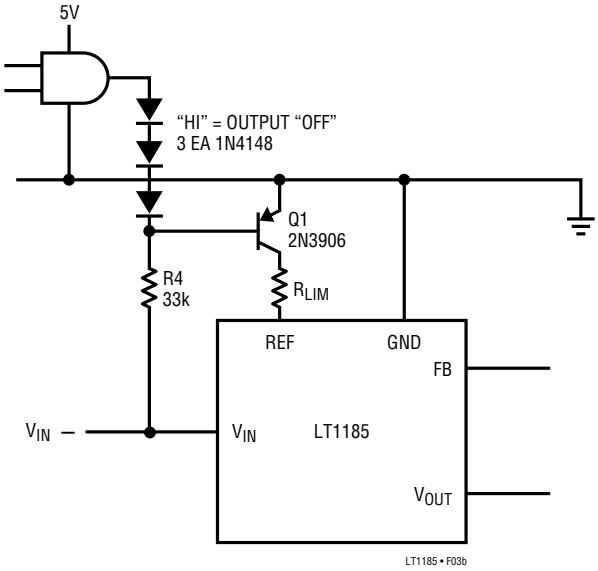


Figure 3. Shutdown Techniques

APPLICATIONS INFORMATION

Thermal Regulation

IC regulators have a regulation term not found in discrete designs because the power transistor is thermally coupled to the reference. This creates a shift in the output voltage which is proportional to power dissipation in the regulator.

$$\Delta V_{OUT} = P(K1 + K2\ \theta_{JA})$$
$$= (I_{OUT})(V_{IN} - V_{OUT})(K1 + K2\ \theta_{JA})$$

K1 and K2 are constants. K1 is a fast time constant effect caused by die temperature *gradients* which are established within 50ms of a power change. K1 is specified on the data sheet as thermal regulation, in percent per watt.

K2 is a long time constant term caused by the temperature drift of the regulator reference voltage. It is also specified, but in percent per degree centigrade. It must be multiplied by overall thermal resistance, junction-to-ambient, θ_{JA}.

As an example, assume a 5V regulator with an input voltage of 8V, load current of 2A, and a total thermal resistance of 4°C/W, including junction-to-case, (use control area specification), interface, and heat sink resistance. K1 and K2, respectively, from the data sheet are 0.014%/W and 0.01%/°C.

$$\Delta V_{OUT} = (2A)(8V - 5V)(0.014 + 0.01 \times 4)$$
$$= 0.32\%$$

This shift in output voltage could be in either direction because K1 and K2 can be either positive or negative.

Thermal regulation is already included in the worst case reference specification.

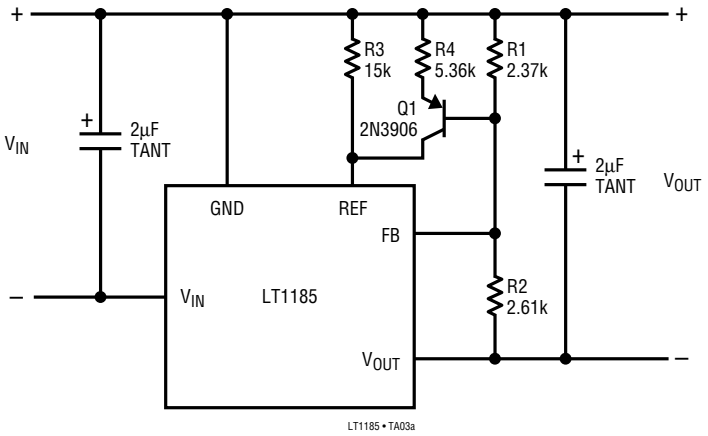
Output Voltage Reversal

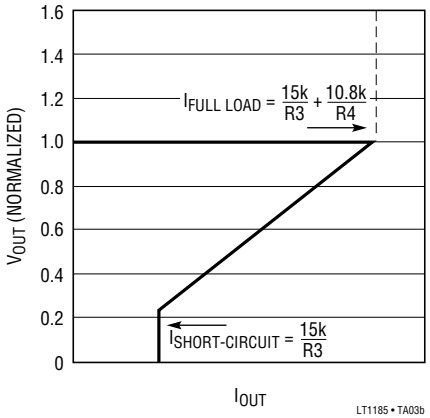
Some IC regulators suffer from a latch-up state when their output is forced to a reverse voltage of as little as one diode drop. The latch-up state can be triggered without a fault condition when the load is connected to an opposite polarity supply instead of to ground. If the second supply is turned on first, it will pull the output of the first supply to a reverse voltage through the load. The first supply may then latch off when turned on. This problem is particularly annoying because the diode clamps which should always be used to protect against polarity reversal do not usually stop the latch-up problem.

The LT1185 is designed to allow output reverse polarity of several volts without damage or latch-up, so that a simple diode clamp can be used.

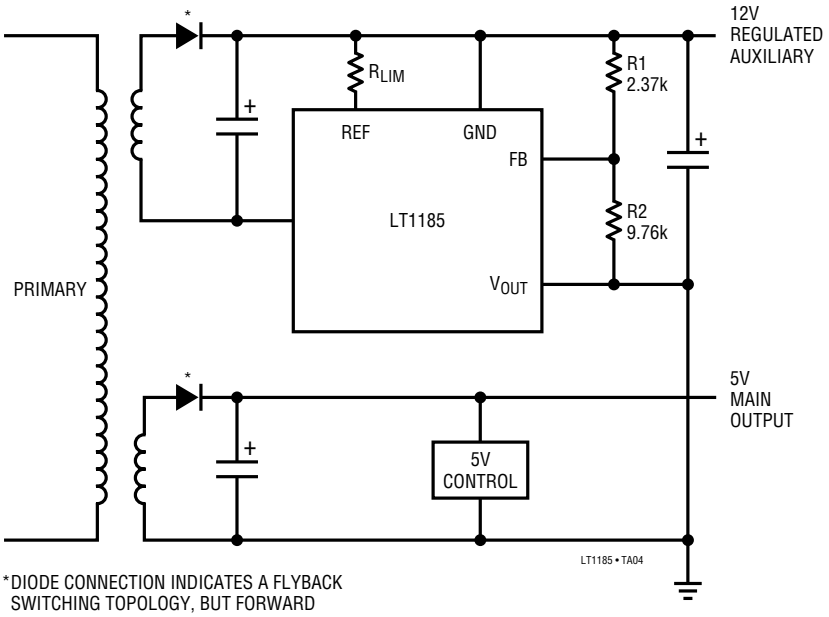
TYPICAL APPLICATIONS

Foldback Current Limiting





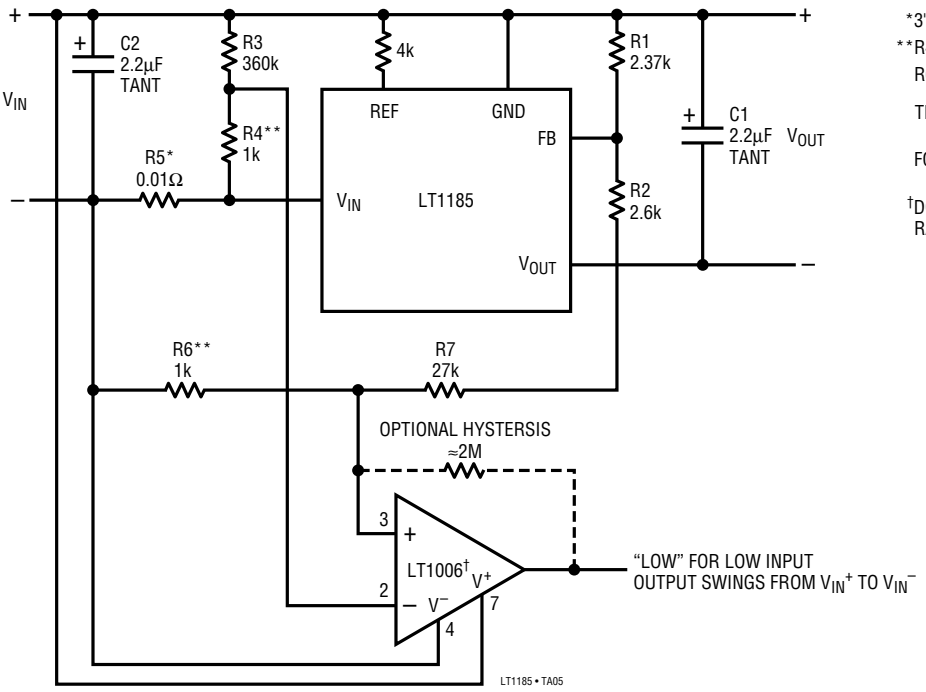
Auxiliary + 12V Low Dropout Regulator for Switching Supply



*DIODE CONNECTION INDICATES A FLYBACK SWITCHING TOPOLOGY, BUT FORWARD CONVERTERS MAY ALSO BE USED.

TYPICAL APPLICATIONS

Low Input Voltage Monitor Tracks Dropout Characteristics



*3" #26 WIRE

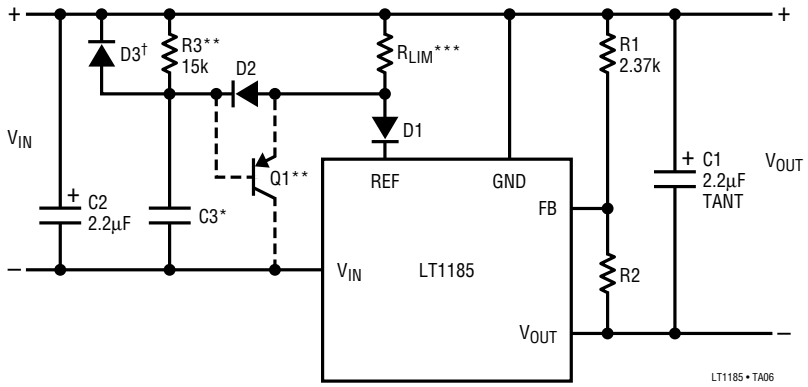
**R4 DETERMINES TRIP POINT AT $I_{OUT} = 0$.
R6 DETERMINES INCREASE OF TRIP POINT AS I_{OUT} INCREASES.

TRIP POINT FOR $V_{IN} = V_{OUT}\left(1 + \frac{R4 \times R7}{R3 \times R6}\right) + I_{OUT}\frac{R5 \times R7}{R6}$

FOR VALUES SHOWN, TRIP POINT FOR V_{IN} IS:
V_{OUT} + 0.37V AT I_{OUT} = 0 AND V_{OUT} = 1.18V AT I_{OUT} = 3A

†DO NOT SUBSTITUTE. OP AMP MUST HAVE COMMON-MODE RANGE EQUAL TO NEGATIVE SUPPLY.

Time Delayed Start-Up



ALL DIODES 1N4148

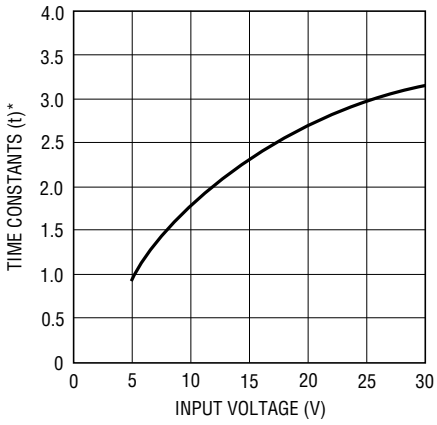
*SEE CHART FOR DELAY TIME VERSUS (C3)(R3//R_{LIM}) PRODUCT.

**FOR LONG DELAY TIMES, REPLACE D2 WITH 2N3906 TRANSISTOR AND USE R3 ONLY FOR CALCULATING DELAY TIME. R3 CAN INCREASE TO 100k.

***I_{LIM} IS ≈11k/R_{LIM}, INSTEAD OF 15k, BECAUSE OF VOLTAGE DROP IN D1. TEMPERATURE COEFFICIENT OF I_{LIM} WILL BE ≈0.11%/°C, SO ADEQUATE MARGIN MUST BE ALLOWED FOR COLD OPERATION.

†D3 PROVIDES FAST RESET OF TIMING. INPUT MUST DROP TO A LOW VALUE TO RESET TIMING.

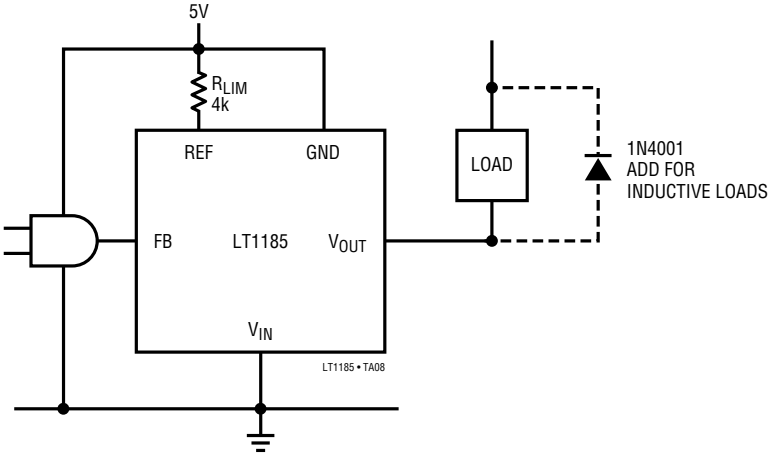
Delay Time



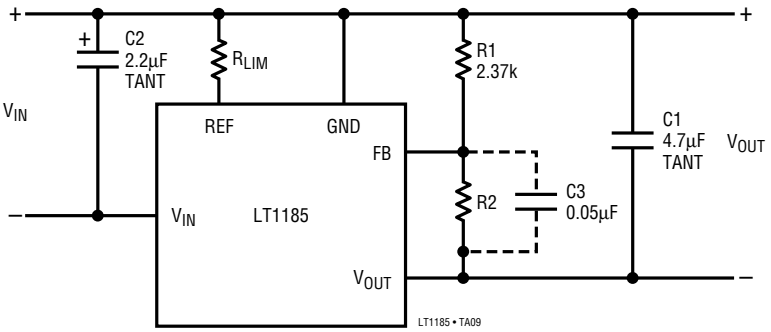
$$*t = (R3//R_{LIM})(C3) = \left(\frac{R3 \times R_{LIM}}{R3 + R_{LIM}}\right)(C3)$$

TYPICAL APPLICATIONS

Logic Controlled 3A Low-Side Switch with Fault Protection

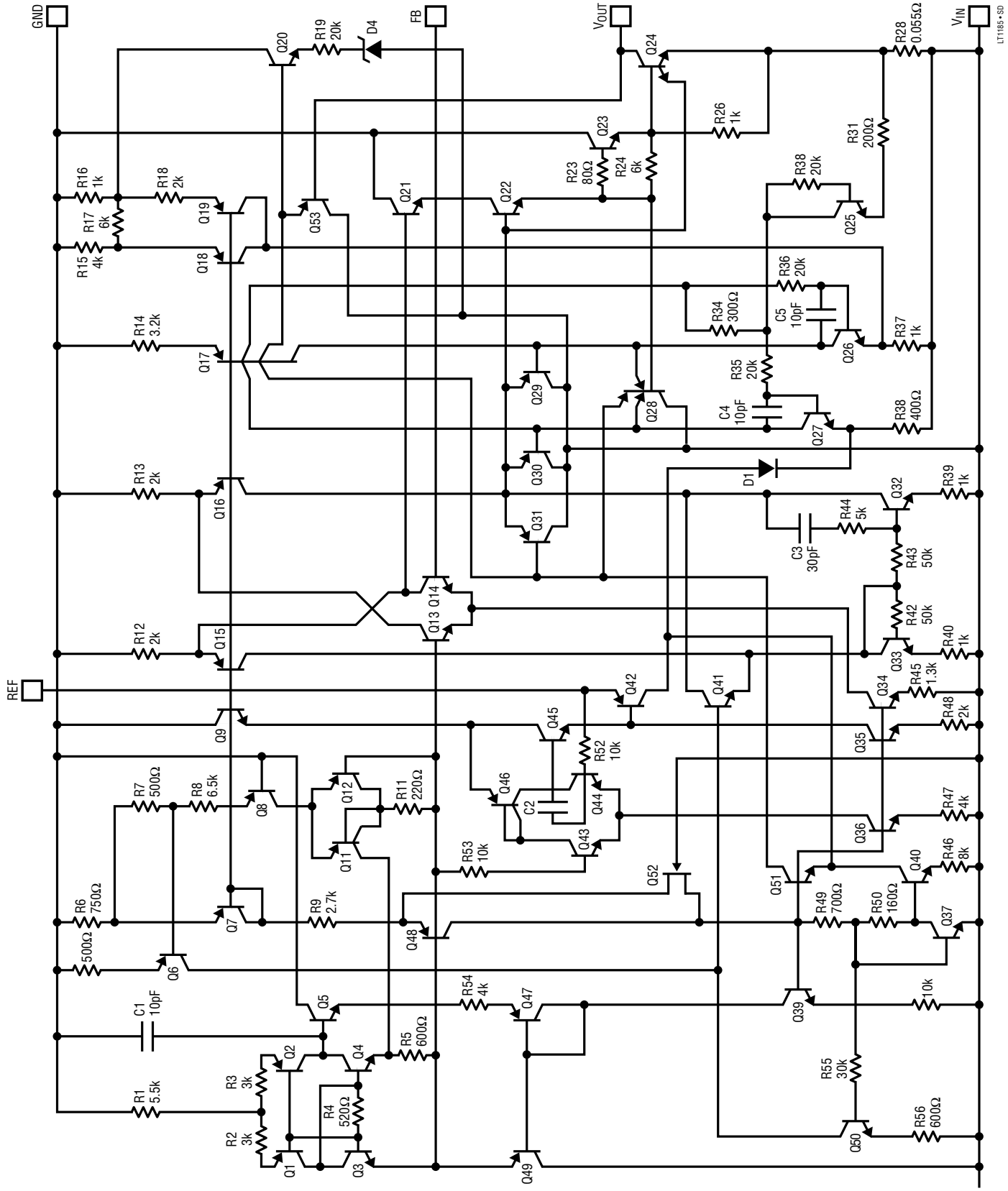


Improved High Frequency Ripple Rejection



NOTE: C3 IMPOVES HIGH FREQUENCY RIPPLE REJECTION BY 6dB AT V_{OUT} = 5V, AND BY 14dB AT V_{OUT} = 12V. C1 IS INCREASED TO 4.7µF TO ENSURE GOOD STABILTITY WHEN C3 IS USED.

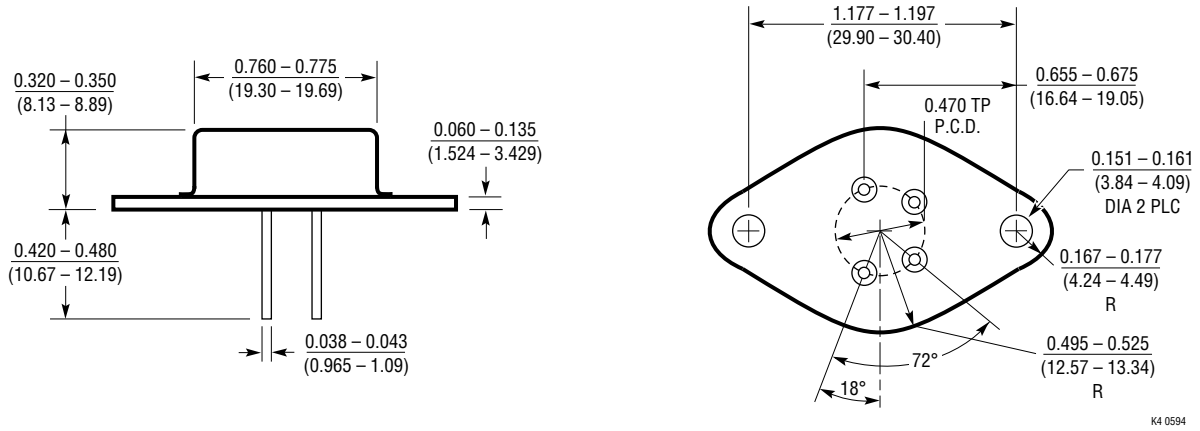
SCHEMATIC DIAGRAM



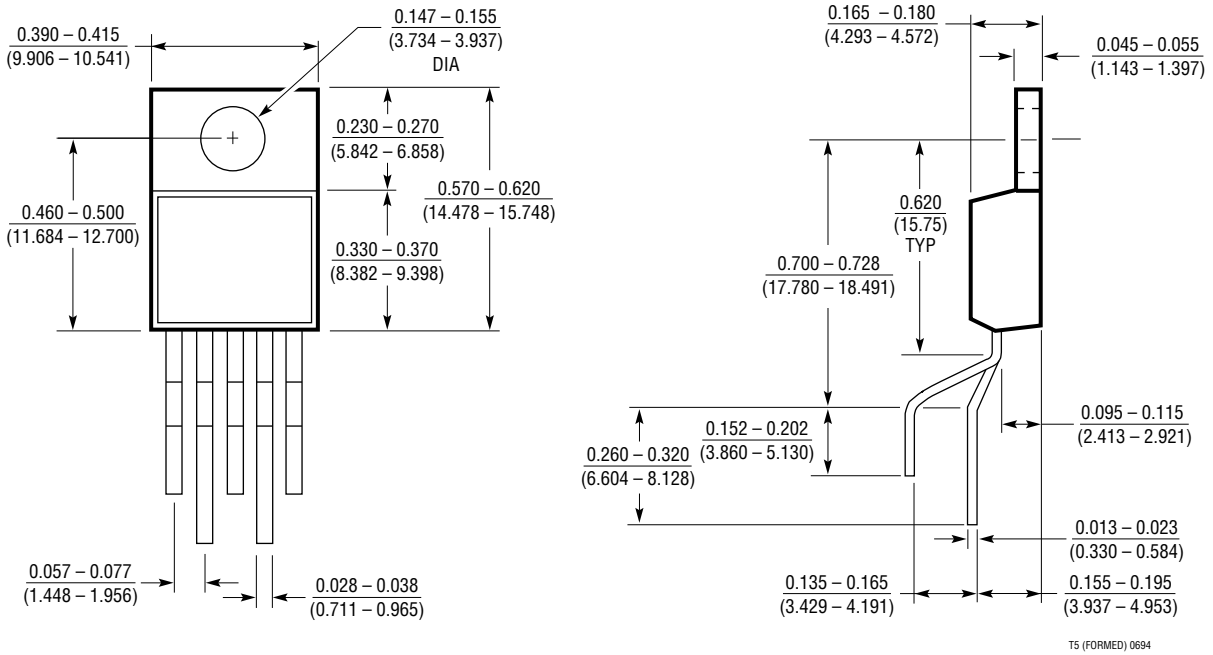
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package
4-Lead TO-3 Metal Can



T Package
5-Lead TO-220 (Formed)



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MIC29150/29300/29500/29750 Series

High-Current Low-Dropout Regulators

General Description

The MIC29150/29300/29500/29750 are high current, high accuracy, low-dropout voltage regulators. Using Micrel's proprietary Super ßeta PNP™ process with a PNP pass element, these regulators feature 300mV to 370mV (full load) dropout voltages and very low ground current. Designed for high current loads, these devices also find applications in lower current, extremely low dropout-critical systems, where their tiny dropout voltage and ground current values are important attributes.

The MIC29150/29300/29500/29750 are fully protected against overcurrent faults, reversed input polarity, reversed lead insertion, overtemperature operation, and positive and negative transient voltage spikes. Five pin fixed voltage versions feature logic level ON/OFF control and an error flag which signals whenever the output falls out of regulation. Flagged states include low input voltage (dropout), output current limit, overtemperature shutdown, and extremely high voltage spikes on the input.

On the MIC29xx1 and MIC29xx2, the ENABLE pin may be tied to V_{IN} if it is not required for ON/OFF control. The MIC29150/29300/29500 are available in 3- and 5-pin TO-220 and surface mount TO-263 packages. The MIC29750 7.5A regulators are available in 3- and 5-pin TO-247 packages.

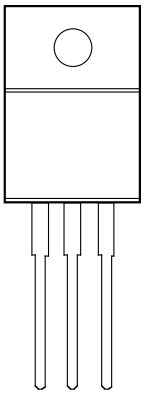
Features

- High Current Capability
  MIC29150/29151/29152/29153 ..... 1.5A
  MIC29300/29301/29302/29303 ..... 3A
  MIC29500/29501/29502/29503 ..... 5A
  MIC29750/29751/29752/29753 ..... 7.5A
- Low-Dropout Voltage ..... 350mV at Full Load
- Low Ground Current
- Accurate 1% Guaranteed Tolerance
- Extremely Fast Transient Response
- Reverse-battery and “Load Dump” Protection
- Zero-Current Shutdown Mode (5-Pin versions)
- Error Flag Signals Output Out-of-Regulation (5-Pin versions)
- Also Characterized For Smaller Loads With Industry-Leading Performance Specifications
- Fixed Voltage and Adjustable Versions

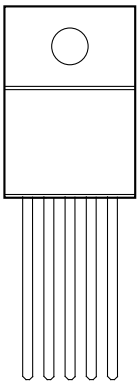
Applications

- Battery Powered Equipment
- High-Efficiency "Green" Computer Systems
- Automotive Electronics
- High-Efficiency Linear Power Supplies
- High-Efficiency Post-Regulator For Switching Supply

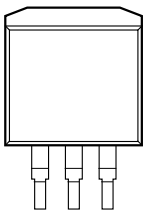
Pin Configuration



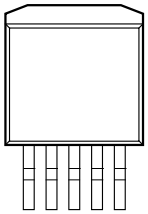
MIC29150/29300/ 29500BT and MIC29750BWT



MIC29151/29152/29153BT
MIC29301/29302/29303BT
MIC29501/29502/29503BT
MIC29751/29752/29753BWT



MIC29150/29300BU



MIC29151/29152/29153BU
MIC29301/29302/29303BU

Pinout **On all devices, the Tab is grounded.**

MIC29150/29300/29500/29750 Three Terminal Devices:

Pin 1 = Input, 2 = Ground, 3 = Output

MIC29151/29301/29501/29751 Five Terminal Fixed Voltage Devices:

Pin 1 = Enable, 2 = Input, 3 = Ground, 4 = Output, 5 = Flag

MIC29152/29302/29502/29752 Adjustable with ON/OFF Control

Pin 1 = Enable, 2 = Input, 3 = Ground, 4 = Output, 5 = Adjust

MIC29153/29303/29503/29753 Adjustable with Flag

Pin 1 = Flag, 2 = Input, 3 = Ground, 4 = Output, 5 = Adjust

Ordering Information

Part Number	Temp. Range*	Volts	Current	Package
MIC29150-3.3BT	–40 to +125°C	3.3	1.5A	TO-220
MIC29150-5.0BT	–40 to +125°C	5.0	1.5A	TO-220
MIC29150-12BT	–40 to +125°C	12	1.5A	TO-220
MIC29150-3.3BU	–40 to +125°C	3.3	1.5A	TO-263
MIC29150-5.0BU	–40 to +125°C	5.0	1.5A	TO-263
MIC29150-12BU	–40 to +125°C	12	1.5A	TO-263
MIC29151-3.3BT	–40 to +125°C	3.3	1.5A	TO-220-5
MIC29151-5.0BT	–40 to +125°C	5.0	1.5A	TO-220-5
MIC29151-12BT	–40 to +125°C	12	1.5A	TO-220-5
MIC29151-3.3BU	–40 to +125°C	3.3	1.5A	TO-263-5
MIC29151-5.0BU	–40 to +125°C	5.0	1.5A	TO-263-5
MIC29151-12BU	–40 to +125°C	12	1.5A	TO-263-5
MIC29152BT	–40 to +125°C	Adj	1.5A	TO-220-5
MIC29152BU	–40 to +125°C	Adj	1.5A	TO-263-5
MIC29153BT	–40 to +125°C	Adj	1.5A	TO-220-5
MIC29153BU	–40 to +125°C	Adj	1.5A	TO-263-5
MIC29300-3.3BT	–40 to +125°C	3.3	3.0A	TO-220
MIC29300-5.0BT	–40 to +125°C	5.0	3.0A	TO-220
MIC29300-12BT	–40 to +125°C	12	3.0A	TO-220
MIC29300-3.3BU	–40 to +125°C	3.3	3.0A	TO-263
MIC29300-5.0BU	–40 to +125°C	5.0	3.0A	TO-263
MIC29300-12BU	–40 to +125°C	12	3.0A	TO-263
MIC29301-3.3BT	–40 to +125°C	3.3	3.0A	TO-220-5
MIC29301-5.0BT	–40 to +125°C	5.0	3.0A	TO-220-5
MIC29301-12BT	–40 to +125°C	12	3.0A	TO-220-5
MIC29301-3.3BU	–40 to +125°C	3.3	3.0A	TO-263-5
MIC29301-5.0BU	–40 to +125°C	5.0	3.0A	TO-263-5
MIC29301-12BU	–40 to +125°C	12	3.0A	TO-263-5
MIC29302BT	–40 to +125°C	Adj	3.0A	TO-220-5
MIC29302BU	–40 to +125°C	Adj	3.0A	TO-263-5
MIC29303BT	–40 to +125°C	Adj	3.0A	TO-220-5
MIC29303BU	–40 to +125°C	Adj	3.0A	TO-263-5

Part Number	Temp. Range*	Volts	Current	Package
MIC29500-3.3BT	–40 to +125°C	3.3	5.0A	TO-220
MIC29500-5.0BT	–40 to +125°C	5.0	5.0A	TO-220
MIC29501-3.3BT	–40 to +125°C	3.3	5.0A	TO-220-5
MIC29501-5.0BT	–40 to +125°C	5.0	5.0A	TO-220-5
MIC29501-3.3BU	–40 to +125°C	3.3	5.0A	TO-263-5
MIC29501-5.0BU	–40 to +125°C	5.0	5.0A	TO-263-5
MIC29502BT	–40 to +125°C	Adj	5.0A	TO-220-5
MIC29502BU	–40 to +125°C	Adj	5.0A	TO-263-5
MIC29503BT	–40 to +125°C	Adj	5.0A	TO-220-5
MIC29503BU	–40 to +125°C	Adj	5.0A	TO-263-5
MIC29750-3.3BWT	–40 to +125°C	3.3	7.5A	TO-247-3
MIC29750-5.0BWT	–40 to +125°C	5.0	7.5A	TO-247-3
MIC29751-3.3BWT	–40 to +125°C	3.3	7.5A	TO-247-5
MIC29751-5.0BWT	–40 to +125°C	5.0	7.5A	TO-247-5
MIC29752BWT	–40 to +125°C	Adj	7.5A	TO-247-5

* Junction Temperature

MIC29xx0 versions are 3-terminal fixed voltage devices. MIC29xx1 are fixed voltage devices with ENABLE and ERROR flag. MIC29xx2 are adjustable regulators with ENABLE control. MIC29xx3 are adjustables with an ERROR flag.

Absolute Maximum Ratings

Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 5 seconds) ..... 260°C
Storage Temperature Range ..... –65°C to +150°C
Input Supply Voltage (Note 1) ..... –20V to +60V

Operating Ratings

Operating Junction Temperature ..... –40°C to +125°C
Maximum Operating Input Voltage 26V
TO-220 θ_{JC} ..... 2°C/W
TO-263 θ_{JC} ..... 2°C/W
TO-247 θ_{JC} ..... 1.5°C/W

Electrical Characteristics

All measurements at T_J = 25°C unless otherwise noted. **Bold** values are guaranteed across the operating temperature range. Adjustable versions aree programmed to 5.0V.

Parameter	Condition	Min	Typ	Max	Units
Output Voltage	I_O = 10mA	–1		1	%
	10mA ≤ I_O ≤ I_{FL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 26V (Note 2)	**–2**		**2**	%
Line Regulation	I_O = 10mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 26V		0.06	0.5	%
Load Regulation	V_{IN} = V_{OUT} + 5V, 10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ (Note 2, 6)		0.2	1	%
$\frac{\Delta V_O}{\Delta T}$	Output Voltage (Note 6) Temperature Coef.		**20**	**100**	ppm/°C
Dropout Voltage	ΔV_{OUT} = – 1%, (Note 3) MIC29150 I_O = 100mA I_O = 750mA I_O = 1.5A MIC29300 I_O = 100mA I_O = 1.5A I_O = 3A MIC29500 I_O = 250mA I_O = 2.5A I_O = 5A MIC29750 I_O = 250mA I_O = 4A I_O = 7.5A		 80 220 350 80 250 370 125 250 370 80 270 425	 **200** **600** **175** **600** **250** **600** **200** **600**	 mV
Ground Current	MIC29150 I_O = 750mA, V_{IN} = V_{OUT} + 1V I_O = 1.5A MIC29300 I_O = 1.5A, V_{IN} = V_{OUT} + 1V I_O = 3A MIC29500 I_O = 2.5A, V_{IN} = V_{OUT} + 1V I_O = 5A MIC29750 I_O = 4A, V_{IN} = V_{OUT} + 1V I_O = 7.5A		8 22 10 37 15 70 35 120	**20** **35** **50** **75** 	mA mA mA mA
I_{GNDDO} Ground Pin Current at Dropout	V_{IN} = 0.5V less than specified V_{OUT}. I_{OUT} = 10mA MIC29150 MIC29300 MIC29500 MIC29750		 0.9 1.7 2.1 3.1		 mA mA mA mA
Current Limit	MIC29150 V_{OUT} = 0V (Note 4) MIC29300 V_{OUT} = 0V (Note 4) MIC29500 V_{OUT} = 0V (Note 4) MIC29750 V_{OUT} = 0V (Note 4)		2.1 4.5 7.5 9.5	**3.5** **5.0** **10.0** **15**	A A A A
e_n, Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 10µF C_L = 33µF		400 260		µV RMS

Electrical Characteristics (Continued)

Reference **MIC29xx2/MIC29xx3**

Parameter	Conditions	Min	Typical	Max	Units
Reference Voltage		1.228 **1.215**	1.240	1.252 **1.265**	V V max
Reference Voltage	(Note 8)	**1.203**		**1.277**	V
Adjust Pin Bias Current			40	80 **120**	nA
Reference Voltage Temperature Coefficient	(Note 7)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C
Flag Output (Error Comparator) MIC29xx1/29xx3					
Output Leakage Current	V_{OH} = 26V		0.01	1.00 **2.00**	µA
Output Low Voltage	Device set for 5V. V_{IN} = 4.5V I_{OL} = 250µA		220	300 **400**	mV
Upper Threshold Voltage	Device set for 5V (Note 9)	40 **25**	60		mV
Lower Threshold Voltage	Device set for 5V (Note 9)		75	95 **140**	mV
Hysteresis	Device set for 5V (Note 9)		15		mV
ENABLE Input	**MIC29xx1/MIC29xx2**				
Input Logic Voltage Low (OFF) High (ON)		 **2.4**		 **0.8**	V
Enable Pin Input Current	V_{EN} = 26V		100	600 **750**	µA
	V_{EN} =0.8V			1 **2**	µA
Regulator Output Current in Shutdown	(Note 10)		10	 **500**	µA

Notes

Note 1: Maximum positive supply voltage of 60V must be of limited duration (<100msec) and duty cycle (≤1%). The maximum continuous supply voltage is 26V.

Note 2: Full Load current (I_{FL}) is defined as 1.5A for the MIC29150, 3A for the MIC29300, 5A for the MIC29500, and 7.5A for the MIC29750 families.

Note 3: Dropout voltage is defined as the input-to-output differential when the output voltage drops to 99% of its nominal value with V_{OUT} + 1V applied to V_{IN}

Note 4: $V_{IN} = V_{OUT\ (nominal)} + 1V$. For example, use V_{IN} = 4.3V for a 3.3V regulator or use 6V for a 5V regulator. Employ pulse-testing procedures to minimize temperature rise.

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 6: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

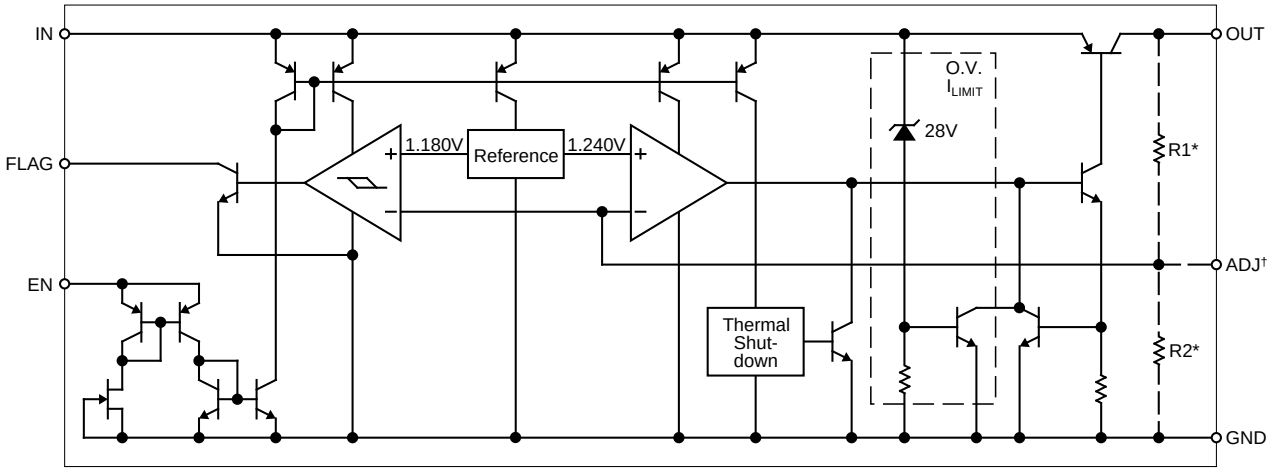
Note 8: $V_{REF} \le V_{OUT} \le (V_{IN} - 1\ V)$, $2.3V \le V_{IN} \le 26V$, $10mA < I_L \le I_{FL}$, $T_J \le T_{J\ MAX}$.

Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.240 V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.7% guaranteed.

Note 10: $V_{EN} \le 0.8V$ and $V_{IN} \le 26V$, $V_{OUT} = 0$.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Block Diagram



* Feedback network in fixed versions only
† Adjustable version only

Typical Applications

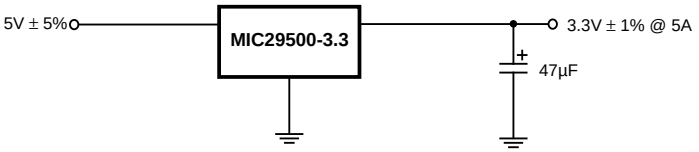
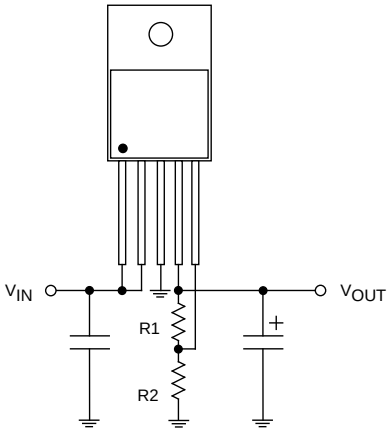


Figure 1. Fixed output voltage.

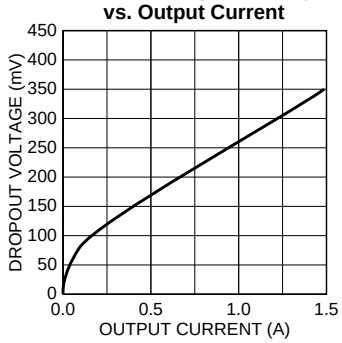


$V_{OUT} = 1.240V \times [1 + (R1 / R2)]$

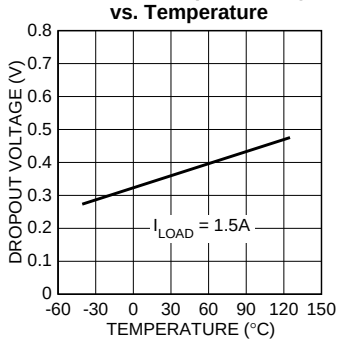
Figure 2. Adjustable output voltage configuration. For best results, the total series resistance should be small enough to pass the minimum regulator load current.

Typical Characteristics MIC2915x

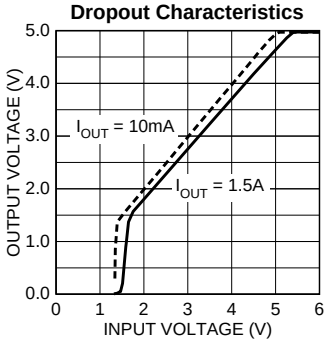
MIC2915x Dropout Voltage vs. Output Current



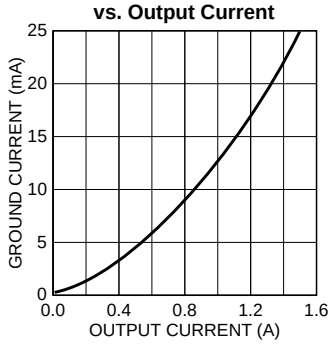
MIC2915x Dropout Voltage vs. Temperature



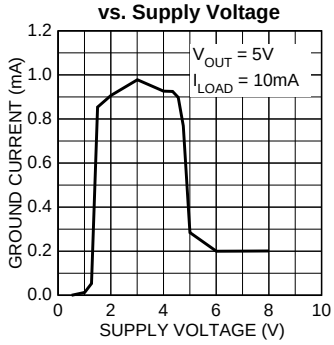
MIC29150-3.3 Dropout Characteristics



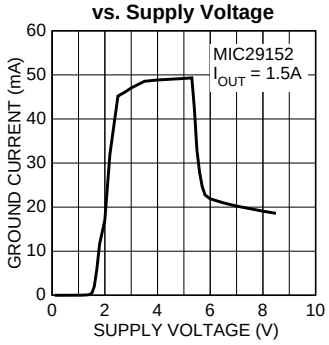
MIC2915x Ground Current vs. Output Current



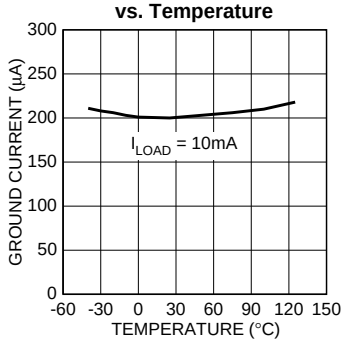
MIC2915x Ground Current vs. Supply Voltage



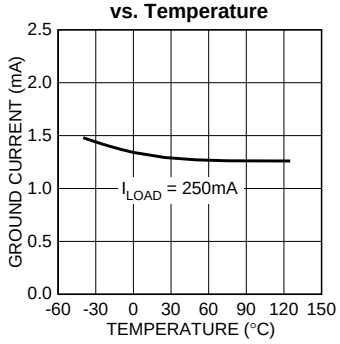
MIC2915x Ground Current vs. Supply Voltage



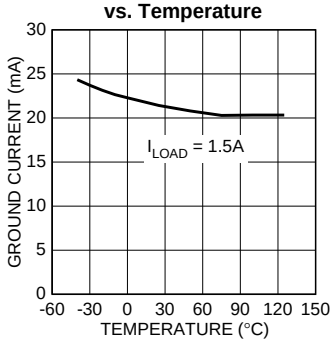
MIC2915x Ground Current vs. Temperature



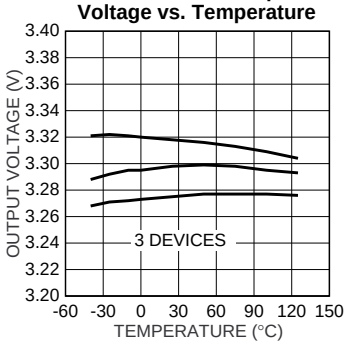
MIC2915x Ground Current vs. Temperature



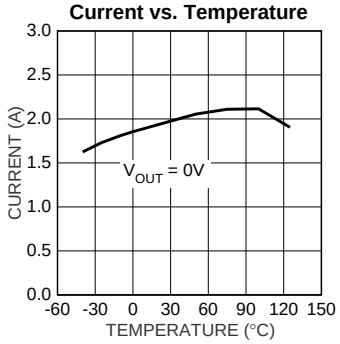
MIC2915x Ground Current vs. Temperature



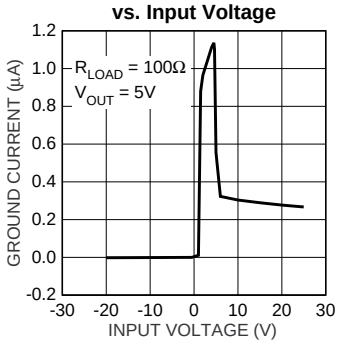
MIC29150-3.3 Output Voltage vs. Temperature



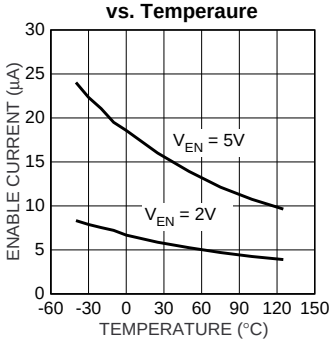
MIC29150-3.3 Short Circuit Current vs. Temperature



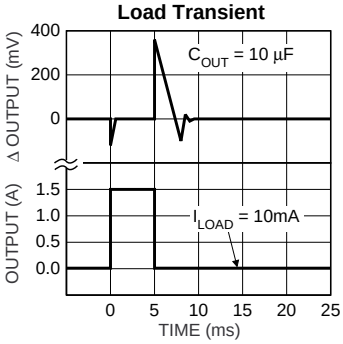
MIC2915x Ground Current vs. Input Voltage



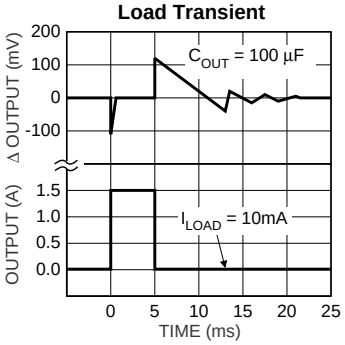
MIC29151-xx/2 Enable Current vs. Temperaure



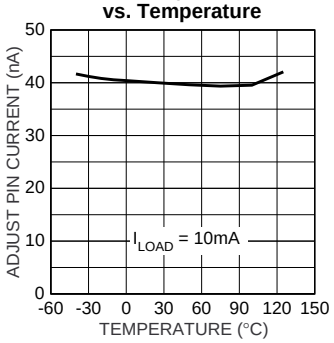
MIC2915x Load Transient



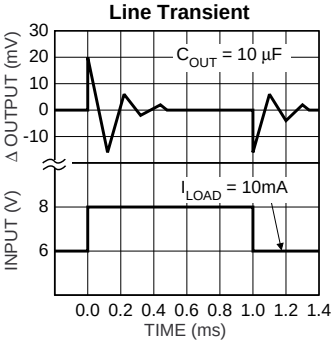
MIC2915x Load Transient



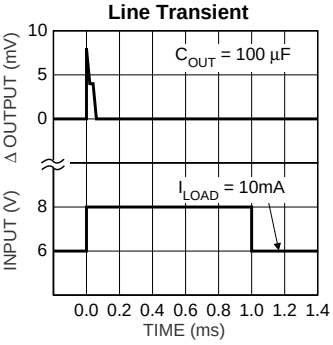
MIC29152/3 Adjust Pin Current vs. Temperature



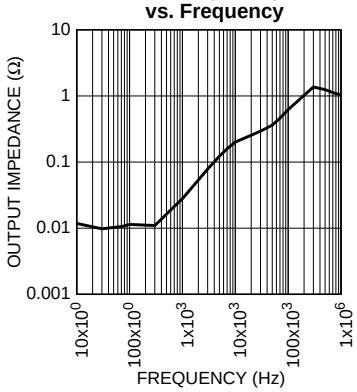
MIC2915x Line Transient



MIC2915x Line Transient

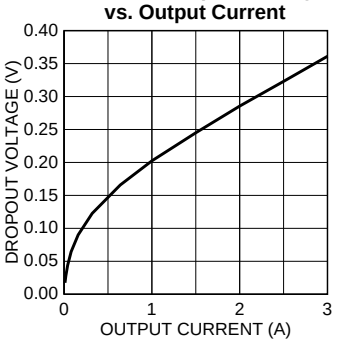


MIC2915x Output Impedance vs. Frequency

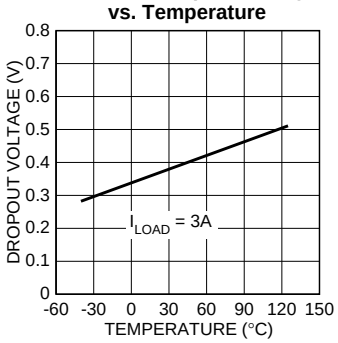


Typical Characteristics MIC2930x

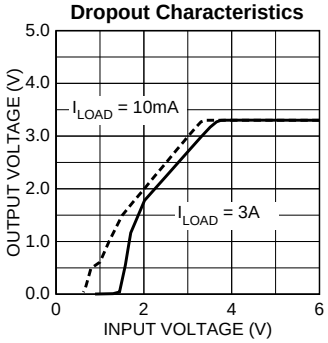
MIC2930x Dropout Voltage vs. Output Current



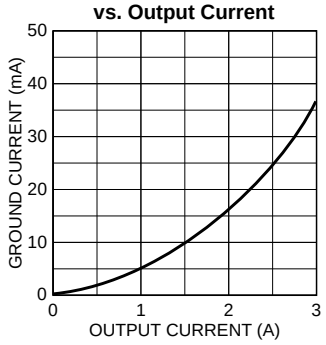
MIC2930x Dropout Voltage vs. Temperature



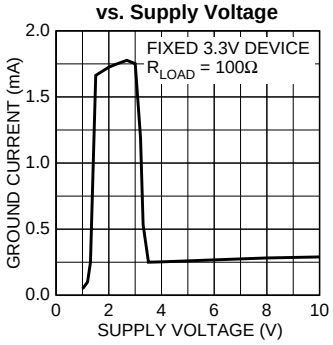
MIC29300-3.3 Dropout Characteristics



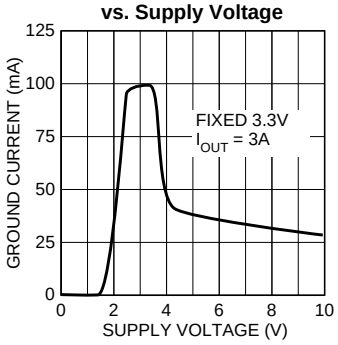
MIC2930x Ground Current vs. Output Current



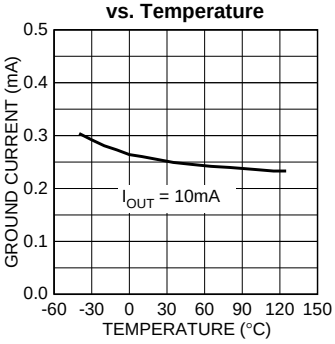
MIC2930x Ground Current vs. Supply Voltage



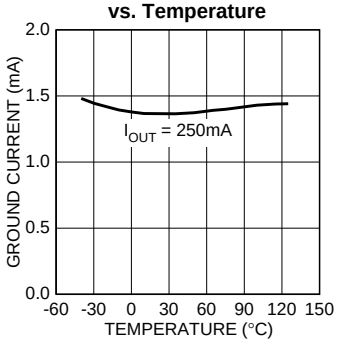
MIC2930x Ground Current vs. Supply Voltage



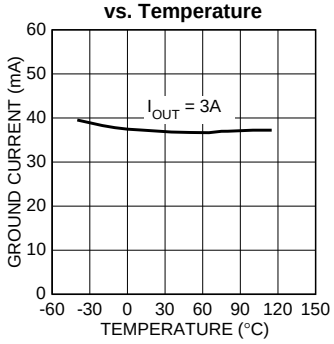
MIC2930x Ground Current vs. Temperature



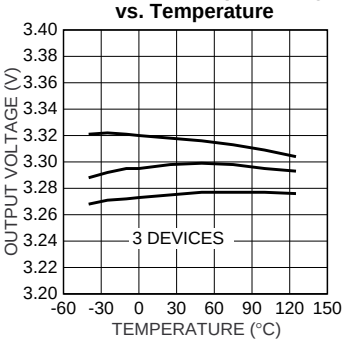
MIC2930x Ground Current vs. Temperature



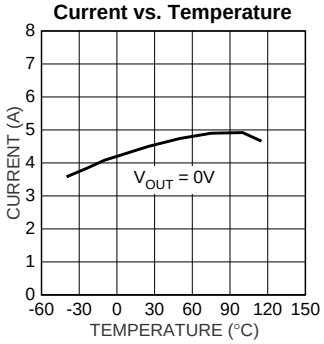
MIC2930x Ground Current vs. Temperature



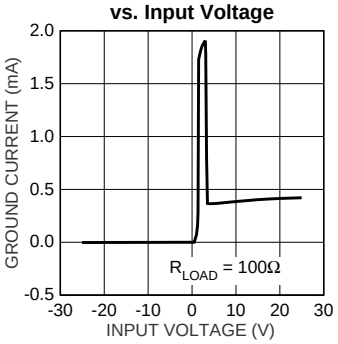
MIC29300-3.3 Output Voltage vs. Temperature



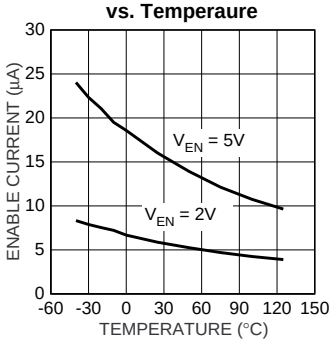
MIC29300-5.0 Short Circuit Current vs. Temperature



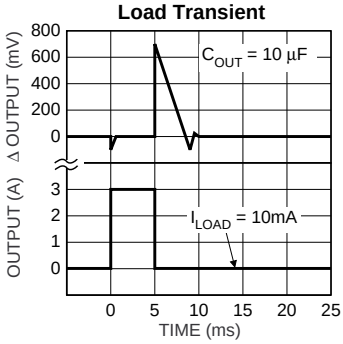
MIC2930x Ground Current vs. Input Voltage



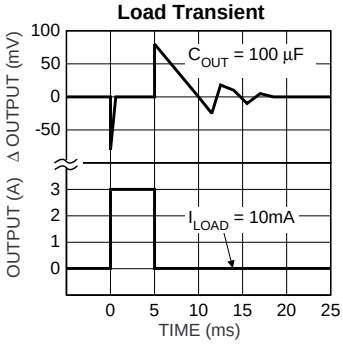
MIC29301-x/2 Enable Current vs. Temperaure



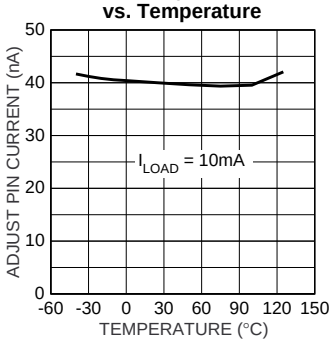
MIC2930x Load Transient



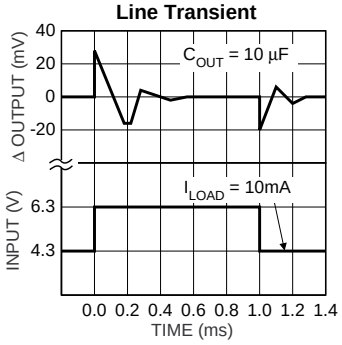
MIC2930x Load Transient



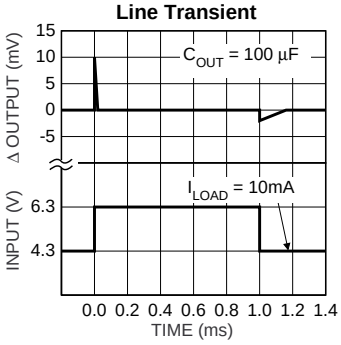
MIC29302/3 Adjust Pin Current vs. Temperature



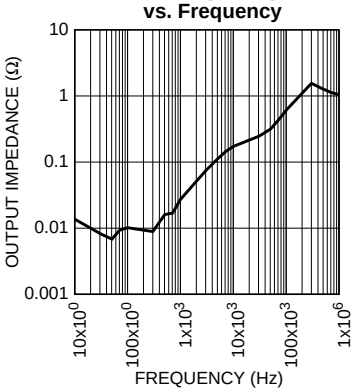
MIC2930x Line Transient



MIC2930x Line Transient

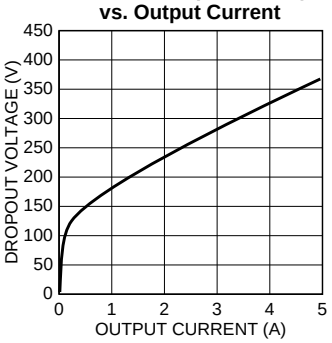


MIC2930x Output Impedance vs. Frequency

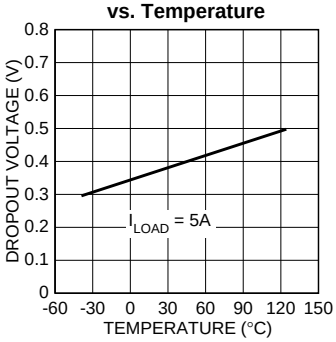


Typical Characteristics MIC2950x

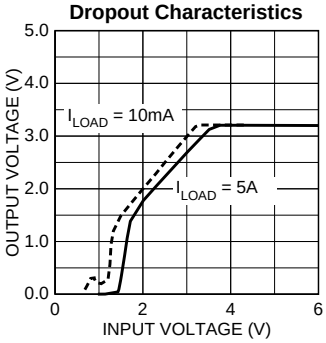
MIC2950x Dropout Voltage vs. Output Current



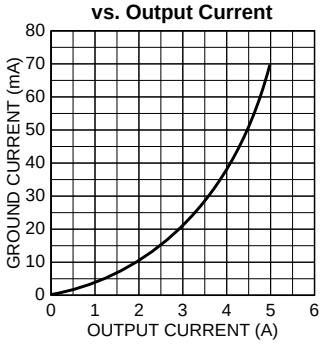
MIC2950x Dropout Voltage vs. Temperature



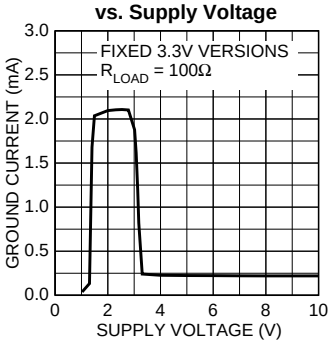
MIC29500-3.3 Dropout Characteristics



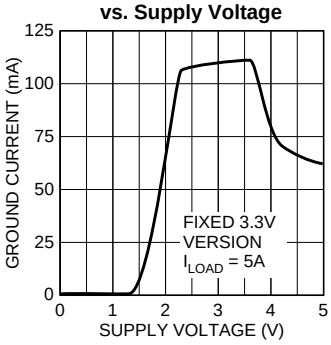
MIC2950x Ground Current vs. Output Current



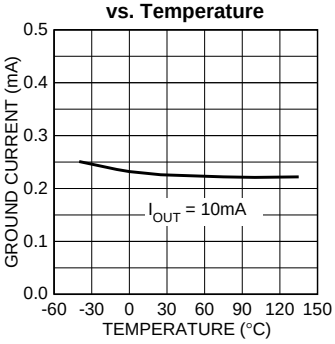
MIC2950x Ground Current vs. Supply Voltage



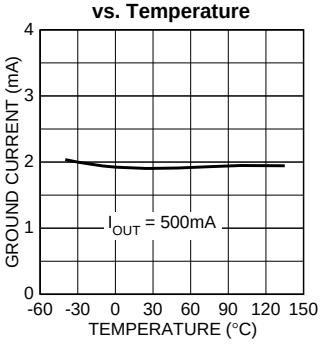
MIC2950x Ground Current vs. Supply Voltage



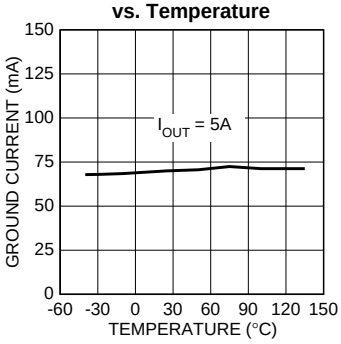
MIC2950x Ground Current vs. Temperature



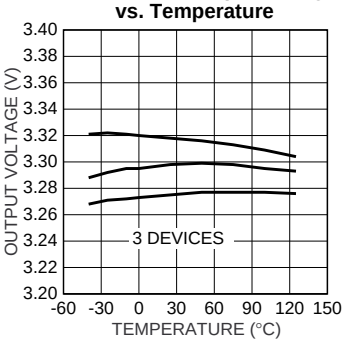
MIC2950x Ground Current vs. Temperature



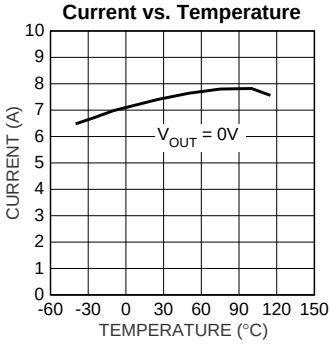
MIC2950x Ground Current vs. Temperature



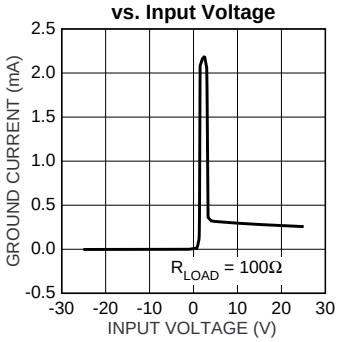
MIC29500-3.3 Output Voltage vs. Temperature



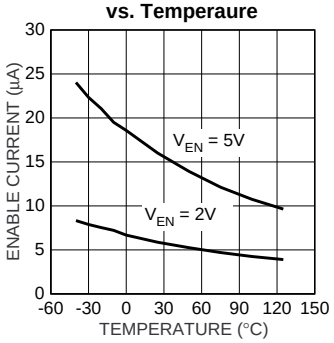
MIC2950x-5.0 Short Circuit Current vs. Temperature



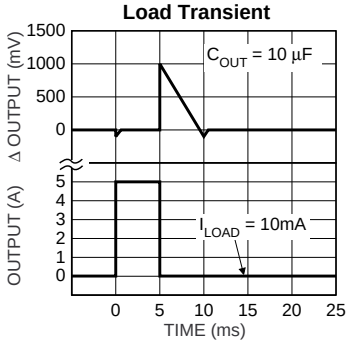
MIC2950x Ground Current vs. Input Voltage



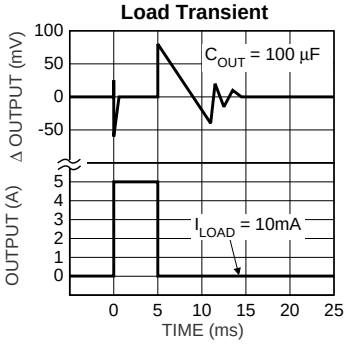
MIC29501-xx/2 Enable Current vs. Temperaure



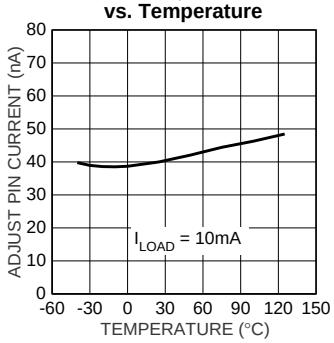
MIC2950x Load Transient



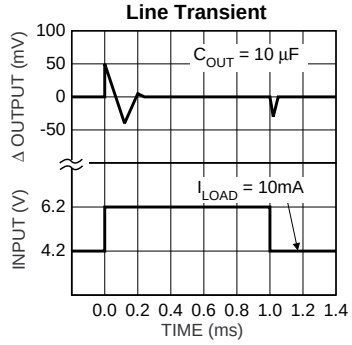
MIC2950x Load Transient



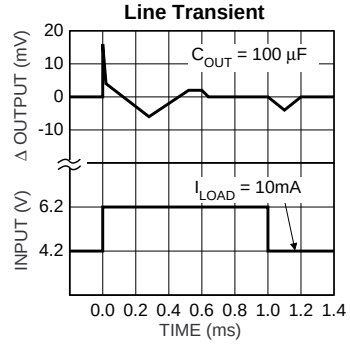
MIC29502/3 Adjust Pin Current vs. Temperature



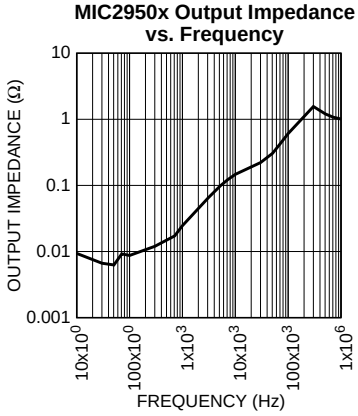
MIC2950x Line Transient



MIC2950x Line Transient

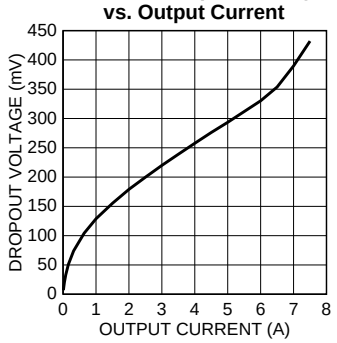


MIC2950x Output Impedance vs. Frequency

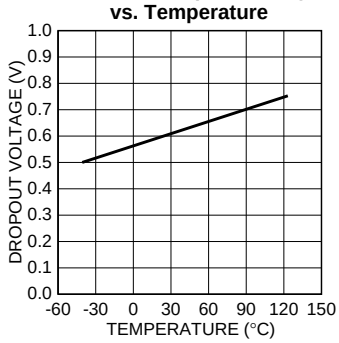


Typical Characteristics MIC2975x

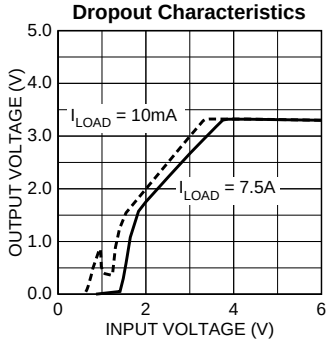
MIC2975x Dropout Voltage vs. Output Current



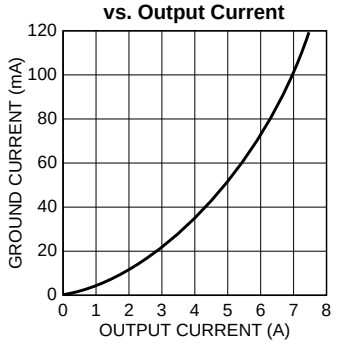
MIC2975x Dropout Voltage vs. Temperature



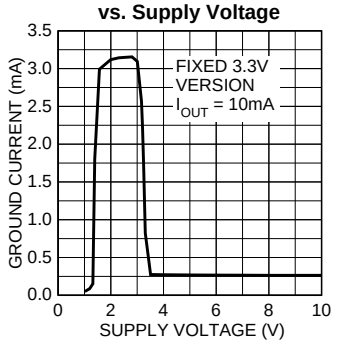
MIC29750-3.3 Dropout Characteristics



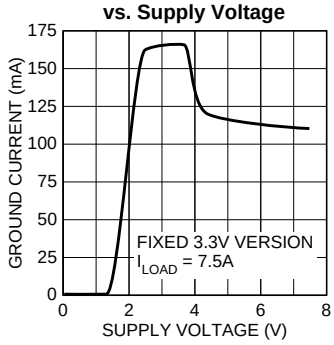
MIC2975x Ground Current vs. Output Current



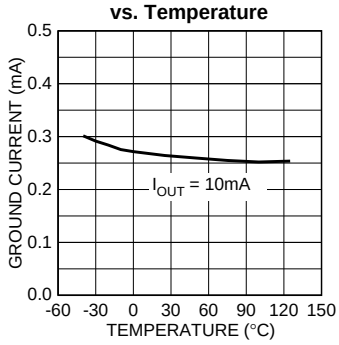
MIC2975x Ground Current vs. Supply Voltage



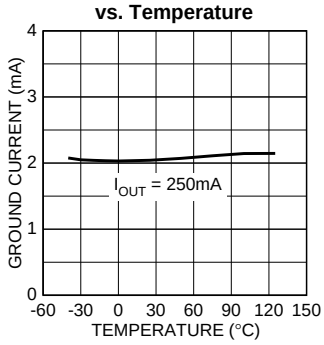
MIC2975x Ground Current vs. Supply Voltage



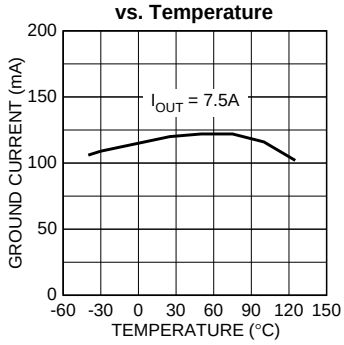
MIC2975x Ground Current vs. Temperature



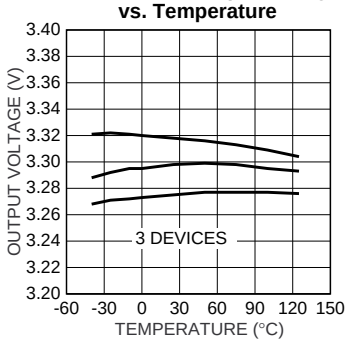
MIC2975x Ground Current vs. Temperature



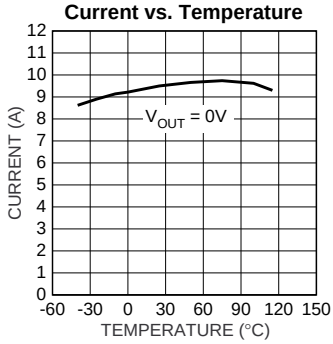
MIC2975x Ground Current vs. Temperature



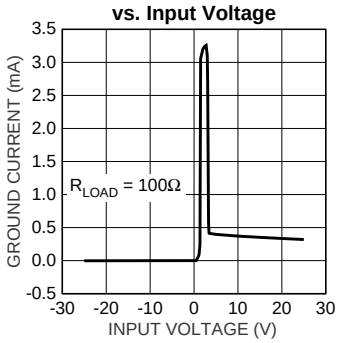
MIC29750-3.3 Output Voltage vs. Temperature



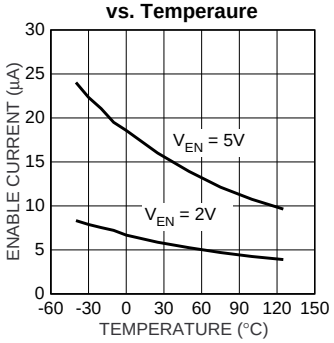
MIC29750-5.0 Short Circuit Current vs. Temperature



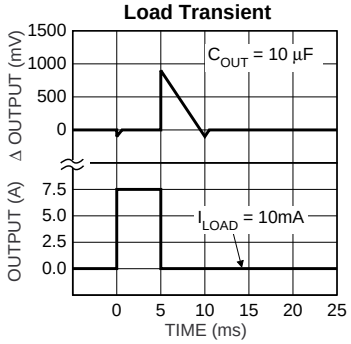
MIC2975x Ground Current vs. Input Voltage



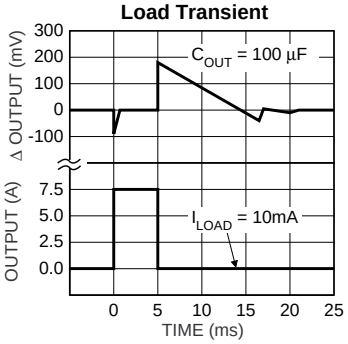
MIC29751-xx/2 Enable Current vs. Temperaure



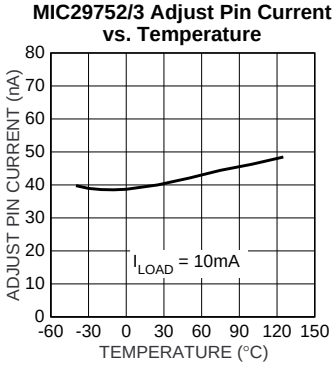
MIC2975x Load Transient



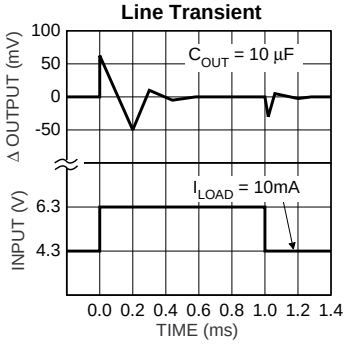
MIC2975x Load Transient



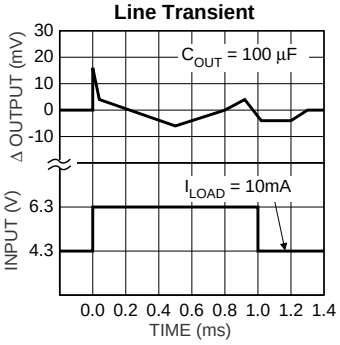
MIC29752/3 Adjust Pin Current vs. Temperature



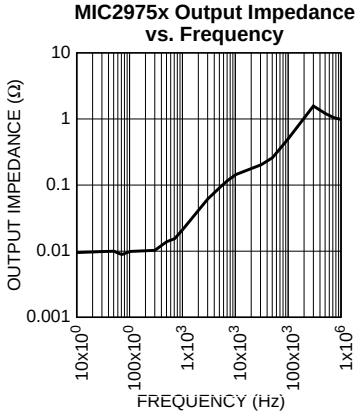
MIC2975x Line Transient



MIC2975x Line Transient



MIC2975x Output Impedance vs. Frequency



Applications Information

The MIC29150/29300/29500/29750 are high performance low-dropout voltage regulators suitable for all moderate to high-current voltage regulator applications. Their 300mV to 400mV dropout voltage at full load make them especially valuable in battery powered systems and as high efficiency noise filters in "post-regulator" applications. Unlike older NPN-pass transistor designs, where the minimum dropout voltage is limited by the base-emitter voltage drop and collector-emitter saturation voltage, dropout performance of the PNP output of these devices is limited merely by the low V_{CE} saturation voltage.

A trade-off for the low dropout voltage is a varying base drive requirement. But Micrel's Super ßeta PNP™ process reduces this drive requirement to merely 1% of the load current.

The MIC29150–29750 family of regulators is fully protected from damage due to fault conditions. Current limiting is provided. This limiting is linear; output current under overload conditions is constant. Thermal shutdown disables the device when the die temperature exceeds the 125°C maximum safe operating temperature. Transient protection allows device (and load) survival even when the input voltage spikes between –20V and +60V. When the input voltage exceeds about 35V to 40V, the overvoltage sensor temporarily disables the regulator. The output structure of these regulators allows voltages in excess of the desired output voltage to be applied without reverse current flow. MIC29xx1 and MIC29xx2 versions offer a logic level ON/OFF control: when disabled, the devices draw nearly zero current.

An additional feature of this regulator family is a common pinout: a design's current requirement may change up or down yet use the same board layout, as all of these regulators have identical pinouts.

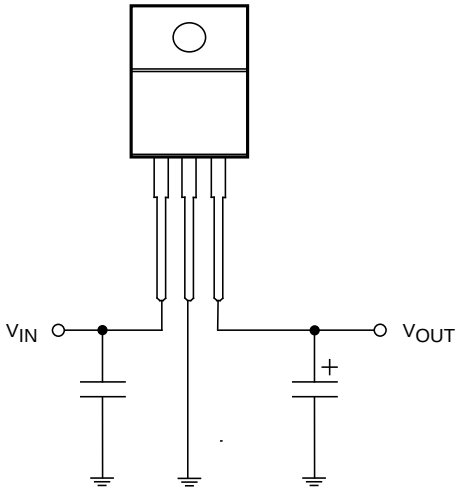


Figure 3. Linear regulators require only two capacitors for operation.

Thermal Design

Linear regulators are simple to use. The most complicated design parameters to consider are thermal characteristics. Thermal design requires the following application-specific parameters:

- Maximum ambient temperature, T_A
- Output Current, I_{OUT}
- Output Voltage, V_{OUT}
- Input Voltage, V_{IN}

First, we calculate the power dissipation of the regulator from these numbers and the device parameters from this datasheet.

$$P_D = I_{OUT} \times (1.01V_{IN} - V_{OUT})$$

Where the ground current is approximated by 1% of I_{OUT}. Then the heat sink thermal resistance is determined with this formula:

$$\theta_{SA} = \frac{T_{J\,MAX} - T_A}{P_D} - (\theta_{JC} + \theta_{CS})$$

Where $T_{J\,MAX} \leq 125°C$ and θ_{CS} is between 0 and 2°C/W.

The heat sink may be significantly reduced in applications where the minimum input voltage is known and is large compared with the dropout voltage. Use a series input resistor to drop excessive voltage and distribute the heat between this resistor and the regulator. The low dropout properties of Micrel Super ßeta PNP regulators allow very significant reductions in regulator power dissipation and the associated heat sink without compromising performance. When this technique is employed, a capacitor of at least 0.1µF is needed directly between the input and regulator ground.

Please refer to Application Note 9 and Application Hint 17 for further details and examples on thermal design and heat sink specification.

Capacitor Requirements

For stability and minimum output noise, a capacitor on the regulator output is necessary. The value of this capacitor is dependent upon the output current; lower currents allow smaller capacitors. MIC29150—29750 regulators are stable with the following minimum capacitor values at full load:

Device	Full Load Capacitor
MIC29150	10µF
MIC29300	10µF
MIC29500	10µF
MIC29750	22µF

This capacitor need not be an expensive low ESR type: aluminum electrolytics are adequate. In fact, extremely low ESR capacitors may contribute to instability. Tantalum capacitors are recommended for systems where fast load transient response is important.

Where the regulator is powered from a source with a high AC impedance, a 0.1µF capacitor connected between Input and GND is recommended. This capacitor should have good characteristics to above 250kHz.

Minimum Load Current

The MIC29150–29750 regulators are specified between finite loads. If the output current is too small, leakage currents dominate and the output voltage rises. The following minimum load current swamps any expected leakage current across the operating temperature range:

Device	Minimum Load
MIC29150	5mA
MIC29300	7mA
MIC29500	10mA
MIC29750	10mA

Adjustable Regulator Design

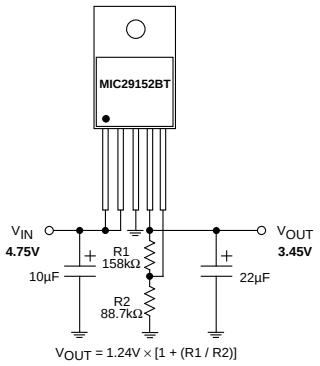


Figure 4. Adjustable Regulator with Resistors

The adjustable regulator versions, MIC29xx2 and MIC29xx3, allow programming the output voltage anywhere between 1.25V and the 26V maximum operating rating of the family. Two resistors are used. Resistors can be quite large, up to 1MΩ, because of the very high input impedance and low bias current of the sense comparator: The resistor values are calculated by:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{1.240} - 1\right)$$

Where V_O is the desired output voltage. Figure 4 shows component definition. Applications with widely varying load currents may scale the resistors to draw the minimum load current required for proper operation (see above).

Error Flag

MIC29xx1 and MIC29xx3 versions feature an Error Flag, which looks at the output voltage and signals an error condition when this voltage drops 5% below its expected value. The error flag is an open-collector output that pulls low under fault conditions. It may sink 10mA. Low output voltage signifies a number of possible problems, including an overcurrent fault (the device is in current limit) and low input voltage. The flag output is inoperative during overtemperature shutdown conditions.

Enable Input

MIC29xx1 and MIC29xx2 versions feature an enable (EN) input that allows ON/OFF control of the device. Special design allows “zero” current drain when the device is disabled—only microamperes of leakage current flows. The EN input has TTL/CMOS compatible thresholds for simple interfacing with logic, or may be directly tied to ≤ 30V. Enabling the regulator requires approximately 20µA of current.

MIC2937A/29371/29372

750mA Low-Dropout Voltage Regulator

Preliminary Information

General Description

The MIC2937A family are “bulletproof” efficient voltage regulators with very low dropout voltage (typically 40mV at light loads and 300mV at 500mA), and very low quiescent current (160µA typical). The quiescent current of the MIC2937A increases only slightly in dropout, thus prolonging battery life. Key MIC2937A features include protection against reversed battery, fold-back current limiting, and automotive “load dump” protection (60V positive transient).

The MIC2937 is available in several configurations. The MIC2937A-xx devices are three pin fixed voltage regulators with 3.3V, 5V, and 12V outputs available. The MIC29371 is a fixed regulator offering logic compatible ON/OFF switching input and an error flag output. This flag may also be used as a power-on reset signal. A logic-compatible shutdown input is provided on the adjustable MIC29372, which enables the regulator to be switched on and off.

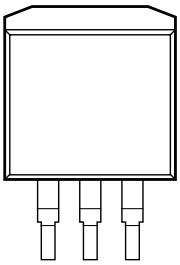
Features

- High output voltage accuracy
- Guaranteed 750mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Input can withstand –20V reverse battery and +60V positive transients
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 26V(MIC29372)
- Available in TO-220, TO-263, TO-220-5, and TO-263-5 packages.

Applications

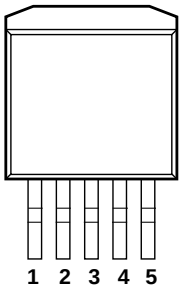
- Battery Powered Equipment
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- Automotive Electronics
- SMPS Post-Regulator/ DC to DC Modules
- High Efficiency Linear Power Supplies

Pin Configuration

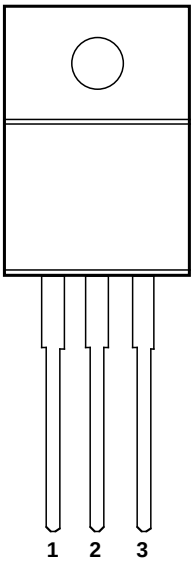


INPUT GROUND OUTPUT

TO-263 Package (MIC2937A-xxBU)

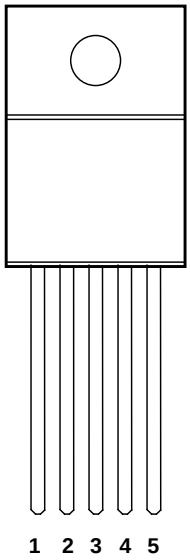


TO-263-5 Package (MIC29371/29372BU)



INPUT GROUND OUTPUT

TO-220 Package (MIC2937A-xxBT)



TO-220-5 Package (MIC29371/29372BT)

Five Lead Package Pin Functions:

	MIC29371	MIC29372
1)	Error	Adjust
2)	Input	Shutdown
3)	Ground	Ground
4)	Output	Input
5)	Shutdown	Output

The TAB is Ground on the TO-220 and TO-263 packages.

Ordering Information

Part Number	Voltage	Temperature Range*	Package
MIC2937A-3.3BU	3.3	–40°C to +125°C	TO-263-3
MIC2937A-3.3BT	3.3	–40°C to +125°C	TO-220
MIC2937A-5.0BU	5.0	–40°C to +125°C	TO-263-3
MIC2937A-5.0BT	5.0	–40°C to +125°C	TO-220
MIC2937A-12BU	12	–40°C to +125°C	TO-263-3
MIC2937A-12BT	12	–40°C to +125°C	TO-220
MIC29371-3.3BT	3.3	–40°C to +125°C	TO-220-5
MIC29371-3.3BU	3.3	–40°C to +125°C	TO-263-5
MIC29371-5.0BT	5.0	–40°C to +125°C	TO-220-5
MIC29371-5.0BU	5.0	–40°C to +125°C	TO-263-5
MIC29371-12BT	12	–40°C to +125°C	TO-220-5
MIC29371-12BU	12	–40°C to +125°C	TO-263-5
MIC29372BT	Adj	–40°C to +125°C	TO-220-5
MIC29372BU	Adj	–40°C to +125°C	TO-263-5

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 1) ..... Internally Limited
Lead Temperature (Soldering, 5 seconds) ..... 260°C
Storage Temperature Range ..... –65°C to +150°C
Operating Junction Temperature Range
..... –40°C to +125°C
TO-220 θ_{JC} ..... 2.5°C/W
TO-263 θ_{JC} ..... 2.5°C/W
Input Supply Voltage ..... –20V to +60V
Operating Input Supply Voltage ..... 2V† to 26V
Adjust Input Voltage (Notes 9 and 10)
.....–1.5V to +26V
Shutdown Input Voltage .....–0.3V to +30V
Error Comparator Output Voltage .....–0.3V to +30V

† Across the full operating temperature, the minimum input voltage range for full output current is 4.3V to 26V. Output will remain in-regulation at lower output voltages and low current loads down to an input of 2V at 25°C.

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the full operating temperature range. Unless otherwise specified, $V_{IN} = V_{OUT}$ + 1V, I_L = 5mA, C_L = 10µF. The MIC29372 are programmed for a 5V output voltage, and $V_{SHUTDOWN} \leq$ 0.6V (MIC29271-xx and MIC29372 only).

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy	Variation from factory trimmed V_{OUT}	–1 **–2**		1 **2**	%
		5mA ≤ I_L ≤ 500mA	**–2.5**		**2.5**	
		MIC2937A-12 and 29371-12 only:	–1.5 **–3**		1.5 **3**	
		5mA ≤ I_L ≤ 500mA	**–4**		**4**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2) Output voltage > 10V		20 80	**100** **350**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1V to 26V		0.03	0.10 **0.40**	%
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 5 to 500mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} – V_O$	Dropout Voltage (Note 4)	I_L = 5mA		80	150 **180**	mV
		I_L = 100mA		200		
		Output voltage > 10V		240		
		I_L = 500mA		300		
		Output voltage > 10V		420		
		I_L = 750mA		370	600 **750**	
I_{GND}	Ground Pin Current (Note 5)	I_L = 5mA		160	250 **300**	µA
		I_L = 100mA		1	2.5 **3**	mA
		I_L = 500mA		8	13 **16**	
		I_L = 750mA		15	25	
I_{GNDDO}	Ground Pin Current at Dropout (Note 5)	V_{IN} = 0.5V less than designed V_{OUT} ($V_{OUT} \geq$ 3.3V) I_O = 5mA		200	**500**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V (Note 6)		1.1	1.5 **2**	A
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 7)		0.05	0.2	%/W
e_n	Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 10µF		400		µV RMS
		C_L = 100µF		260		

Electrical Characteristics (Continued)

MIC29372

Parameter	Conditions	Min	Typical	Max	Units
Reference Voltage		1.223 **1.210**	1.235	1.247 **1.260**	V V max
Reference Voltage	(Note 8)	**1.204**		**1.266**	V
Adjust Pin Bias Current			20	40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 7)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C
Error Comparator	**MIC29371**				
Output Leakage Current	V_{OH} = 30V		0.01	1.00 **2.00**	µA
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 250µA		150	250 **400**	mV
Upper Threshold Voltage	(Note 9)	40 **25**	60		mV
Lower Threshold Voltage	(Note 9)		75	95 **140**	mV
Hysteresis	(Note 9)		15		mV
Shutdown Input	**MIC29371/MIC29372**				
Input Logic Voltage Low (ON)			1.3		V
	High (OFF)	**2.0**		**0.7**	
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V		30	50 **100**	µA
	$V_{SHUTDOWN}$ = 30V		450	600 **750**	µA
Regulator Output Current in Shutdown	(Note 10)		3	10 **20**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J\,(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At low values of programmed output voltage, the minimum input supply voltage of 4.3V over temperature must be taken into account. The MIC2937A operates down to 2V of input at reduced output current at 25°C.

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 6: The MIC2937A family features fold-back current limiting. The short circuit (V_{OUT} = 0V) current limit is less than the maximum current with normal output voltage.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

Note 8: $V_{REF} \le V_{OUT} \le (V_{IN} - 1\ V)$, $4.3V \le V_{IN} \le 26V$, $5mA < I_L \le 750\ mA$, $T_J \le T_{J\,MAX}$.

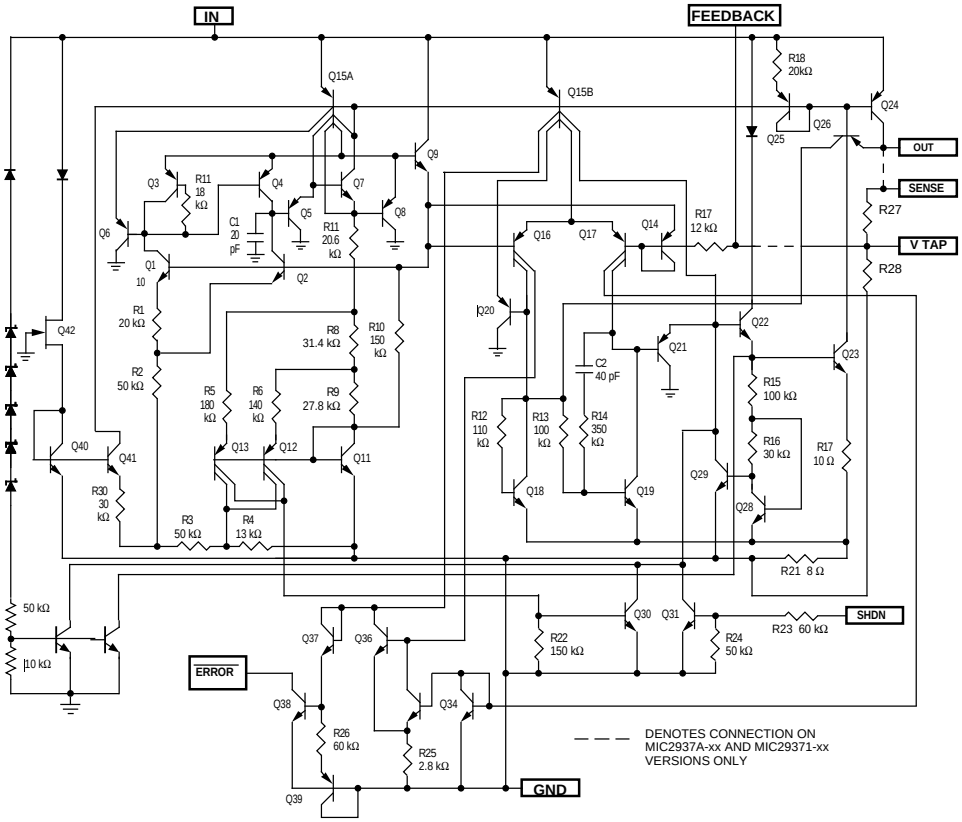
Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input (for a 5V regulator). To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.7% guaranteed.

Note 10: Circuit of Figure 3 with R1 ≥ 150kΩ. $V_{SHUTDOWN} \ge 2V$ and $V_{IN} \le 26V$, $V_{OUT} = 0$.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

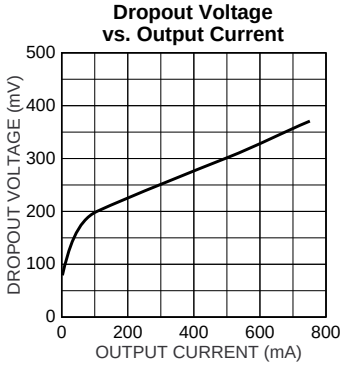
Note 12: Maximum positive supply voltage of 60V must be of limited duration (< 100ms) and duty cycle (≤ 1%). The maximum continuous supply voltage is 26V.

Schematic Diagram

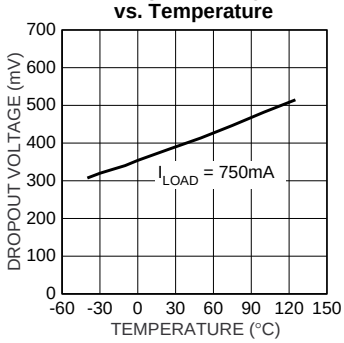


Typical Characteristics

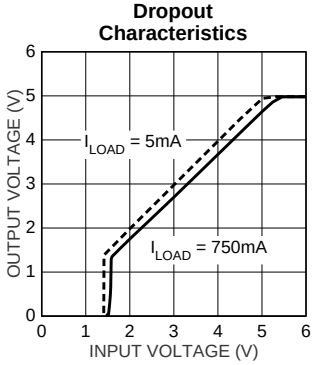
Dropout Voltage vs. Output Current



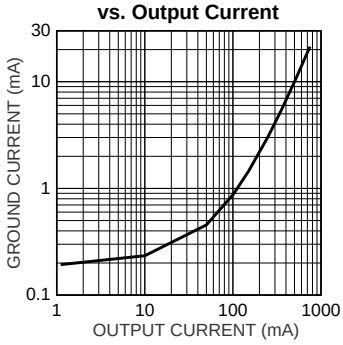
Dropout Voltage vs. Temperature



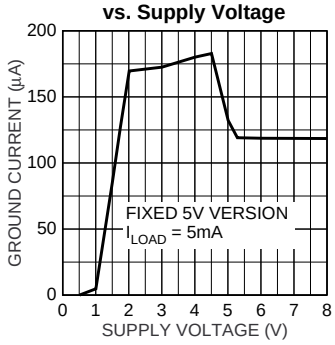
Dropout Characteristics



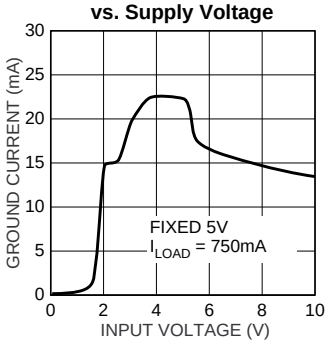
Ground Current vs. Output Current



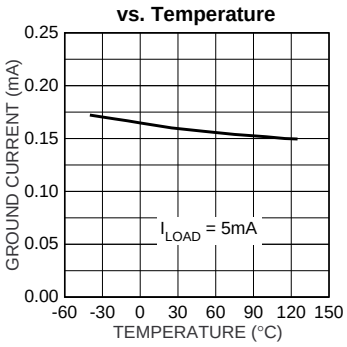
Ground Current vs. Supply Voltage



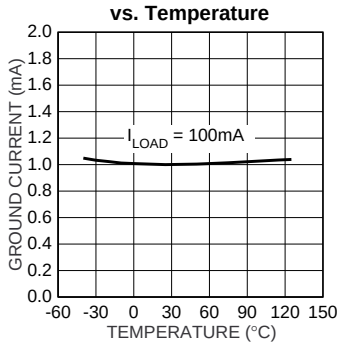
Ground Current vs. Supply Voltage



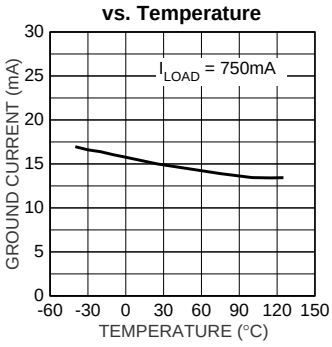
Ground Current vs. Temperature



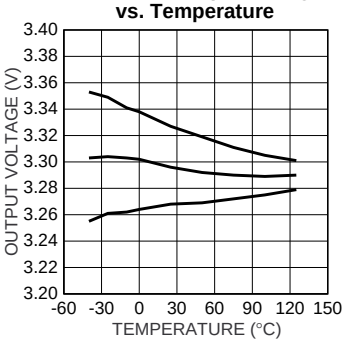
Ground Current vs. Temperature



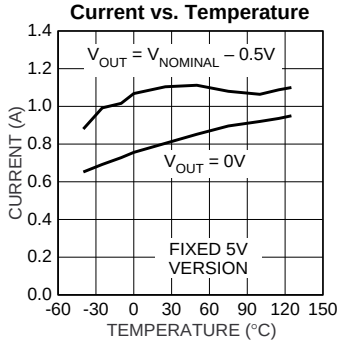
Ground Current vs. Temperature



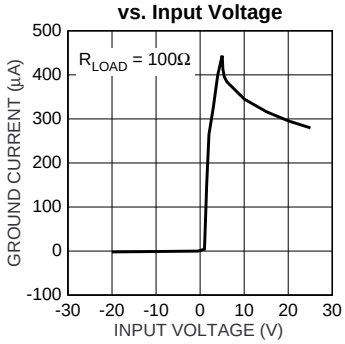
Fixed 3.3V Output Voltage vs. Temperature



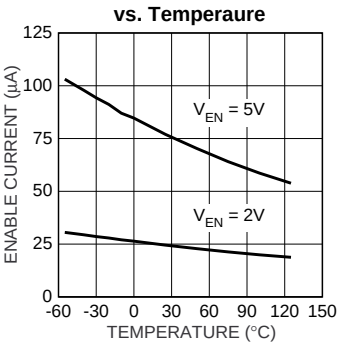
Short Circuit and Maximum Current vs. Temperature



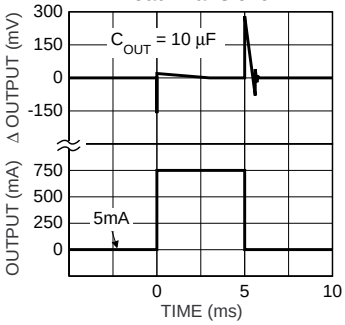
Ground Current vs. Input Voltage



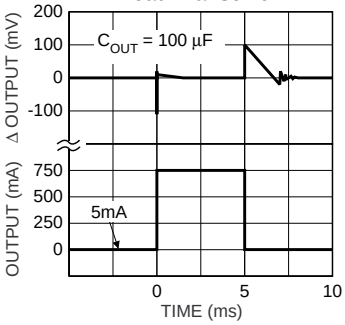
MIC29371/2 Shutdown Current vs. Temperaure



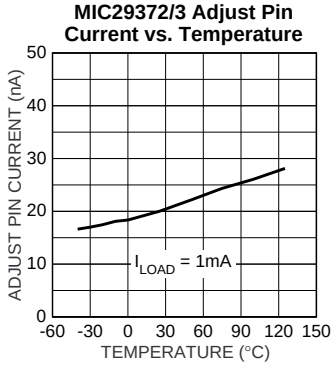
Load Transient



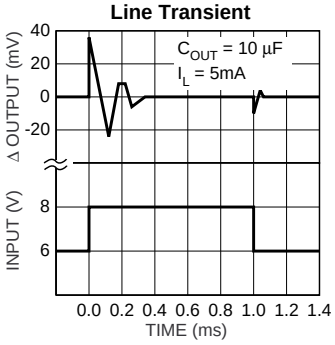
Load Transeint



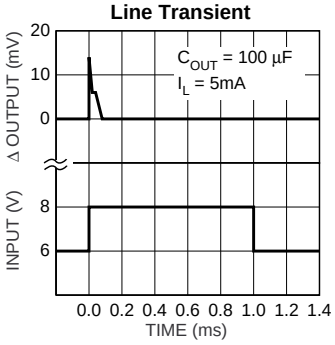
MIC29372/3 Adjust Pin Current vs. Temperature



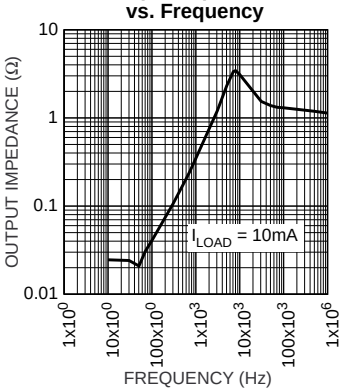
Line Transient



Line Transient



Output Impedance vs. Frequency



Applications Information

External Capacitors

A 10µF (or greater) capacitor is required between the MIC2937A output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.5µF for current below 10mA or 0.15µF for currents below 1 mA. Adjusting the MIC29372 to voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 750mA load at 1.23V output (Output shorted to Adjust) a 22µF (or greater) capacitor should be used.

The MIC2937A/29371 will remain in regulation with a minimum load of 5mA. When setting the output voltage of the MIC29372 version with external resistors, the current through these resistors may be included as a portion of the minimum load.

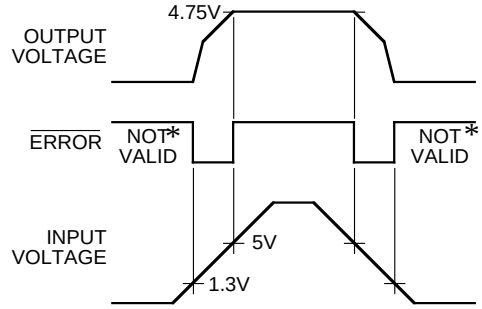
A 1µF capacitor should be placed from the input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC29372 Adjust terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Adjust and increasing the output capacitor to at least 22µF will remedy this.

Error Detection Comparator Output (MIC29371)

A logic low output will be produced by the comparator whenever the MIC29371 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 75mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC29371. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, extremely high input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC29371 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the MIC29371's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.



* SEE APPLICATIONS INFORMATION

Figure 1. $\overline{\text{ERROR}}$ Output Timing

The error comparator has an NPN open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 250µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

Programming the Output Voltage (MIC29372)

The MIC29372 may programmed for any output voltage between its 1.235V reference and its 26V maximum rating. An external pair of resistors is required, as shown in Figure 3.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} - |I_{FB}| R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the Adjust pin bias current, nominally 20nA. The minimum recommended load current of 1µA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a –2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the MIC29372 typically draws 100µA at no load with SHUTDOWN open-circuited, this is a negligible addition.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160µV_{RMS} for a 100kHz bandwidth at 5V output. Noise can be reduced by a factor of four with the adjustable regulators with a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \cdot 200\ \text{Hz}}$$

or about 0.01µF. When doing this, the output capacitor must be increased to 10µF to maintain stability. These changes reduce the output noise from 430µV to 100µV_{RMS} for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Automotive Applications

The MIC2937A is ideally suited for automotive applications for a variety of reasons. It will operate over a wide range of input voltages with very low dropout voltages (40mV at light loads), and very low quiescent currents (100µA typical). These features are necessary for use in battery powered systems, such as automobiles. It is a "bulletproof" device with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

Typical Applications

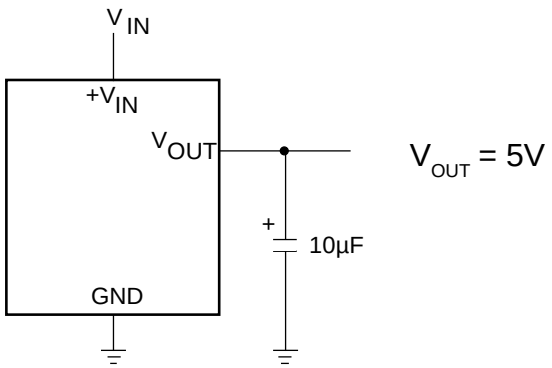


Figure 2. MIC2937A-5.0 Fixed +5V Regulator

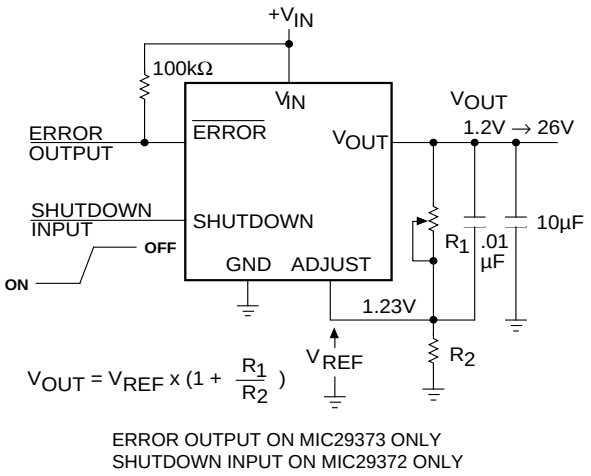
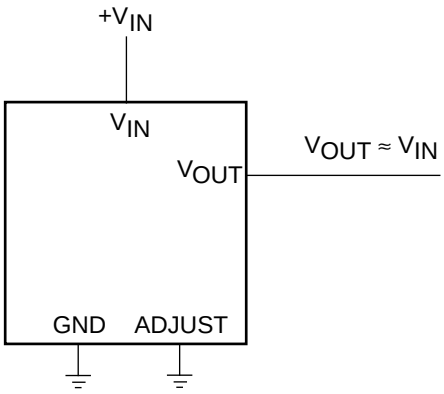
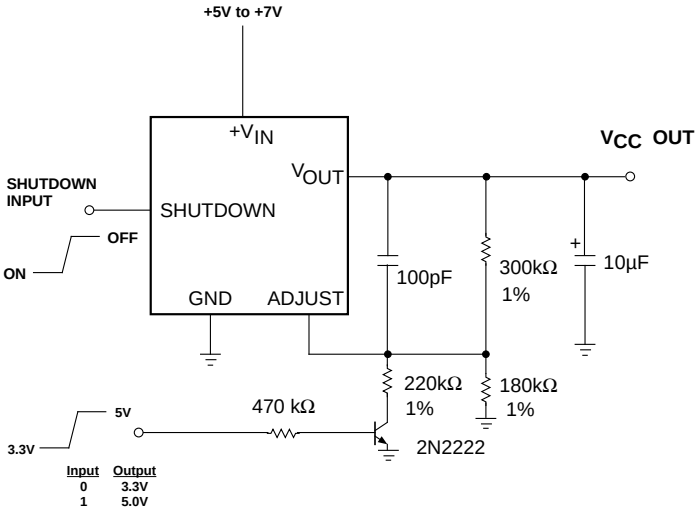


Figure 3. MIC29372 Adjustable Regulator



*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Figure 4. MIC29372 Wide Input Voltage Range Current Limiter



SHUTDOWN PIN LOW= ENABLE OUTPUT. Q1 ON = 3.3V, Q1 OFF = 5.0V.

Figure 5. MIC29372 5.0V or 3.3V Selectable Regulator with Shutdown.

National Semiconductor

November 1995

MM54HC14/MM74HC14 Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

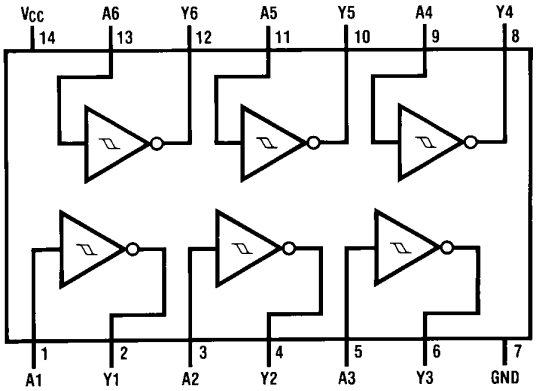
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC}=4.5V$

Connection and Schematic Diagrams

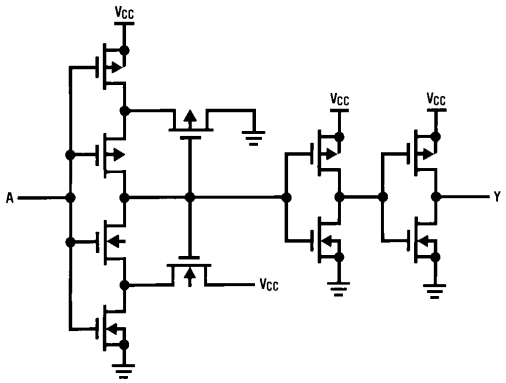
Dual-In-Line Package



TL/F/5105–1

Top View

Order Number MM54HC14 or MM74HC14



TL/F/5105–2

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	1.0	V
			4.5V	2.7	2.0	2.0	2.0	V
			6.0V	3.2	3.0	3.0	3.0	V
		Maximum	2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	0.3	V
			4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	1.0	V
			4.5V	1.8	2.2	2.2	2.2	V
			6.0V	2.2	3.0	3.0	3.0	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.5	0.5	0.5	V
		Maximum	2.0V	0.5	1.0	1.0	1.0	V
			4.5V	0.9	1.4	1.4	1.4	V
			6.0V	1.0	1.5	1.5	1.5	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\lvert I_{OUT}\rvert=20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IL}$ $\lvert I_{OUT}\rvert=4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert=5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert=20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert=4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert=5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

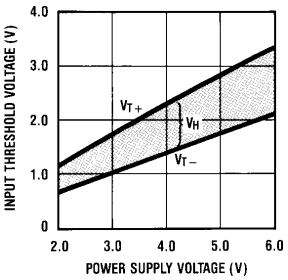
AC Electrical Characteristics $V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

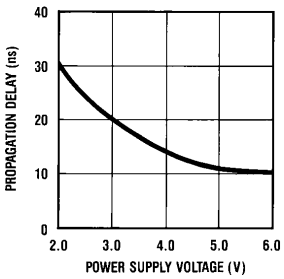
Typical Performance Characteristics

Input Threshold, V_{T+}, V_{T-}, vs Power Supply Voltage



TL/F/5105–3

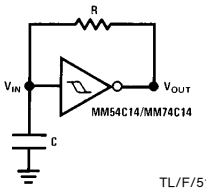
Propagation Delay vs Power Supply



TL/F/5105–4

Typical Applications

Low Power Oscillator



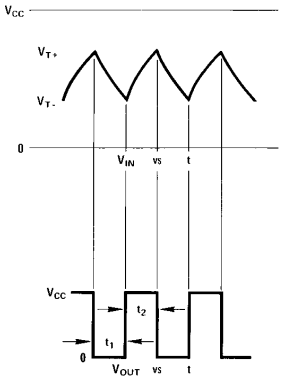
TL/F/5105–5

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$$

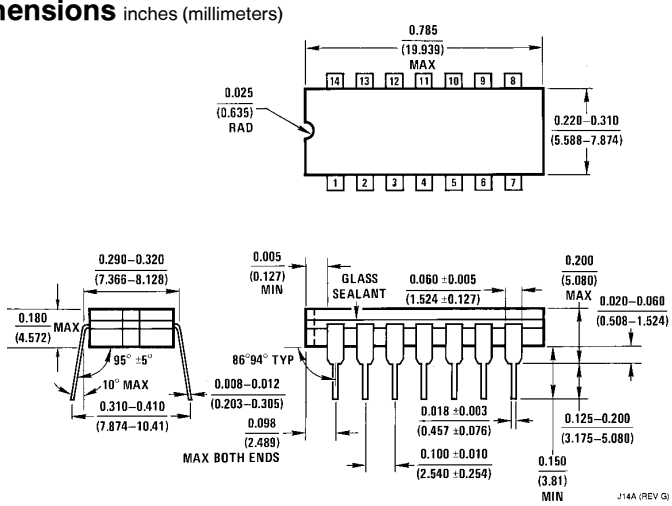
$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC}-V_{T-})}{V_{T-}(V_{CC}-V_{T+})}}$$

Note: The equations assume $t_1+t_2 \gg t_{pd0}+t_{pd1}$

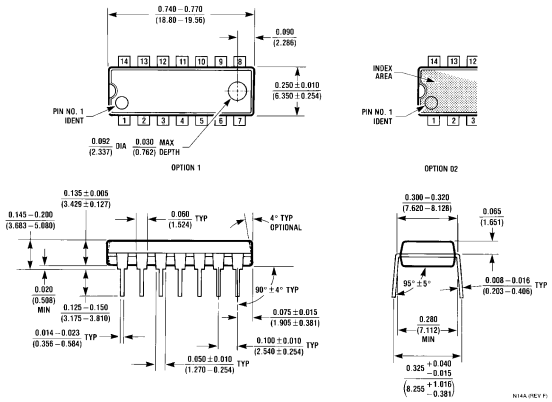


TL/F/5105–6

Physical Dimensions inches (millimeters)



Dual-In-Line Package (J)
Order Number MM54HC14J or MM74HC14J
NS Package J14A



Dual-In-Line Package (N)
Order Number MM74HC14N
NS Package N14A

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Surface Mount Tantalum Capacitors

Foreword

AVX offers a broad line of molded solid tantalum capacitors in a wide range of sizes, styles, and ratings to meet your design needs. This catalog combines into one source AVX's SMD tantalum capacitor information from its worldwide tantalum operations.

The TAJ series includes EIA standard case sizes and ratings, along with extended range values. Low profile packages and EIAJ standard case sizes, MIL-Style CWR11 components are available as part of the TAJ family.

The TPS Low ESR SMD product line was introduced last year and is included in this catalog to provide a comprehensive listing of our tantalum surface mount lines. TPS has its own catalog which covers performance and applications in depth. This catalog may be obtained from your local AVX representative.

The TAZ Series offers high volume efficiency components in a wide variety of footprints. Five of those footprints have a nominal height of 0.050 inches which make them ideal for low profile applications.

The TAZ series is qualified as the MIL-Style CWR09, the molded equivalent of the MIL-Style CWR06. Two new case sizes are added to this series, increasing the capacitance/voltage ratings available for both low and high values. Extended range values are also available in all series.

AVX offers tantalum applications service for use by our customers, please contact your local representative if you wish to discuss any special requirements.

AVX has become a world leader in tantalum capacitor technology and is continuing to make significant investments in equipment and research to maintain that leadership.

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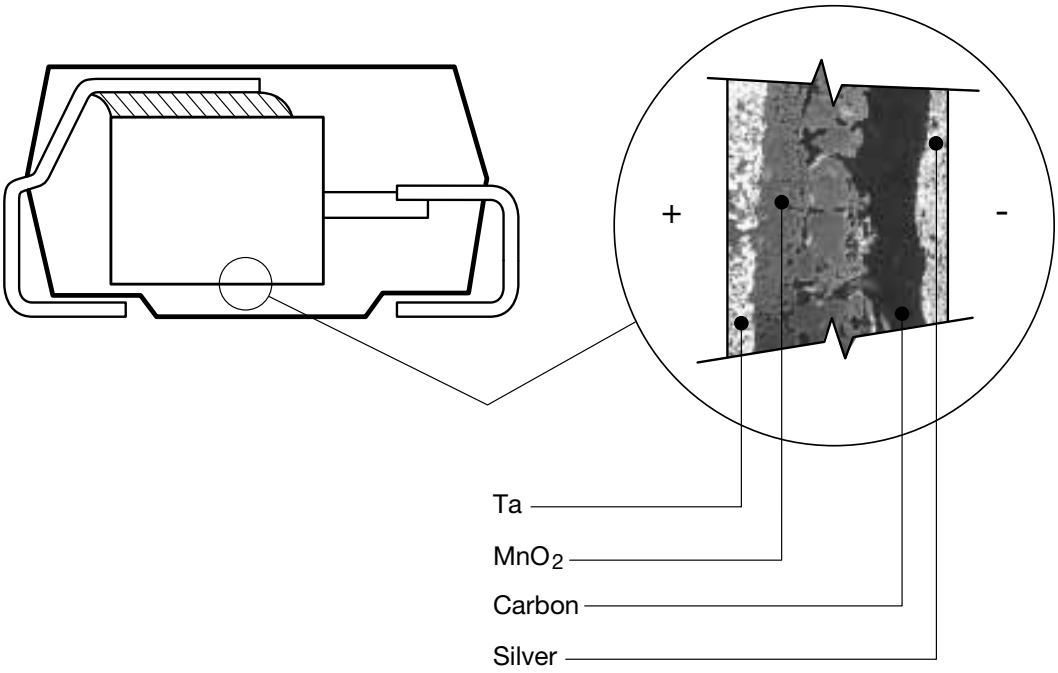
Section 1 – TAJ, TAZ, and TPS

The AVX series of molded tantalum chips are designed for surface mount applications and are equally suitable for hybrid applications. They are available tape and reel packaged for high volume automatic assembly techniques.



Design and Application Features

1. Flat top surface for high speed pick-up — compatible with high speed automatic onsertion equipment.

2. Regular molded shape — allows accurate transfer and placement during onsertion.

3. Glue pads on underside of TAJ/TPS ranges permit consistent, strong bonding to circuit board prior to soldering.

4. Consistent termination dimensions — allows reliable pad design and a consistent “fit” — helps to eliminate “tombstoning” effects and reduces rotational effects.

5. Compliant terminations — transfer of thermo-mechanical stresses during operation and mechanical stresses during equipment servicing to the component are reduced.

6. Rugged construction helps to prevent damage during mounting and to ensure compatibility with all systems for soldering (infra-red, wave solder, reflow solder, vapor phase) and conductive epoxy resin mounting techniques.

7. Resistant to flux removal solvents including Aqueous systems used with vapor phase soldering.

8. All parts are coded on uppermost surface with videcon-readable polarity marking, cap value, and voltage.

9. High density packaging on 8 and 12 mm blister tape, available on 7" and 13" reels.

10. Qualified to IECQ, CECC and MIL specifications, TAJ/TPS in compliance with EIA standards.

11. New low profile case sizes including the new “R” case compatible with “0805” footprint. Maximum height for low profile is 1.2mm (0.047").

TAJ Series — Solid Tantalum Chip Capacitors (EIA Standard)

The TAJ standard series encompasses the four key sizes recognized by major OEMs throughout the world, together with the new high profile E case (7343H size) and two cases conforming to the EIA-J standard.

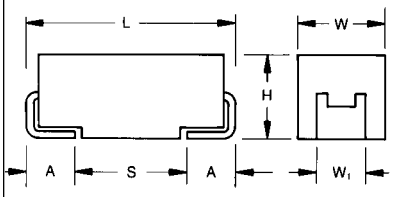
Available with standard capacitance tolerances of ±10% and ±20%.

Operational temperature -55°C to +85°C at rated voltage and up to +125°C with voltage derating in applications utilizing recommended series resistance.

TAJ is available in standard and extended ranges.

Note on sizes: A, B, C, D - EIA standard EIA-535BAAC
E - Extended range (high profile D case, 7343H EIA-535BAAC)
M, N - EIA-J standard

For CWR11 ratings see pages 19 - 21.



Case Dimensions millimeters (inches)

Code	EIA Code	W+0.2 (0.008) -0.1 (0.004)	L± 0.2 (0.008)	H+0.2 (0.008) - 0.1 (0.004)	W_1±0.2 (0.008)	A+ 0.3 (0.012) - 0.2 (0.008)	S Min.
A	3216	1.6 (0.063)	3.2 (0.126)	1.6 (0.063)	1.2 (0.047)	0.8 (0.031)	1.1 (0.043)
B	3528	2.8 (0.110)	3.5 (0.138)	1.9 (0.075)	2.2 (0.087)	0.8 (0.031)	1.4 (0.055)
C	6032	3.2 (0.126)	6.0 (0.236)	2.6 (0.102)	2.2 (0.087)	1.3 (0.051)	2.9 (0.114)
D	7343	4.3 (0.169)	7.3 (0.287)	2.9 (0.114)	2.4 (0.094)	1.3 (0.051)	4.4 (0.173)
E	7343H	4.3 (0.169)	7.3 (0.287)	4.1 (0.162)	2.4 (0.094)	1.3 (0.051)	4.4 (0.173)
M	4726*	2.6 (0.102)	4.7 (0.185)	2.1 (0.083)	1.4 (0.055)	0.8 (0.031)	2.7 (0.106)
N	5846*	4.6 (0.181)	5.8 (0.228)	3.2 (0.126)	2.4 (0.094)	1.3 (0.051)	2.8 (0.110)

W_1 dimension applies to the termination width for A dimensional area only.
*EIA-J Case Reference

How to Order: **TAJ** **C** **106** **M** **025** **R** ******

Type — TAJ

Case Code (See table above) — C

Capacitance Code — 106
pF code: 1st two digits represent significant figures, 3rd digit represents multiplier (number of zeros to follow)

Tolerance — M
K=±10%, M=±20%, (J=±5%, consult your AVX representative for details)

Rated DC Voltage — 025

Packaging/Leadframe Finish (Consult page 10 for details) — R

Additional characters may be added for special requirements — **

Technical Data:		All technical data relate to an ambient temperature of +25°C								
Capacitance Range:		0.1 µF to 330 µF								
Capacitance Tolerance:		±20%; ±10%								
Rated Voltage DC (V_R)	≦+85°C:	4	6.3	10	16	20	25	35	50	
Category Voltage (V_C)	+125°C:	2.7	4	7	10	13	17	23	33	
Surge Voltage (V_S)	≦+85°C:	5.2	8	13	20	26	32	46	65	
	+125°C:	3.2	5	8	12	16	20	28	40	
Temperature Range:		-55°C to +125°C								
Environmental Classification:		55/125/56 (IEC 68-2)								
Dissipation Factor:		≦0.04 for C_R ≦1.0 µF								
		≦0.06 for C_R >1.0 µF								
		≦0.08 for E case with C_R ≧100 µF								

TAJ Series — Solid Tantalum Chip Capacitors (EIA Standard)

Standard Range (EIA and EIA-J sizes). See below for extended range.

Capacitance Range (letter denotes case code)																	
Capacitance		Rated voltage DC (V_R) at 85°C															
µF	Code	4V		6.3V		10V		16V		20V		25V		35V		50V	
		Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.
0.1	104													A		A	
0.15	154													A		B	
0.22	224													A		B	
0.33	334													A		B	
0.47	474											A		B	M	C	
0.68	684									A		A		B	M	C	
1.0	105							A		A				B	M	C	
1.5	155					A		A				B	M	C		D	
2.2	225			A		A		B	M	B	M			C		D	
3.3	335	A		A				B	M	B	M	C		C		D	
4.7	475	A				B	M	B	M	C		C		D		D	
6.8	685			B	M	B	M	C		C		D		D	N		
10	106	B	M	B	M	C		C				D	N	D	N		
15	156	B	M	C		C				D		D	N				
22	226	C		C				D		D	N						
33	336	C				D		D	N								
47	476	D		D	N	D	N										
68	686	D		D	N												
100	107	D	N														

"Std" denotes EIA standard sizes
"Alt" denotes EIA J sizes

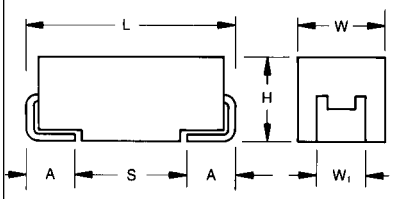
Extended Range/Developmental Range

Capacitance Range (letter denotes case code)									
Capacitance		Rated voltage DC (V_R) at 85°C							
µF	Code	4V	6.3V	10V	16V	20V	25V	35V	50V
0.1	104								
0.15	154								A
0.22	224								A
0.33	334								
0.47	474							A	
0.68	684							A	
1.0	105						A	A	
1.5	155					A	A	B M	
2.2	225				A		B	B M	
3.3	335			A	A		B	B	
4.7	475		A	A	A	A/B	B	C	
6.8	685	A	A	A	A/B		C	C	D
10	106	A	A	A/B	B M	B/C	C		
15	156	A	A/B	B	B/C	C		D	
22	226	A/B	B	B/C M	C	C	D	E	
33	336	B	B/C	C	C	D	E		
47	476	B/C M	C	C	D	D E			
68	686	C	C	D	D	E			
100	107	C	D	D	E				
150	157	D	D	D/E	E				
220	227	D	E	E					
330	337	E	E						

Ratings outside this matrix may be available upon request.
Please contact your AVX representative for availability of developmental range.

TAJ Series — Low Profile Solid Tantalum Chip Capacitors (EIA Standard)

Three additional case sizes are available in the TAJ range offering ultra low profile solid tantalum chip capacitors. Designed for applications where maximum height of components above or below board are of prime consideration, this height of 1.2mm equates to that of a standard integrated circuit package after mounting. Also available is the ultra compact 0805 equivalent in a fully molded package. The S&T footprints are identical to the A&B case size parts.



Case Dimensions millimeters (inches—Metric Dimensions Govern)

Code	EIA Code	W+0.2 (0.008) - 0.1 (0.004)	L±0.2 (0.008)	H max.	W_1±0.1 (0.004)	A+ 0.3 (0.012) - 0.1 (.004)	S Min.
0805 Equivalent							
R	2012	1.3 (0.05)	2.05 (0.08)	1.2 (0.047)	1.2 (0.047)	0.5 (0.020)	0.85 (0.033)
Low Profile Versions of A & B Case							
S	3216L	1.6 (0.06)	3.2 (0.12)	1.2 (0.047)	1.2 (0.047)	0.8 (0.031)	1.1 (0.043)
T	3528L	2.8 (0.11)	3.5 (0.14)	1.2 (0.047)	2.2 (0.087)	0.8 (0.031)	1.4 (0.055)

W_1 dimension applies to the termination width for A dimensional area only.
Pad Stand-off is 0.1±0.1.

Capacitance and Voltage Range (letter denotes case code)/Developmental Range

Capacitance		Rated voltage DC (V_R) at 85°C					
µF	Code	2V	4V	6.3V	10V	16V	20V
0.1	104						R/S
0.15	154						R/S
0.22	224						R/S
0.33	334						R/S
0.47	474						R/S
0.68	684					R/S	R/S/T
1.0	105				R/S	R/S	R/S/T
1.5	155			R/S	R/S	S	T
2.2	225		R/S	R/S	S	T	T
3.3	335		R/S	R/S	T	T	
4.7	475	R	R/S	S/T	T		
6.8	685	R	S/T	T			
10	106	S	T		T		

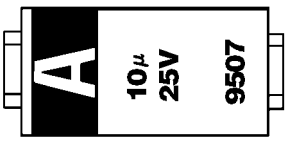
Please contact your AVX representative for availability of Developmental Range.

Marking: TAJ Series

For TAJ, the positive end of body has videcon readable polarity bar marking, with the AVX logo "A" as shown in the diagram. Bodies are marked by indelible laser marking on top surface with capacitance value, voltage and date of manufacture. Due to the small size of the A, B, M, R, S and T cases, a voltage code is used as shown below:

Voltage Code A, B, S and T Cases	Rated Voltage at 85°C
G	4
J	6.3
A	10
C	16
D	20
E	25
V	35
T	50

A, B, M, R, S and T Case:
1. Voltage Code (see table)
2. Capacitance in µF
3. Date Code



C, D, E and N Case:
1. Capacitance in µF
2. Rated Voltage at 85°C
3. Date Code

Polarity bar indicates anode (+) termination

Ratings and Part Number Reference

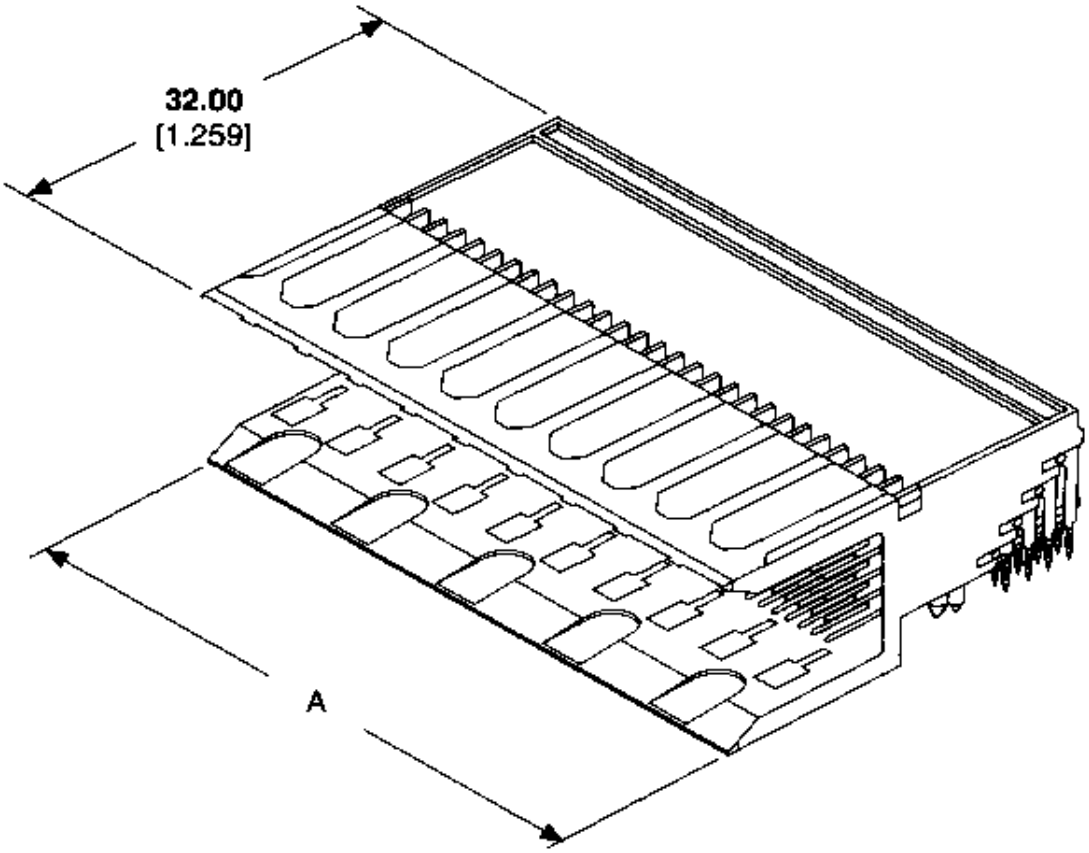
AVX Part No.	Case Size	Capacitance µF	DCL (µA) Max.	DF % Max.	ESR max. (Ω) @ 100 kHz
4 volt @ 85°C (2.5 volt @ 125°C)					
TAJA335(*)004	A	3.3	0.5	6	9.0
TAJA475(*)004	A	4.7	0.5	6	7.5
TAJA685(*)004	A	6.8	0.5	6	6.5
TAJA106(*)004	A	10	0.5	6	6.0
TAJB106(*)004	B	10	0.5	6	4.0
TAJM106(*)004	M	10	0.5	6	4.5
TAJA156(*)004	A	15	0.6	6	4.0
TAJB156(*)004	B	15	0.6	6	3.0
TAJM156(*)004	M	15	0.6	6	3.5
TAJA226(*)004	A	22	0.9	6	3.5
TAJB226(*)004	B	22	0.9	6	2.5
TAJC226(*)004	C	22	1.4	6	2.3
TAJB336(*)004	B	33	1.4	6	2.8
TAJC336(*)004	C	33	1.9	6	2.0
TAJB476(*)004	B	47	1.9	6	2.4
TAJC476(*)004	C	47	1.9	6	1.8
TAJD476(*)004	D	47	1.9	6	1.8
TAJC686(*)004	C	68	2.7	6	1.6
TAJD686(*)004	D	68	2.7	6	1.1
TAJC107(*)004	C	100	4.0	6	1.3
TAJD107(*)004	D	100	4.0	6	0.9
TAJN107(*)004	N	100	4.0	6	1.5
TAJD157(*)004	D	150	6.0	6	0.9
TAJE227(*)004	E	220	8.8	8	0.9
TAJE337(*)004	E	330	13.2	8	0.9
6.3 volt @ 85°C (4 volt @ 125°C)					
TAJA225(*)006	A	2.2	0.5	6	9.0
TAJA335(*)006	A	3.3	0.5	6	7.0
TAJA475(*)006	A	4.7	0.5	6	6.0
TAJA685(*)006	A	6.8	0.5	6	5.0
TAJB685(*)006	B	6.8	0.5	6	4.0
TAJM685(*)006	M	6.8	0.5	6	4.5
TAJA106(*)006	A	10	0.6	6	4.0
TAJB106(*)006	B	10	0.6	6	3.0
TAJM106(*)006	M	10	0.6	6	3.5
TAJA156(*)006	A	15	1.0	6	3.5
TAJB156(*)006	B	15	1.0	6	2.5
TAJC156(*)006	C	15	1.0	6	2.5
TAJM156(*)006	M	15	1.0	6	3.5
TAJB226(*)006	B	22	1.4	6	2.5
TAJC226(*)006	C	22	1.4	6	2.0
TAJB336(*)006	B	33	2.1	6	2.2
TAJC336(*)006	C	33	2.1	6	1.8
TAJC476(*)006	C	47	3.0	6	1.6
TAJD476(*)006	D	47	3.0	6	1.1
TAJC686(*)006	C	68	4.3	6	1.6
TAJD686(*)006	D	68	4.3	6	0.9
TAJD107(*)006	D	100	6.3	6	0.9
TAJD157(*)006	D	150	9.0	6	0.9
TAJE227(*)006	E	220	13.2	8	0.9
TAJE337(*)006	E	330	19.8	8	0.9

AVX Part No.	Case Size	Capacitance µF	DCL (µA) Max.	DF % Max.	ESR max. (Ω) @ 100 kHz
10 volt @ 85°C (6.3 volt @ 125°C)					
TAJA155(*)010	A	1.5	0.5	6	10.0
TAJA225(*)010	A	2.2	0.5	6	7.0
TAJA335(*)010	A	3.3	0.5	6	5.5
TAJA475(*)010	A	4.7	0.5	6	5.0
TAJB475(*)010	B	4.7	0.5	6	4.0
TAJM475(*)010	M	4.7	0.5	6	4.5
TAJA685(*)010	A	6.8	0.7	6	4.0
TAJB685(*)010	B	6.8	0.7	6	3.0
TAJM685(*)010	M	6.8	0.7	6	3.5
TAJA106(*)010	A	10	1.0	6	3.0
TAJB106(*)010	B	10	1.0	6	2.5
TAJM106(*)010	M	10	1.0	6	3.5
TAJC106(*)010	C	10	1.0	6	2.5
TAJB156(*)010	B	15	1.6	6	2.8
TAJC156(*)010	C	15	1.5	6	2.0
TAJB226(*)010	B	22	2.2	6	2.4
TAJC226(*)010	C	22	2.2	6	1.8
TAJC336(*)010	C	33	3.3	6	1.6
TAJD336(*)010	D	33	3.3	6	1.1
TAJC476(*)010	C	47	4.7	6	1.2
TAJD476(*)010	D	47	4.7	6	0.9
TAJN476(*)010	N	47	4.7	6	1.5
TAJD686(*)010	D	68	6.8	6	0.9
TAJD107(*)010	D	100	10.0	6	0.9
TAJE157(*)010	E	150	15.0	6	0.9
TAJE227(*)010	E	220	22.0	8	0.9
16 volt @ 85°C (10 volt @ 125°C)					
TAJA105(*)016	A	1.0	0.5	4	11.0
TAJA155(*)016	A	1.5	0.5	6	8.0
TAJA225(*)016	A	2.2	0.5	6	6.5
TAJB225(*)016	B	2.2	0.5	6	5.5
TAJM225(*)016	M	2.2	0.5	6	6.5
TAJA335(*)016	A	3.3	0.5	6	5.0
TAJB335(*)016	B	3.3	0.5	6	4.5
TAJM335(*)016	M	3.3	0.5	6	5.0
TAJA475(*)016	A	4.7	0.8	6	4.0
TAJB475(*)016	B	4.7	0.8	6	3.5
TAJM475(*)016	M	4.7	0.8	6	3.5
TAJB685(*)016	B	6.8	1.1	6	2.5
TAJC685(*)016	C	6.8	1.1	6	2.5
TAJB106(*)016	B	10	1.6	6	2.8
TAJM106(*)016	M	10	1.6	6	2.8
TAJC106(*)016	C	10	1.6	6	2.0
TAJB156(*)016	B	15	2.4	6	2.5
TAJC156(*)016	C	15	2.4	6	1.8
TAJC226(*)016	C	22	3.5	6	1.6
TAJD226(*)016	D	22	3.5	6	1.1
TAJD336(*)016	D	33	5.3	6	0.9
TAJN336(*)016	N	33	5.3	6	1.5
TAJD476(*)016	D	47	7.5	6	0.9
TAJD686(*)016	D	68	10.8	6	0.9
TAJE107(*)016	E	100	16.0	6	0.9

For 10% tolerance, insert 'K' in (*) above.
For 20% tolerance, insert 'M' in (*) above. (K tolerance may be supplied in lieu of M tolerance.)
NOTE: Voltage ratings are minimum values. We reserve the right to supply higher voltage ratings in the same case size, to the same reliability standards.

223513-1 -- *1 of 1 products*

High Speed Connectors
Z-PACK 2mm FB (Futurebus+) Connectors



Line art represents typical product only.

- Line Art
- Rec. PC Bd Hole Layout

Searchable Features:	
# of Positions	24
Mating Type	Receptacle Assembly
Connector Type	Free-Board (Receptacle)
Module Type	Signal
PCB Mount Angle	Right Angle
Post Length	.115 [2.92] in. [mm]
Post Type	Solder Post
Shunted	No
Other Properties:	
Dim. A	.468 [11.88] in. [mm]
Dim. B	.394 [10.00] in. [mm]
Centerline Spacing	.079 [2.00] x .079 [2.00] in. [mm]
Contact Material	Phosphor Bronze
Contact Mating Area Plating	Gold Flash over Palladium-Nickel
Solder Tail Plating	Tin-Lead
Housing Material	Liquid Crystal Polymer (LCP)

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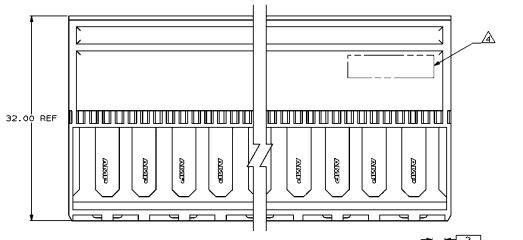
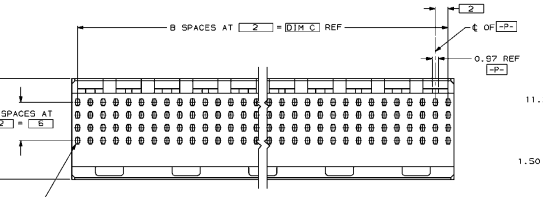
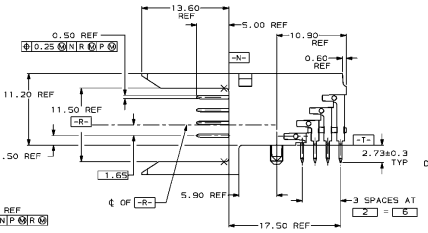
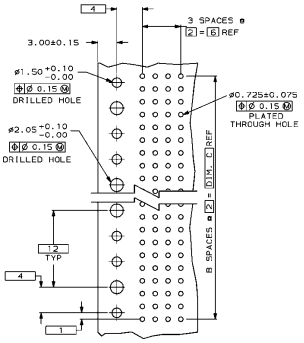
REVISIONS				
P	LTR	DESCRIPTION	DATE	DWN	APVD
	D	REVISED PER ECN 0503-0039-97	20JAN97	JDL	SAS



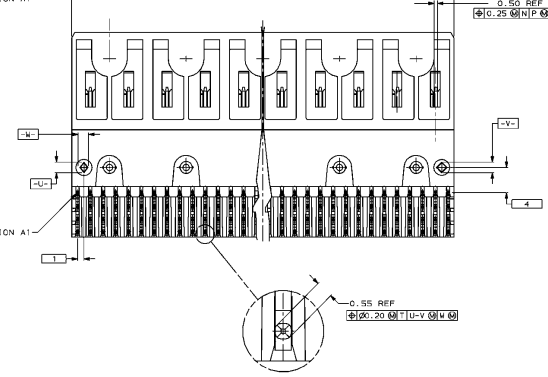
1. HOUSING MATERIAL: LIQUID CRYSTAL POLYMER
   COLOR: NATURAL.
2. CONTACT MATERIAL: PHOSPHOR BRONZE PER UNS ALLOY NO. C51100, TEMPER: H04.
3. CONTACT FINISH:
   UNDERPLATE (ENTIRE CONTACT)-
   0.0013 MIN NICKEL
   ON MATING SURFACES-
   FLASH GOLD PER AMP INCORPORATED SPECIFICATION, OVER
   0.0008 MIN PALLADIUM-NICKEL PER AMP INCORPORATED SPECIFICATION, OVER
   UNDERPLATE.
   ON LEADS-
   0.0039 MIN TIN-LEAD, OVER
   UNDERPLATE.
   SURFACE CONDITIONER PER AMP SPECIFICATION 112-1002(ENTIRE CONTACT AFTER PLATING).
4. PART MARKING LOCATED APPROXIMATELY AS SHOWN.
5. NOT RELEASED FOR PRODUCTION.
6. PART TO BE MARKED WITH DATE CODE ONLY.







RECOMMENDED CIRCUIT PATTERN
PER IPC-D300 TYPE II, CLASS C
(COMPONENT SIDE)



	C	B	A	NO. OF POSN	PART NUMBER
	34	17	35.88	72	223513-7
	58	29	59.88	120	223513-6
3	70	35	71.88	144	223513-5
5	94	47	55.88	192	223513-4
	46	23	47.88	96	223513-3
	22	11	23.88	48	223513-2
6	10	5	11.88	24	223513-1

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DR. J. BUCHESTER — DRAWN
CK. D. BATCHILE — CHECKED
APV. D. BATCHILE — APPROVED

AMP
AMP Incorporated
Harrisburg, PA 17105-3608

ASSEMBLY, PIN, SIGNAL, RIGHT ANGLE, 4 ROW, Z-PACK 2mm FB

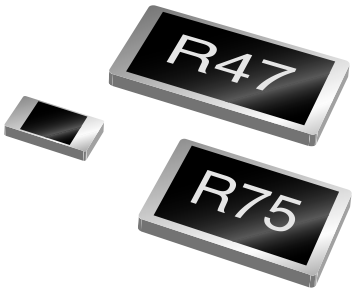
SIZE A1 | CODE IDENT 00779 | DRAWING NO 223513

CUSTOMER DRAWING | SCALE 4:1 | SHEET 1 OF 1 | REV D

Thick Film Chip Resistors

Type **ERJ**

ERJ, 2G, 3G, 6G, 8G, 14, 12, 1W



Features

- **Small size and lightweight**
  For PCB size reduction and lightweight products
- **High reliability**
  Metal glaze thick film resistive element and three layers of electrodes result in high reliability
- **Matching with placement machine**
  Bulk, taping, and bulk case packagings for automatic placement machine
- **Solderability**
  Suitable for both reflow soldering and flow soldering
- **High power**
  One rank up approval of power rating is available for 3G, 6G, 8G type
- Approved under the ISO-9001 system

Conforming to: IEC115-8, JIS C225

Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11	12
E	R	J	8	G	E	J	J	1	0	2	
Product Code			Power Rating			Marking	Resistance Tolerance	Nominal Resistance Value			Packaging

Product Code: Thick Film Resistor Networks

Power Rating

2GE	1/16W
3GS	1/16W
6GE	1/10W
8GE	1/8W
14	1/4W
12	1/2W
1W	1 W

Marking

Y	Value Marking on black side
Nil	No marking ★

Resistance Tolerance

J	±5%
K	±10%
0	Jumper

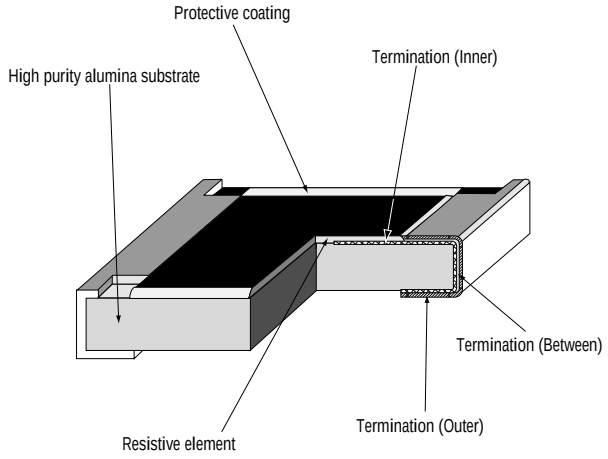
Nominal Resistance Value: The first two digits are significant figures of resistance value and the third one denotes the number of zeros following. Jumper is expressed by R00.

Packaging

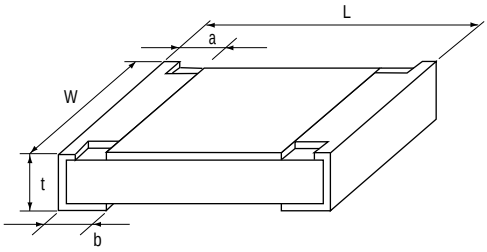
V	Std. taped and reel
U	Plastic embossed tape and reel
B	Bulk case
X	2mm pitch T. and R. (Only 2G, 3G type)

★ When omitted, the remaining part numbers shall be moved up respectively.

Construction



Dimensions in mm (not to scale)



Part No.	Dimensions L	W	a	b	t	Net Weight (1000 pcs.)
ERJ2GE	$1.00^{\pm0.05}$	$0.50^{\pm0.05}$	$0.20^{\pm0.10}$	$0.25^{\pm0.05}$	$0.35^{\pm0.05}$	0.8 g
ERJ3GS	$1.60^{\pm0.15}$	$0.80^{+0.05}_{-0.05}$	$0.30^{\pm0.20}$	$0.30^{\pm0.15}$	$0.45^{\pm0.10}$	2 g
ERJ6GE	$2.00^{\pm0.20}$	$1.25^{\pm0.10}$	$0.40^{\pm0.20}$	$0.40^{\pm0.20}$	$0.60^{\pm0.10}$	4 g
ERJ8G3	$3.20^{\pm0.20}$	$1.60^{+0.10}_{-0.05}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	10 g
ERJ14	$3.20^{\pm0.20}$	$2.50^{+0.10}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	16 g
ERJ12	$4.50^{\pm0.20}$	$3.20^{+0.10}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	27 g
ERJ1W	$6.40^{\pm0.20}$	$3.20^{+0.10}$	$0.65^{\pm0.20}$	$1.30^{\pm0.20}$	$1.10^{\pm0.10}$	79 g

Design and specifications are subject to change without notice. Ask factory for technical specifications before purchase and/or use.
Whenever a doubt about safety issues arises from this product, please inform us immediately for technical consultation.

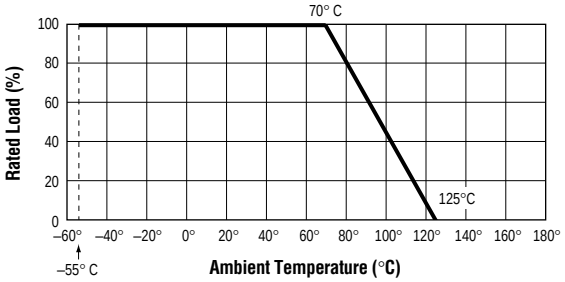
Ratings

	Power Rating at 70°C	Maximum RCWV*	Maximum Overload Voltage▲	Resistance Tolerance●	Resistance Range (Ω) min.	Resistance Range (Ω) max.	T.C.R. (ppm/°C)	Standard Resistance Values
ERJ2G	1/16W	50V	100V	±5	1.0	2.2 M		E-24
ERJ3G	1/16W (1/10W)◆	50V	100V	±5	1.0	10 M	<10Ω –100 to	E-24 E-12
ERJ6G	1/10W (1/8W)◆	150V 150V	200V 200V	±5 ±10	1.0 0.47	10 M 10 M	600	E-24 E-12
ERJ8G	1/8W (1/4W)◆	200V	400V	±5 ±10	1.0 0.39	10 M 10 M	100Ω to 1 MΩ	E-24 E-12
ERJ14	1/4W	200V	400V	±5 ±10	1.0 1.0	10 M 1.0 M	±200	E-24 E-12
ERJ12	1/2W	200V	400V	±5 ±10	1.0 1.0	10 M 1.0 M	1MΩ< –400 to	E-24 E-12
ERJ1W	1W	250V	500V	±5 ±10	10 1.0	1.0 M 1.0 M	+150	E-24 E-12

		Rated Current	Max. Overload Current
Jumper	2G • 3G	1.0A	2A
	6G • 8G • 14 • 12	2.0A	4A
	1W	2.5A	5A

* Rated Continuous Working Voltage (RCWV) shall be determined from RCWV = $\sqrt{\text{Power Rating x Resistance Value}}$, or max. RCWV listed above, whichever less.
◆ Available for reduction of load of pulse characteristics (RCWV x 2.5 RCW x 2.0, R≥1.1 kΩ)
● Available for ±1% or ±2% of resistance tolerance.
▲ Short-time Overload Test Voltage (SOTV) shall be determined from SOTV + 2.5 x Power Rating or max. Overload Voltage listed above whichever less.

Power Derating Curve
For resistors operated in ambient temperature above 70°C, power rating shall be derated in accordance with the figure to the right.



Packing Methods

Type	Thickness	Paper Taping (4mm pitch)	Embossed Taping (4mm pitch)	Bulk Case
ERJ2G	0.35	10,000 (2mm pitch)		50,000 pcs./case
ERJ3G	0.45	10,000 (2mm pitch)* 5,000, 10,000*, 20,000*		25,000 pcs./case
ERJ6G	0.60	5,000, 10,000*, 20,000*		10,000 pcs./case
ERJ8G	0.60	5,000, 10,000*, 20,000*		
ERJ14	0.60		5,000 pcs./reel	
ERJ12	0.60		5,000 pcs./reel (4mm pitch)	
ERJ1W	1.10		3,000 pcs./reel (4mm pitch)	

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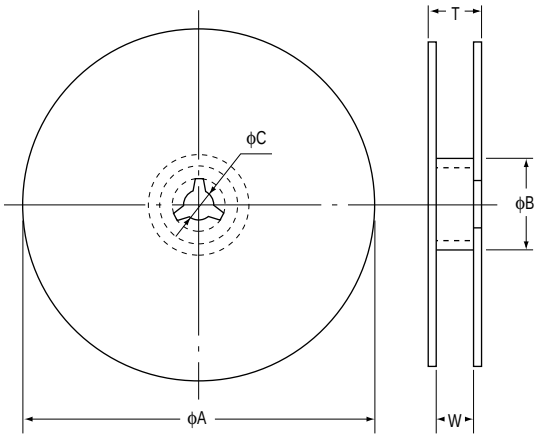
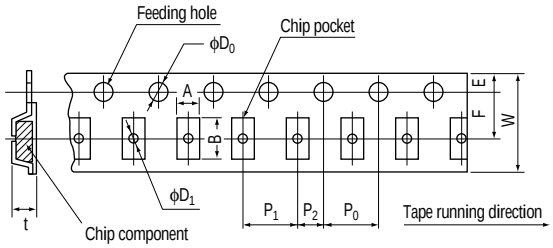
■ Packaging Methods *(cont'd)*

Taping Reel



	Dimensions				
	ϕA	ϕB	ϕC	W	T
2G, 3G, 6G, 8G, 14	$180.0^{+0}_{-3.0}$	60 min.	$13.0^{\pm1.0}$	$10.0^{\pm1.0}$	$12.0^{\pm2.0}$
12, 1W				$14.0^{\pm1.0}$	$16.0^{\pm2.0}$

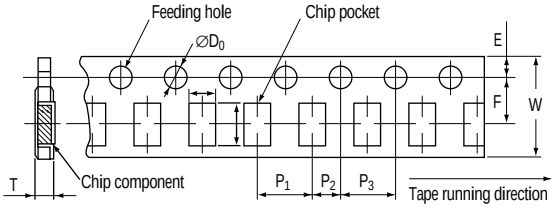
Embossed Taping



	Dimensions					
Type	A	B	W	F	E	P_1
14	$2.80^{\pm0.05}$	$3.50^{\pm0.20}$	$8.00^{\pm0.30}$	$3.50^{\pm0.05}$	$1.75^{\pm0.10}$	$4.00^{\pm0.10}$
12	$3.50^{\pm0.20}$	$4.80^{\pm0.20}$	$12.0^{\pm0.30}$	$5.50^{\pm0.05}$		$8.00^{\pm0.20}$
1W	$3.60^{\pm0.20}$	$6.90^{\pm0.20}$				$8.00^{\pm0.20}$

Type	P_2	P_0	ϕD0	t	ϕD1
14	$2.00^{\pm0.10}$	$4.00^{\pm0.10}$	$1.50^{\pm0.10}$	$1.00^{\pm0.10}$	1.00
12					1.50 min.
1W				$1.60^{\pm0.10}$	

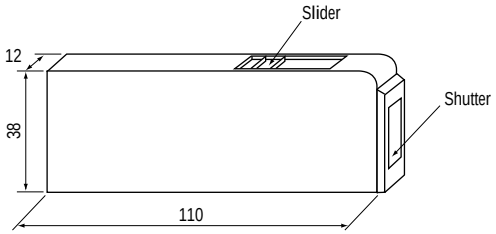
Paper Taping



	Dimensions				
Type	A	B	W	F	E
2G	$0.70^{\pm0.05}$	$1.20^{\pm0.20}$	$8.00^{\pm0.20}$	$3.50^{\pm0.05}$	$1.75^{\pm0.10}$
3G	$1.10^{\pm0.10}$	$1.90^{\pm0.10}$			
6G	$1.60^{\pm0.15}$	$2.40^{\pm0.20}$			
8G	$1.90^{\pm0.15}$	$3.50^{\pm0.20}$			

Type	P_1	P_2	P_0	ϕD0	t_2
2G	$2.00^{\pm0.10}$	$2.00^{\pm0.05}$	$4.00^{\pm0.10}$	$1.50^{+0.10}$	$0.45^{\pm0.05}$
3G	$4.00^{\pm0.10}$				$0.64^{\pm0.05}$
6G					$0.84^{\pm0.05}$
8G					$0.84^{\pm0.05}$

Bulk Case



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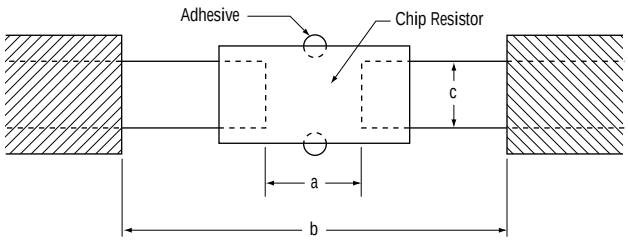
Whenever a doubt about safety issues arises from this product, please inform us immediately for technical consultation.

■ Safety Precautions

In the case of flow soldering, the land width must be smaller than the Chip Resistor width to control the solder amount properly. Generally, the land width should be chip resistor width (W) 0.7 to 0.8 times of the width of chip resistor. In the case of reflow soldering, solder amount can be adjusted, therefore the land width should be set to 1.0 to 1.3 times chip resistor width (W).



	Dimensions		
Part No.	**a**	**b**	**c**
ERJ2G	0.5 to 0.6	1.4 to 1.6	0.4 to 0.6
ERJ3G	0.7 to 0.9	2.0 to 2.2	0.8 to 1.0
ERJ6G	1.0 to 1.4	3.2 to 3.8	0.9 to 1.4
ERJ8G	2.0 to 2.4	4.4 to 5.0	1.2 to 1.8
ERJ14	2.0 to 2.4	4.4 to 5.0	1.8 to 2.8
ERJ12	3.3 to 3.7	5.7 to 6.5	2.3 to 3.5
ERJ1W	3.6 to 4.0	7.6 to 8.6	2.3 to 3.5

1. If transient load (heavy load in a short time) like pulse is expected to be aplied, carry out evaluation and confirmation tset with the resistors actually mounted on your own board.

   When the load of more than rated power is applied under the load condition at a steady rate, it may impair performance and/or reliability of resistor. Never exceed the rated power.
2. Chlorine-type or other high-activity flux is not recommended as the residue may affect performmance or reliability of resistors.
3. When soldering with soldering iron, never tough the body of the chip resistor with the tip of the soldering iron. When using a soldering iron with a tip at high temperature, solder for a time as short as possible (three seconds or less up to 350°C.)
4. Avoid physical shock to the resistor and nipping of the resistor with hard tool (a pair of pliers or tweezers) as it may damage protective film or the body of resistor and may affect resistor's performance.

Design and specifications are subject to change without notice. Ask factory for technical specifications before purchase and/or use.
Whenever a doubt about safety issues arises from this product, please inform us immediately for technical consultation.

1.25mm (.049") Pitch Wire-to-Board - Crimp Terminal, 50058 / 50079

Reference Information

- Packaging: **Chain or loose**
- Use With: **Receptacle Housing 51021**
- Designed In: **Millimeters**

Electrical

- Voltage: **125V**
- Current: **1.0A (0.8A for 32 AWG)**
- Contact Resistance: **20mΩ max.**
- Dielectric Withstanding Voltage: **250V AC/1 min.**
- Insulation Resistance: **100 MΩ min.**

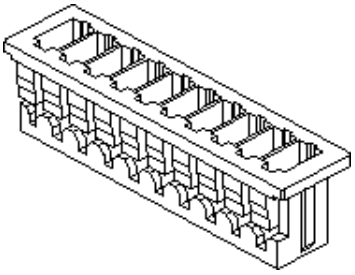
Physical

- Contact: **Phosphor Bronze**
- Plating: **Tin**
- Wire Range: **50058-28 to 32 AWG 50079-26 to 28 AWG**
- Insulation Range: **1.00mm dia. max.**
- Strip Length: **1.40 to 1.90mm**

Top, Front, Side View

ORDERING INFORMATION								
Order No.	**Term-inal**	**Wire Range AWG**	**Automatic Tooling**		**Mini-Mac Applicator**	**TM-40/42 Crimp Die**	**Hand Tool**	**Extractio Tool**
			Press	**Crimp Die**				
50058-8000 50079-8000	Chain	28 - 32	M15A 57117-4000	57067-3000	11-18-2154	11-40-2245	-	57072-600
		26 - 28					-	
50058-8100 50079-8100	Loose	28 - 32	-	-	11-18-2156	-	57068-5000	
		26 - 28					57177-5000	

1.25mm (.049") Pitch Wire-to-Board - Receptacle Housing, 51021



Reference Information

- Packaging: **Bag**
- UL File No.: **E29179**
- CSA File No.: **LR19980**
- Mates With: **Headers Straight 53047, Right Angle 53048, SMT Straight 53398, SMT Right Angle 53261 and Wire-to-Wire Plug 51047**
- Use With: **Terminals 50058 and 50079**
- Designed In: **Millimeters**

Electrical

- Voltage: **125V**
- Current: **1.0A (0.8A for 32 AWG)**
- Contact Resistance: **20mΩ max.**
- Dielectric Withstanding Voltage: **250V AC/1 min.**
- Insulation Resistance: **100 MΩ min.**

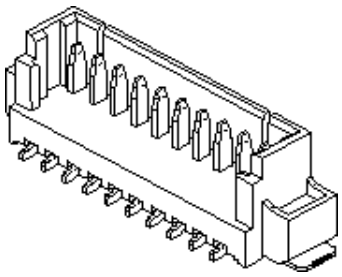
Physical

- Housing: **PBTP, UL 94V-0**
- Temperature: **-40 to +85°C**

Top, Front, Side View

ORDERING INFORMATION AND DIMENSIONS			
Circuits	**Order No.**	**Dimension**	
		A	**B**
2	51021-0200	4.25 (.167)	2.95 (.116)
3	51021-0300	5.50 (.217)	4.20 (.165)
4	51021-0400	6.75 (.266)	5.45 (.215)
5	51021-0500	8.00 (.315)	6.70 (.264)
6	51021-0600	9.25 (.364)	7.95 (.313)
7	51021-0700	10.50 (.413)	9.20 (.362)
8	51021-0800	11.75 (.463)	10.45 (.411)
9	51021-0900	13.00 (.512)	11.70 (.461)
10	51021-1000	14.25 (.561)	12.95 (.510)
11	51021-1100	15.50 (.610)	14.20 (.559)
12	51021-1200	16.75 (.659)	15.45 (.608)
13	51021-1300	18.00 (.709)	16.70 (.657)
14	51021-1400	19.25 (.758)	17.95 (.707)
15	51021-1500	20.50 (.807)	19.20 (.756)

1.25mm (.049") Pitch Wire-to-Board - Header, SMT, Straight, 53398



Reference Information

- Packaging: **Embossed tape**
- Mates With: **Crimp Housing 51021**
- Designed In: **Millimeters**

Electrical

- Voltage: **125V**
- Current: **1.0A (0.8A for 32 AWG)**
- Contact Resistance: **20mΩ max.**
- Dielectric Withstanding Voltage: **250V AC/1 min.**
- Insulation Resistance: **100 MΩ min.**

Physical

- Housing: **Glass-filled 4/6 nylon, UL 94V-0**
- Contact: **Phosphor Bronze**
- Plating: **Tin/Lead**
- Temperature: **-40 to +85°C**

Top, Front, Side View

ORDERING INFORMATION AND DIMENSIONS								
Circuits	**Order No.**	**Dimension**						**Tape Width**
		A	**B**	**C**	**D**	**E**	**F**	
2	53398-0290	1.25 (.049)	3.05 (.120)	2.35 (.092)	4.25 (.167)	7.25 (.285)	7.65 (.301)	16.00 (.630)
3	53398-0390	2.50 (.098)	4.30 (.169)	3.60 (.141)	5.50 (.216)	8.50 (.334)	8.90 (.350)	
4	53398-0490	3.75 (.147)	5.55 (.218)	4.85 (.190)	6.75 (.265)	9.75 (.383)	10.15 (.399)	24.00 (.945)
5	53398-0590	5.00 (.196)	6.80 (.267)	6.10 (.240)	8.00 (.314)	11.00 (.433)	11.40 (.448)	
6	53398-0690	6.25 (.246)	8.05 (.316)	7.35 (.289)	9.25 (.364)	12.25 (.482)	12.65 (.498)	
7	53398-0790	7.50 (.295)	9.30 (.366)	8.60 (.338)	10.50 (.413)	13.50 (.531)	13.90 (.547)	
8	53398-0890	8.75 (.344)	10.55 (.415)	9.85 (.387)	11.75 (.462)	14.75 (.580)	15.15 (.596)	
9	53398-0990	10.00 (.393)	11.80 (.464)	11.10 (.437)	13.00 (.511)	16.00 (.629)	16.40 (.645)	
10	53398-1090	11.25 (.442)	13.05 (.513)	12.35 (.486)	14.25 (.561)	17.25 (.679)	17.65 (.694)	
11	53398-1190	12.50 (.492)	14.30 (.562)	13.60 (.535)	15.50 (.610)	18.50 (.728)	18.90 (.744)	32.00 (1.260)
12	53398-1290	13.75 (.541)	15.55 (.612)	14.85 (.584)	16.75 (.659)	19.75 (.777)	20.15 (.793)	
13	53398-1390	15.00 (.590)	16.80 (.661)	16.10 (.633)	18.00 (.708)	21.00 (.826)	21.40 (.842)	
14	53398-1490	16.25 (.639)	18.05 (.710)	17.35 (.683)	19.25 (.757)	22.25 (.875)	22.65 (.891)	44.00 (1.732)
15	53398-1590	17.50 (.688)	19.30 (.759)	18.60 (.732)	20.50 (.807)	23.50 (.925)	23.90 (.940)	

TEC PS Revision Components

No	Device	DeviceDescription	AdditionalDescription	DeviceDecal	Manufacturer	Mfgr Part Number	Distributor1	Dist. 1 Part Number	Qtyperboard
1	Capacitor	Multilayer Ceramic Chip Capacitor	0.1uF	0603	Johansen	160R14Z104MV	M.S. Hi-Tech	160R14Z104MV	62
2	Capacitor	Multilayer Ceramic Chip Capacitor	0.01uF	0603	PANASONIC	ECU-V1H103KBV	Digikey	PCC103BVCT-ND	1
3	Capacitor	Multilayer Ceramic Chip Capacitor	220pF	0603	PANASONIC	ECU-V1H221JCV	Digikey	PCC221ACVCT-ND	1
4	Capacitor	Multilayer Ceramic Chip Capacitor	0.033uF	0402	Johansen	160R07Z333MV	Semi-Dice	160R07Z333MV	20
5	Capacitor	Multilayer Ceramic Chip Capacitor	47pF	0805	Johansen	160R15N470FV	M.S. Hitech	160R15N470FV	1
6	Capacitor	Multilayer Ceramic Chip Capacitor	390pF	0805	Johansen	160R15N391FV	M.S. Hitech	160R15N391FV	1
7	Capacitor	Tantalum Electrolytic Capacitor	1uF	3216	AVX	TAJA105K016R	Allied Electronics	213-1000	14
8	Capacitor	Tantalum Electrolytic Capacitor	4.7uF	3528	AVX	TAJB475K010R	Allied Electronics	213-6116	12
9	Capacitor	Tantalum Electrolytic Capacitor	10uF	6032	AVX	TAJC106K016R	Allied Electronics	213-1008	2
10	Connector	2mm ZPACK Future Bus Connector	24 pins	223513-1	AMP Inc.	223513-1		223513-1	4
11	DAC	DAC for Calibration of Preamp-Shaper	12 Bit	SO16M1	Analog Devices	DAC8562FS	M.S Hitech	DAC8562FS	1
12	DIGITAL ID	Digital ID and Temperature Sensor	Aux. Device	S08M1	Dallas Semi.	DS1624		DS1624	1
13	Diode	Dual Diodes for ESD on CMOS Inputs	Common Anode	SOT23D	ZETEX	BAW56ZX	Digikey	BAW56ZXCT-ND	16
14	Diode	Ouput Short Circuit protection on LM337T		SOD-87	Diodes Inc.	DL4002	Digikey	DL4002CT-ND	1
15	EMI Filter	Multiple Inductor Pack	6	BLA41B01	Murata-Erie	BLA41B01T1	Standard Radio Corp.	BLA41B01T1	2
16	Ferrite Bead	Inductor for Power Supply Filtering	500 mA rated	1805	Murata-Erie	BLM41A800SPT	Standard Radio Corp.	BLM41A800SPT	2
17	Ferrite Bead	Inductor for Power Supply Filterin	3A rated	1805	Murata-Erie	BLM41P750SPT	Standard Radio Corp.	BLM41P750SPT	2
18	FUSE	Polyswitch Fuse	750mA Trip,FUSE	MSMD075	Raychem	miniSMD075-2	Digikey	MINISMD075CT-ND	2
19	FUSE	Polyswitch Fuse	2A Trip, FUSE	SMD200	Raychem	SMD200-2	Digikey	SMD200CT-ND	2
20	HEADER	2 pin SIP Hdr. for Ext. Calib Pulse input	0.1"	SIP-2P	Sullins	S1012-36	Digikey	S1012-36-ND	1
21	HEADER	2 pin SIP Header as Jumper	0.1"	SIP-2P	Sullins	S1012-36	Digikey	S1012-36-ND	3
22	HEADER	1.25mm MOLEX SMT HEADERS	4 pins	53398-0490	Molex	53398-0490	Digikey	WM1766-ND	1
23	HEADER	1.25mm MOLEX SMT HEADERS	8 pins	53398-0890	Molex	53398-0890	Digikey	WM1770-ND	1
24	HEADER	1 Pin header for test points	Test Pads						5
25	HEADERS	IDC Headers for 0.025" TPC	80 conductors	845-A080P-ALA55	Amphenol	845-A080P-ALA55	Sager	845-A080P-ALA55	2
26	INVERTER	Schmitt Trigger Inverter	HEX	SO14M1	National Semi.	MM74HC14M	Digikey	MM74HC14M-ND	1
27	LDO	Negative LDO for -5.0V	3A rated	TO-220/5	Linear Tech.	LM1185-CT	Marshall Industries	LT1185-CT	1
28	LDO	LDO for +5.0 V	3A rated	TO-263	Micrel	MIC29300-5.0BU	Harwood Associates	MIC29300-5.0BU	1
29	LDO	LDO for -2.50 V	750mA	TO-263/5	Micrel	MIC29372BU	Harwood Associates	MIC29372BU	1
30	Line Driver	RS-422 Line Driver	Quad	SO16M1	National Semi.	DS26C31TM	Digikey	DC26C31TM-ND	2
31	Line Rcvr.	RS-422 Line Receiver	Quad	SO16M1	National Semi.	DS26C32ATM	Digikey	DS26C32ATM-ND	1
32	MOSFET	N-Channel DMOS FET for Calib. Switch		SOT143	TEMIC/Siliconix	SST211	M.S Hitech	SST211	1
33	OPAMP	Line Driver Opamps	Quad	SO14M1	Analog Devices	AD8044AR-R14	M.S. Hitech	AD8044AR-R14	16
34	PLD	PLD for serial link for the TEC-PS board	15ns	QFP44-5	Altera	EPM7032QC44-15	Wyle Electronics	EPM7032QC44-15	1
35	Regulator	Neg. Adj. Voltage Regulator for -2.5V	1.5A rated	TO-220	National Semi.	LM337T	Digikey	LM337T-ND	1
36	Resistor	5% Thick Film Chip Resistor	1K ohm	0402	Panasonic	ERJ-2GEJ102	Digikey	P1.0KJCT-ND	1
37	Resistor	5% Thick Film Chip Resistor	47K Ohm	0402	Panasonic	ERJ-2GEJ473	Digikey	P1.0MJCT-ND	1
38	Resistor	1% Thick Film Chip Resistor	2.37K ohm	0603	Panasonic	ERJ-3EKF2371	Digikey	P2.37KHCT-ND	1
39	Resistor	1% Thick Film Chip Resistor	2.67K ohm	0603	Panasonic	ERJ-3EKF2671	Digikey	P2.67KHCT-ND	1
40	Resistor	1% Thick Film Chip Resistor	6.81K ohm	0603	Panasonic	ERJ-3EKF6811	Digikey	P6.81KHCT-ND	1
41	Resistor	5% Thick Film Chip Resistor	10.0K ohm	0603	Panasonic	ERJ-3GSYJ103	Digikey	P10.0KGCT-ND	2
42	Resistor	1% Thick Film Chip Resistor	24.9 ohm	0402	Panasonic	ERJ-2RKF24R9	Digikey	P24.9LCT-ND	32
43	Resistor	5% Thick Film Chip Resistor	51.1 ohm	0402	Panasonic	ERJ-2GEJ510	Digikey	P51JCT-ND	1
44	Resistor	1% Thick Film Chip Resistor	102K ohm	0603	Panasonic	ERJ-3EKF1023	Digikey	P102KHCT-ND	1
45	Resistor	1% Thick Film Chip Resistor	105K ohm	0603	Panasonic	ERJ-3EKF1053	Digikey	P105KHCT-ND	1
46	Resistor	1% Thick Film Chip Resistor	121 ohm	0603	Panasonic	ERJ-3EKF1210	Digikey	P121HCT-ND	2
47	Resistor	1% Thick Film Chip Resistor	60.4 ohm	0402	Panasonic	ERJ-2RKF60R4	Digikey	P60.4LCT-ND	132
48	TECPS	TEC CMOS PREAMP SHAPER CHIPS	IC31A	MQFP64-M108	Hewlett Packard		MOSIS		4