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Low-Noise Monolithic and Hybrid CMOS-Based Sensors

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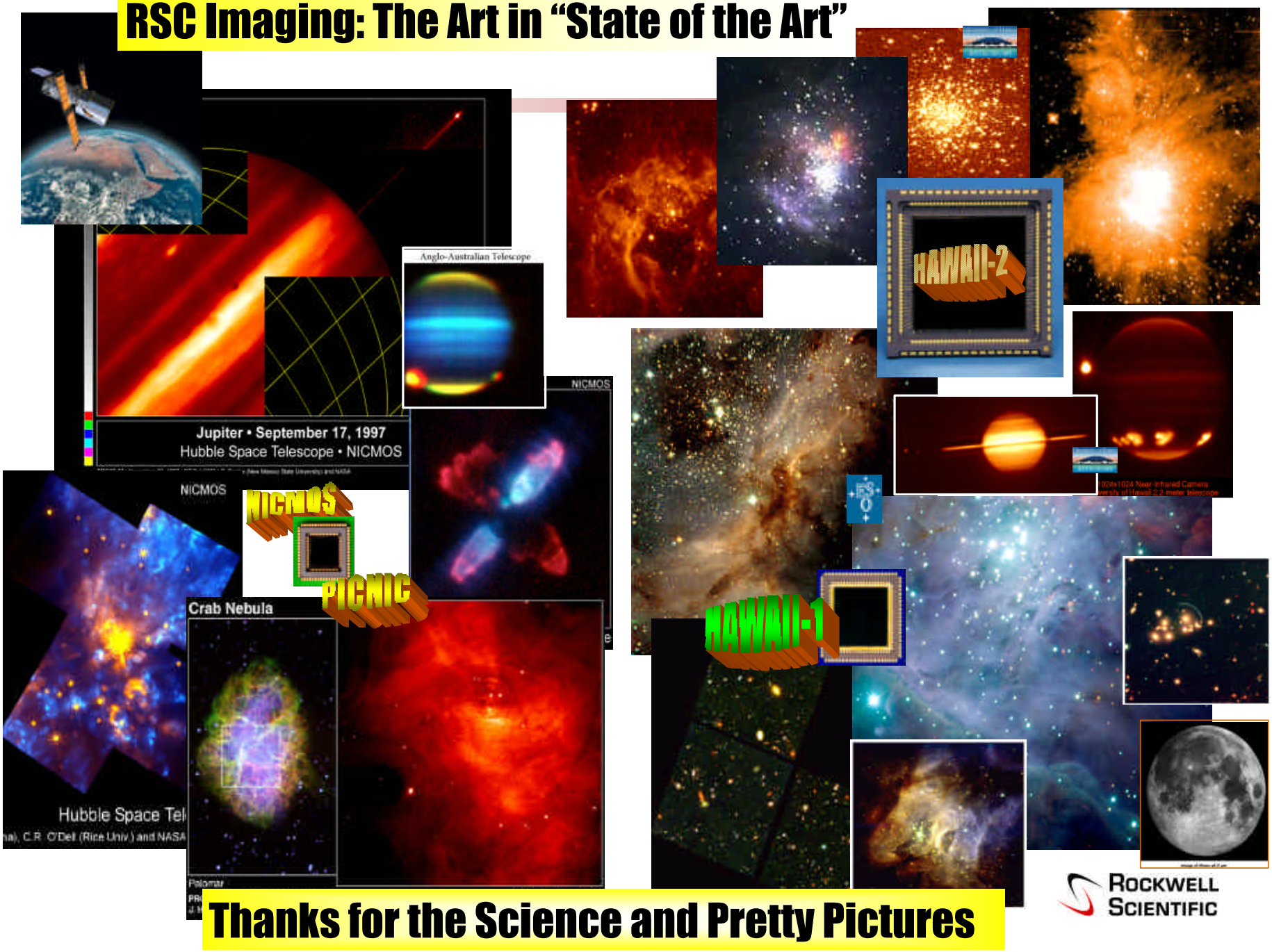
Outline

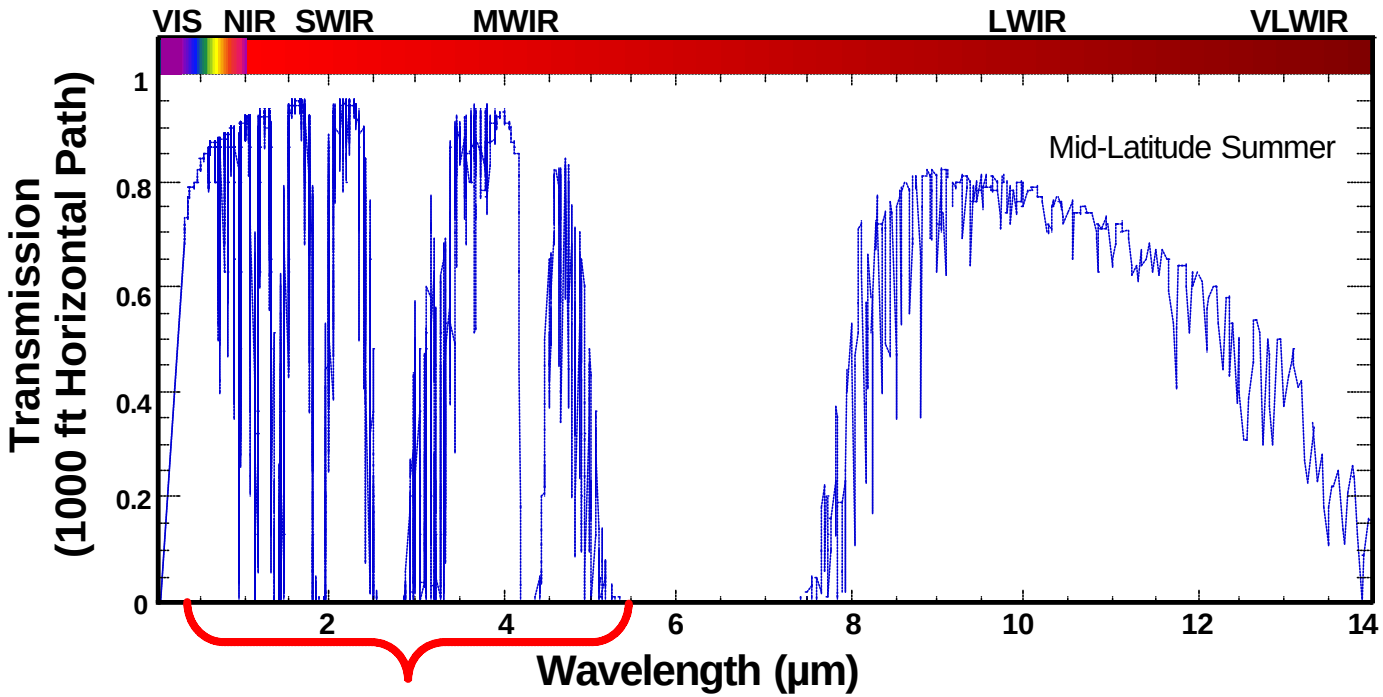
- Introduction
- Large Infrared Sensors
  - HAWAII-2 (2048^2) is Proliferating
  - HAWAII-2RG Development Well Underway
    - Reference Pixels, Guide Mode, Even Simpler Interface
- Visible Sensors
  - Hybrid Visible Silicon Imager (HyViSI)
    - 1st HAWAII-2 Hybrid
  - Monolithic CMOS (Front-Side Illuminated For Now)
    - Imaging System-on-Chip (SoC) with 12-b Digital Output
      - ProCam-1: 1936x1088, 5µm Pitch, 20e- at 75 MHz
    - Coming Soon?: 15.3 Mpixel

RSC Imaging: The Art in "State of the Art"



Thanks for the Science and Pretty Pictures

Detector Candidates for Astronomy



- Visible to l_{co}: MBE $Hg_xCd_{1-x}Te$ with Substrate Removed
- ~0.85µm to l_{co}: $Hg_xCd_{1-x}Te$ (MBE or PACE)
- VUV to 1.1µm with High Quantum Efficiency: HyViSI
- UV to 1.1µm: Monolithic CMOS

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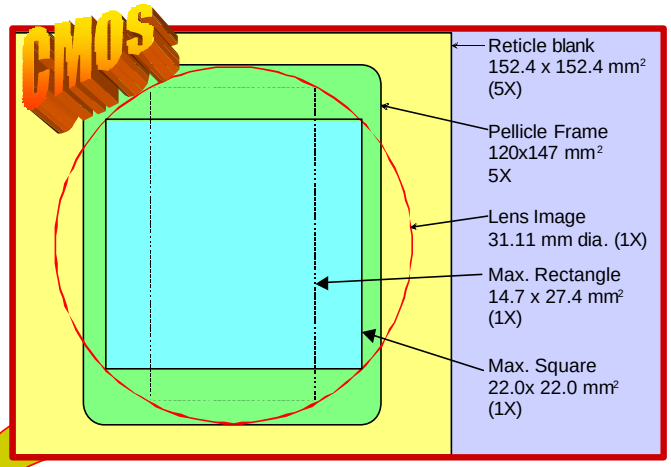
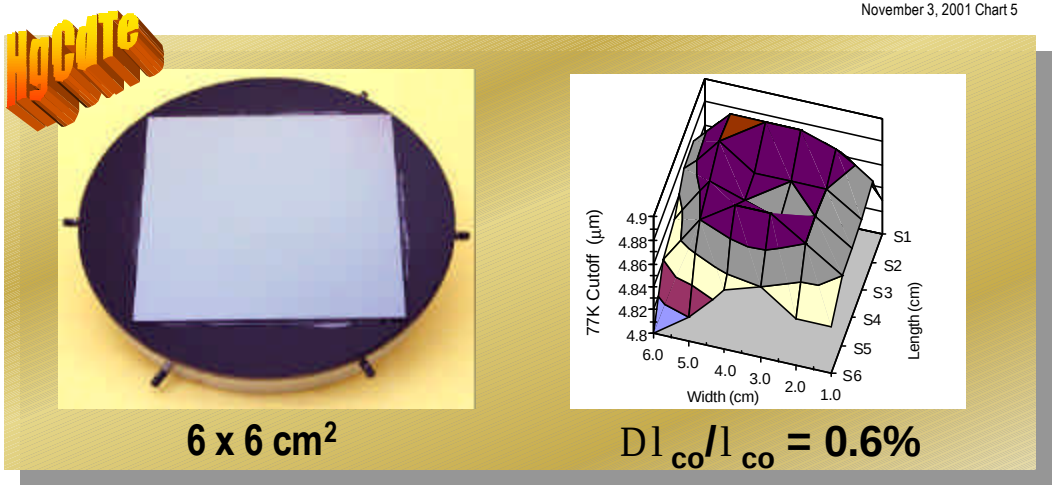
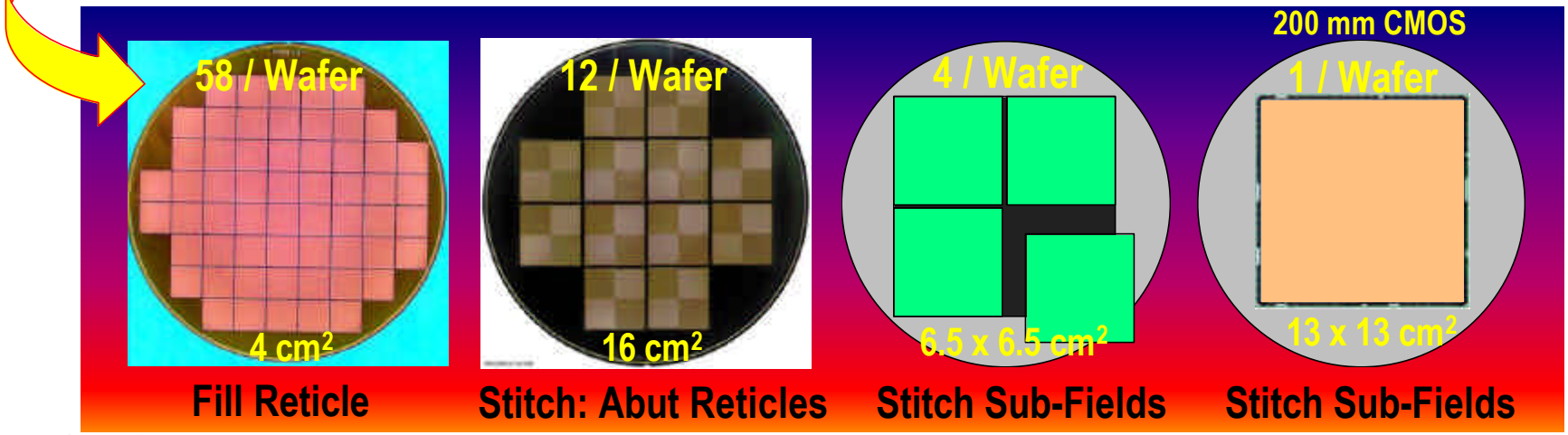
Risk, Cost & Size for Large Sensors







	Fill Reticle	Stitch: Abut Reticles	Stitch Sub-Fields	Stitch Sub-Fields	
IR/HyViSI:	1M-2M	2M-4M	4M-10M	10M-45M	pixels
CMOS (Vis):	1M-30M	4M-100M	£225M	£1000M	

Increasing Risk, $ (NRE & Prototypes) and Resolution

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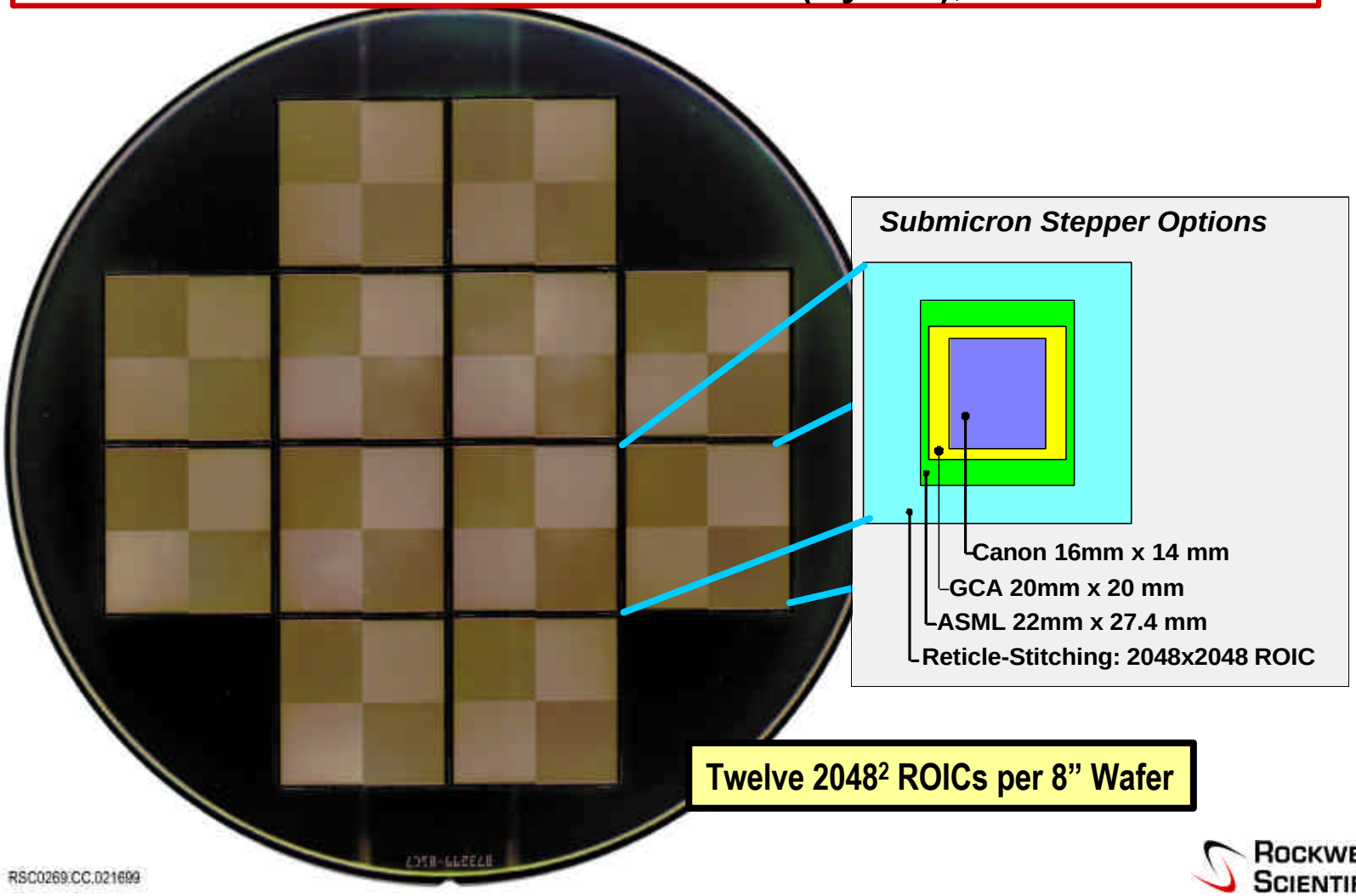
HAWAII 2048^2: Four Optical fields $\Rightarrow$ 1 ROIC

2048^2 Readout Can be Used for Visible (HyViSI), SWIR and MWIR



Twelve 2048^2 ROICs per 8" Wafer

RSC0269.CC.021699

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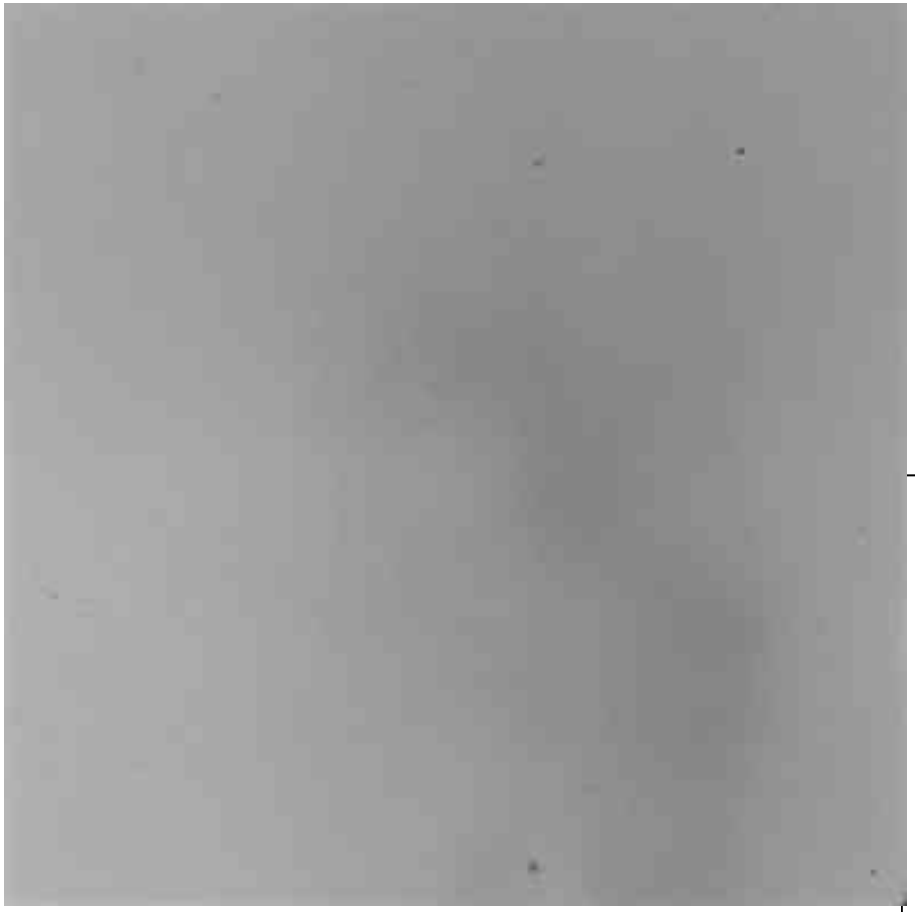
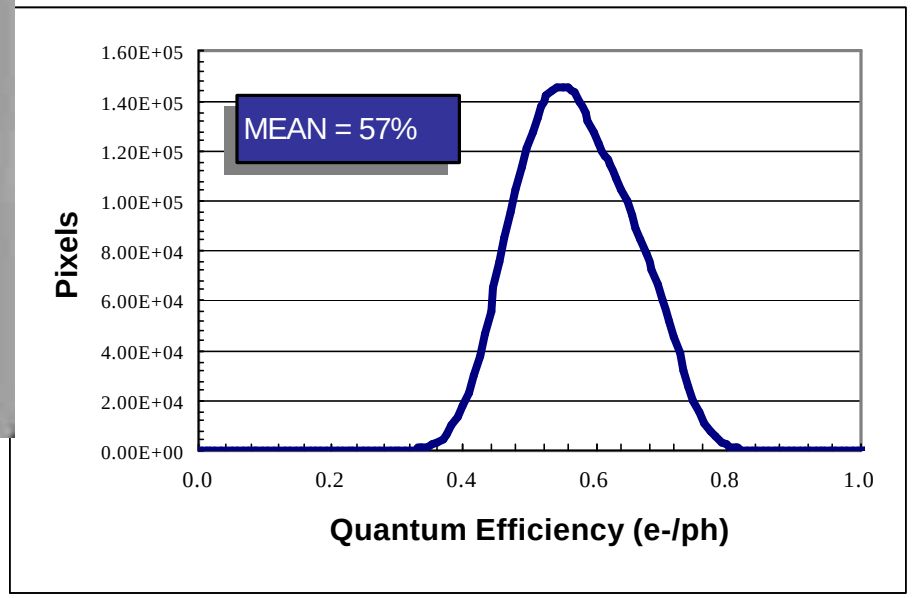
H-Band QE of 2048^2 PACE HgCdTe Array



l : 1.5mm - 1.8mm
FPA Temperature =78K



QE>25%: 99.95%

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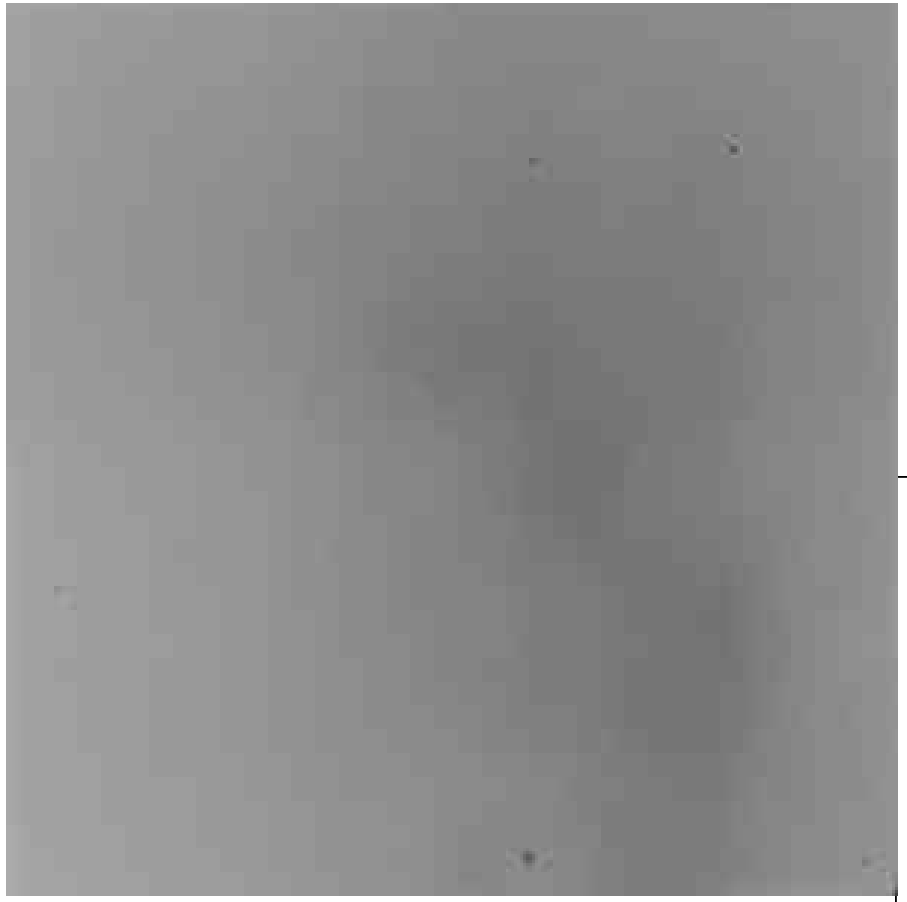
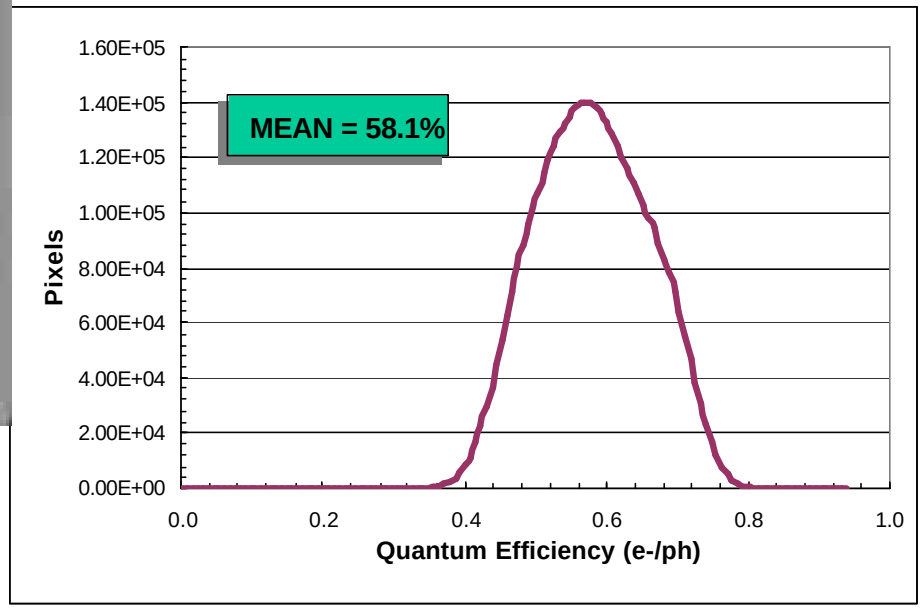
K-Band QE of 2048^2 PACE HgCdTe Array



l : 2.0mm - 2.4mm
FPA Temperature = 78K



QE>25%: 99.97%

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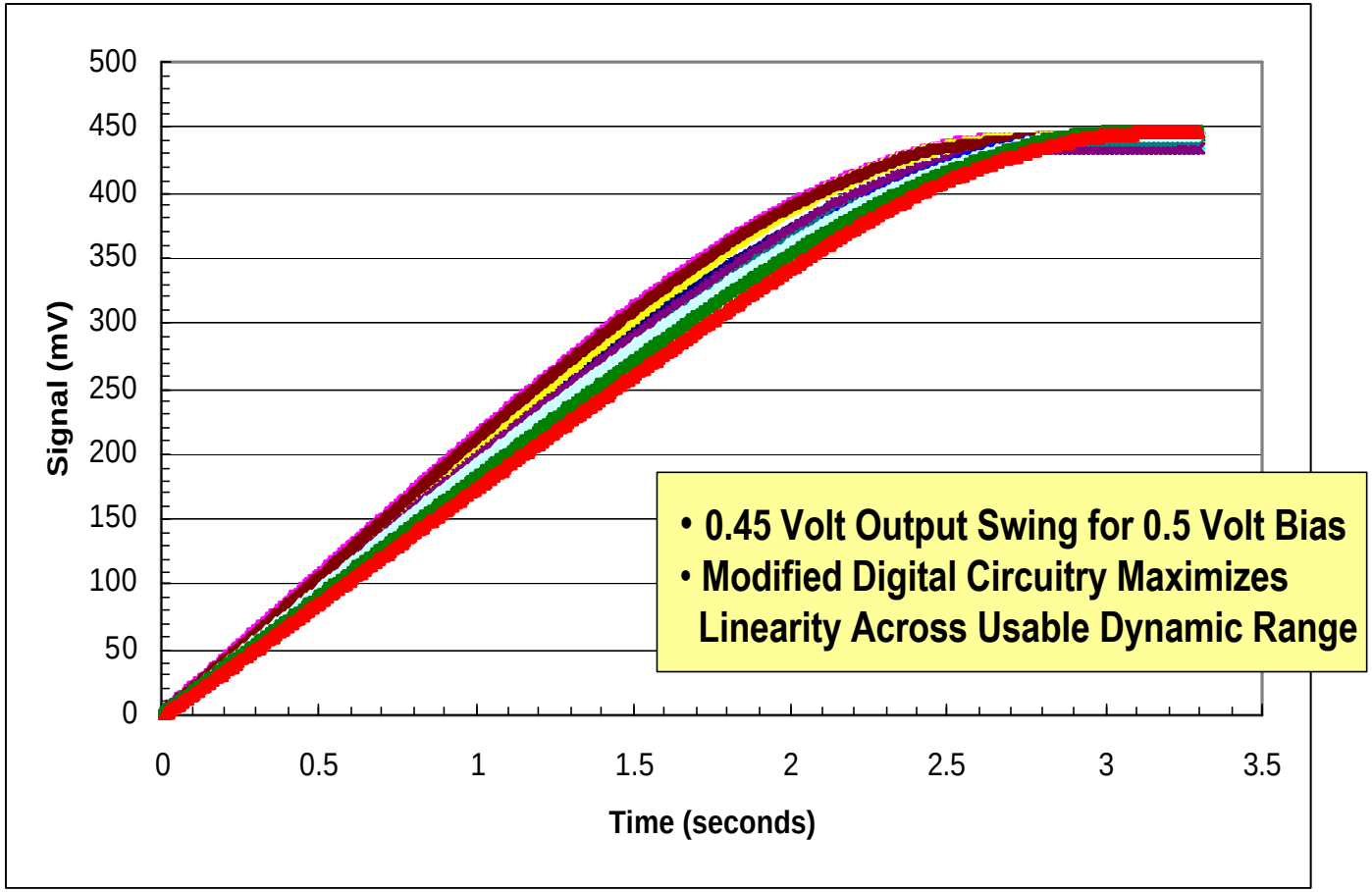
2.5µm PACE: <2% Nonlinearity Across 120ke-



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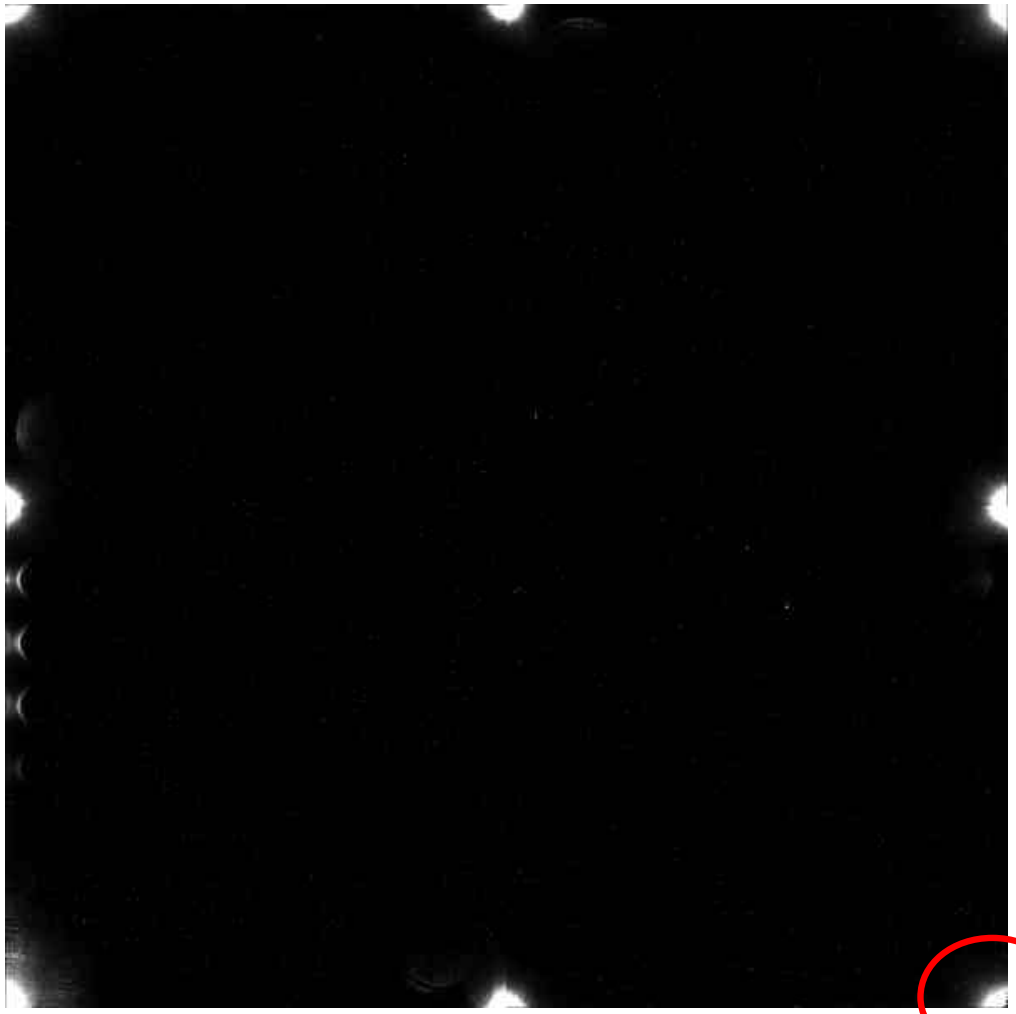
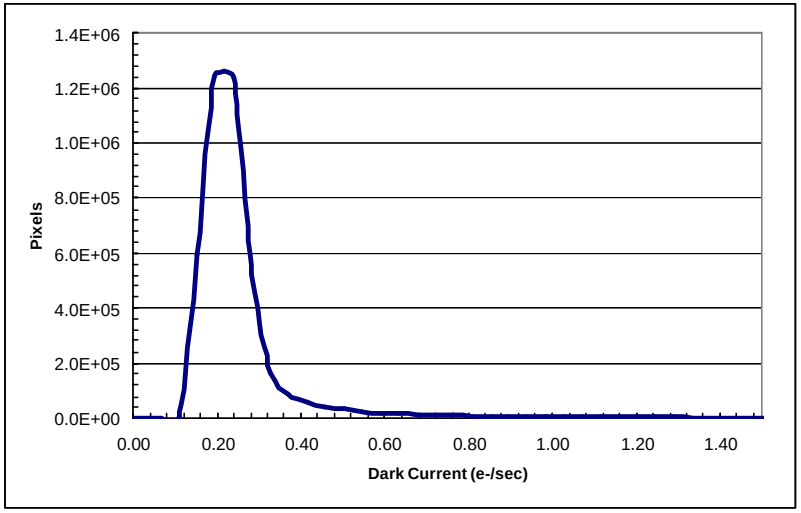
2.5µm PACE: I_{dark} @ 78K: On-Chip Amps



I_{dk} = .311 e-/sec

>98.5% of the Pixels < 2 e-/sec



Highest emission is about 35 e-/sec

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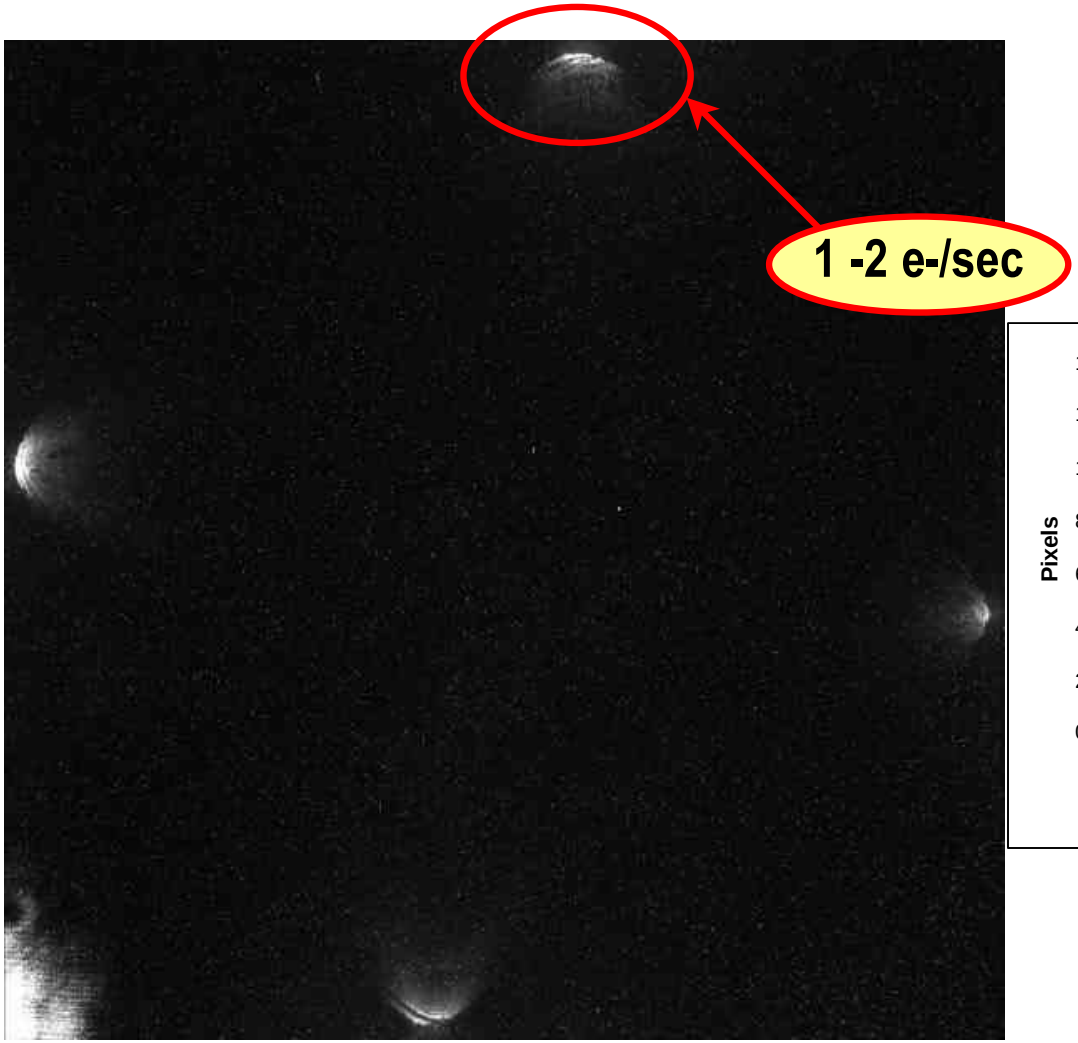
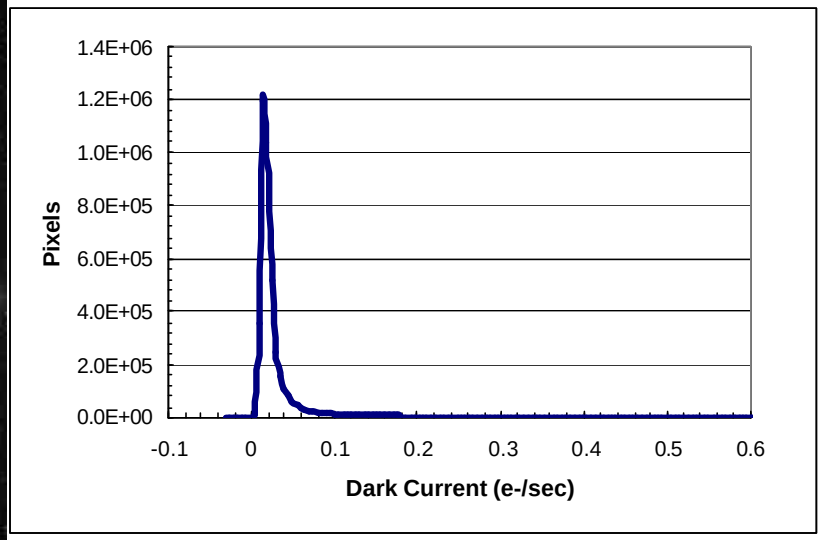
2.5µm PACE: I_{dark} @ 78K: Off-Chip Amps



I_{dark} = 0.026 e-/sec
99.36% of the Pixels < 1e-/sec



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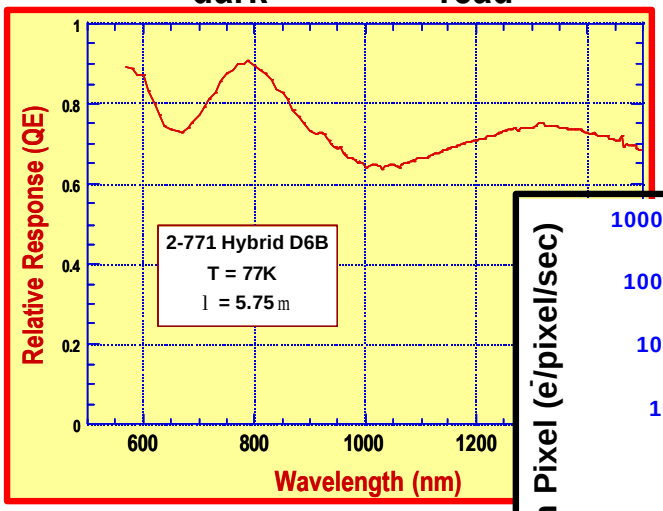
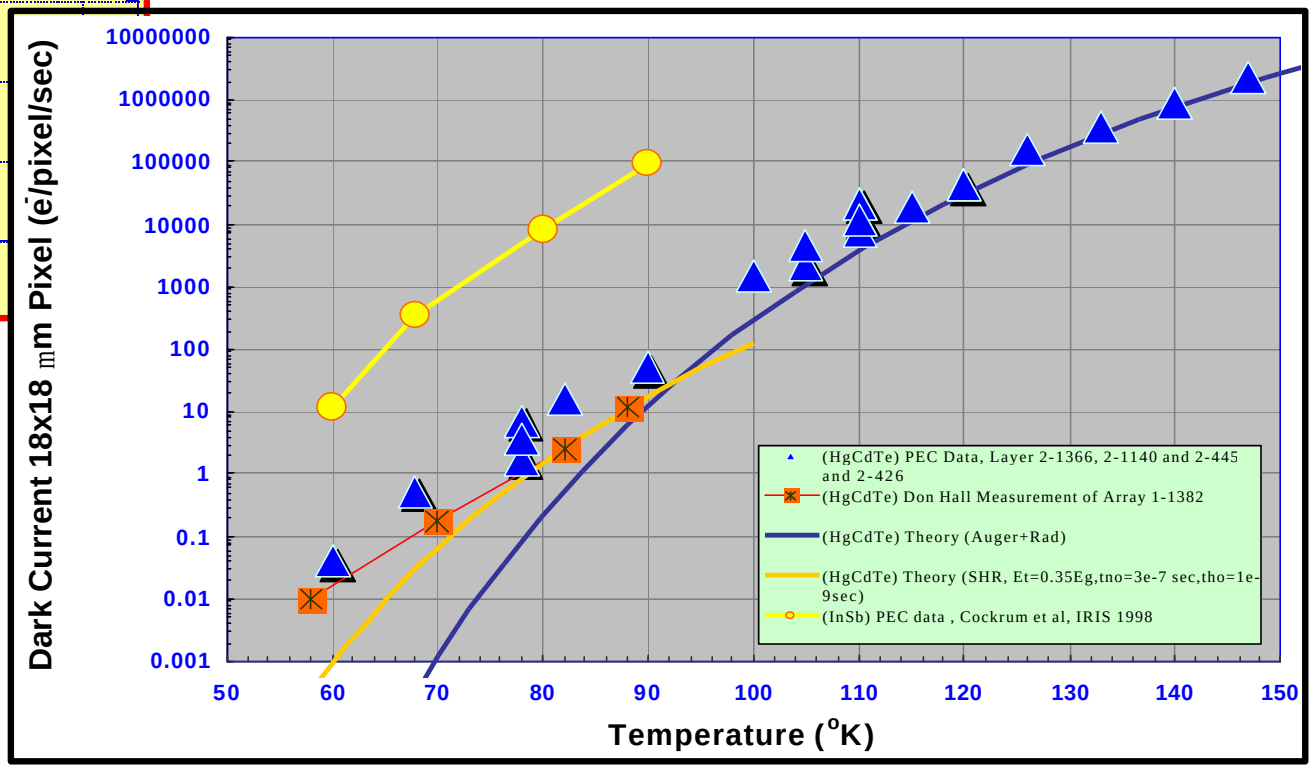
MWIR-Vis: Meets All NGST Specs at ~55K

- I_{dark}, h & N_{read} Unchanged After Substrate Removal





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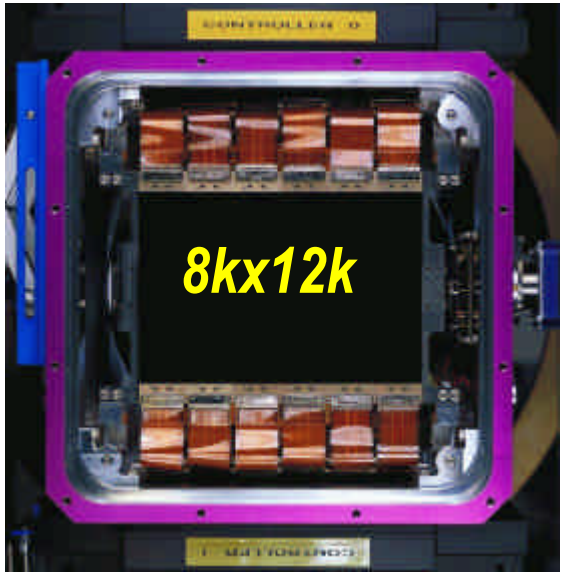
Candidate Visible Sensor Technologies

- **Packaging of Many-Sensor Mosaic Strongly Suggests CMOS Content to Enable Practical System Solution with Digital I/O**

CCD

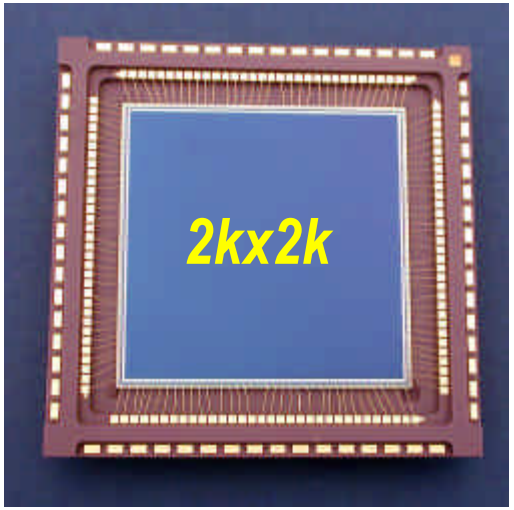


- Low Noise
- High QE
- Many Wire Interface
- High Power

CMOS i-SoC

- Low-Moderate Noise
- High Visible QE
- High MTF
- Simple Interface
- Low Power

HyViSI: Si/CMOS



- Low Noise
- High QE
- Simple Interface
- Low Power

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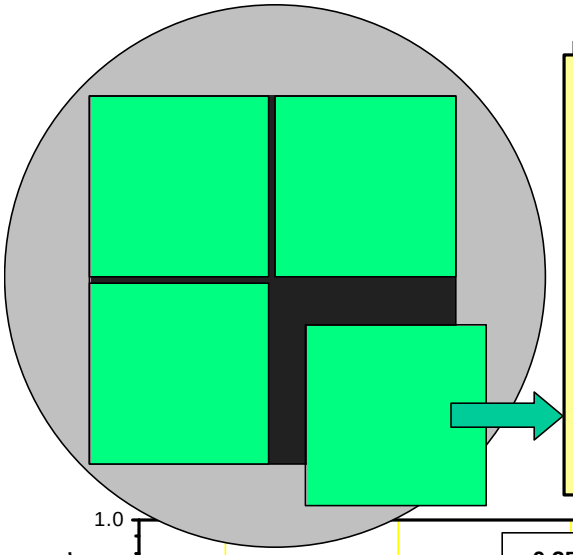
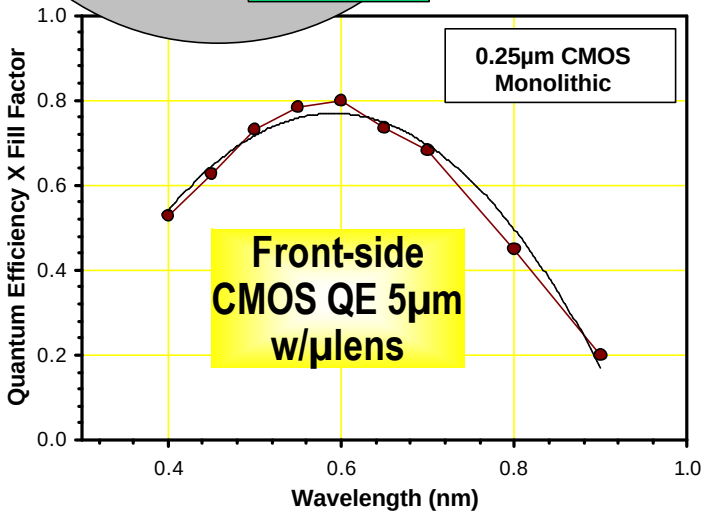
MegaPixel Visible a la CMOS Readout

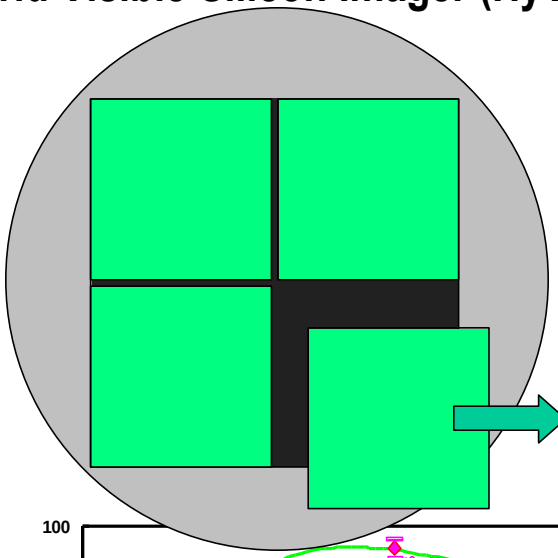
Monolithic CMOS



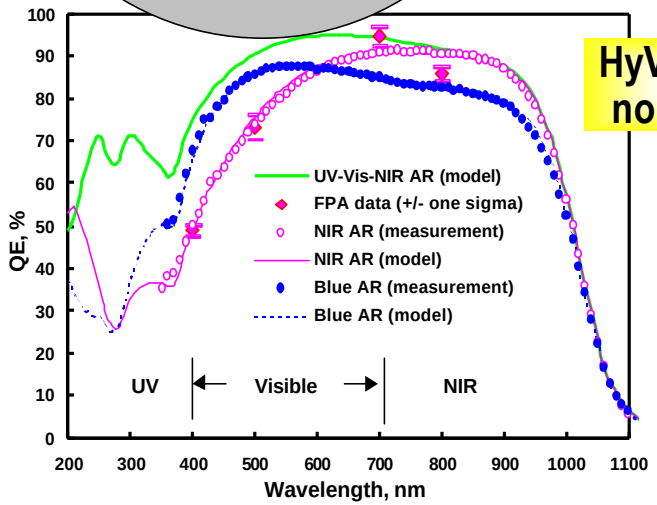
- 64 Million Pixels
- CMOS System-on-Chip
- 7.4µm Pitch
- 2 mW/Mpix/sec
- DR ³ 70 dB
- on-chip 12-bit A/D
- Superb MTF
- Read Noise £15 e-
- FPN £1 LSB
- 30 fps
- 294K
- High Programmability
- 4 Die per 8-inch Wafer



Hybrid Visible Silicon Imager (HyViSI)



- 16 Million Pixels
- CMOS System-on-Chip
- 13 µm Pitch
- 2 mW/Mpix/sec
- DR ³ 70 dB
- on-chip 12-bit A/D
- Read Noise £5 e-
- FPN £1 LSB
- 100 fps
- 294K
- High Programmability
- 4 Die per 8-inch Wafer



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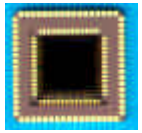
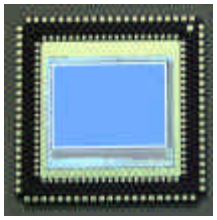
HyViSI Development Chronology

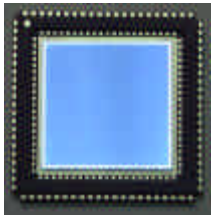
- 18µm Pitch: Proven
- 13.3µm: Soon
- ~10µm: 1 to 2 Years?



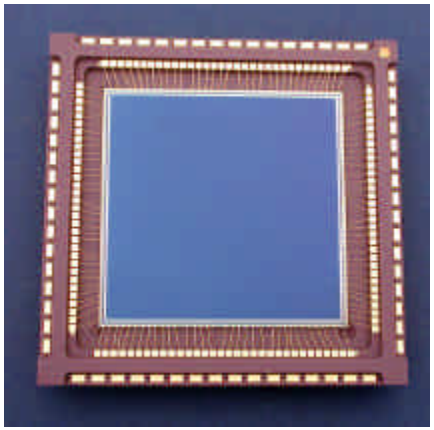
TCM2620 128X128
40mm pitch



TCM6600 640X480
27mm pitch



Hawaii 1024X1024
18.5 mm pitch



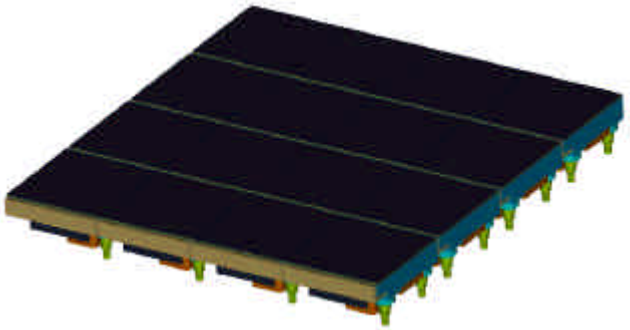
Hawaii 2048X2048
18 mm pitch

1998 1999 2000 2001

Not too Distant Future:

4x4 Mosaic

8k x 8k Pixels w/ASIC



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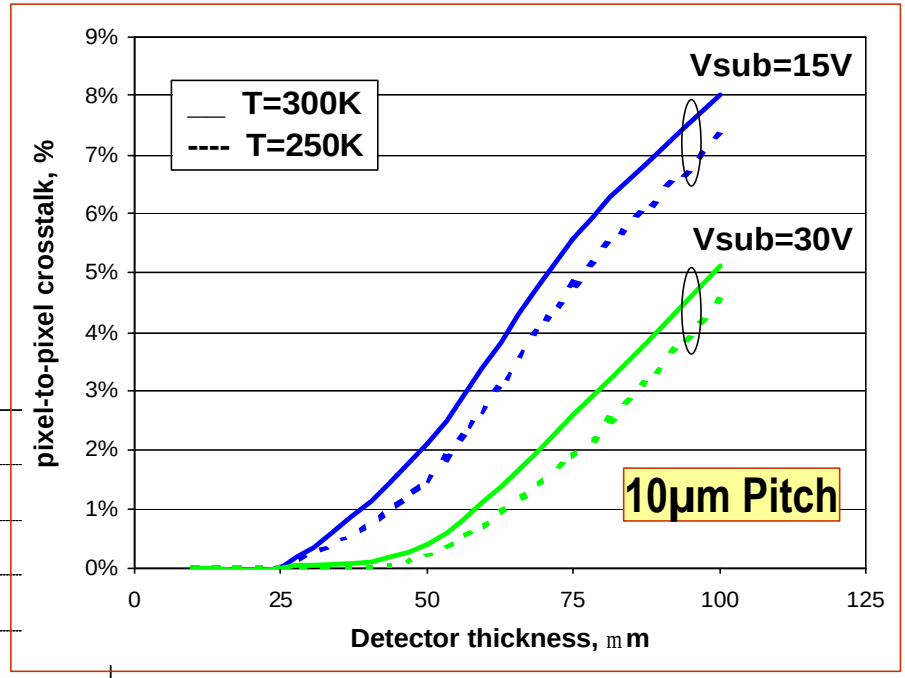
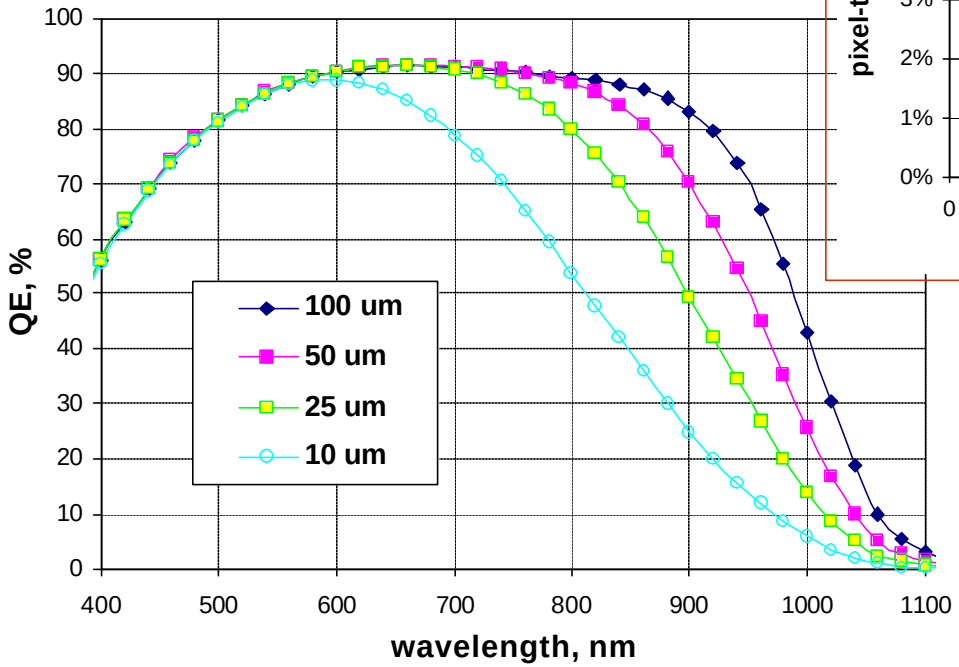
HyViSI: Trade NIR QE vs. Crosstalk

- e.g., Targeting 70% QE at 900 nm vs. <2% Crosstalk for "~10µm Pitch"





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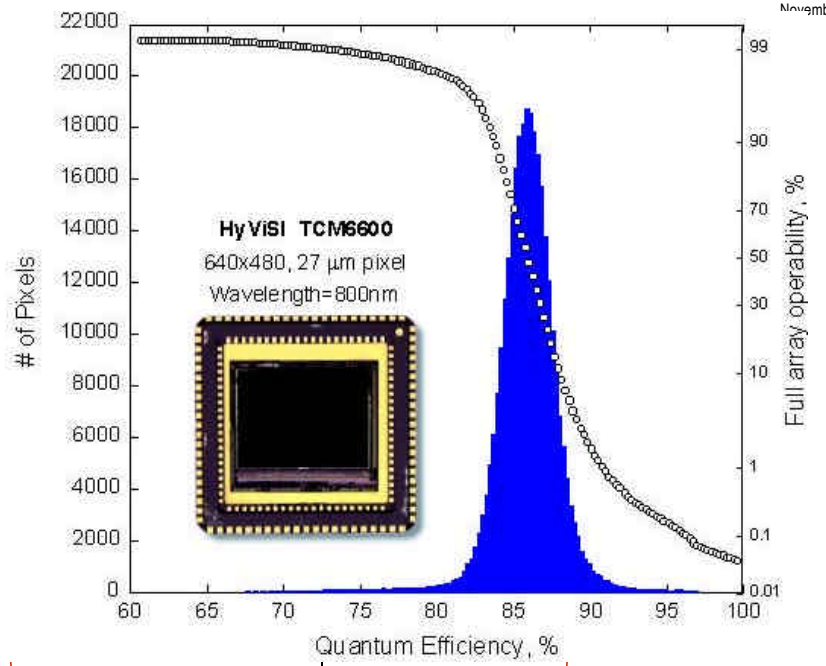
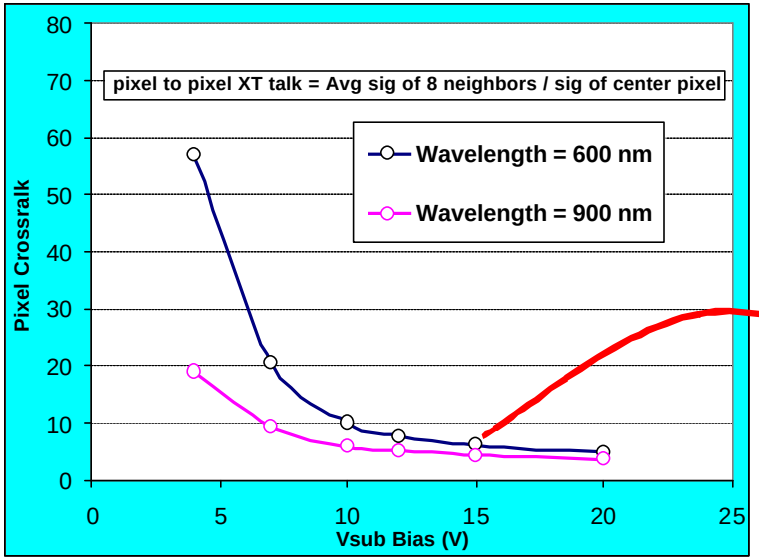
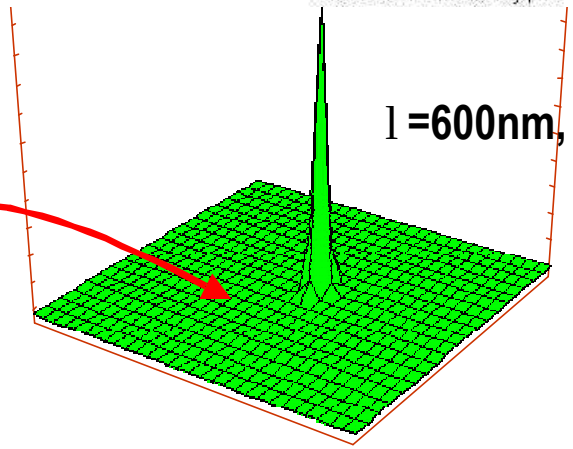
HyViSI 640x480 @ 27µm Pitch







l =600nm, 15V bias

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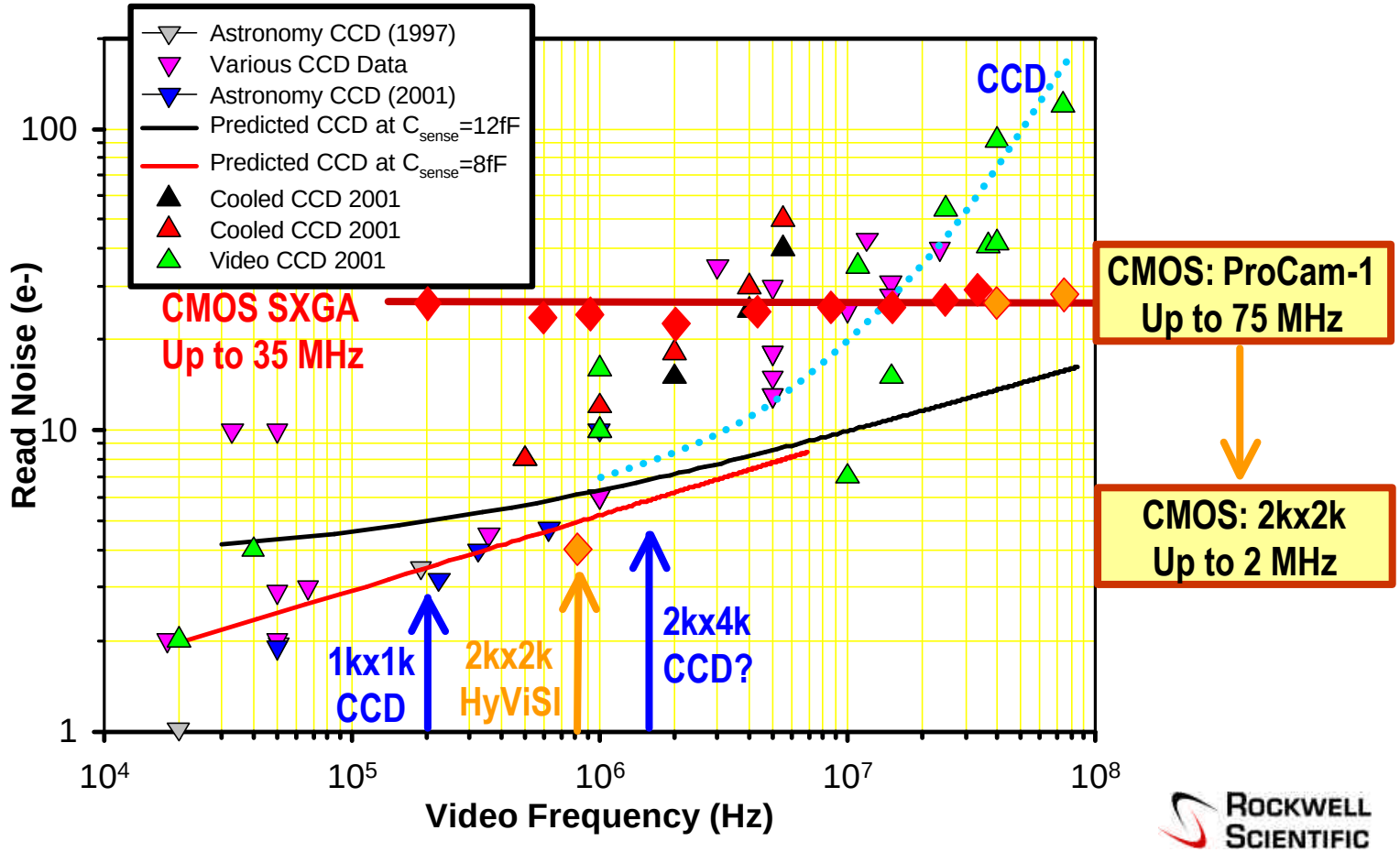
CCD: <5e- at 200kps; CMOS: 4e- at 800kps

- But, 1400 1kx1k CCDs Likely Poses Packaging Nightmare
- And, 175 2kx4k CCDs Still Reresents Very Difficult Packaging & 10-20 e- Noise
- Alternatively, 350 2kx2k HyViSI at 5e- w/ASIC (or *i*-SoC) Ease Packaging



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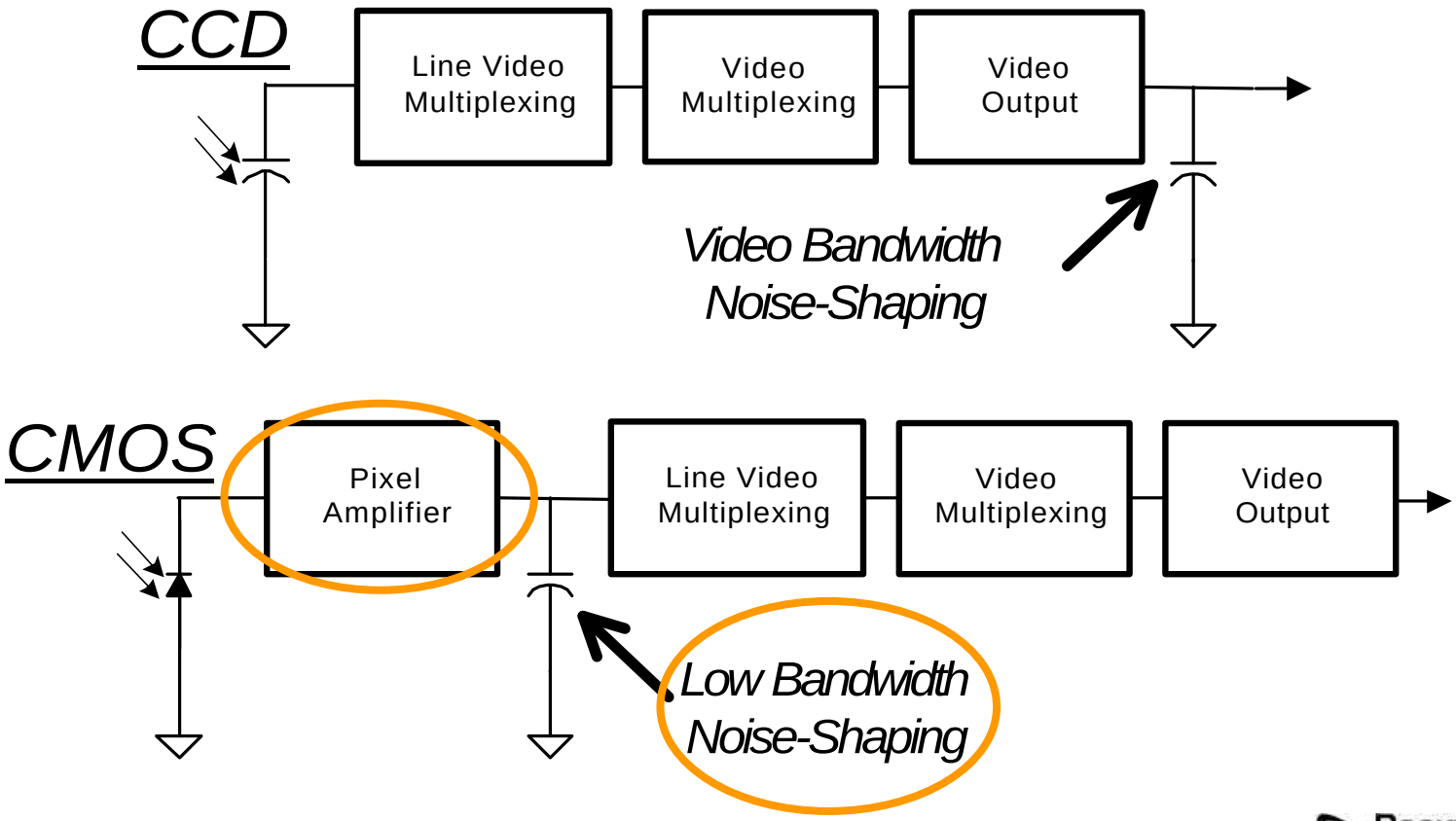
Why CMOS Can Excel for Video

- **CMOS Bandlimiting is More Optimal vs. CCD, CDS Efficacy Degrades as Frequency is Increased**



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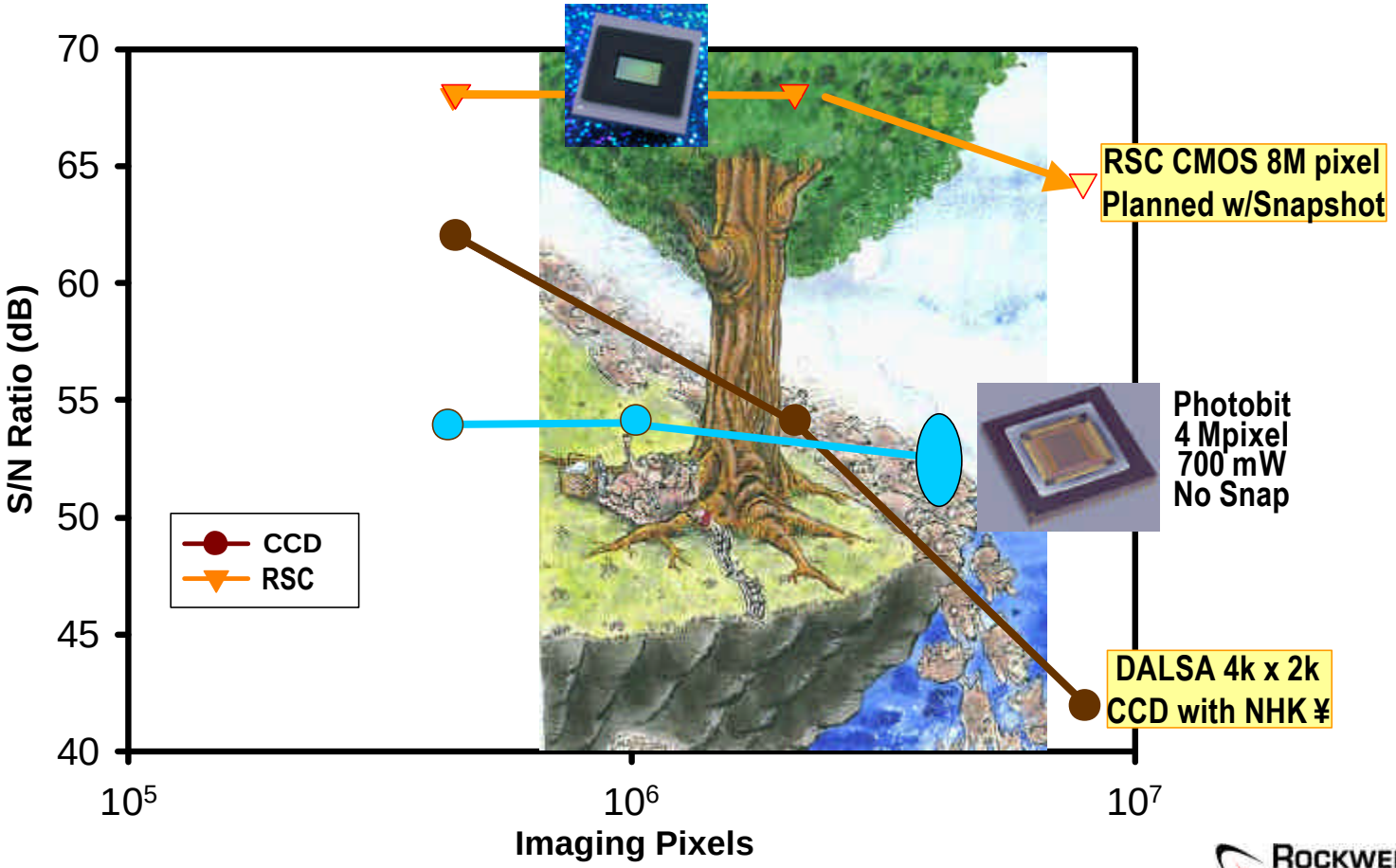
Large Video CMOS Beats Large CCD

- New 4k x 2k CCD from DALSA Validates CMOS Superiority for Fast Framing
- Video CCD Data Tends to Follow Lemming Model, i.e., “Falling off the Cliff”



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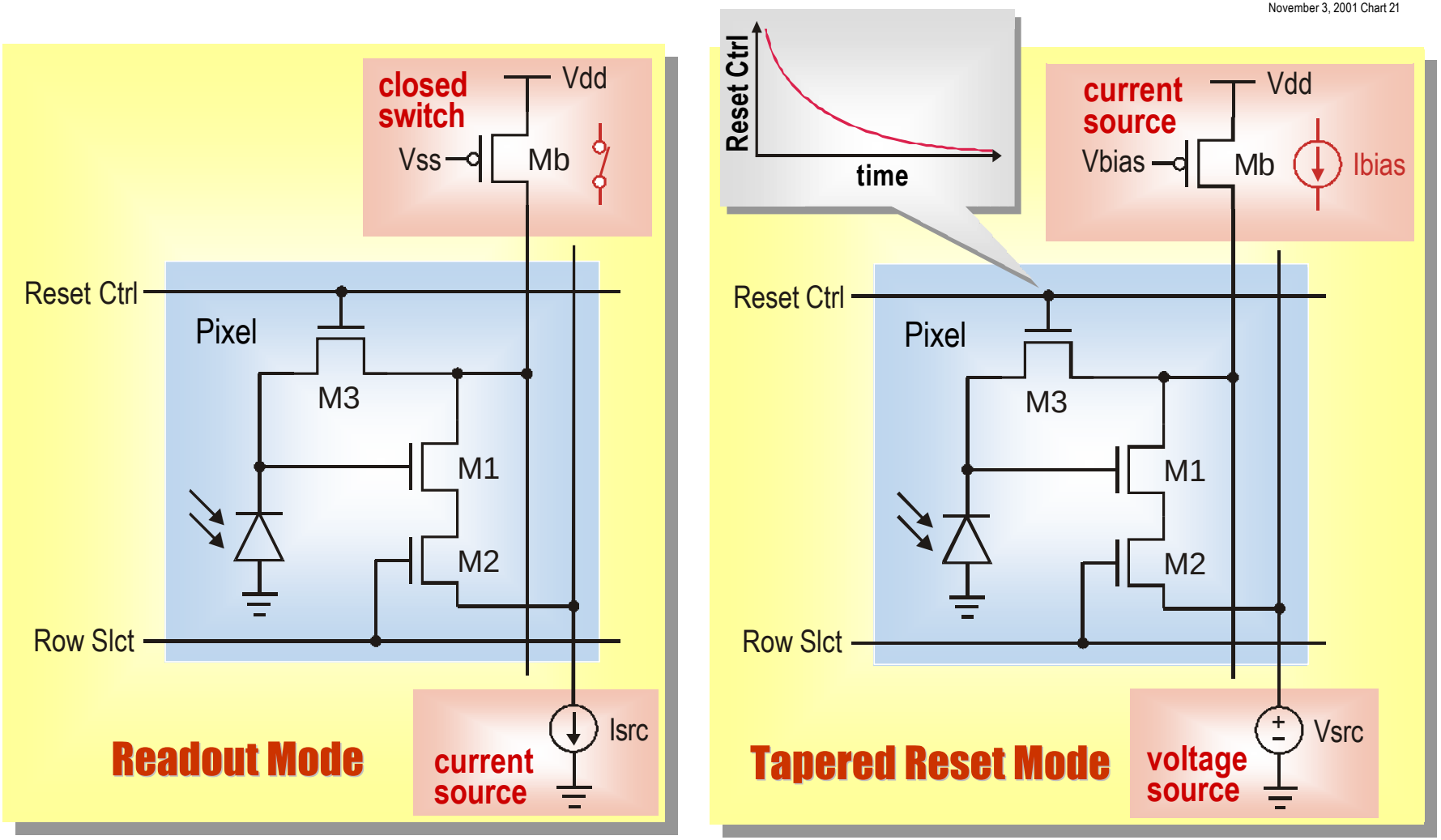
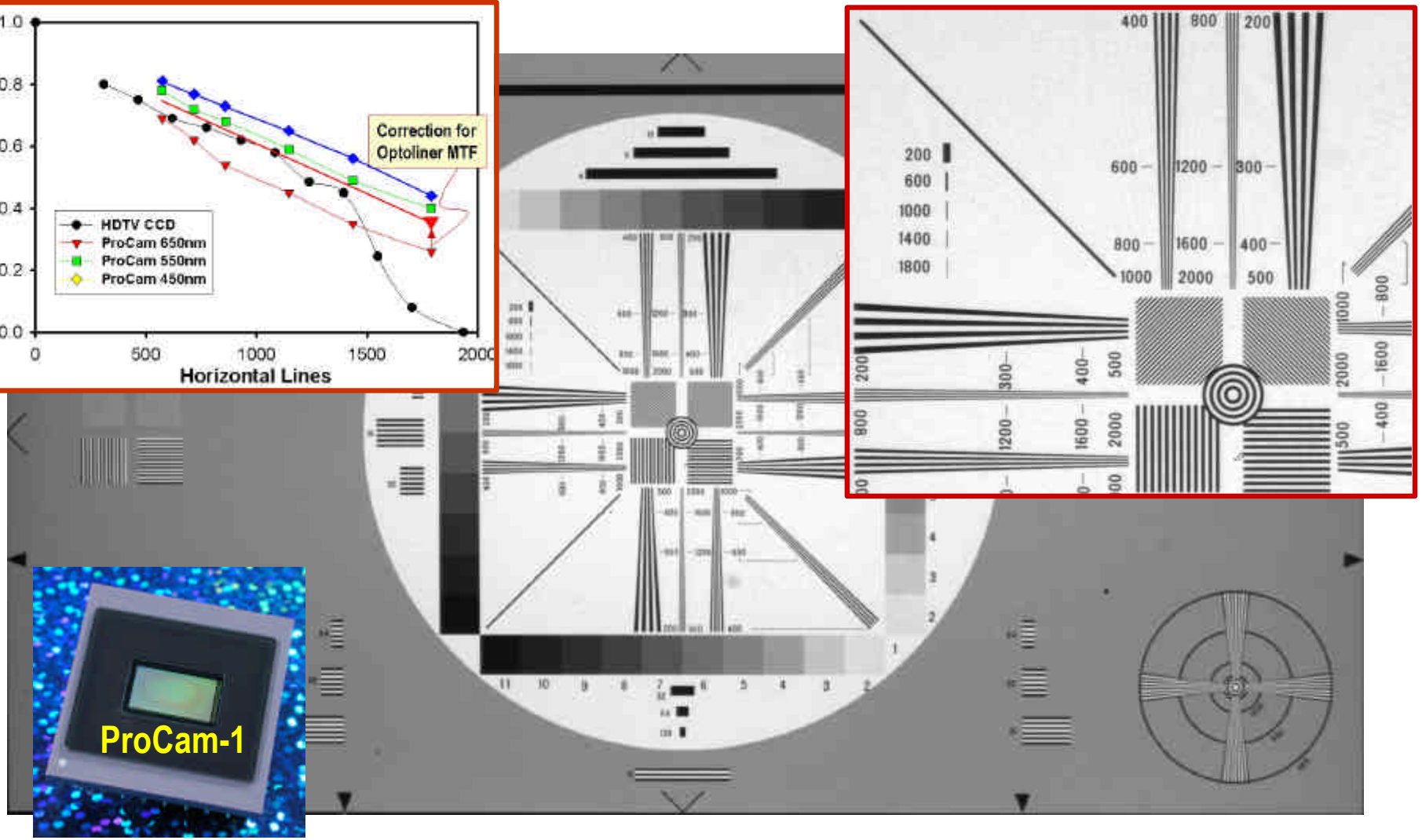
Tapered Reset: Low N_{read}, High QE, Multi-MHz



Proven *i*-SoC/ASIC Features/Controls

- Very Low Power A/D Conversion (0.3 pJ/LSB @ 40MHz)
- 12-b Digital Video: ~20 e- at 75 MHz, ~12 e- to 25 MHz
- Low-Noise Bias Voltage Generation
- Serial interface for controlling the sensor operation
- Freely programmable windowing/guide-mode control
- Freely programmable timing (master and slave modes)
- Programmable gain from -24 dB to 72 dB at 0.006 dB/step
- Electronic shutter programmable from 1/30 to 1/30000 s
- Hot and dead pixel identification and replacement:
  - isolated bright and dark pixels are replaced by the average of left and right neighbor
- Automatic black-clamping to keep black level video at 64 counts
- Fixed Pattern Noise suppression to below 0.025%

High MTF: Monolithic *i*-SoC (20e-)



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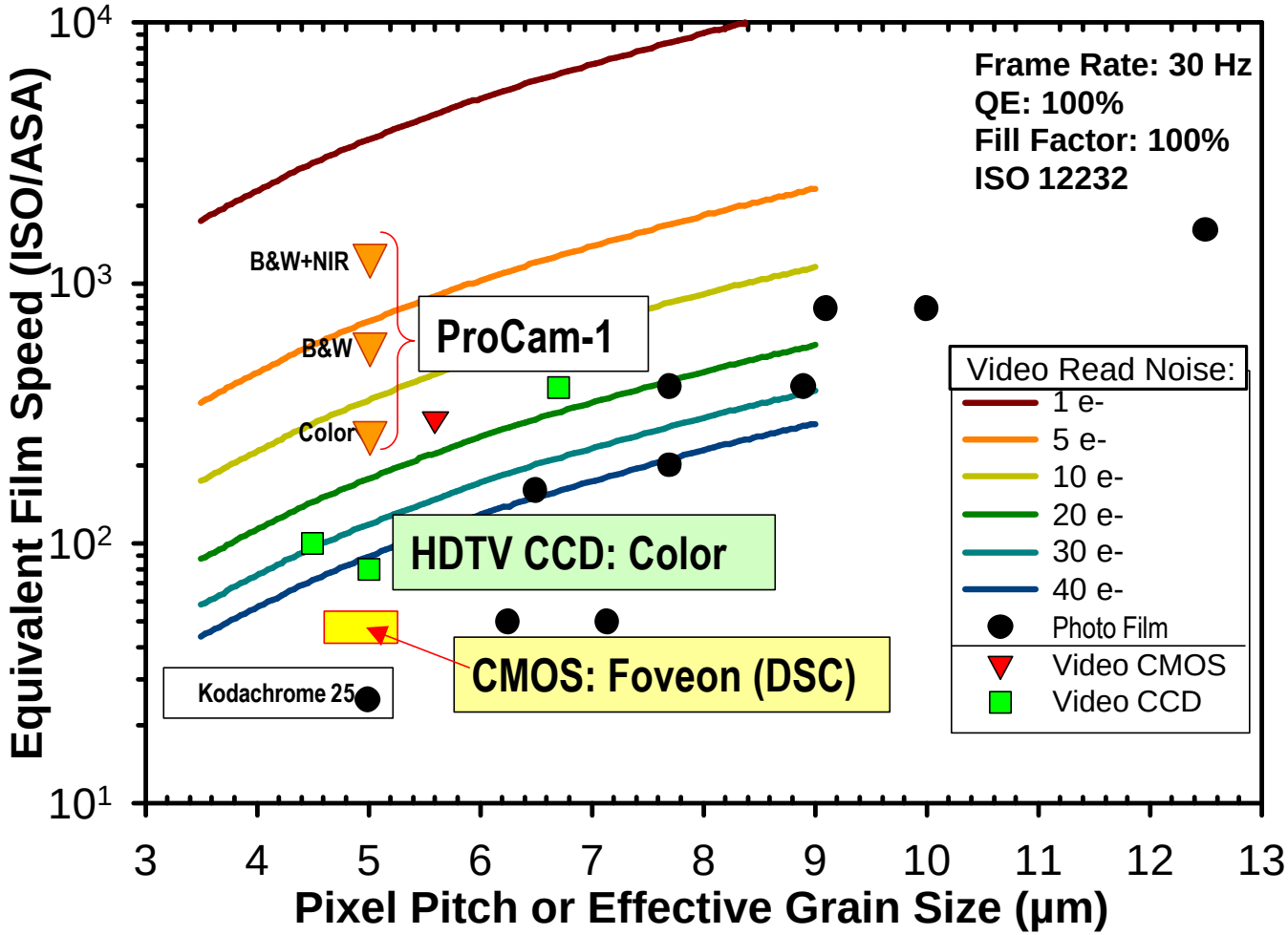
20e- at 75MHz ⇒ "Fast" ISO e-Film Speed

- ProCam is "Faster" Than HDTV CCDs



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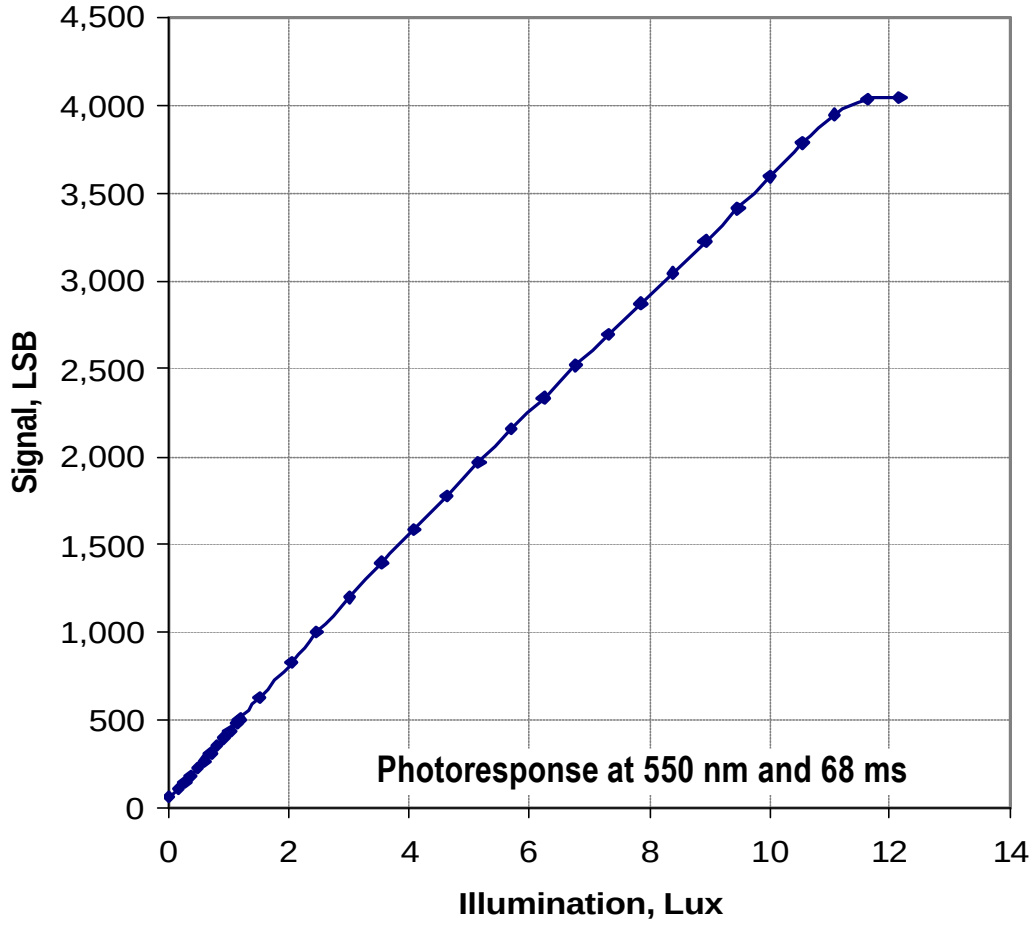
CMOS: Measured Photoresponse

- Sensitivity
  - 5500 LSB / lx * s
  - 2.2 V / lx * s
- Conversion Gain
  - 0.07 LSB / e-
  - 31 uV / e-
- Nonlinearity < 0.1 %



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Summary & Conclusion

- IR FPA Technology Continues to Grow in Size and Improve in Performance
  - MWIR-Visible HgCdTe Meets NGST Specs at ~55K
  - 4k x 4k Mosaic Development Well Underway
- Competitive Alternatives to CCD Technology for Visible Now Exist
  - LSST Could Benefit from HyViSI Technology Since Mosaic Development with Supporting ASIC is Already Underway
  - Monolithic CMOS Could Also Be an Attractive Alternative by Thinning the Sensors and Using Backside Illumination
    - However, Peripheral *i*-SoC Circuits Increase Intra-Mosaic Gaps