

Brookhaven National Laboratory
Instrumentation Division Seminar
21st April 2004

Radiation-hard circuits in deep submicron CMOS technologies



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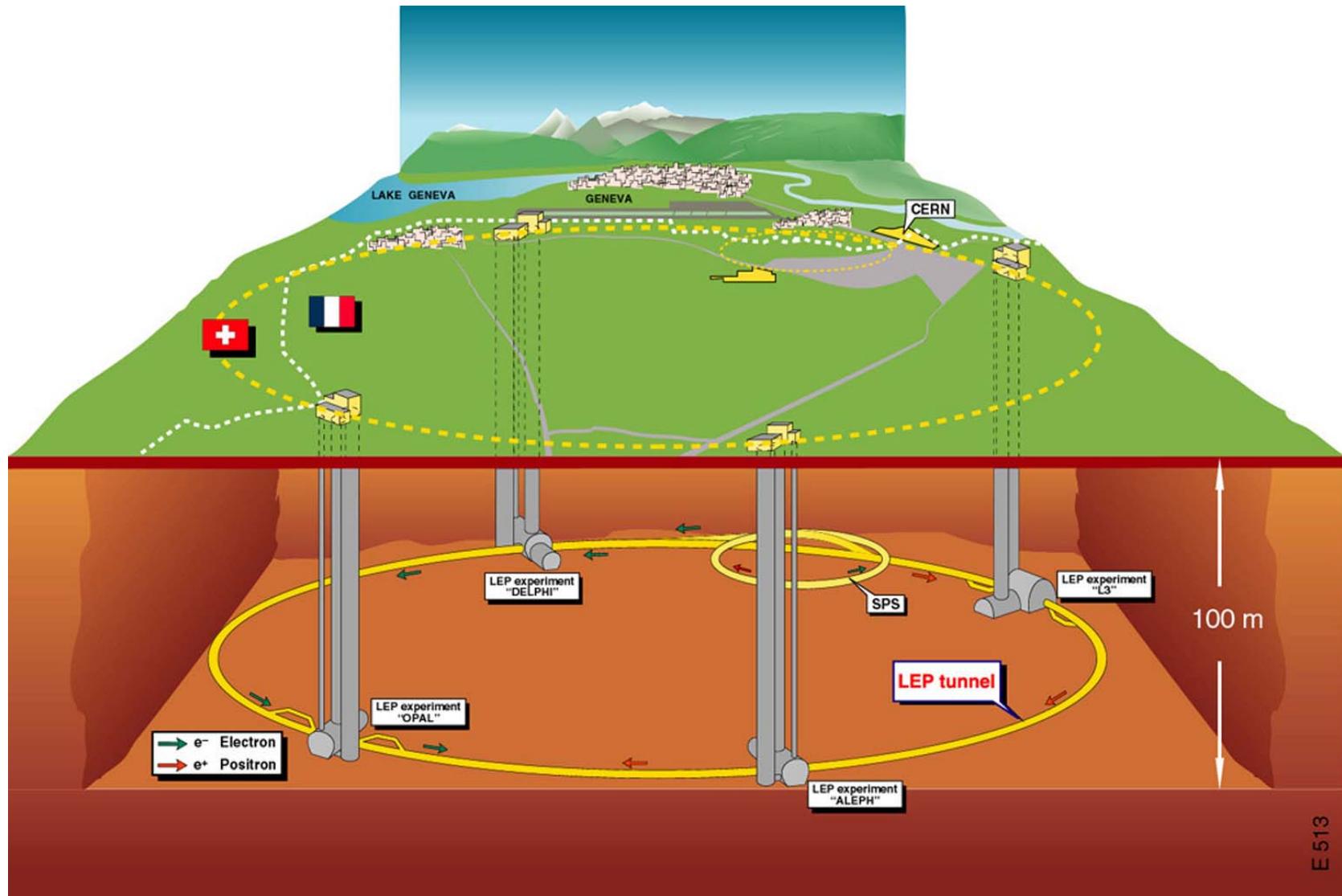
Outline

- **Introduction and motivation**
- **Radiation effects on CMOS devices and circuits**
- **Scaling impact on the radiation tolerance**
- **A radiation tolerant layout approach**
- **The Enclosed Layout Transistor (ELT): special features**
- **One circuit example: a radiation tolerant analog memory**
- **Conclusions**

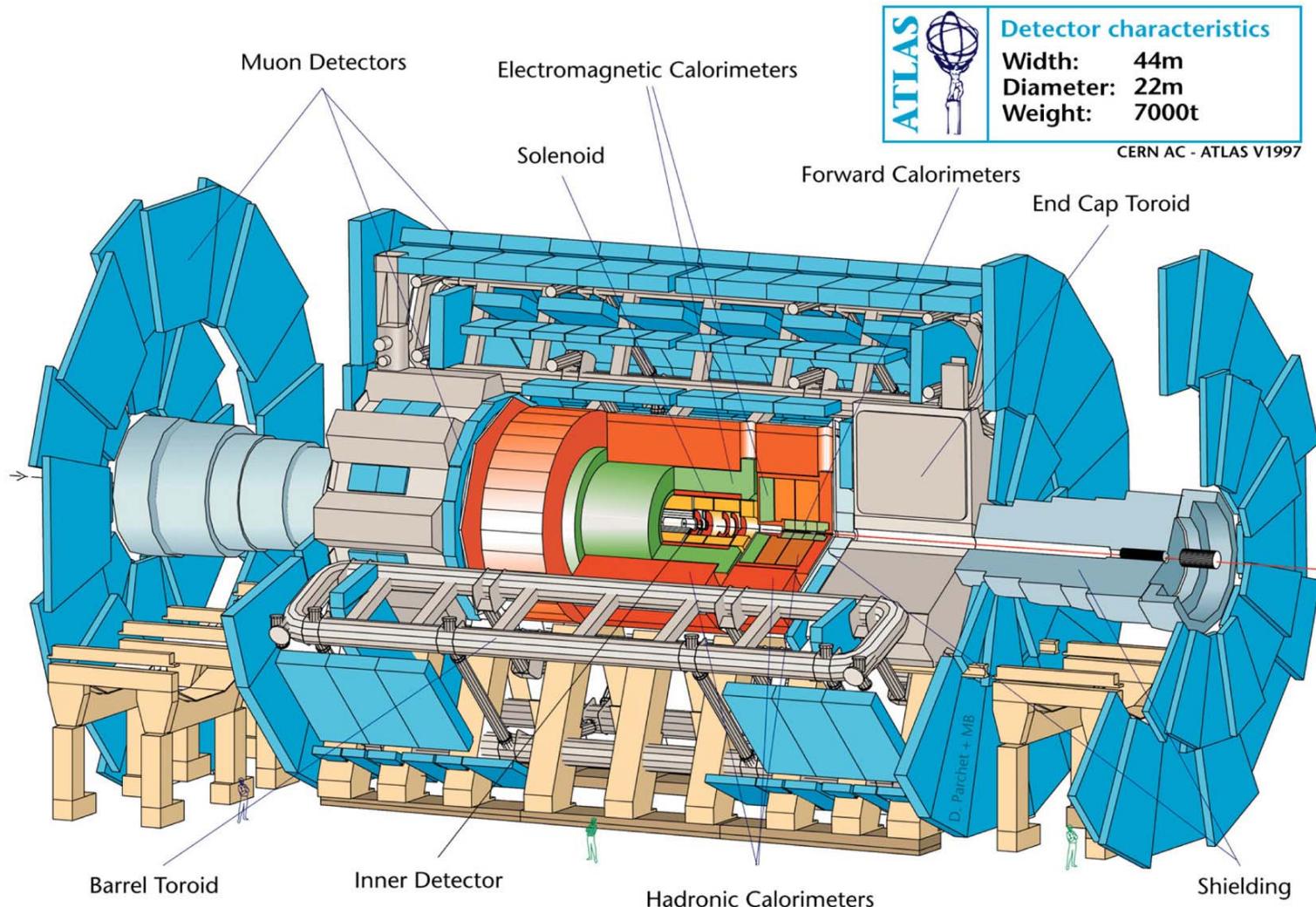
CERN: above ground...



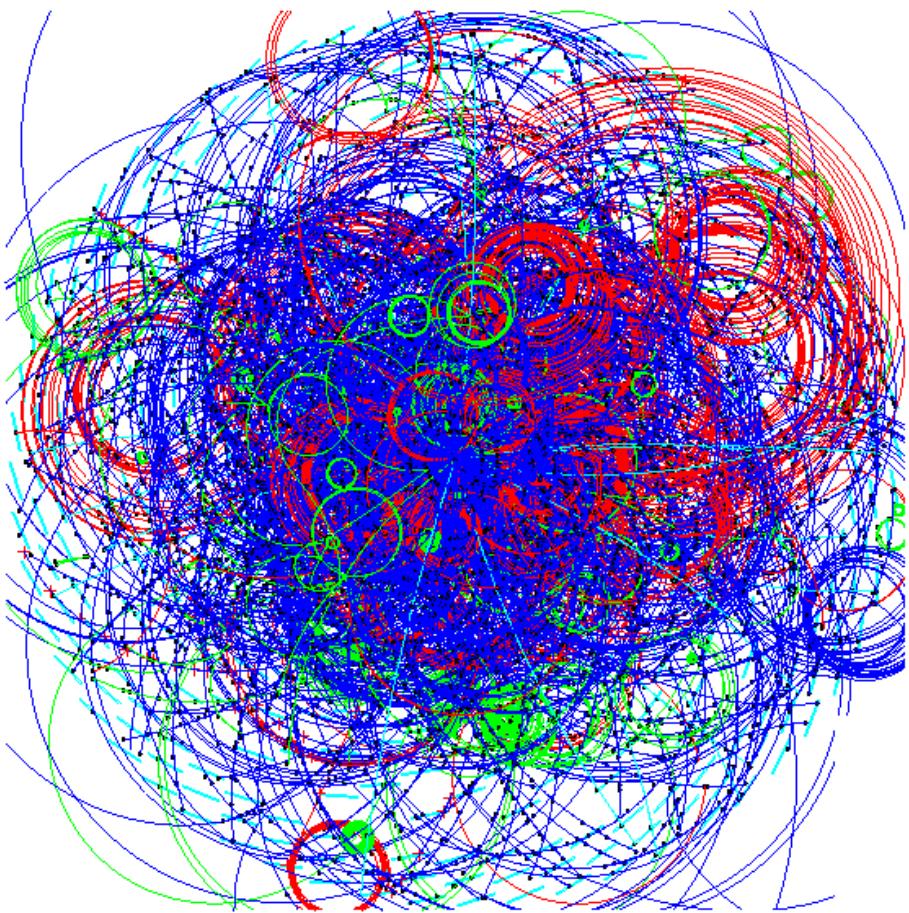
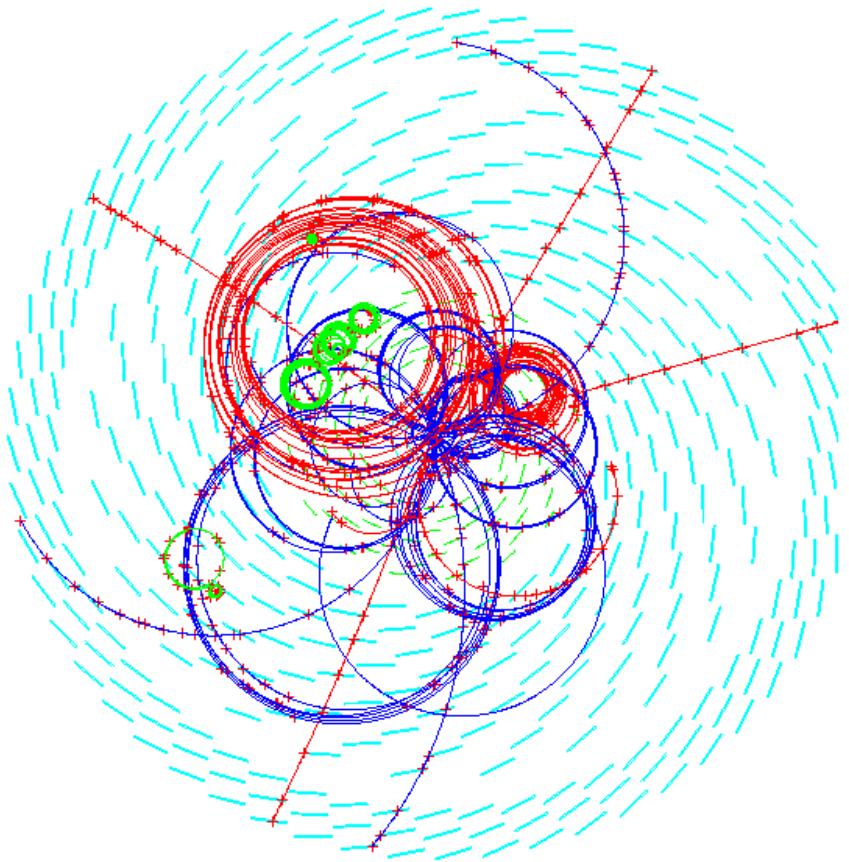
... and under ground



One of the 4 LHC experiments

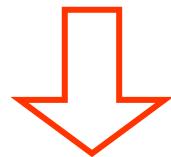


Finding the Higgs boson...

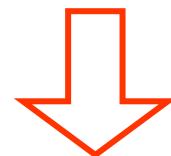


Why rad-tolerant CMOS ICs?

High luminosity colliders generate a very harsh radiation environment, which requires radiation hard read-out ICs



Radiation hardened technologies represent a possible solution, but they are expensive and have several other problems



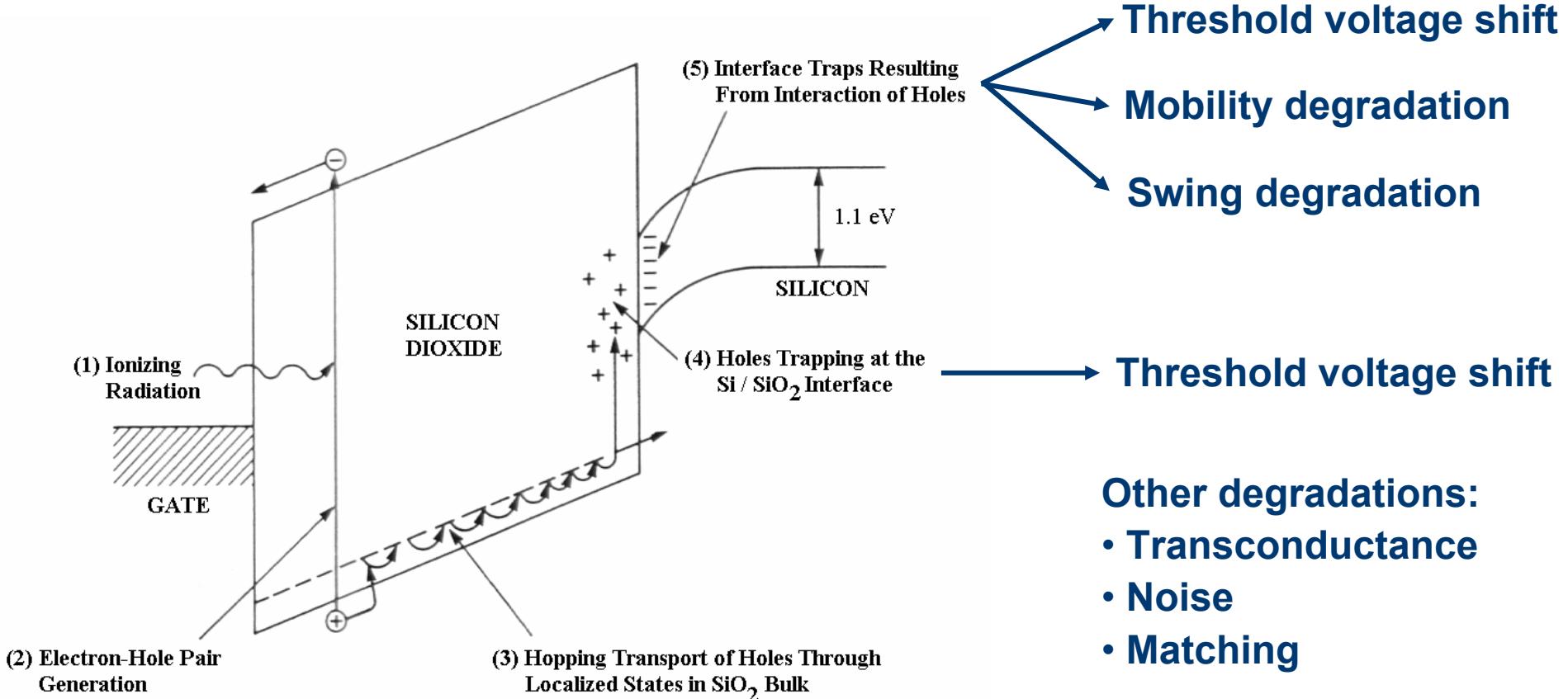
Can we use, with some tricks, a commercial, “inexpensive” CMOS technology for our circuits ?

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 - **Total Ionizing Dose (TID) Effects**
 - **Single Event Effects (SEE)**
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Ionizing particles through a MOST



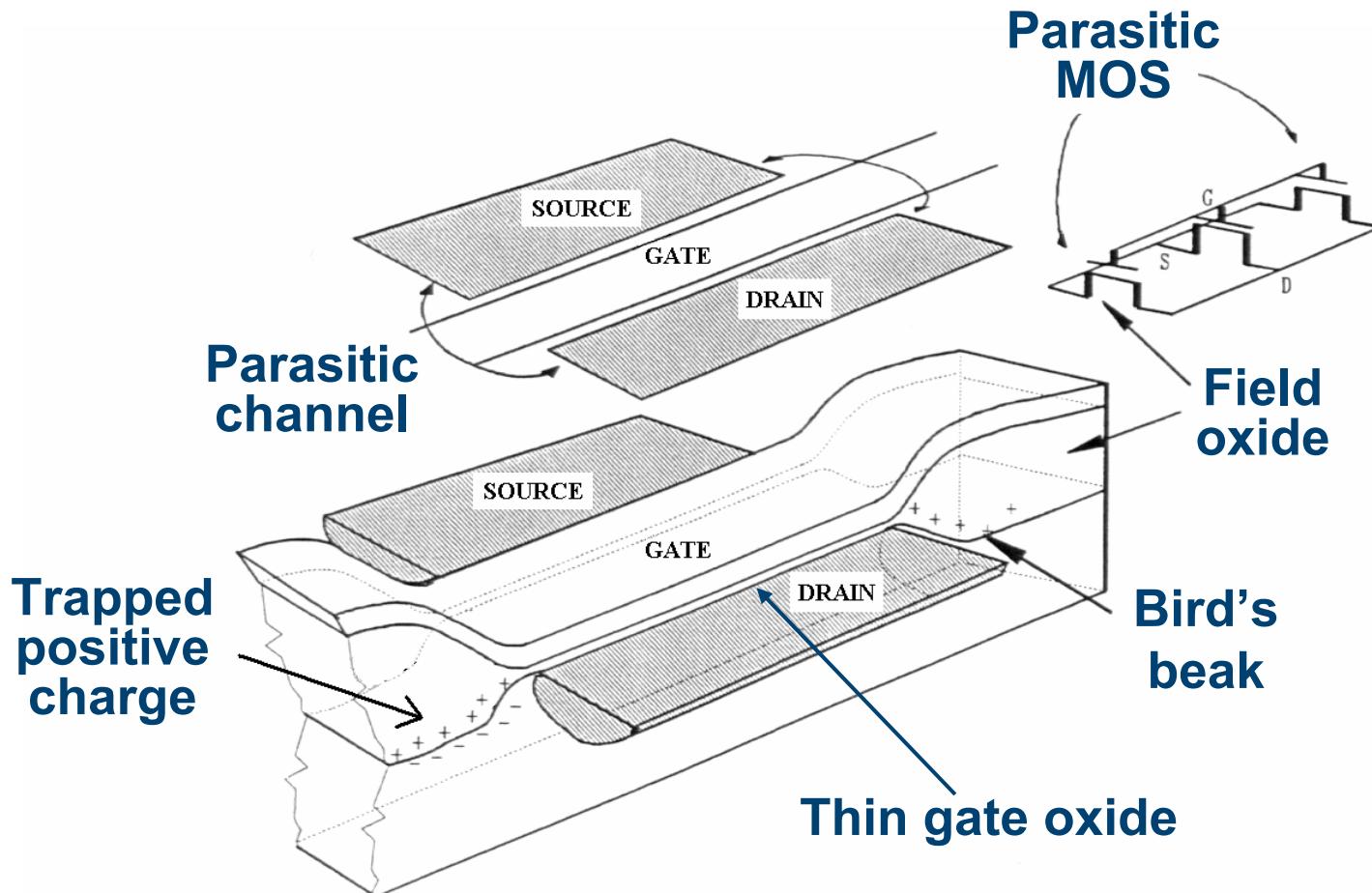
F. B. McLean and T. R. Oldham, Harry Diamond Laboratories Technical Report, No. HDL-TR-2129, September 1987.

Contributions to the V_T shift

	Oxide charges	Interface states	Total
NMOS	—	+	+ or —
PMOS	—	—	—

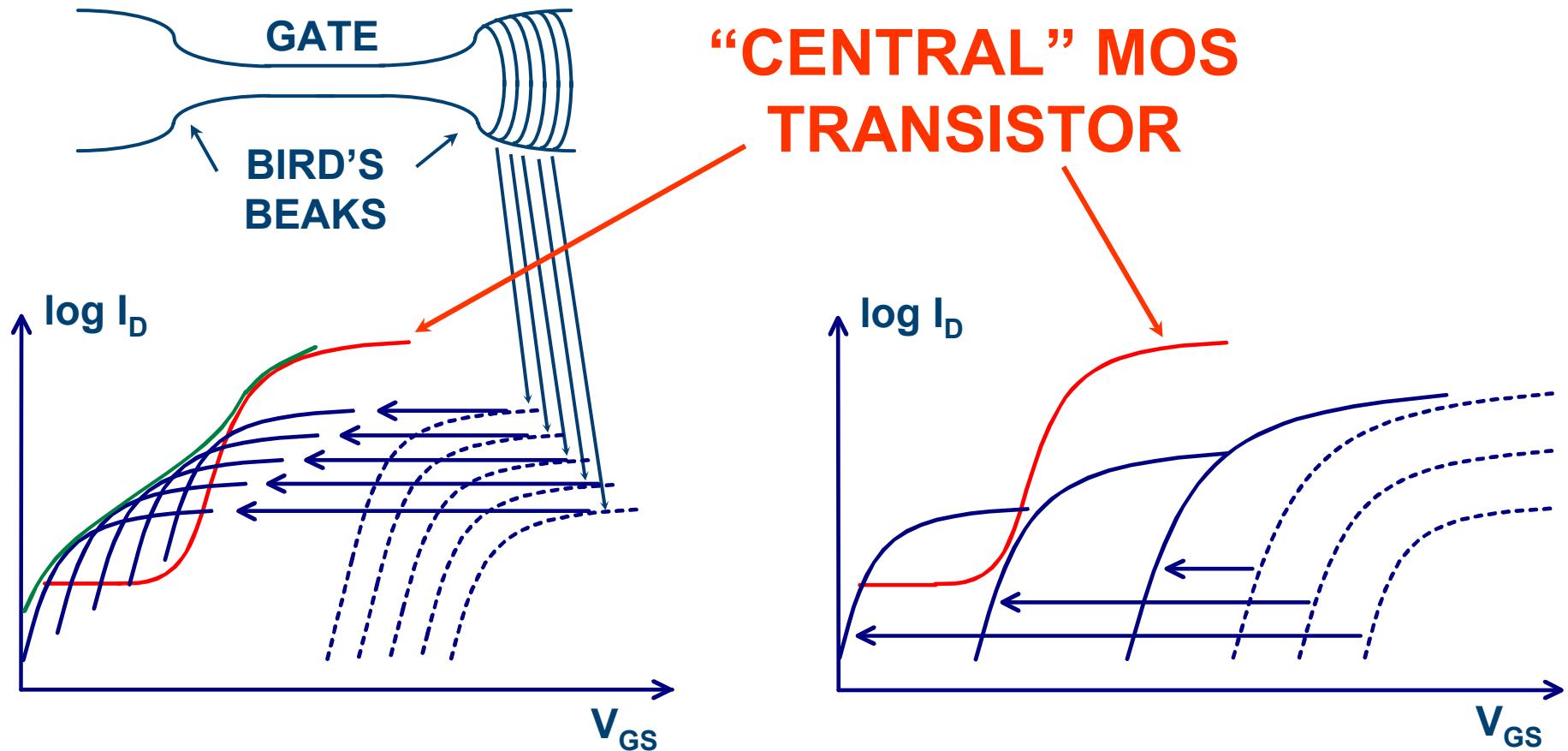
- For deep submicron processes the sign of the V_T shift for NMOS transistors tends to be positive
- The bias conditions during irradiation have a great influence on the absolute value of the V_T shift

Transistor level leakage (NMOS)



R. Gaillard, J.-L. Leray, O. Musseau et al., "Techniques de durcissement des composant, circuits, et systemes electroniques", Notes of the Short Course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), Sept. 1995.

Transistor level leakage

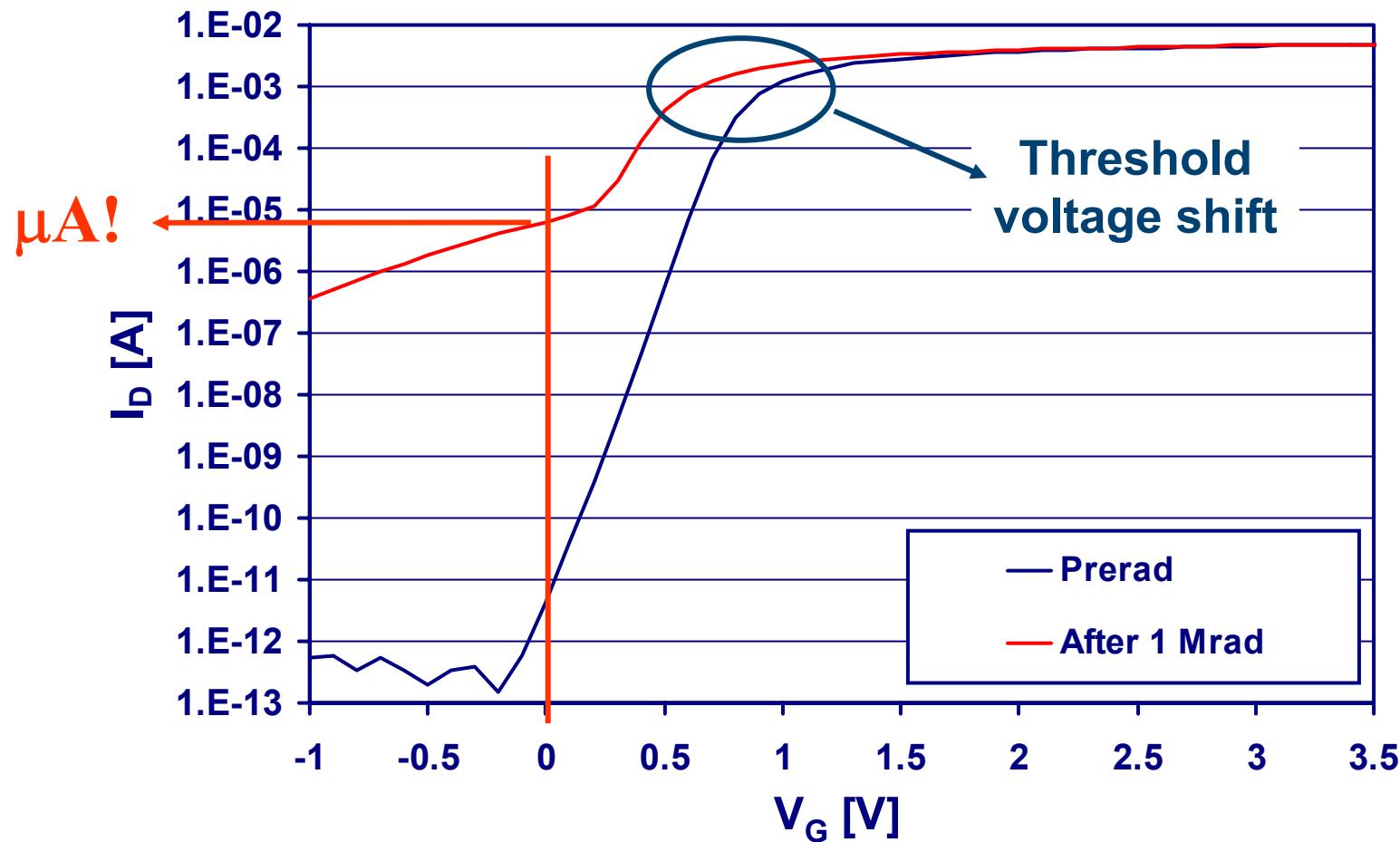


This is for LOCOS, what about STI? Things did not improve!

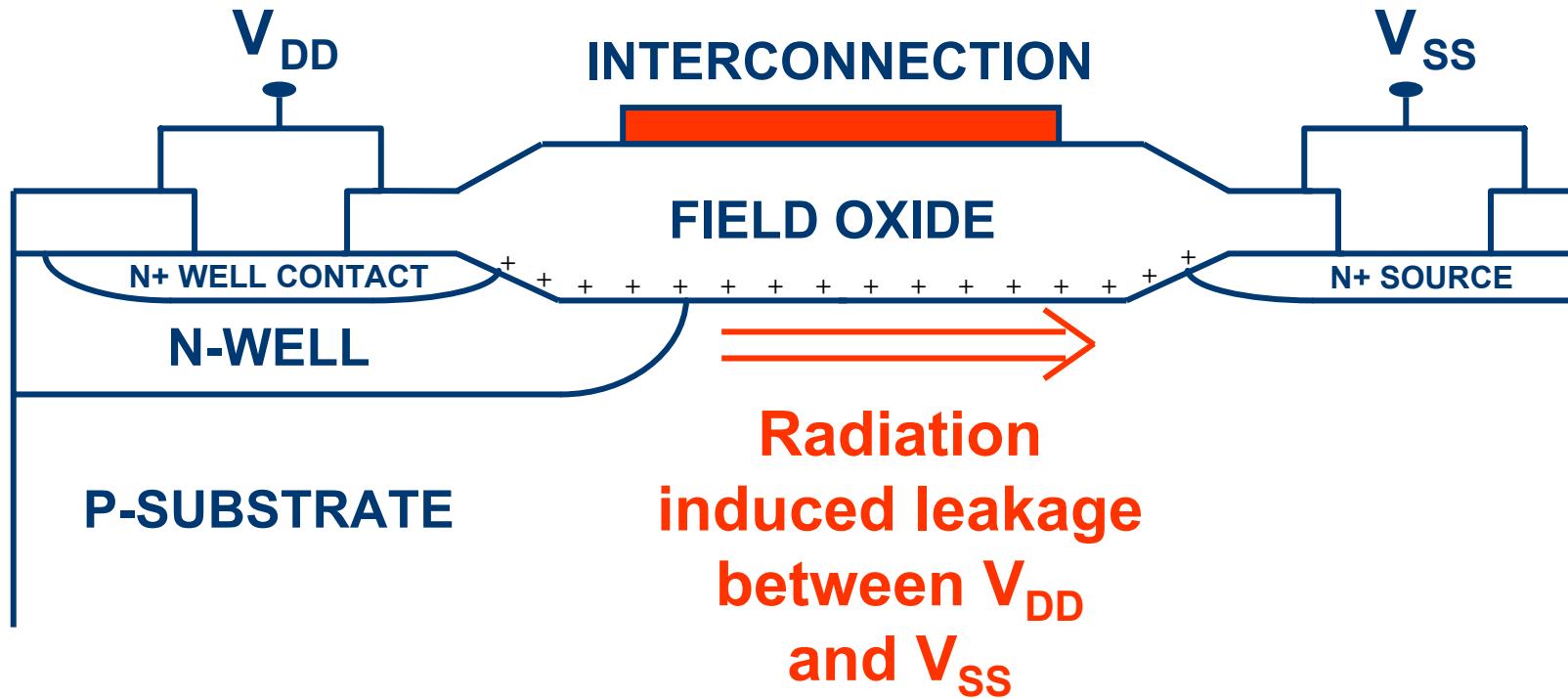
M. R. Shaneyfelt et al., "Challenges in Hardening Technologies Using Shallow-Trench Isolation", *IEEE TNS*, vol. 45, Dec. 1998, pp. 2584-2592.

Transistor level leakage: example

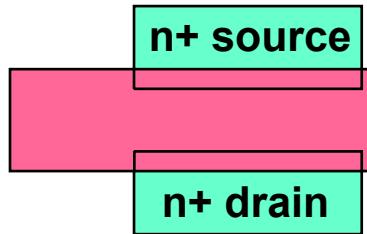
NMOS - 0.7 μm technology - $t_{\text{ox}} = 17 \text{ nm}$



Field oxide leakage

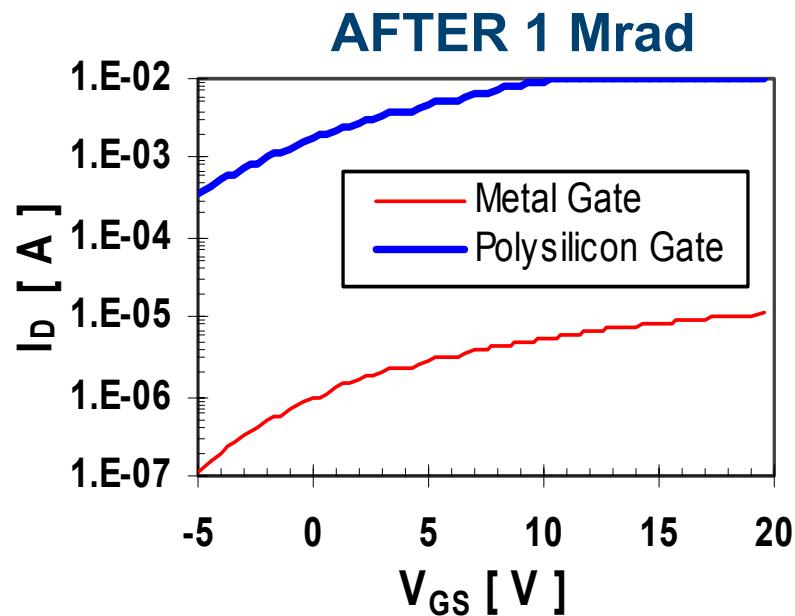
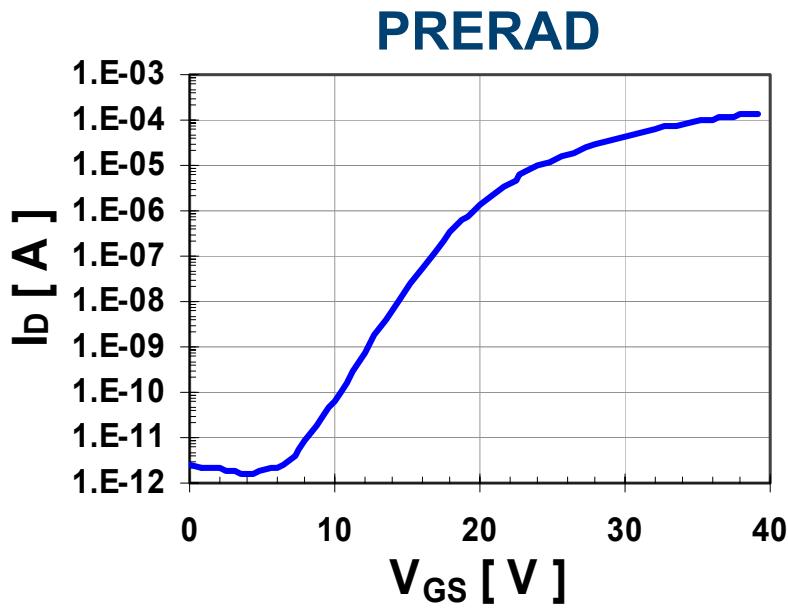


The Field Oxide Transistor

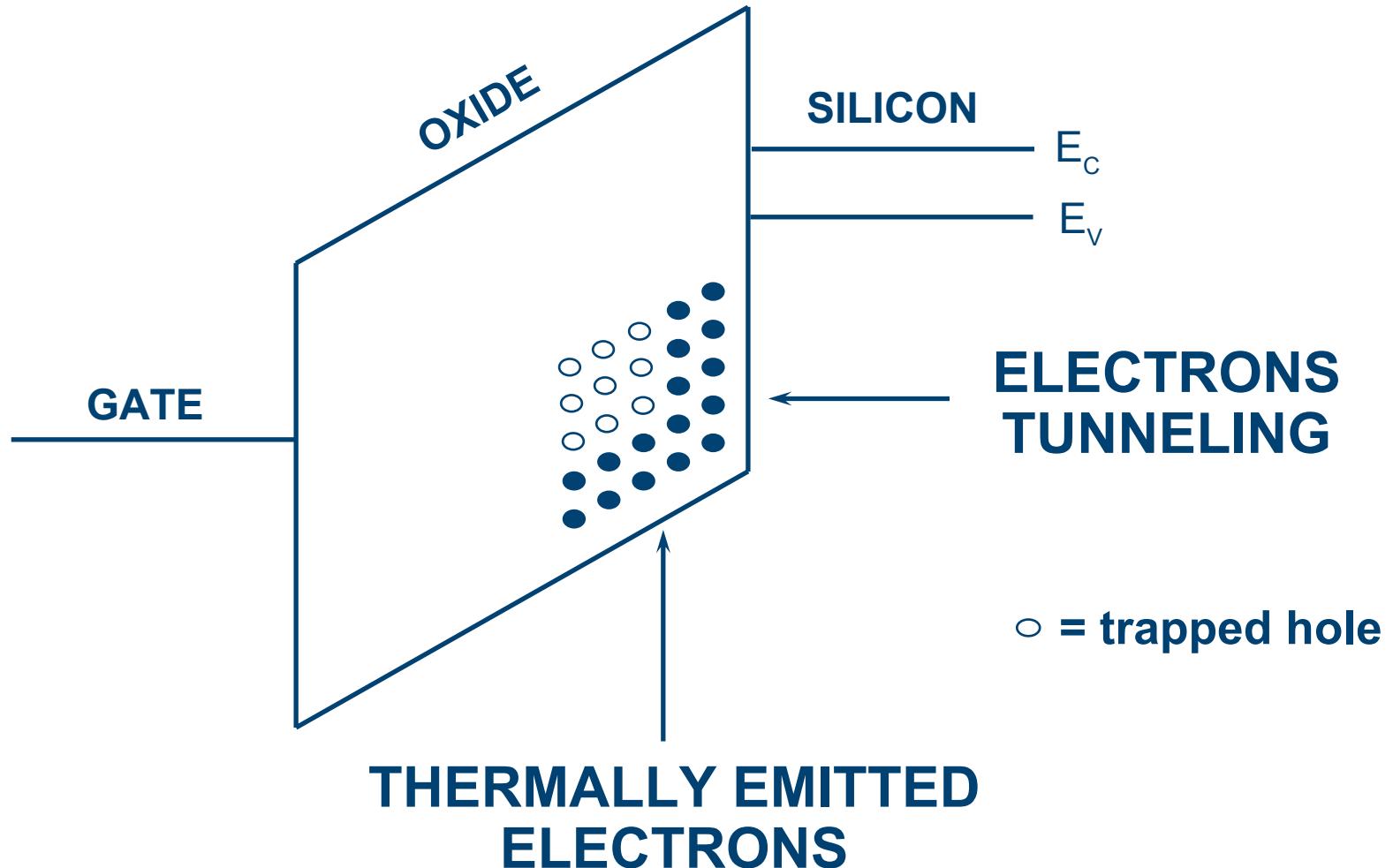


**Post-irradiation
leakage currents
depend on**

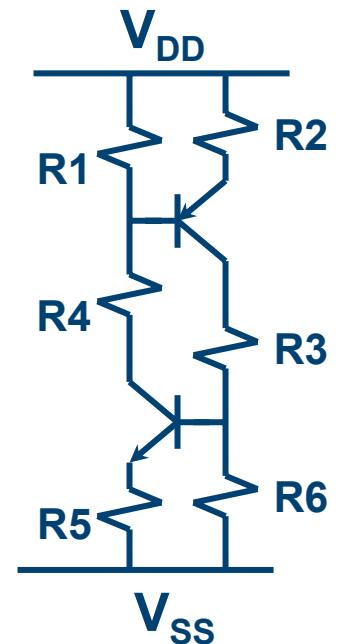
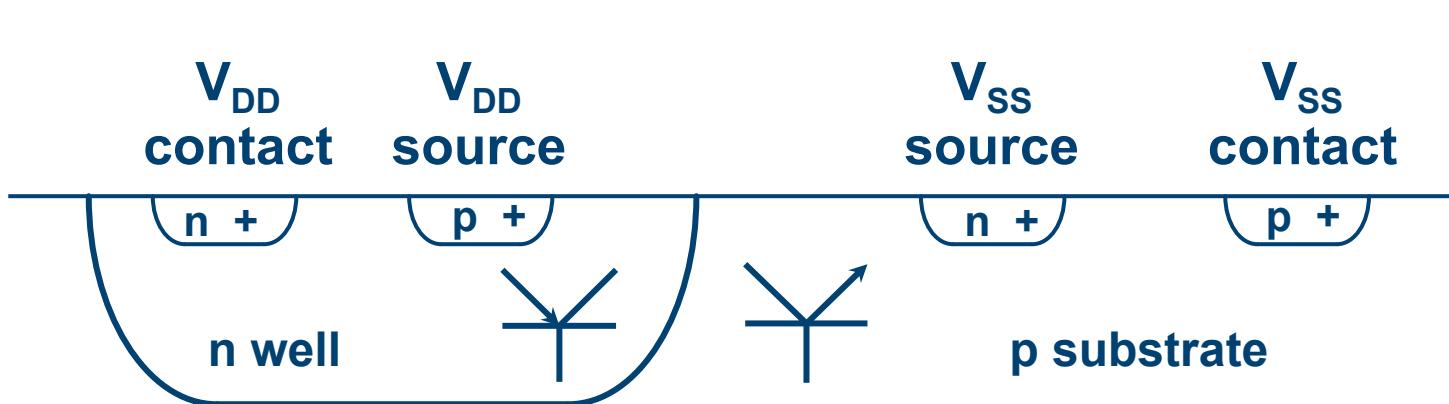
Total Dose
Bias conditions
Gate Material
Field oxide quality



Annealing (mainly in the oxide!)



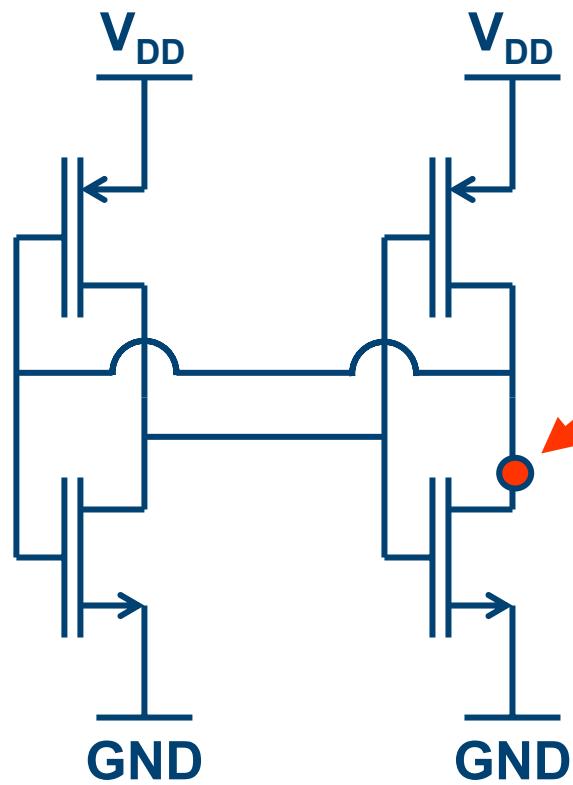
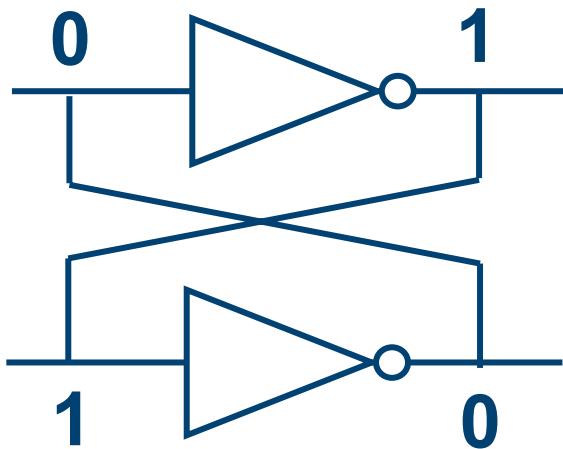
Single Event Latch-up (SEL)



Latch-up can be initiated by ionizing particles (SEL)

Single Event Upset (SEU)

Static RAM cell



Highly
energetic
particle

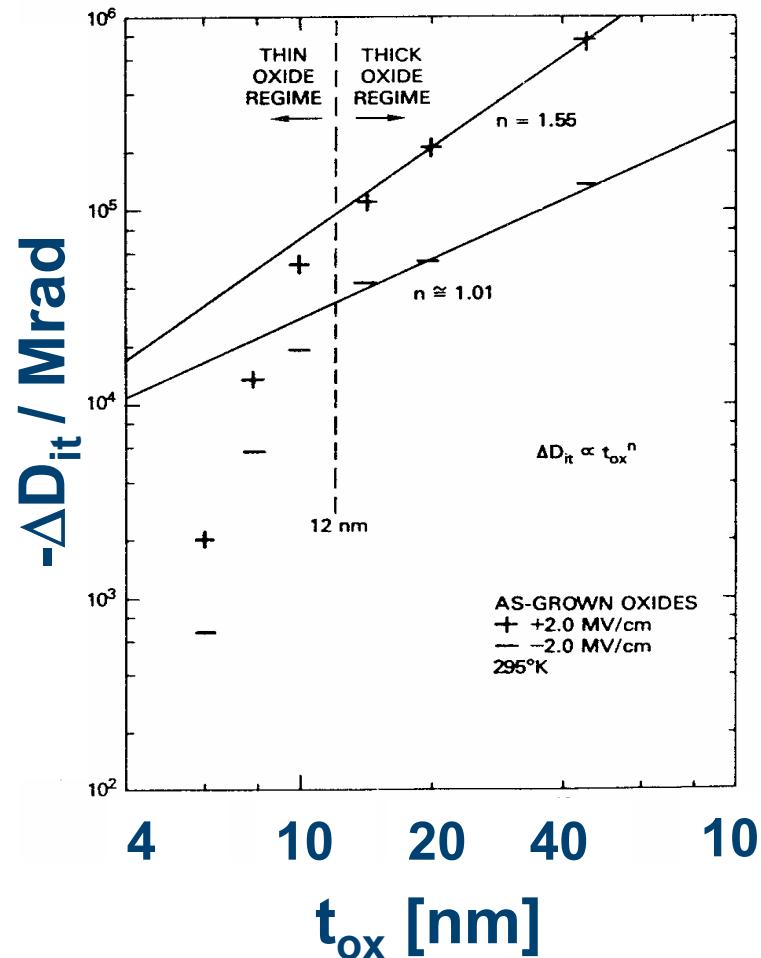
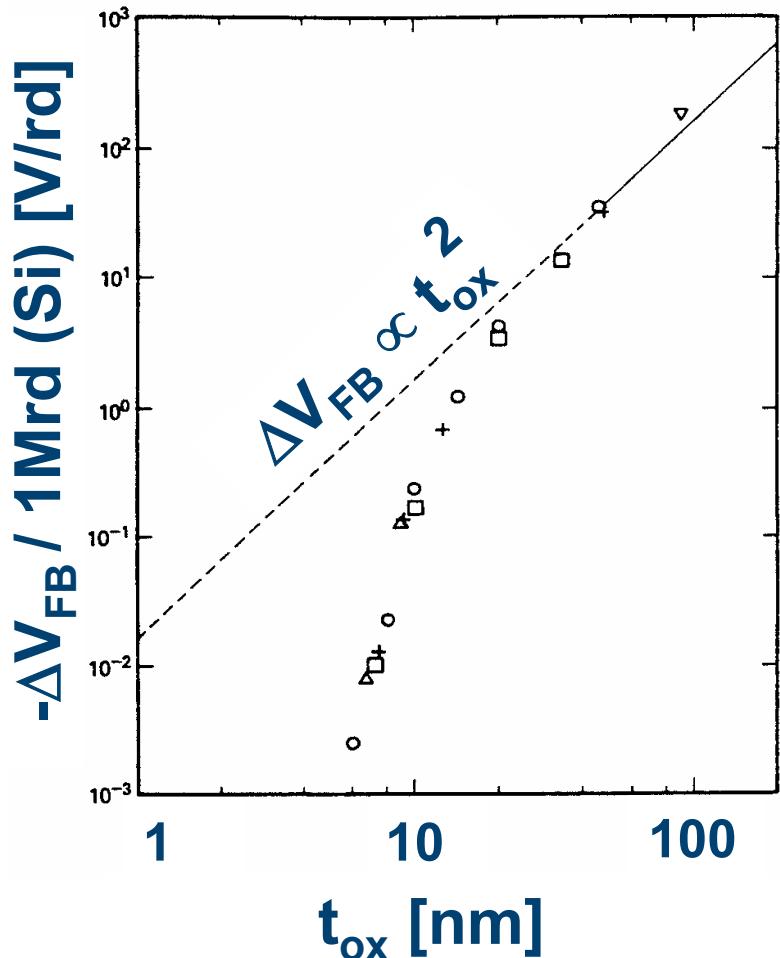
$1 \rightarrow 0$

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- **Scaling impact on the radiation tolerance**
 - **Scaling impact on TID effects**
 - **Scaling impact on SEEs**
- **A radiation tolerant layout approach**
- **The Enclosed Layout Transistor (ELT): special features**
- **One circuit example: a radiation tolerant analog memory**
- **Conclusions**

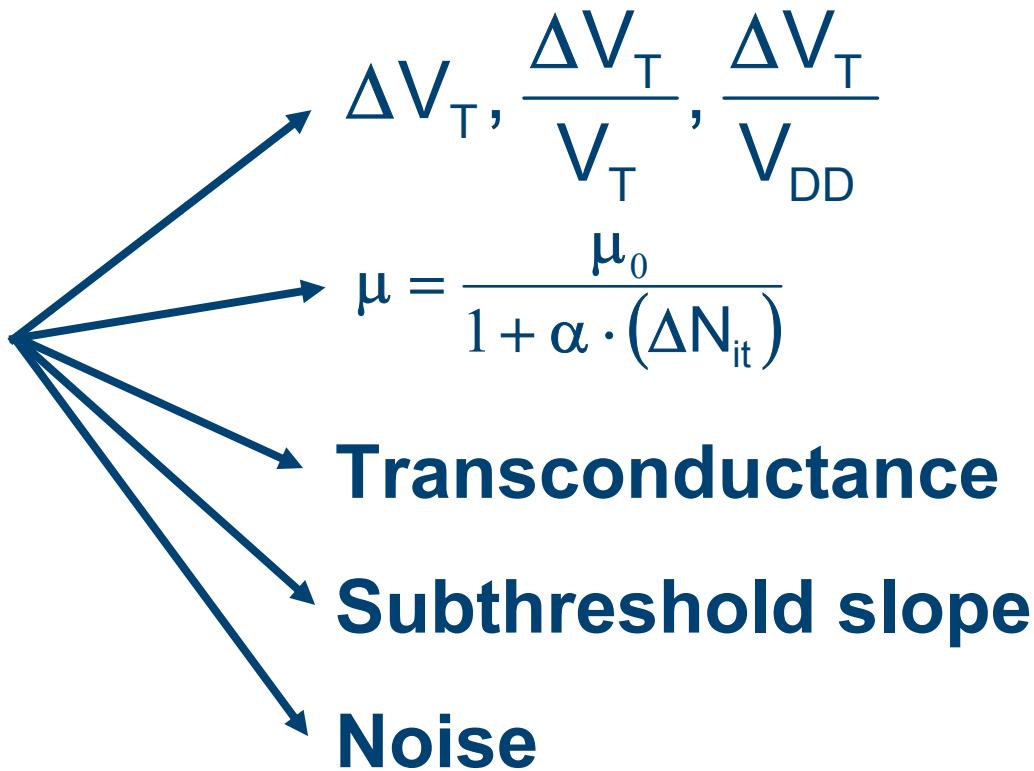
Total Dose damage and scaling



N. S. Saks et al., *IEEE TNS*, vol. 31, no. 6, Dec. 1984, and vol. 33, no. 6, Dec. 1986.

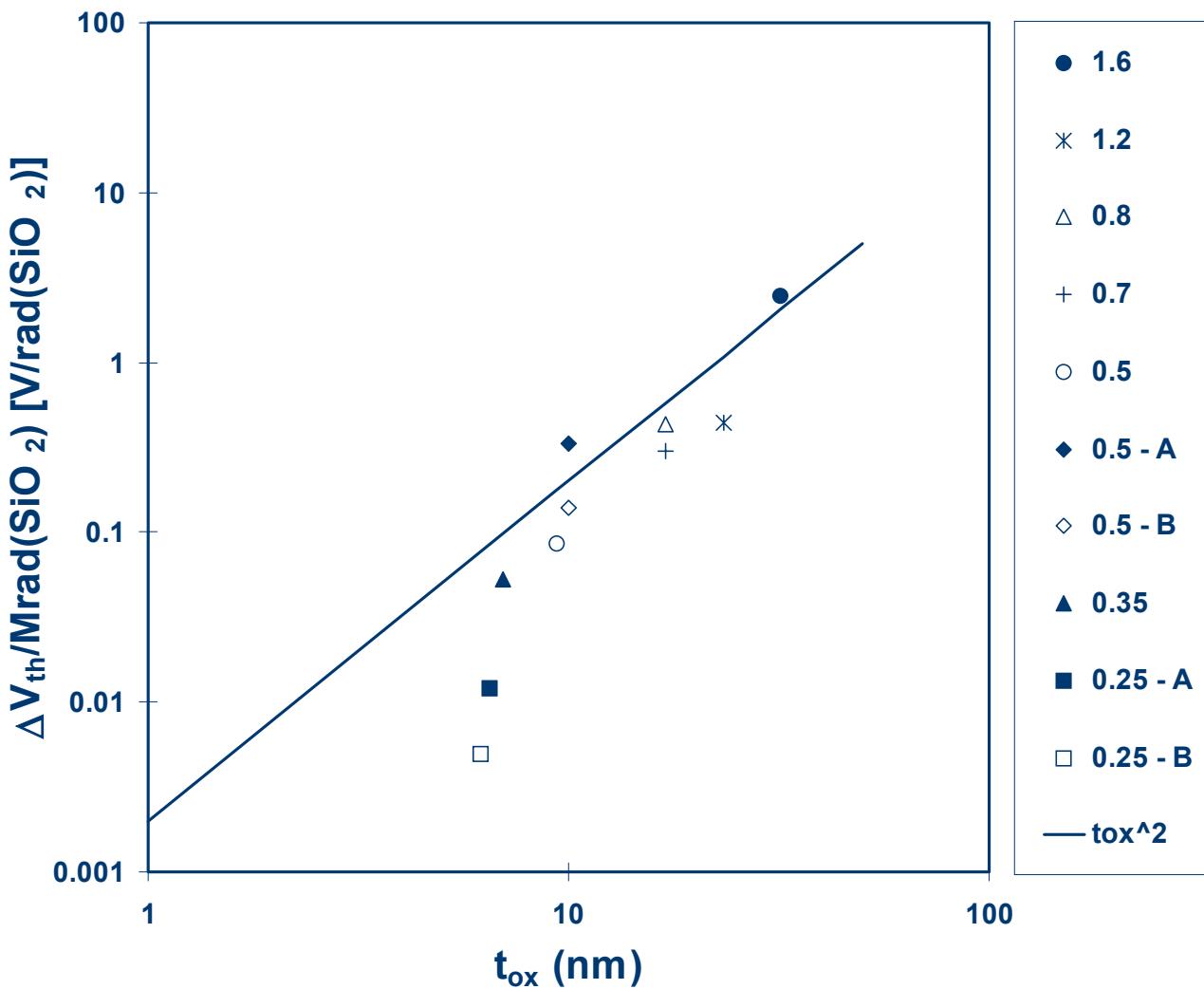
Total Dose damage and scaling

Decreasing t_{ox} we decrease the degradation of:



And the threshold voltage shift for n-channel transistors might not be negative anymore...

ΔV_T and t_{ox} scaling



SEL and scaling

Modern CMOS technologies have:

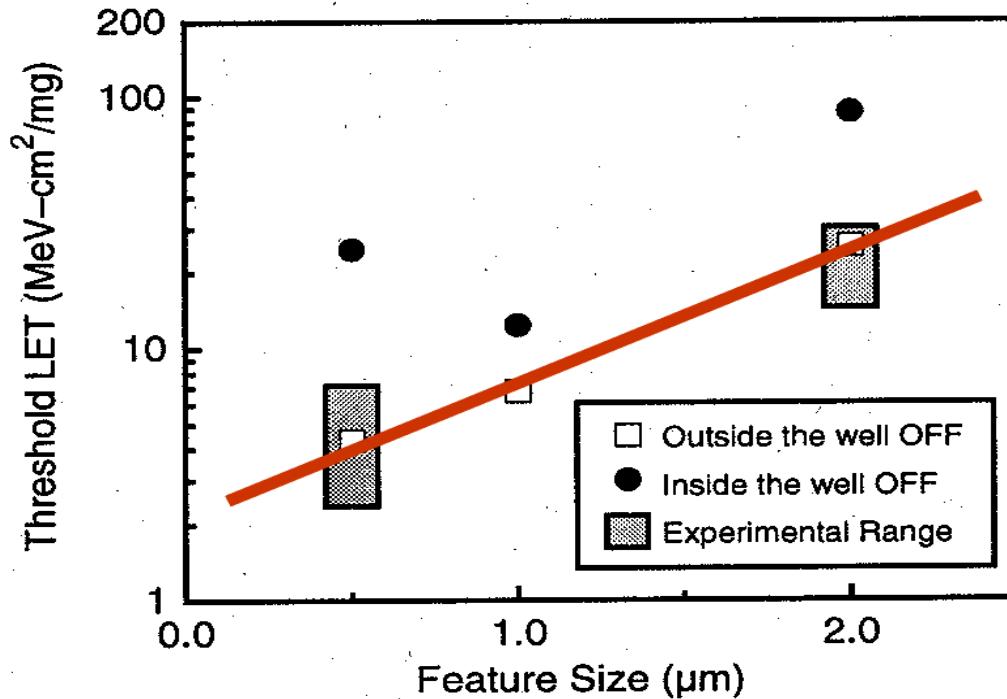
- **Retrograde wells**
- **Thinner epitaxial layers**
- **Trench isolation**
- **V_{DD} reduced**

**All these issues help in preventing SEL,
but they might not be always effective**

A. H. Johnston, "The Influence of VLSI Technology Evolution on Radiation-Induced Latchup in Space Systems", *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, Apr. 1996, pp. 505-521.

SEU and scaling

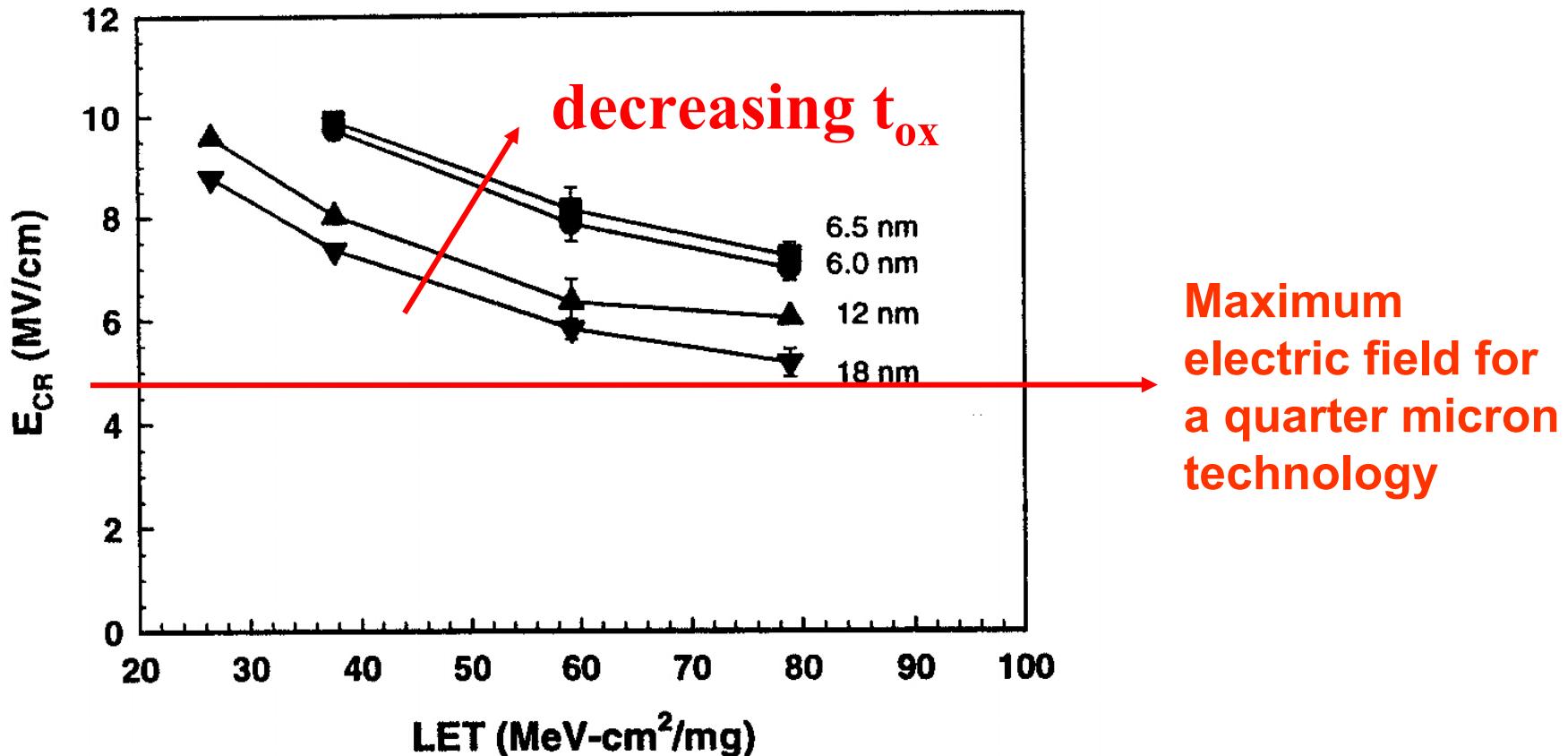
- V_{DD} reduced
 - Node C reduced
- BUT
- Charge collected reduced



The SEU problem may worsen with scaling

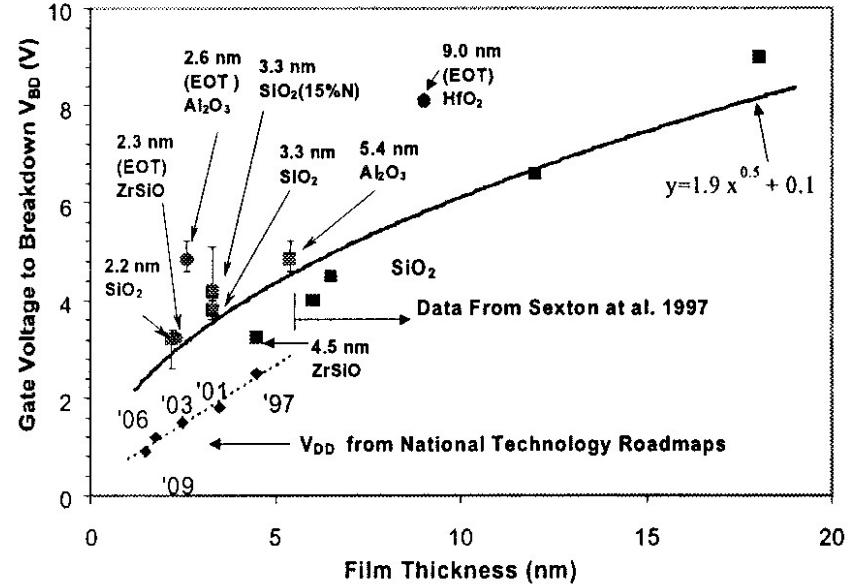
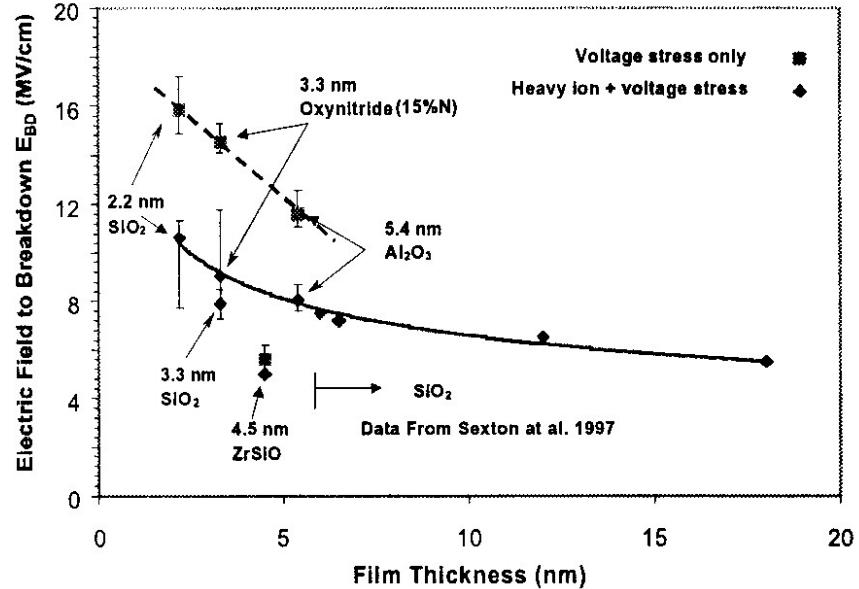
P.E. Dodd et al., "Impact of technology trends on SEU in CMOS SRAMs", *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, Dec. 1996, pp. 2797-2804.

SEGR and scaling



F.W. Sexton, D.M. Fleetwood et al., "Single Event Gate Rupture in Thin Gate Oxides", *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, December 1997, pp. 2345-2352.

SEGR in ULSI CMOS



SEGR is not a problem even in the most advanced CMOS processes

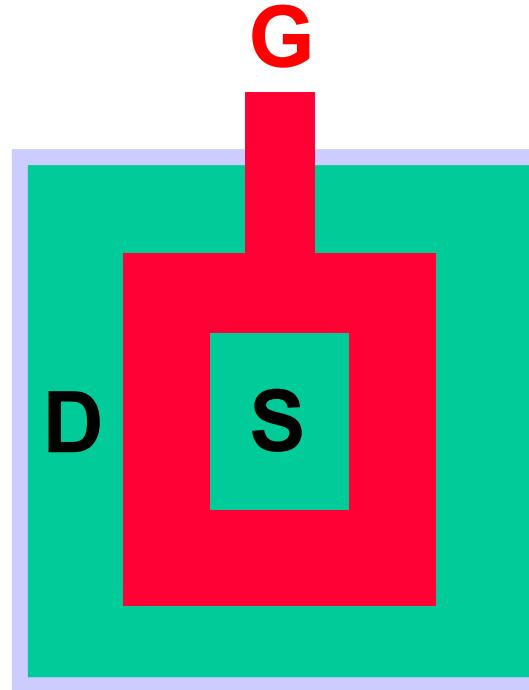
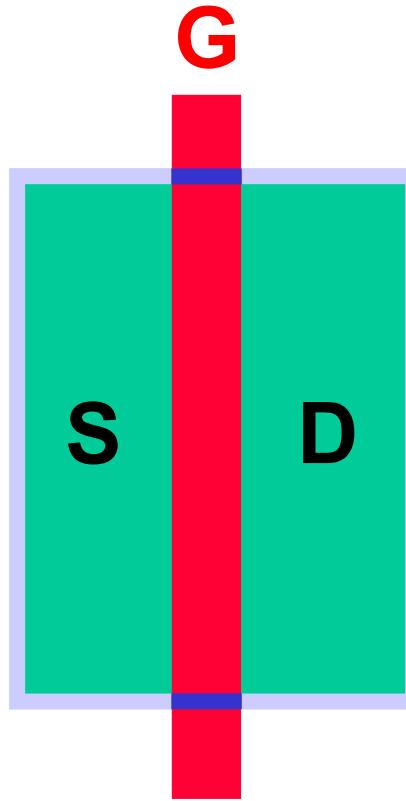
F.W. Massengill et al., "Heavy-Ion-Induced Breakdown in Ultra-Thin Gate Oxides and High-k Dielectrics", *IEEE Transactions on Nuclear Science*, vol. 48, no. 6, December 2001, pp. 1904-1912.

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- Introduction and motivation
- Radiation effects on CMOS devices and circuits
- Scaling impact on the radiation tolerance
- A radiation tolerant layout approach
 - Total Ionizing Dose tolerance
 - Enclosed Layout Transistors drawbacks (more later...)
 - Single Event Effects tolerance
 - Density and Speed considerations
- The Enclosed Layout Transistor (ELT): special features
- One circuit example: a radiation tolerant analog memory
- Conclusions

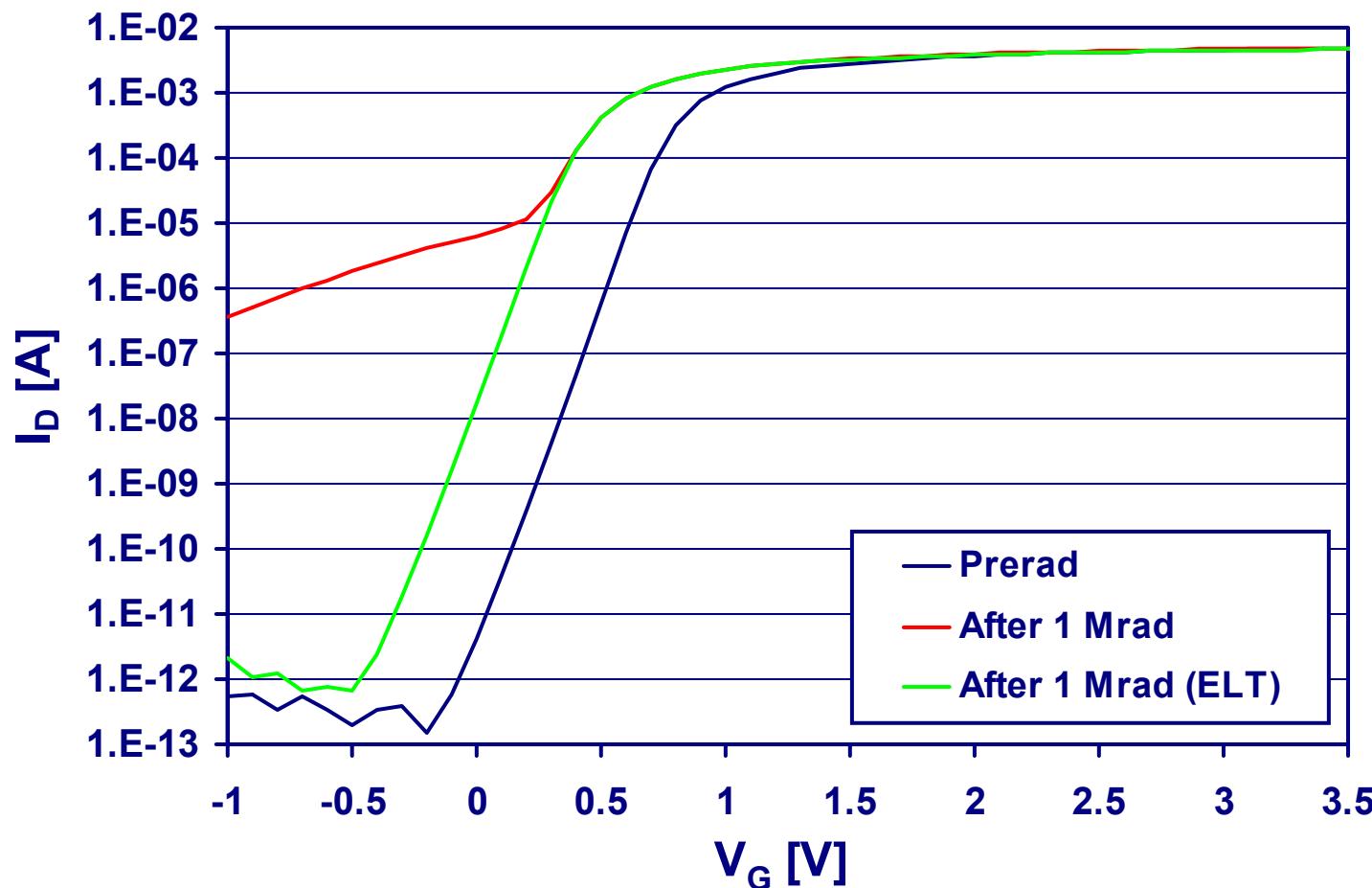
Enclosed Layout Transistor (ELT)



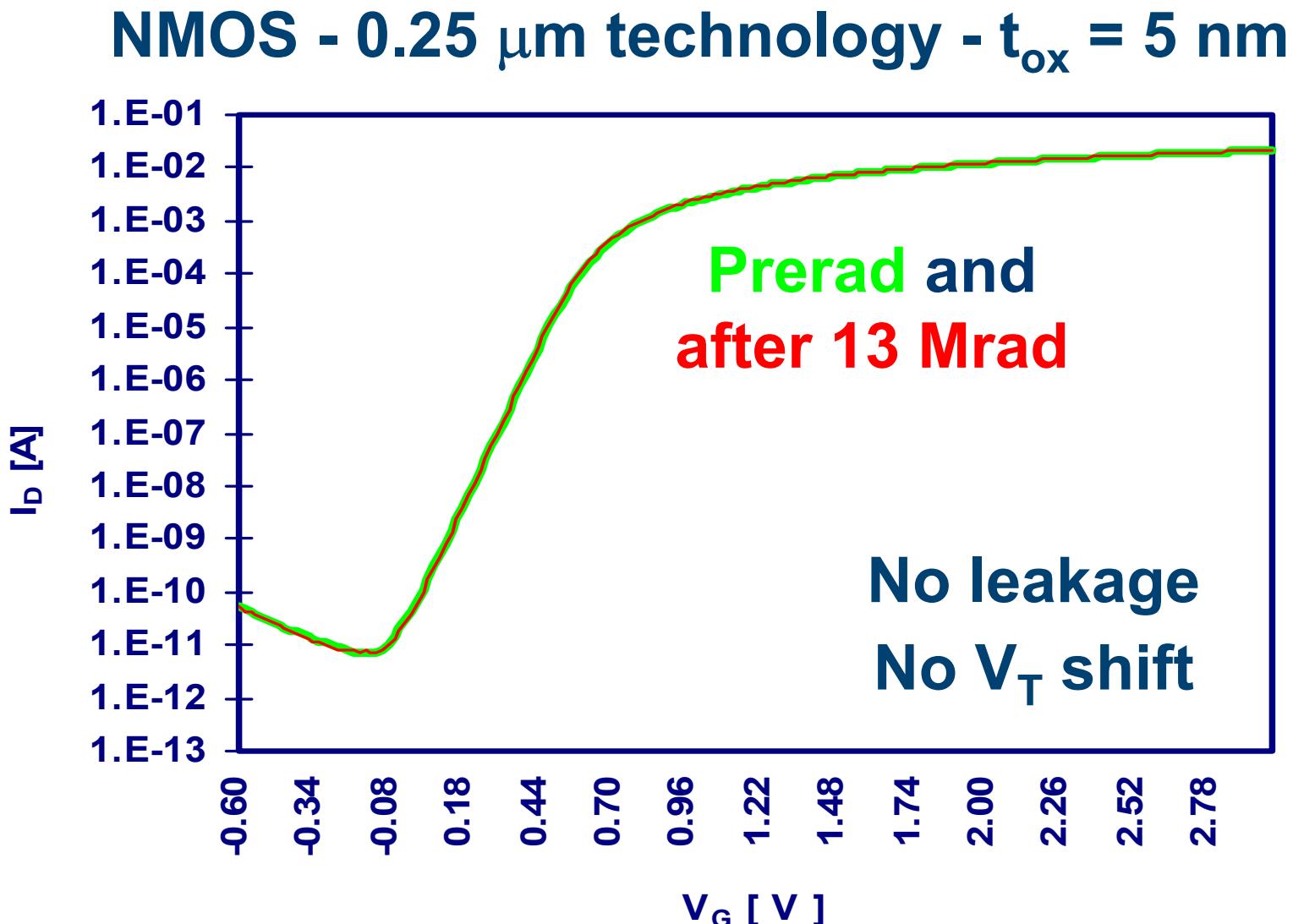
ELTs solve the leakage problem in the NMOS transistors
At the circuit level, guard rings are necessary

Effectiveness of ELTs

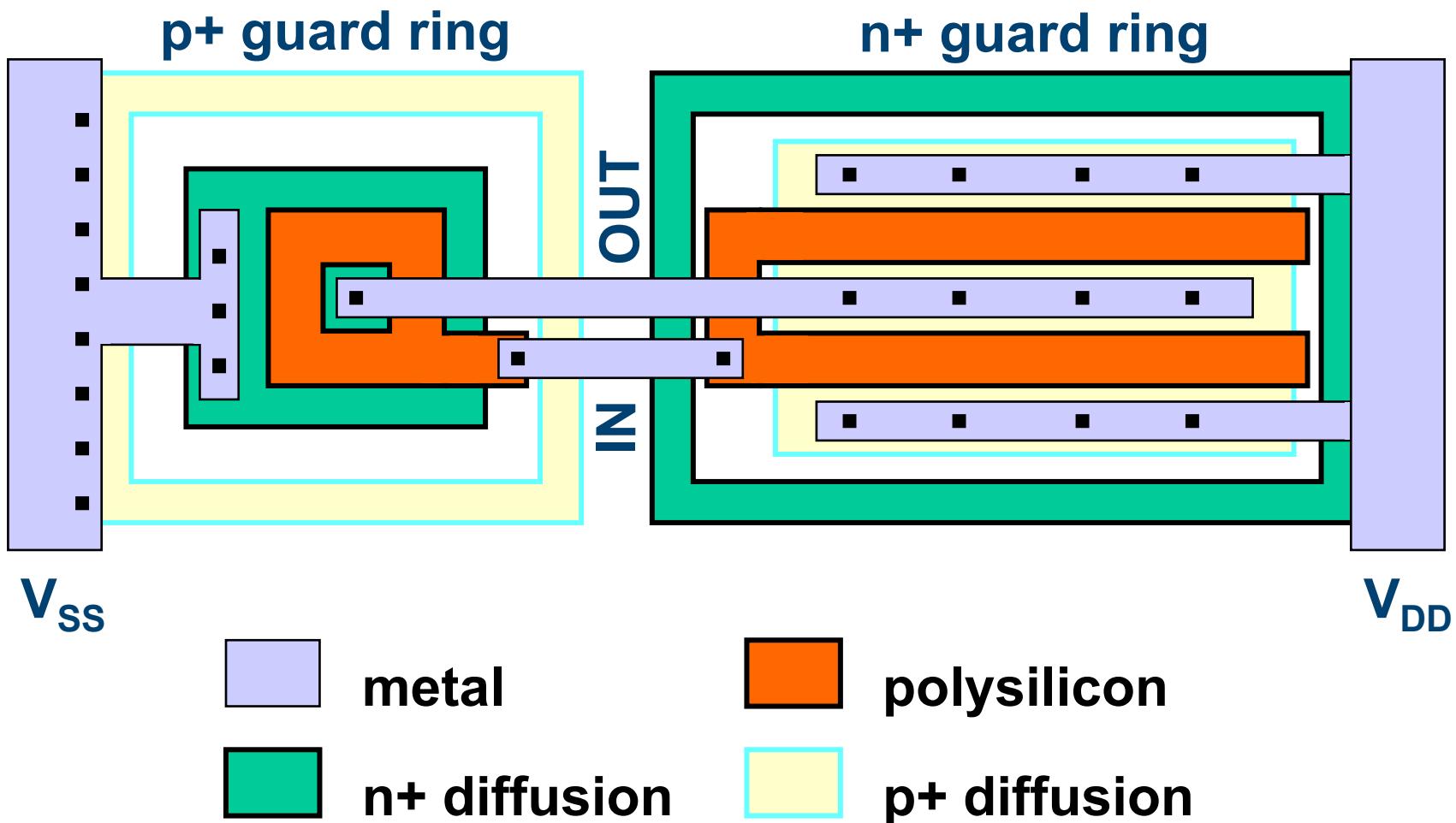
NMOS - 0.7 μm technology - $t_{\text{ox}} = 17 \text{ nm}$



ELT & deep submicron



A radiation-hard inverter



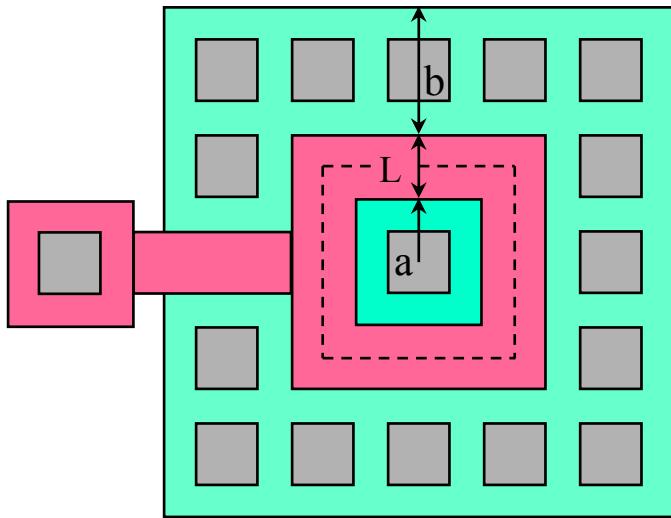
Total ionizing dose tolerance



Deep sub- μm means also:

- speed
- low power
- VLSI
- low cost
- high yield

Drawbacks of ELTs



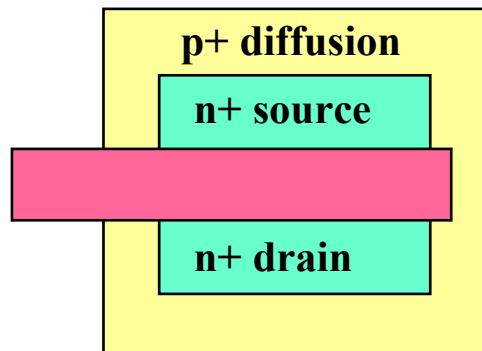
- Waste of area
- Increase in the parasitic gate and source/drain capacitances
- Modeling problems
- Lack of symmetry

$$W = 8a + 4L$$

$$W/L = 8a/L + 4$$

$$\text{Area} = 4(a+b+L)^2$$

Another possible solution? →



Single Event Effect tests

SEL

The systematic use of guard rings is
ALSO an effective tool against SEL
NO latch-up observed up to $89 \text{ MeVcm}^2\text{mg}^{-1}$

SEGR

Never observed in our circuits

SEU

The higher gate capacitance of ELTs
decreases the sensitivity

F. Faccio et al., "Single Event Effects in Static and Dynamic Registers in a 0.25 μm CMOS Technology", *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, Dec. 1999 , pp. 1434-1439.

SEU: comparison with the trend

This static cell

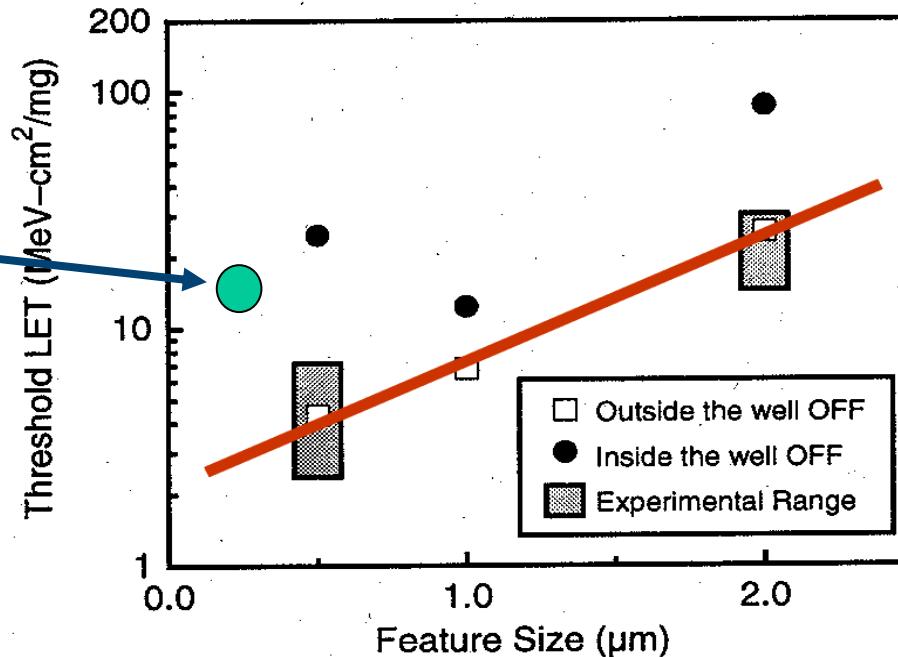
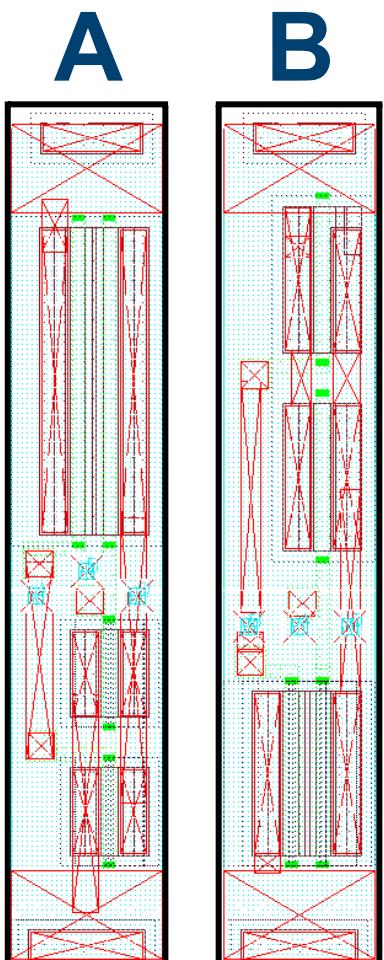


Figure 5. Experimentally-measured and simulated upset thresholds in three Sandia SRAM technology generations (no feedback resistors). The 1- and 2- μm technologies are n-substrate, 5 V; the 0.5- μm technology is p-substrate, 3.3 V.

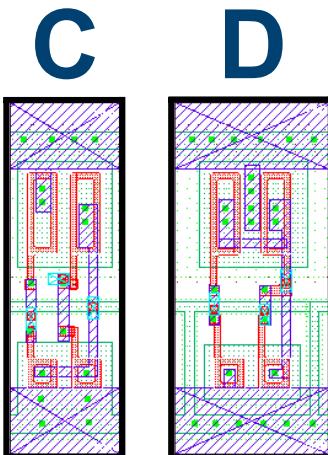
P.E. Dodd et al., "Impact of technology trends on SEU in CMOS SRAMs", *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, Dec. 1996, pp. 2797-2804.

Density and speed



$$\frac{\text{Area A}}{\text{Area C}} = 3.2$$

$$\frac{\text{Area B}}{\text{Area D}} = 2.2$$



A & B : 0.6 μm standard

C & D : 0.25 μm rad-tol

Inverter with F.O. = 1

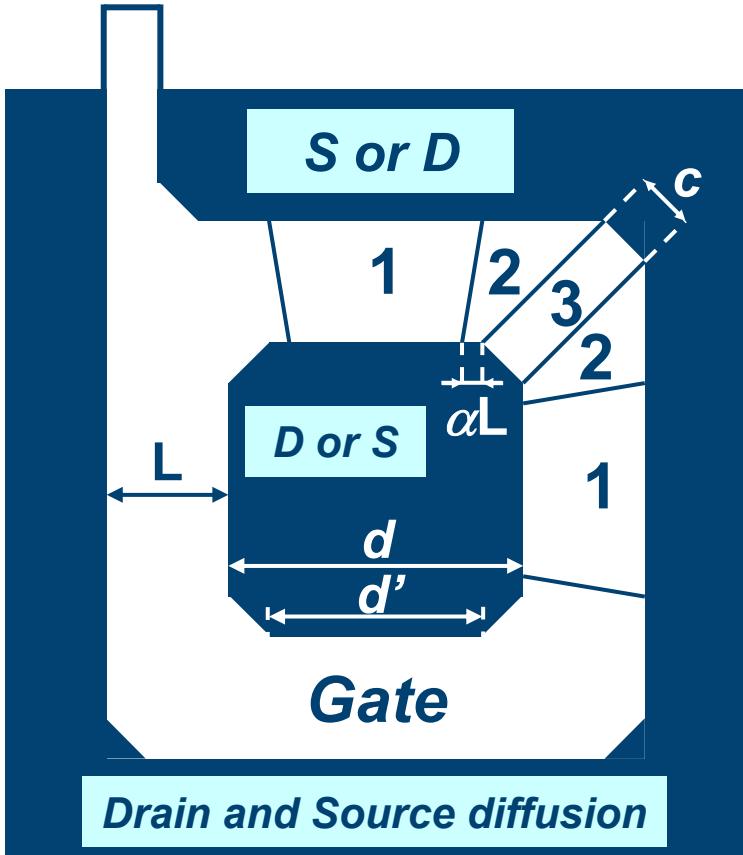
	0.6 μm	0.25 μm
V_{DD} [V]	3.3	2
Delay [ps]	114	48
Pwr [$\mu\text{W}/\text{MHz}$]	1.34	0.14
Area [μm^2]	162	50

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special UNWANTED features**
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Aspect ratio modeling



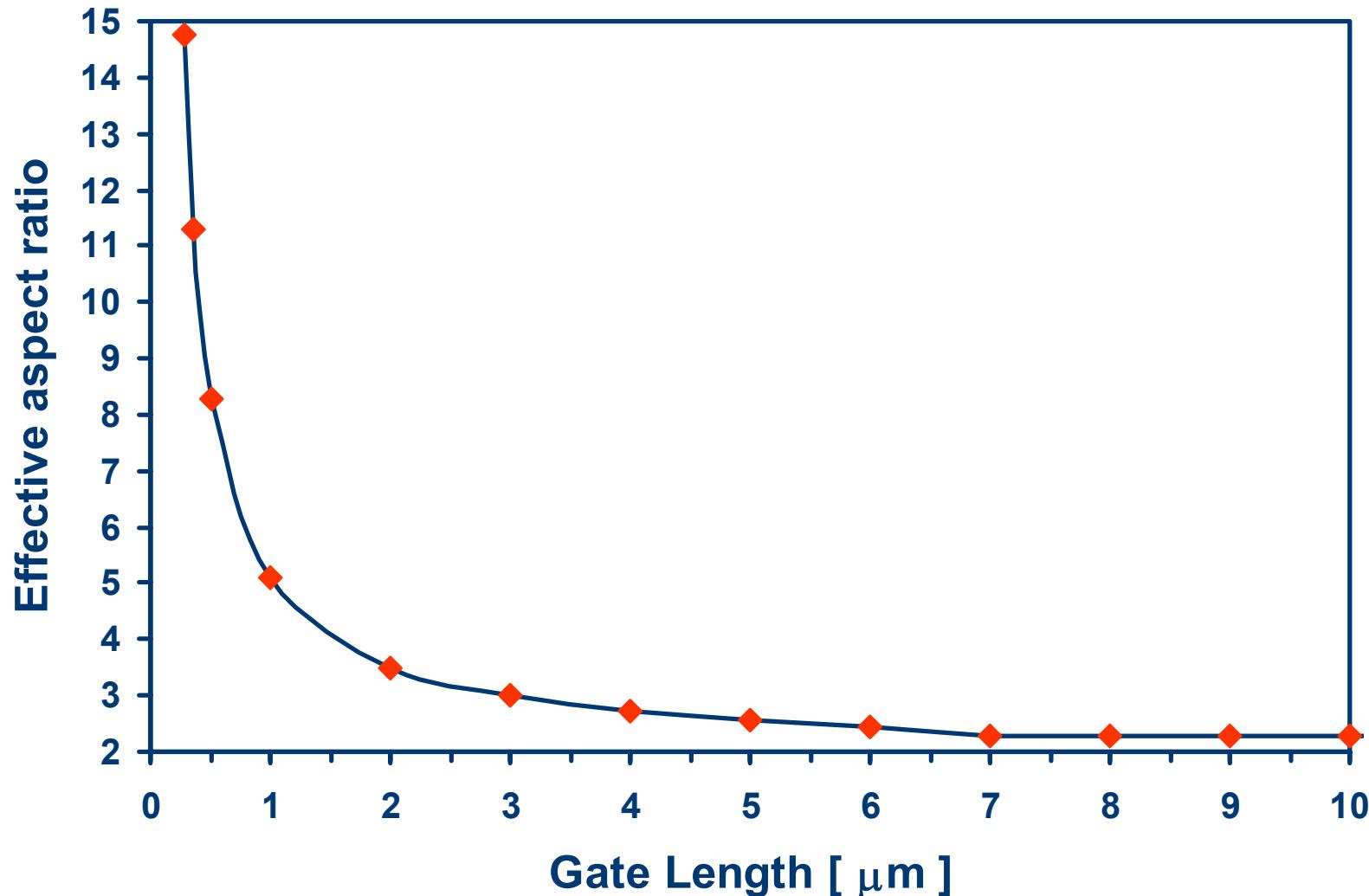
$$\frac{W}{L} = 4 \frac{2\alpha}{\ln \frac{d'}{d' - 2\alpha L}} + 2K \frac{1 - \alpha}{\frac{1}{2} \sqrt{\alpha^2 + 2\alpha + 5} \cdot \ln \frac{1}{\alpha}} + 3 \frac{\frac{d - d'}{2}}{L}$$

1 2 3

L (μm)	Calc. W/L	Extr. W/L
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

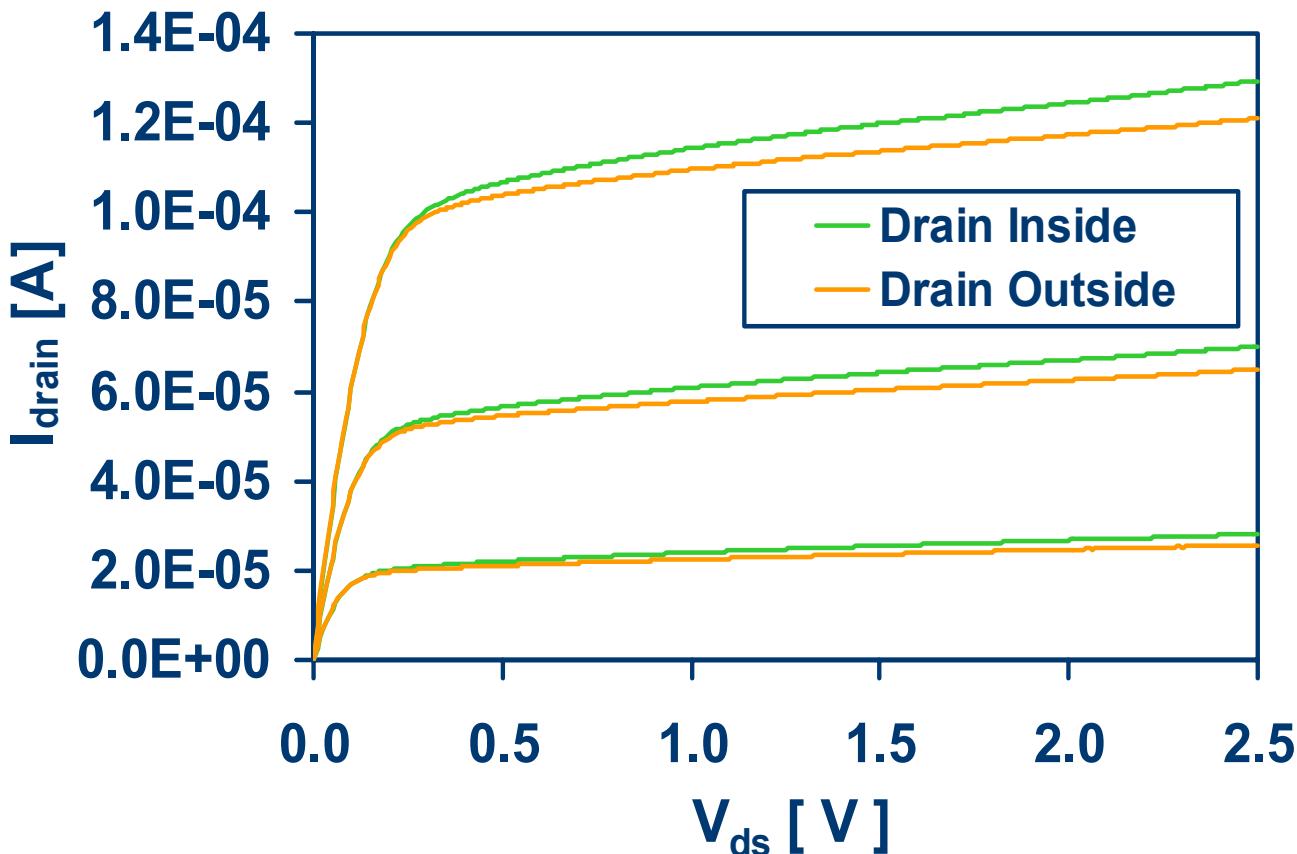
A. Giraldo et al., "Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout", *Solid-State Electronics*, vol. 44, June 2000, pp. 981-989.

Limitation in the W/L ratio values



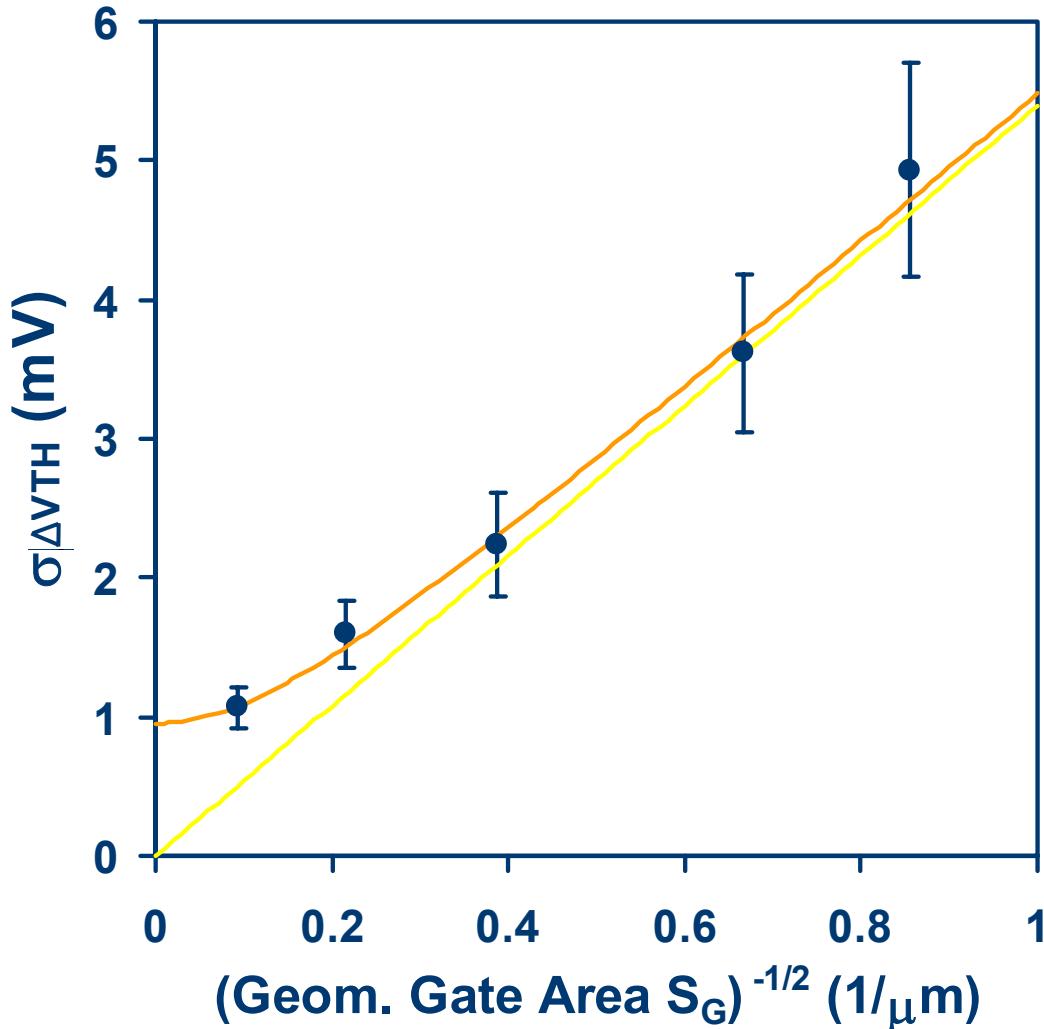
Output conductance

$$L = 0.28 \text{ } \mu\text{m} \quad G_{DI} = 11.9 \text{ } \mu\text{S} \quad G_{DO} = 9.6 \text{ } \mu\text{S}$$



L (μm)	$\Delta G/G_{DI}$
0.28	19 %
0.36	23 %
0.5	33 %
1	53 %
3	70 %
5	75 %

Matching of ELTs



$$\sigma_{\Delta P}^2 = \left(\frac{A_P}{\sqrt{S_G}} \right)^2 + \sigma_0^2$$

$$A_{V_{th}} = 5.4 \text{ mV} \cdot \mu\text{m}$$

$$\sigma_0 V_{th} = 0.95 \text{ mV}$$

$$A_{\beta} = 1.5 \% \cdot \mu\text{m}$$

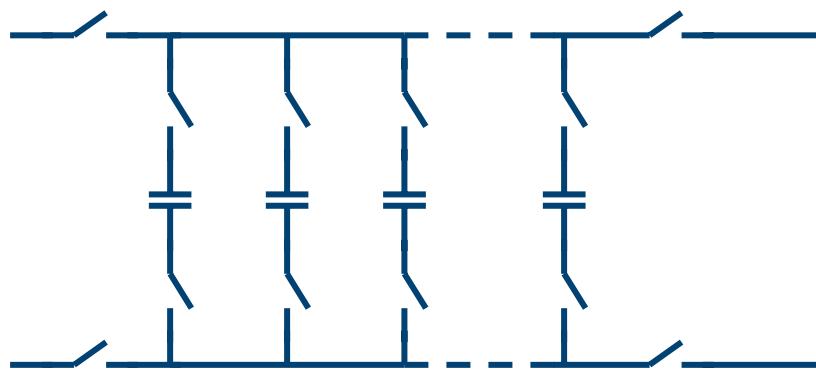
$$\sigma_0 \beta = 0.33 \%$$

Outline



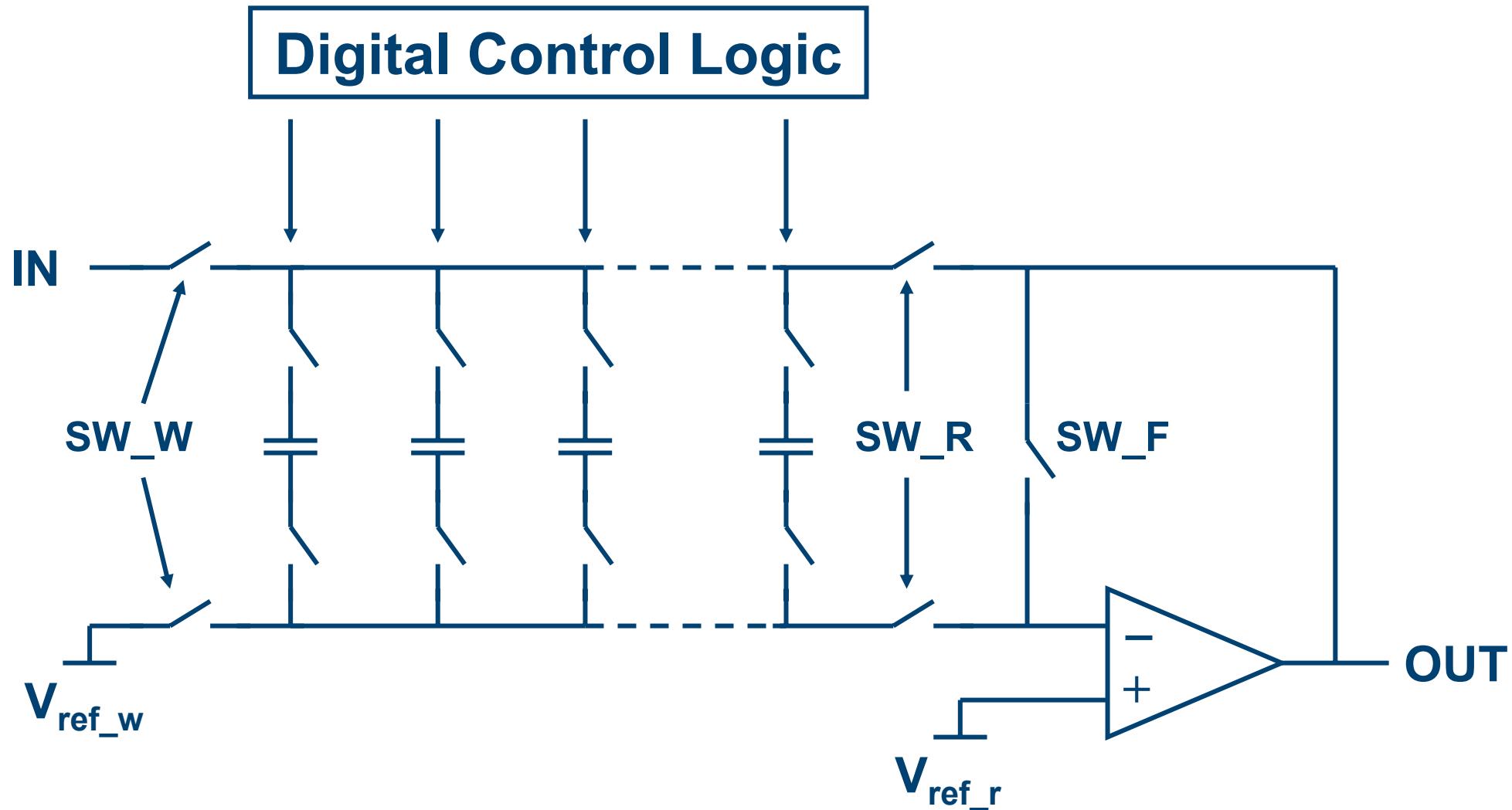
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Why an analog memory?

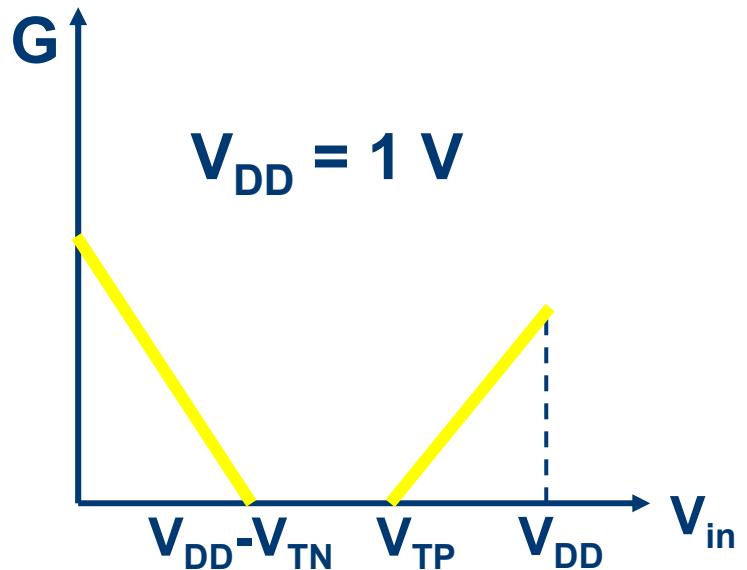
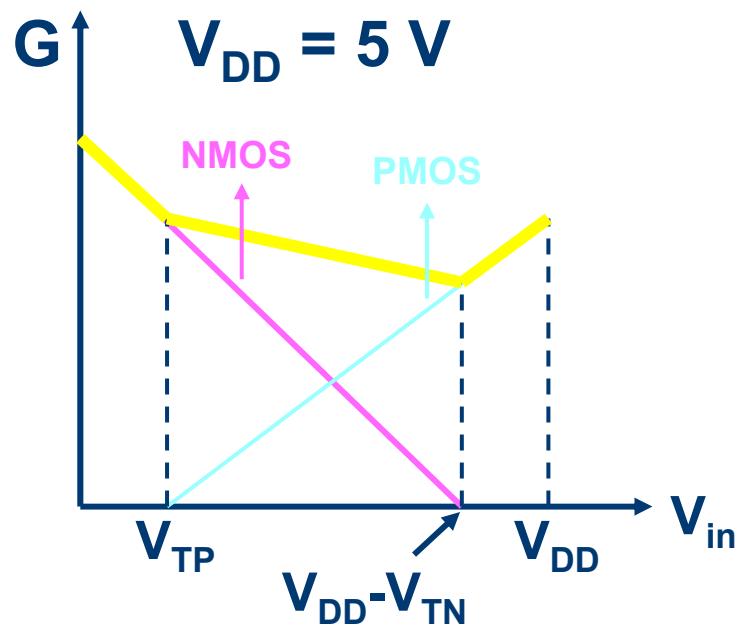
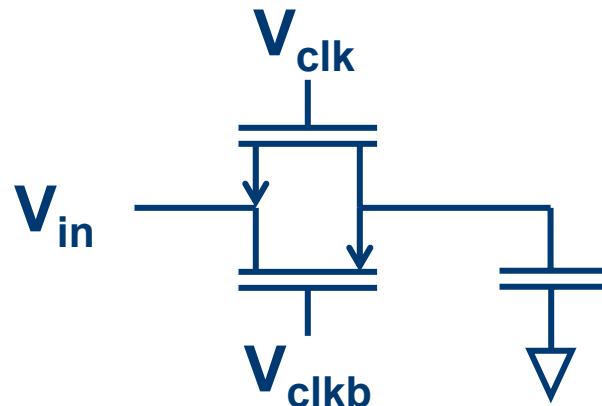


- Analog memories are often used in High Energy Physics applications
- Allows studying how to implement switched capacitor circuits in deep submicron CMOS processes
- Thin oxides (needed for radiation tolerance) requires low supply voltages, making difficult to have large dynamic ranges
- Allows to study the problems related to mixed signal circuits

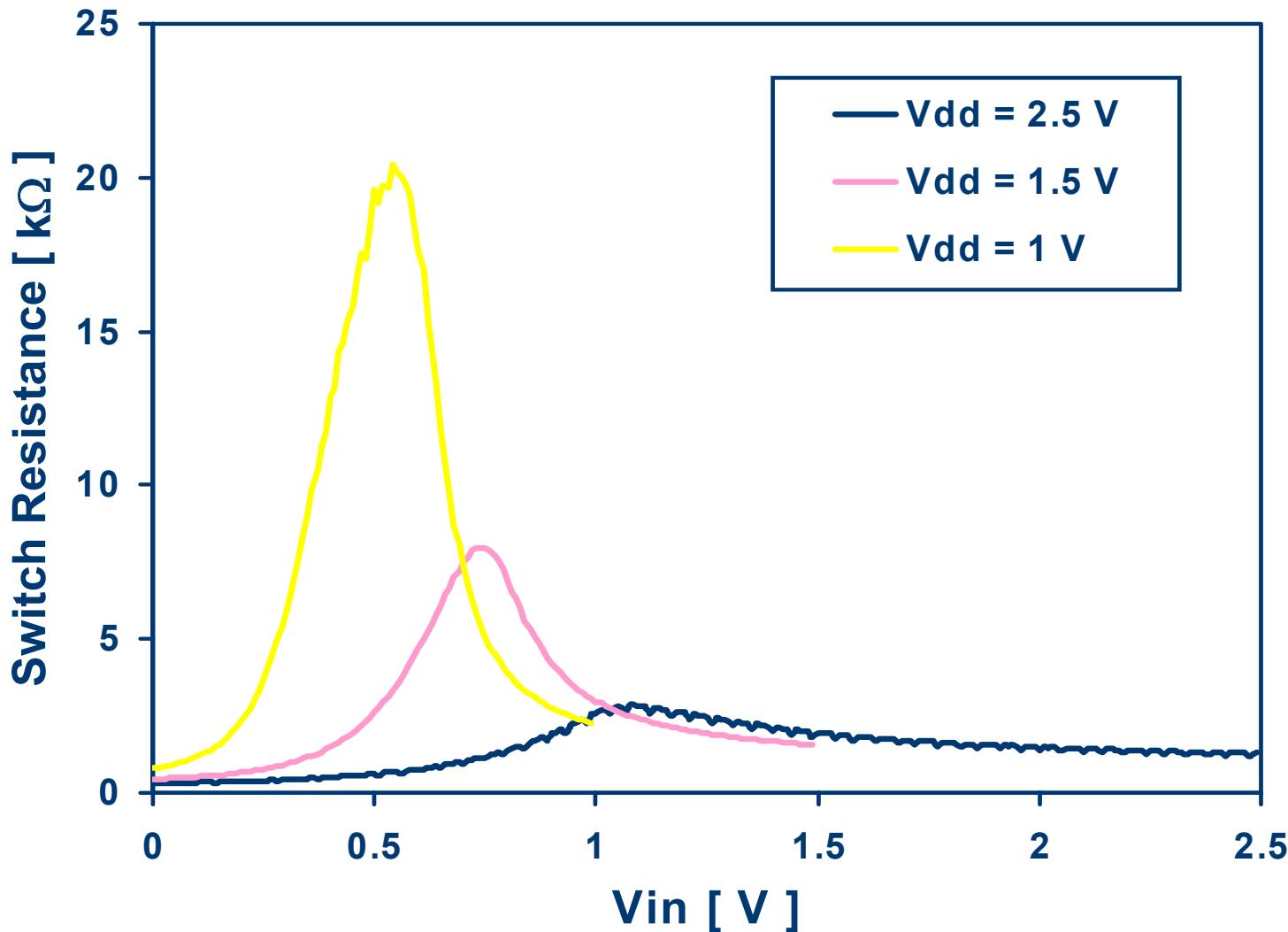
Memory channel schematic



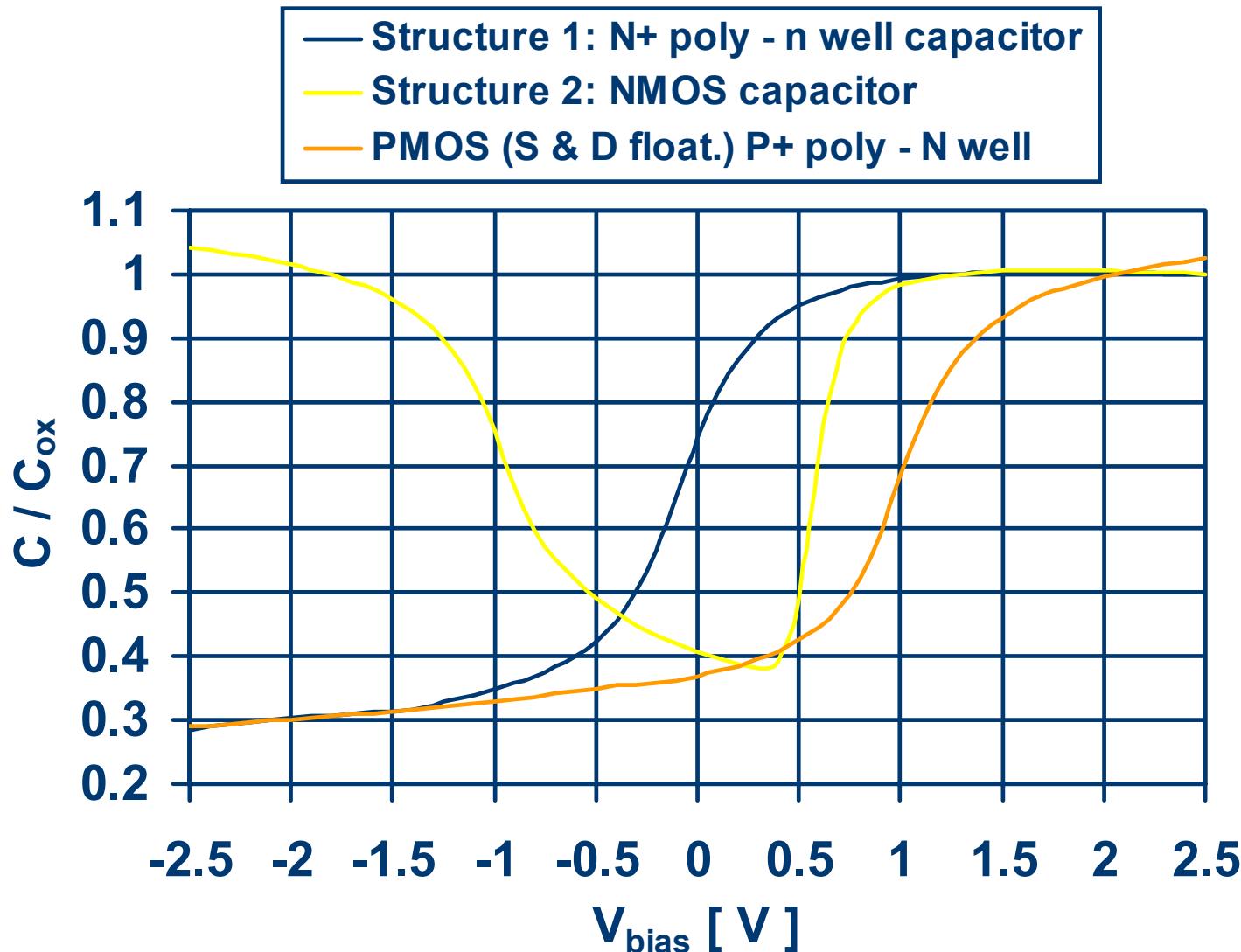
Switch “on” conductance



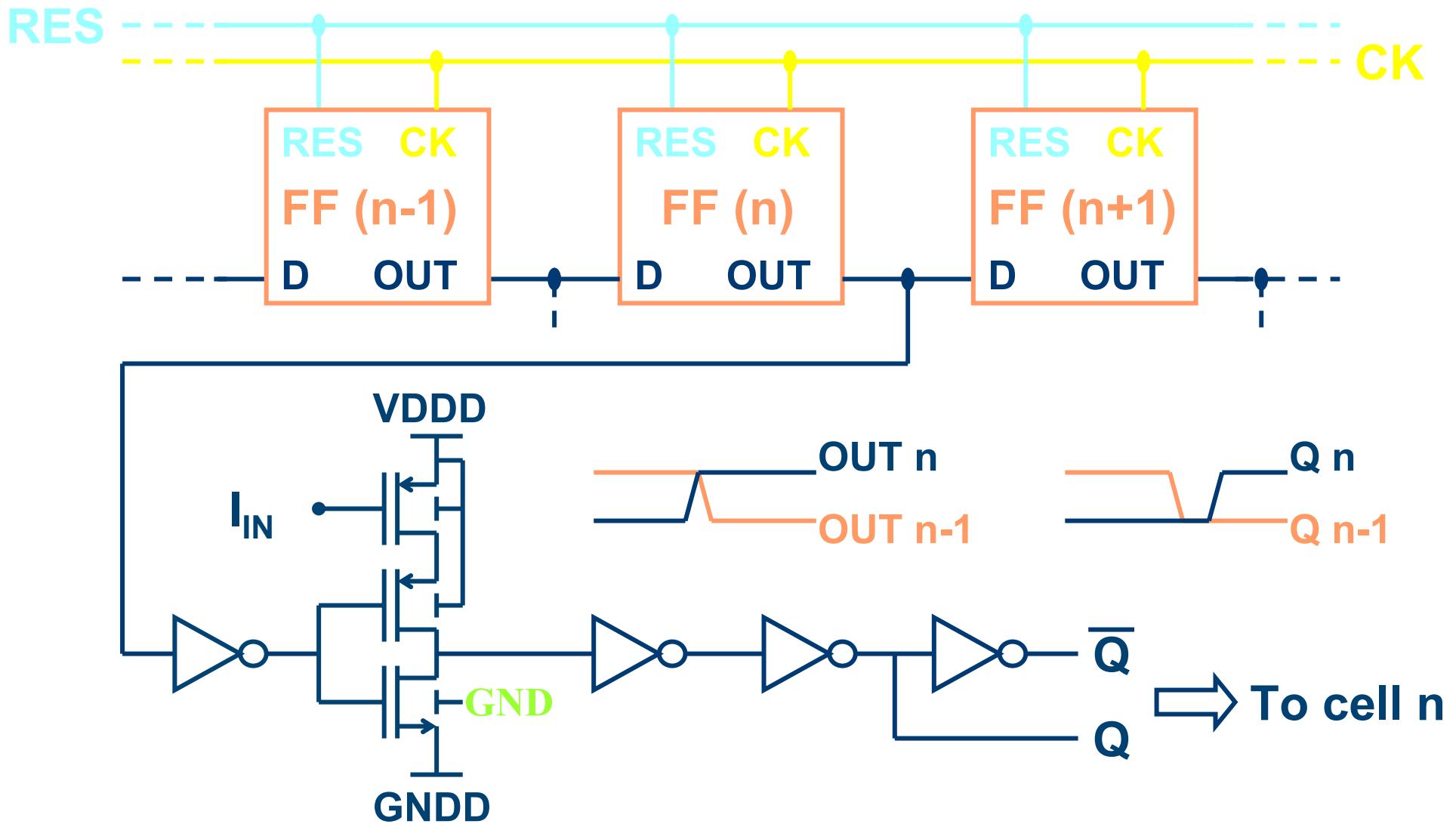
Switch “on” resistance



Which capacitor for storage?

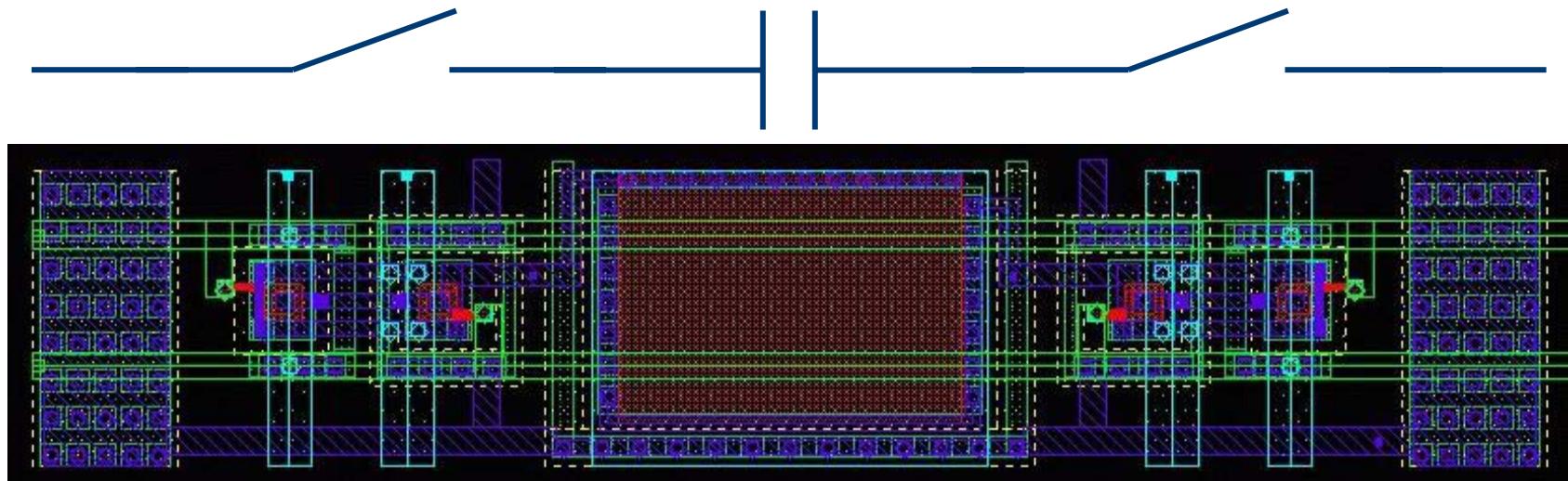


Shift register schematic

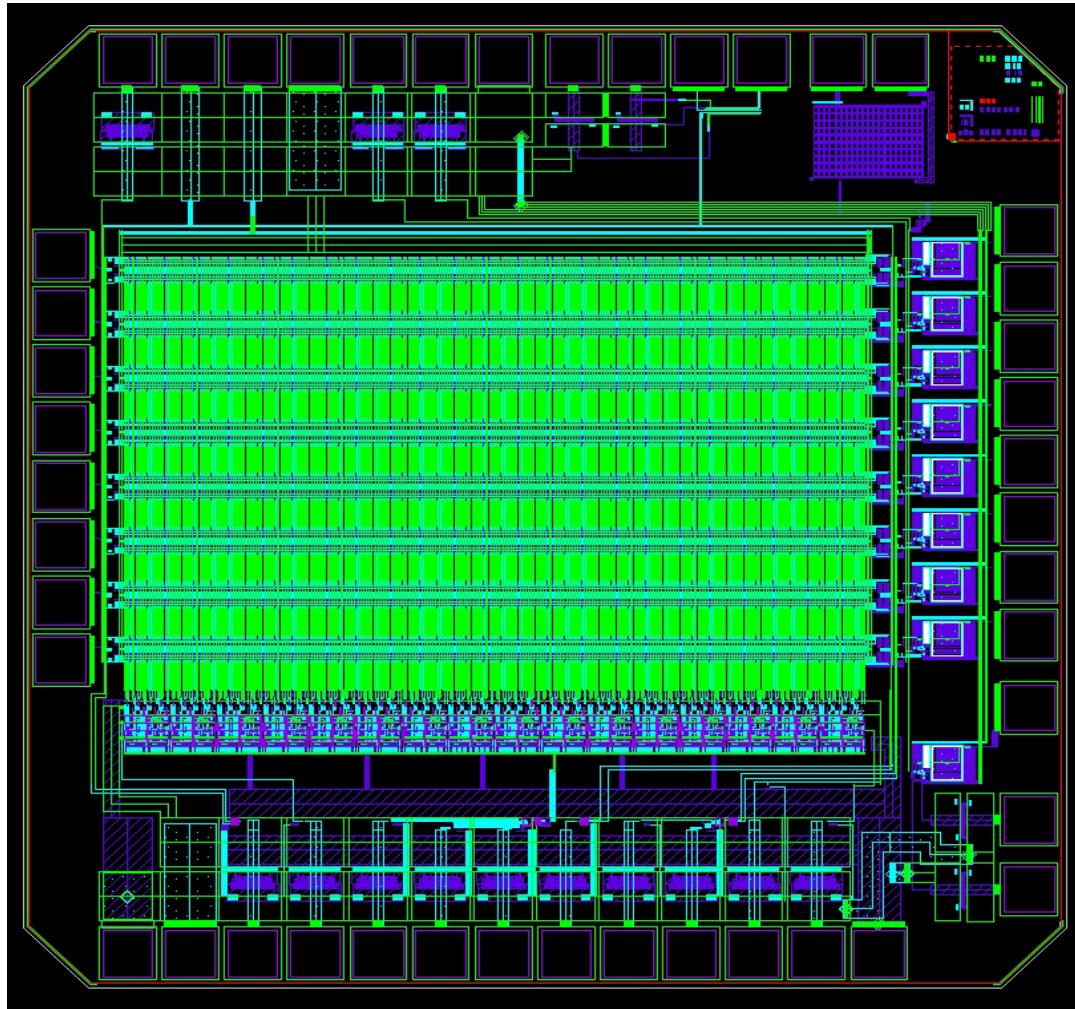


Memory cell layout

- Cell area: $56.1 \times 11.1 \mu\text{m}^2$
- Minimum size edgeless transistors for the CMOS switches
- $\text{Cox} \approx 5.5 \text{ fF}/\mu\text{m}^2$ $C = 600 \text{ fF}$
- Shielding

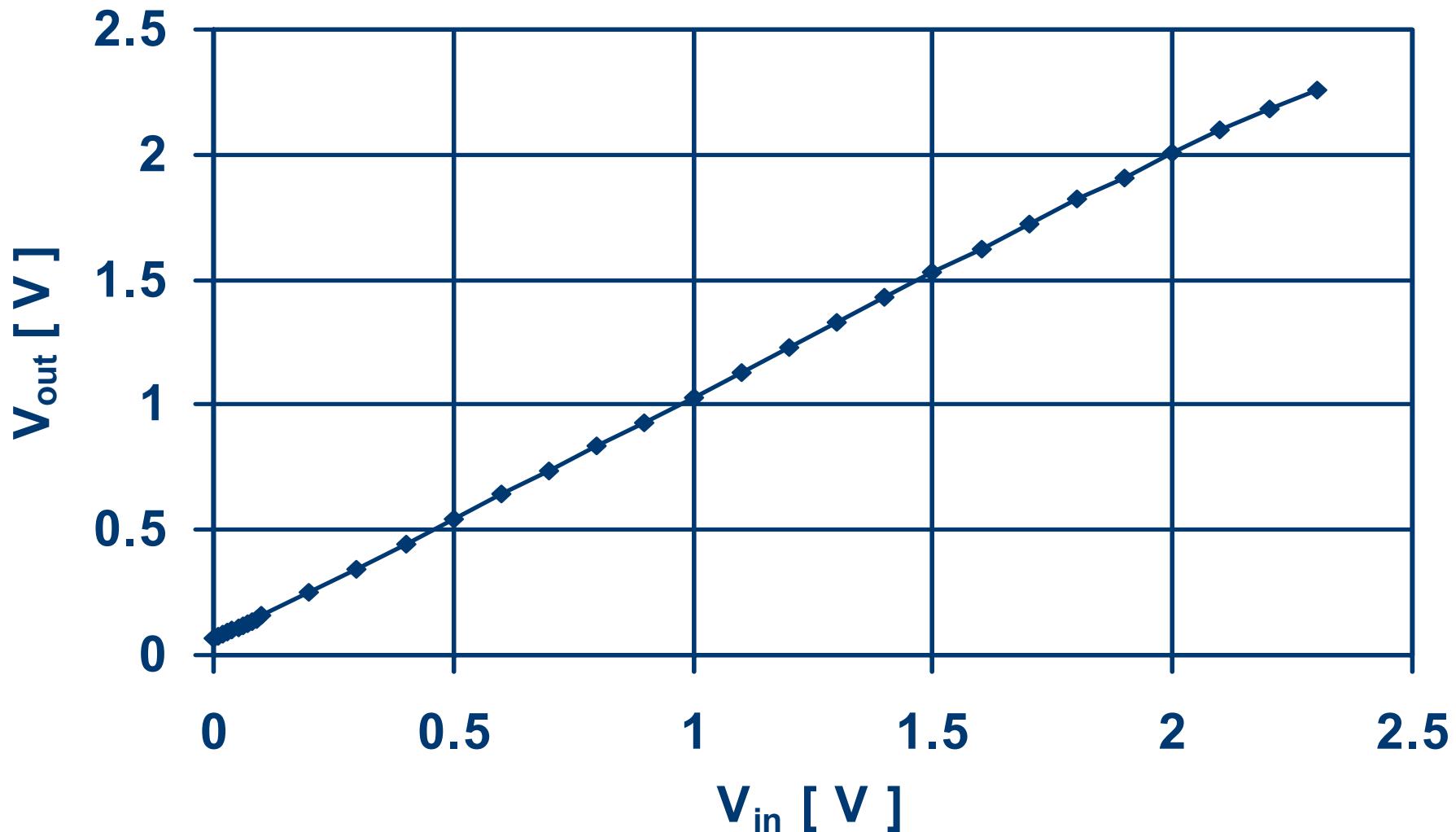


Test chip layout

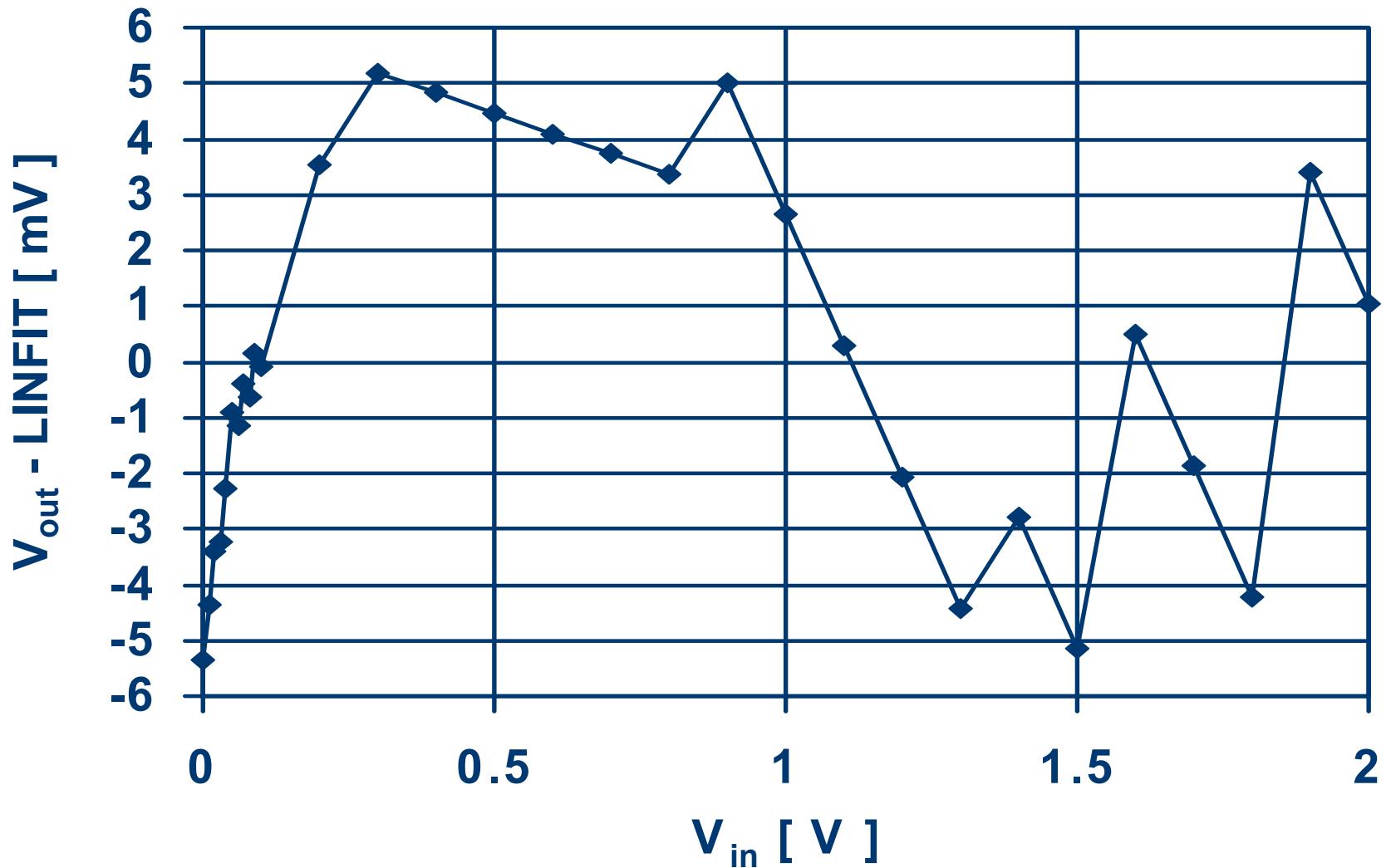


- 0.25 μm CMOS Tech.
- Rad-Tol Layout
- area: 2 x 2 mm²
- 8 channels
- 8 x 128 cells
- 9300 transistors
- capacitors
area: 0.11 mm²
- power consumption:
31.6 mW

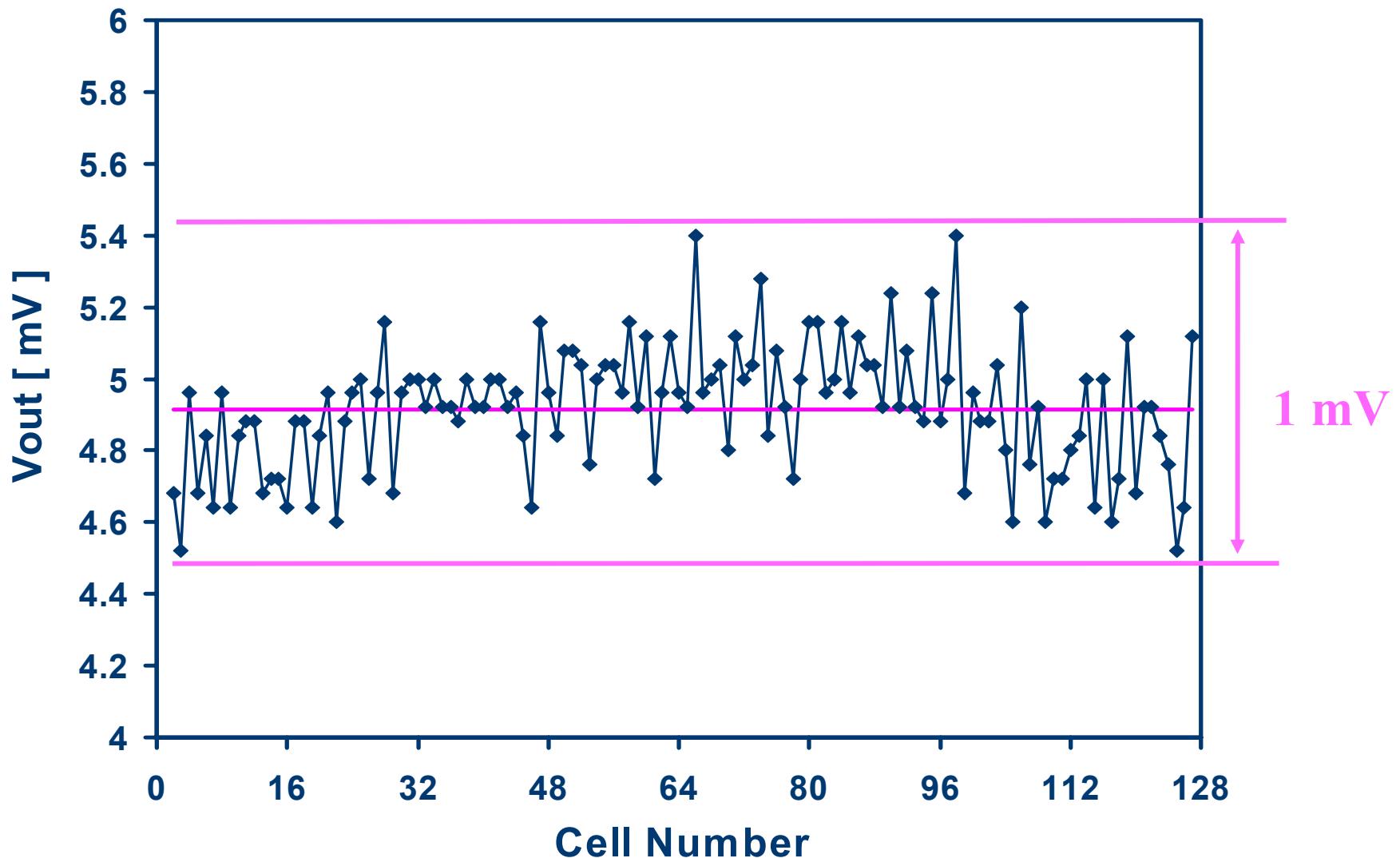
I-O characteristic linearity



Deviation from linearity



Pedestal variation



Performance summary

- **Noise measured $\approx 0.8 \text{ mV rms}$**
- **Pedestal variation $< 1 \text{ mV peak-to-peak}$**
- **Dynamic Range $> 11 \text{ bits}$**
- **Linearity $> 7.5 \text{ bits over } 2 \text{ V}$**
- **Cross talk $< 0.4\%$**

Radiation test results

- Source: 10 KeV X-rays
- Dose rate: 31.6 Krad/min
- The memory is written and read continuously
- Total dose: 10 Mrad
- $V_{in} = 1.5 \text{ V}$

$V_{DDA} [\text{V}]$	PWR pre	PWR after	$\Delta \%$
2.5	30.95 mW	30.5 mW	1.45

$V_{DDD} [\text{V}]$	$f_w [\text{MHz}]$	PWR pre	PWR after	$\Delta \%$
2.5	25	390 μW	377 μW	3.3
2	25	216 μW	212 μW	1.8
2.5	50	707 μW	685 μW	3.2
2.5	12.5	225 μW	215 μW	4.4

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Conclusions

- Scaling is a general trend in CMOS, since it allows to have faster, denser and less power consuming integrated circuits. Generally it improves TID and SEL tolerance but it might worsen SEU
- We have demonstrated that deep submicron technologies can stand very high radiation doses (30 Mrad) provided special layout rules are obeyed
- Guard rings are effective against SEL, and there are special architectures to reduce SEU sensitivity
- In this work we have developed the know-how necessary to design radiation tolerant ICs using ELTs: modeling, matching and noise issues have been characterized in detail
- The validity of this approach has been demonstrated on several mixed-mode ICs which will be used in the LHC experiments
- Due to the possibility of consistent costs reduction, many experiments decided and are deciding to adopt our approach to make the integrated circuits for detector read-out
- To pursue this approach in the future, and therefore follow the CMOS technology down-scaling, many issues will have to be addressed:
 - Radiation effects in new materials (low and high K dielectrics)
 - New SEU-tolerant architectures
 - Low-voltage architectures
 - Modeling, matching, noise issues
 - Gate leakage current