

High linearity CMOS circuits for signal processing

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Outline

- Continuous-time integrators
- Linearization methods for transistor-only OTAs
- Resistor-based highly linear OTAs
- Conclusions

Active-RC integrators

- good linearity if linear resistors and capacitors are available
- require large die area for resistors and/or capacitors
- large value resistors=substantial thermal noise
- small value resistors=high current output capability op-amps

Ideal op-amp

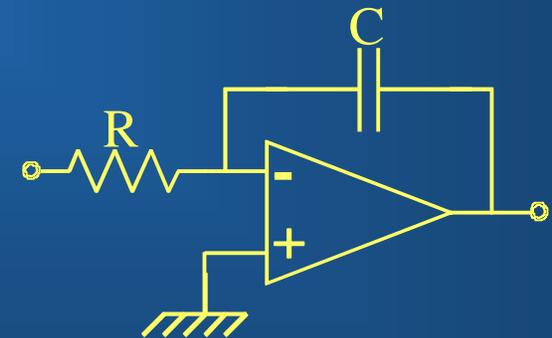
$$T(s) = -\frac{RC}{s}$$

$$A(s) = \frac{A\omega_a}{s + \omega_a} = \frac{\omega_t}{s + \omega_a} \Rightarrow$$

Finite gain op-amp

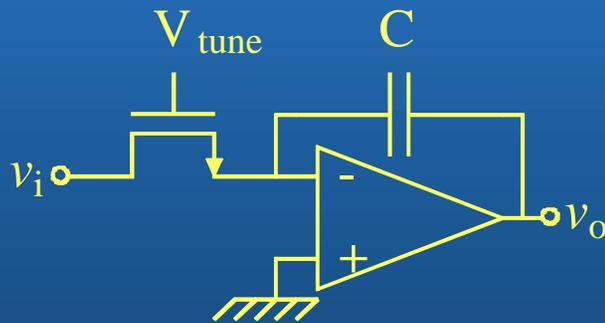
$$T(s) = -\frac{1}{sRC + \frac{1}{A(s)}(sRC + 1)}$$

$$T(s) \approx -\frac{\omega_t}{RC} \frac{1}{(s + p_1)(s + p_2)}$$

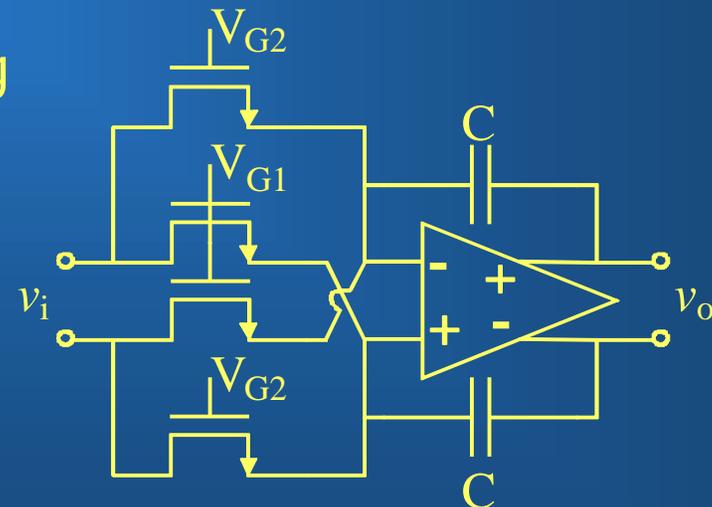


MOSFET-C integrators

- reduced linearity due to nonlinear characteristic of input MOS transistors functioning in triode region (the linearity can be improved by using cross-coupled transistors)
- reduced dynamic range (to keep the MOSFETs in the triode region)
- possibility of electronic tuning



Single-ended



Fully differential with improved linearity

OTA-C (G_m -C) integrators

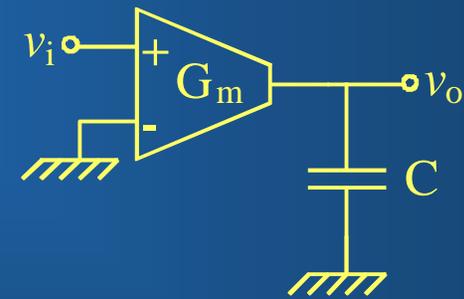
- poor linearity; require linearization circuitry for the transistor-only transconductors or use of resistor-based transconductors
- better frequency response compared to active-RC and MOSFET-C integrators
- possibility of electronic tuning (for transistor-only ones)

Ideal OTA: $T(s) = \frac{G_m}{sC}$

Real OTA (finite output resistance, frequency dependent transconductance)

$$G_m(s) = G_m \frac{p_2}{s + p_2}$$

$$T(s) = \frac{G_m}{C} \frac{p_2}{(s + p_1)(s + p_2)}, \quad p_1 = \frac{1}{CR_0} = \frac{G_m}{AC}, \quad G_m R_0 = A$$



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Transistor-only linear OTAs

- An operational transconductance amplifier has the same structure as an operational amplifier, but without the output stage. Therefore, the output of an OTA is characterized by a high output resistance, behaving as a current source.
- Because the G_m -C integrators are implemented using feed-forward topologies, the distortions introduced by the nonlinearity of the OTA will not be decreased by any feedback loop. Therefore, linearization techniques are used in the input stage of the transconductor.
- All linearization methods to be presented introduce additional devices. As a result the noise of such structures is higher, the bandwidth is smaller, the offset is larger.
- Only the modifications in the input differential pair will be presented. The complete transconductors will contain active loads and/or subsequent gain stages.

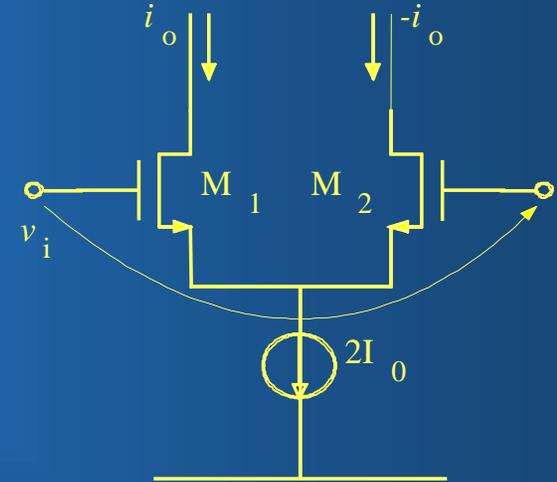
Simple differential pair

$$i_{D1} = I_0 + i_o; \quad i_{D2} = I_0 - i_o$$

$$v_i = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}}$$

$$i_o = \sqrt{\frac{\beta I_0}{2}} v_i \sqrt{1 - \frac{\beta v_i^2}{8I_0}} = \sqrt{\frac{\beta I_0}{2}} v_i \sqrt{1 - \frac{v_i^2}{4(V_{GS} - V_T)^2}}$$

$$G_m = \frac{i_o}{v_i} = \sqrt{\frac{\beta I_0}{2}}, \quad \text{for } v_i \ll 2(V_{GS} - V_T)$$



Differential pair with source degeneration using MOS transistors

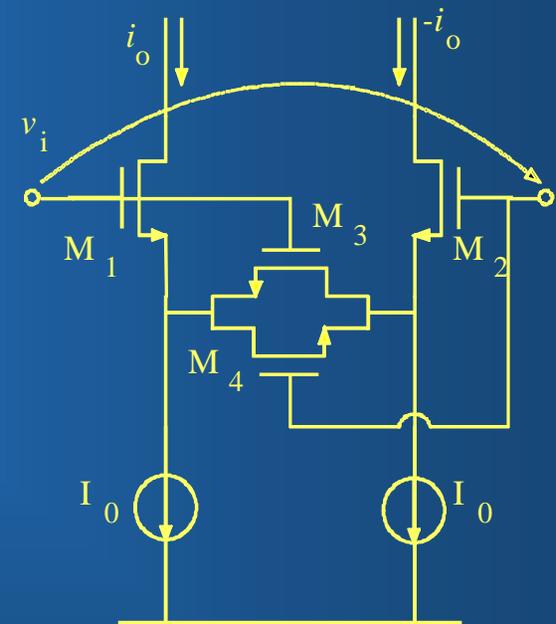
- M_3 and M_4 in triode region:

$$i_o = \sqrt{\frac{\beta I_0}{2}} \frac{v_i}{a} \sqrt{1 - \frac{\beta v_i^2}{a^2 I_0}}, \quad a = 1 + \frac{\beta_1}{4\beta_3}$$

$$G_m = \frac{i_o}{v_i} = \frac{1}{a} \sqrt{\frac{\beta I_0}{2}}, \quad a_{opt} \approx 2.5 \quad (\beta_1 \approx 6\beta_3)$$

- The linear region extends for the case in which one of transistors M_3 , M_4 is in saturation and the other one in triode.

(Krummenacher and Joel-1988)



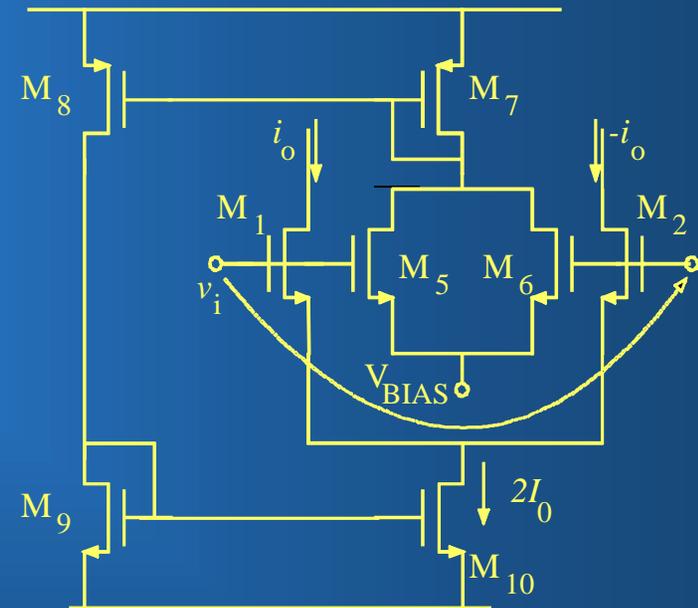
Differential pair with adaptive biasing

$$I_0 = I'_0 + \frac{\beta_1 v_i^2}{8}$$

$$i_o = \sqrt{\frac{\beta_1 I_0}{2}} v_i \sqrt{1 - \frac{\beta_1 v_i^2}{8 I_0}} = \sqrt{\frac{\beta_1 I'_0}{2}} v_i$$

$$G_m = \frac{i_o}{v_i} = \sqrt{\frac{\beta_1 I'_0}{2}}$$

$$2I_0 = \frac{\beta_5 v_i^2}{4} + \beta_5 (V_{BIAS} + V_T)^2$$



- The adaptive biasing current I_0 is generated by the M_5 - M_6 pair (having the same geometric aspect as the differential pair M_1 - M_2) and the two current mirrors M_7 - M_8 , M_9 - M_{10} .

Cross-coupled differential pairs

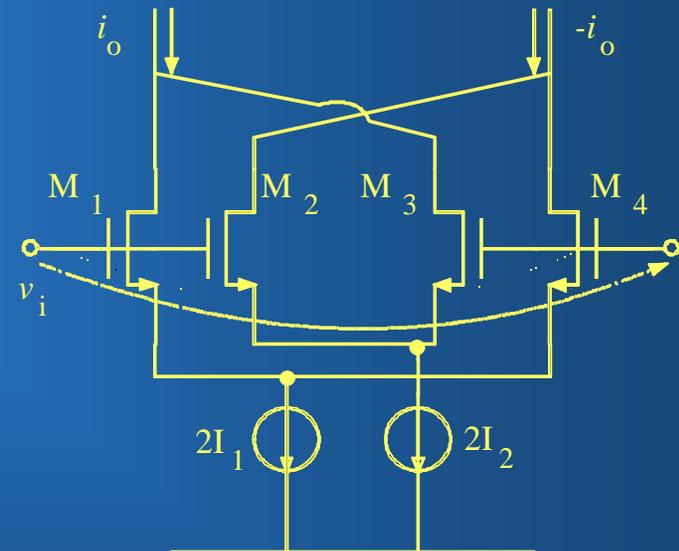
- Cross-couple two differential pairs with different linear parts and identical nonlinear parts

$$i'_o = \sqrt{\frac{\beta_1 I_1}{2}} v_i \sqrt{1 - \frac{\beta_1 v_i^2}{8I_1}} \approx \sqrt{\frac{\beta_1 I_1}{2}} v_i \left(1 - \frac{\beta_1 v_i^2}{16I_1}\right)$$

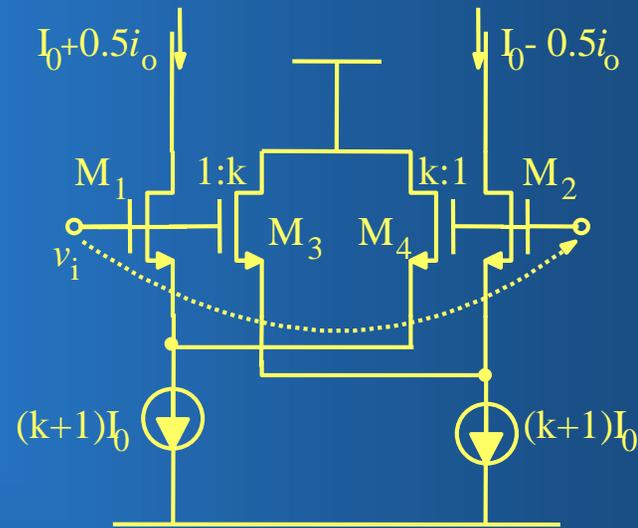
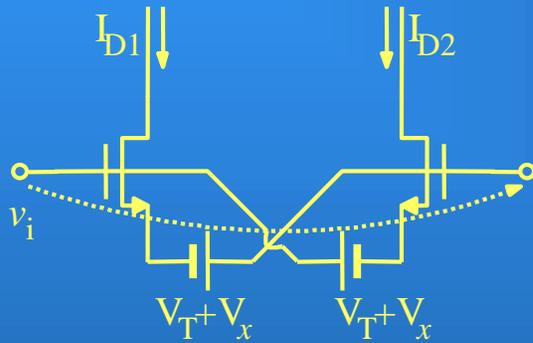
$$i''_o = \sqrt{\frac{\beta_2 I_2}{2}} v_i \sqrt{1 - \frac{\beta_2 v_i^2}{8I_2}} \approx \sqrt{\frac{\beta_2 I_2}{2}} v_i \left(1 - \frac{\beta_2 v_i^2}{16I_2}\right)$$

$$i_o = i'_o - i''_o = \left(\sqrt{\frac{\beta_1 I_1}{2}} - \sqrt{\frac{\beta_2 I_2}{2}} \right) v_i, \text{ if } \frac{\beta_1^3}{I_1} = \frac{\beta_2^3}{I_2}$$

$$G_m = \frac{i_o}{v_i} = \sqrt{\frac{\beta_1 I_1}{2}} - \sqrt{\frac{\beta_2 I_2}{2}}$$



Shift level biasing



$$i_o = I_{D1} - I_{D2} = 2\beta V_x v_i.$$

$$G_m = 2\beta V_x$$

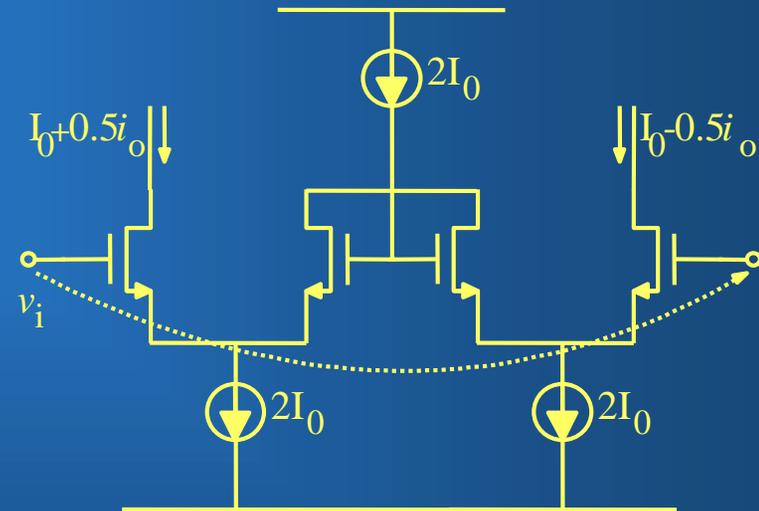
- The right side circuit shows a possible implementation of the voltage sources used for level shifting.

Series connection of multiple differential pairs

- Split the input voltage between N differential pairs connected in series

$$i_o = \frac{v_i}{N} \sqrt{\beta \frac{I_0}{2}} \sqrt{1 - \beta \frac{v_i^2}{8N^2 I_0}}$$

$$G_m = \frac{1}{N} \sqrt{\frac{\beta I_0}{2}}$$



Pseudo-differential pair

- Transistors M_1 and M_2 are operating in the triode region. Transistors M_3 and M_4 are source-followers and current buffers.

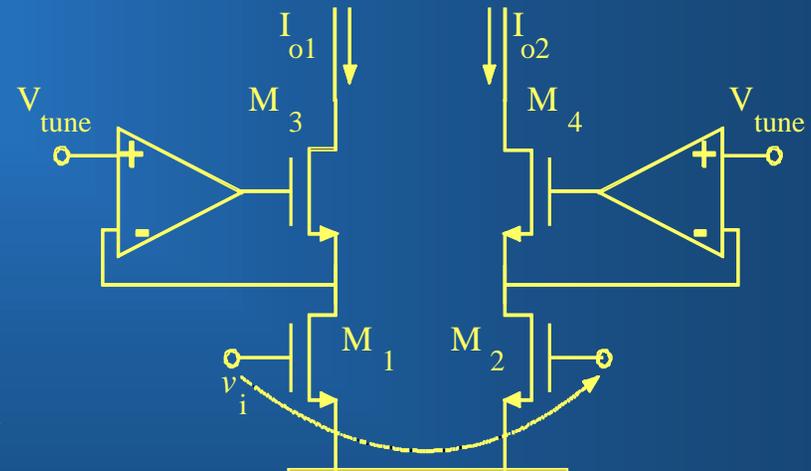
$$I_{o1} = i_{D1} = \frac{\beta}{2} [2(v_{GS1} - V_T)v_{DS1} - v_{DS1}^2]$$

$$I_{o2} = i_{D2} = \frac{\beta}{2} [2(v_{GS2} - V_T)v_{DS2} - v_{DS2}^2]$$

$$v_{DS1} = v_{DS2} = V_{tune}$$

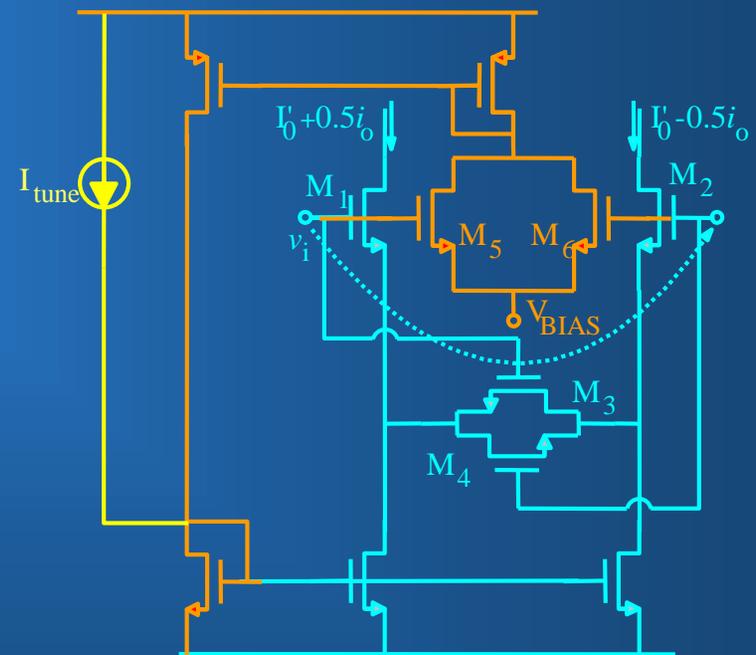
$$i_o = \frac{I_{o1} - I_{o2}}{2} = \frac{\beta}{2} (v_{GS1} - v_{GS2})V_{tune} = \frac{\beta}{2} v_i V_{tune}$$

$$G_m = \frac{i_o}{v_i} = \frac{\beta V_{tune}}{2}$$

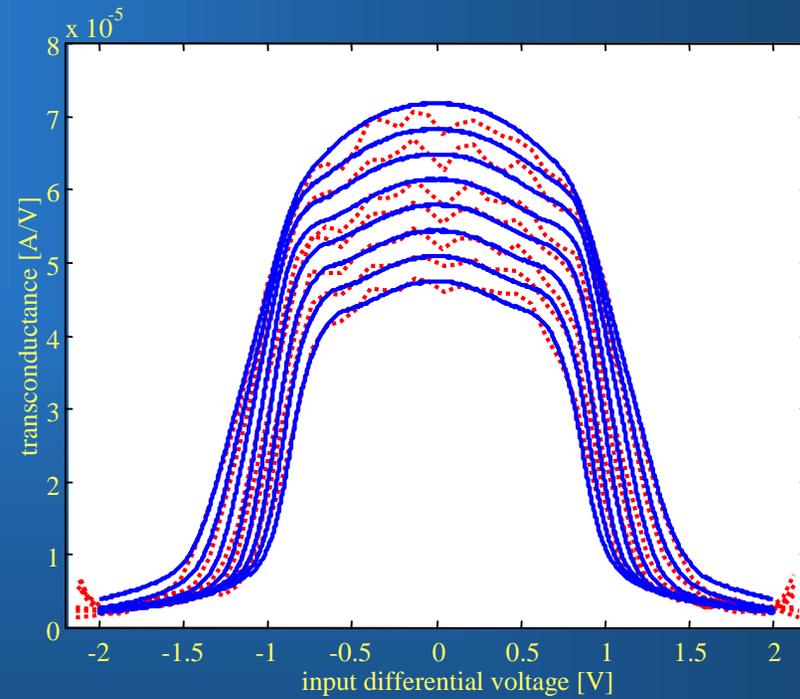
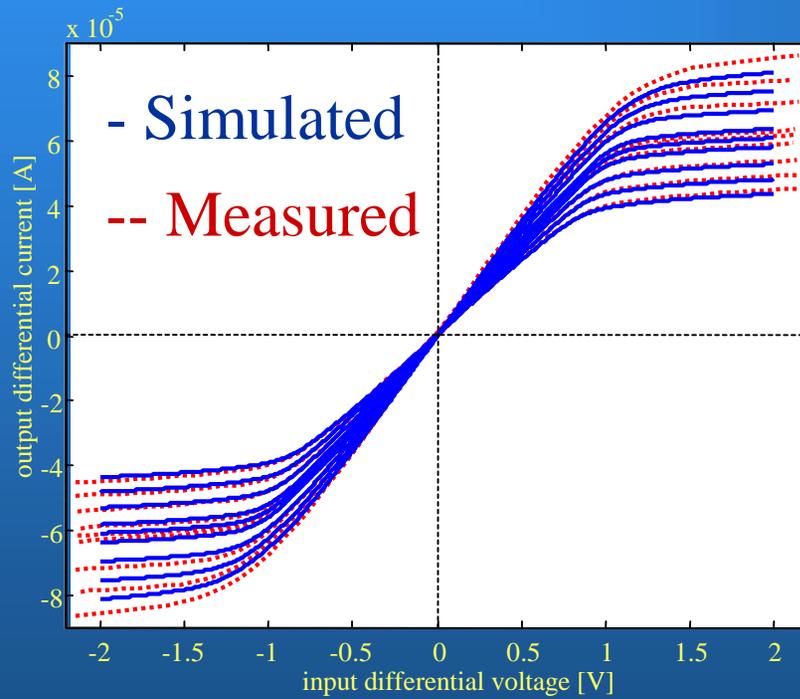


Original linear CMOS transconductor

- Combines two previously reported linearization techniques (Krummenacher and Joel-1988, Nedungadi and Viswanathan-1984).
- K.-C. Kuo and A. Leuciuc, "A novel linear tunable MOS transconductor", MWSCAS 2000, Lansing, Michigan, August 8-11, 2000.
- K.-C. Kuo and A. Leuciuc - "A Linear MOS Transconductor Using Source Degeneration and Adaptive Biasing", IEEE Trans. on Circuits and Systems-Part II, vol. 48, no. 10, Oct. 2001, pp. 937-943.

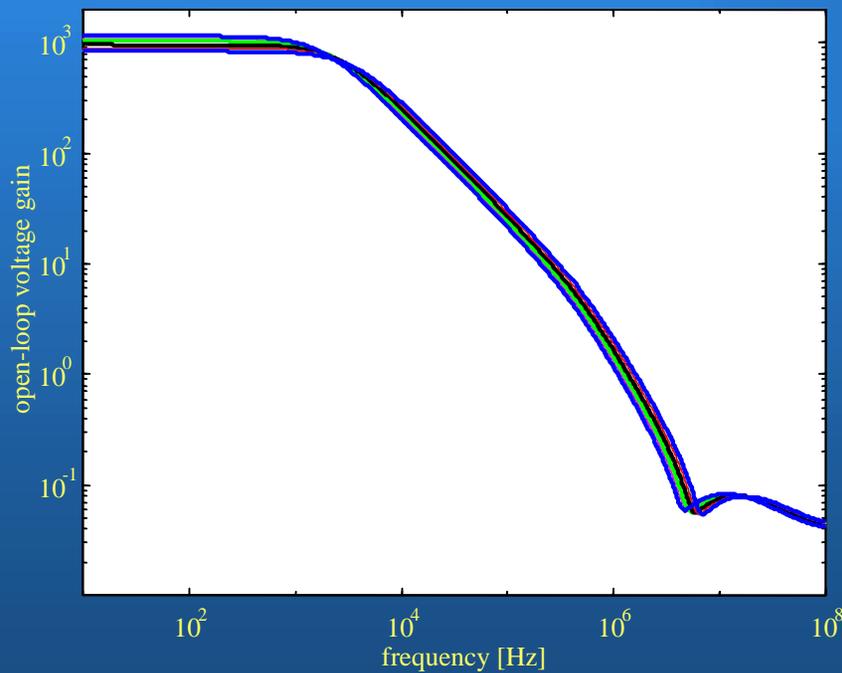


Measured vs. simulated DC characteristics

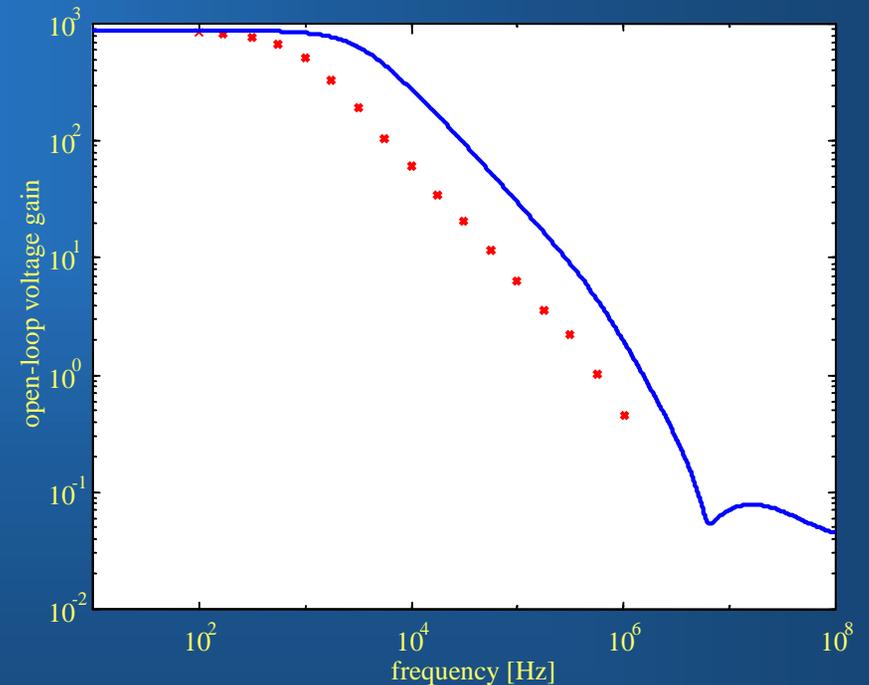


Open-loop voltage gain: simulated and measured

Simulated for different values of the tuning voltage

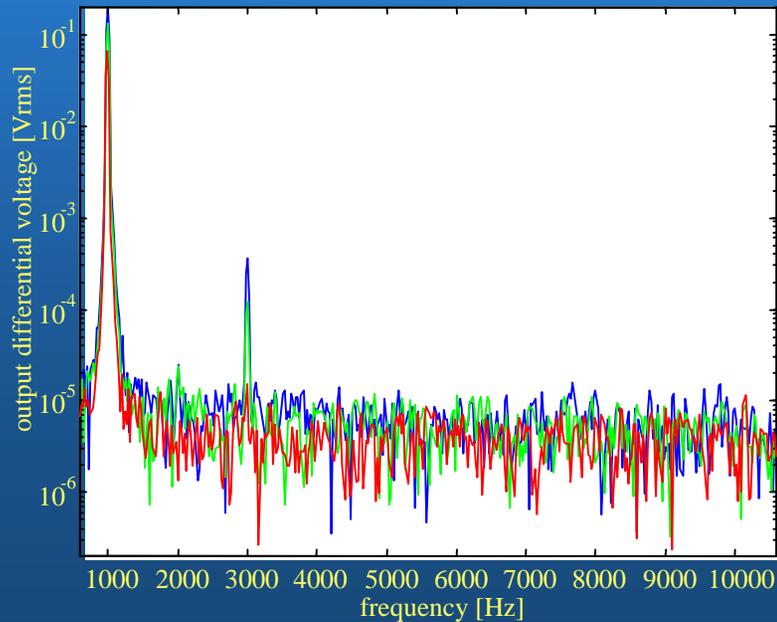
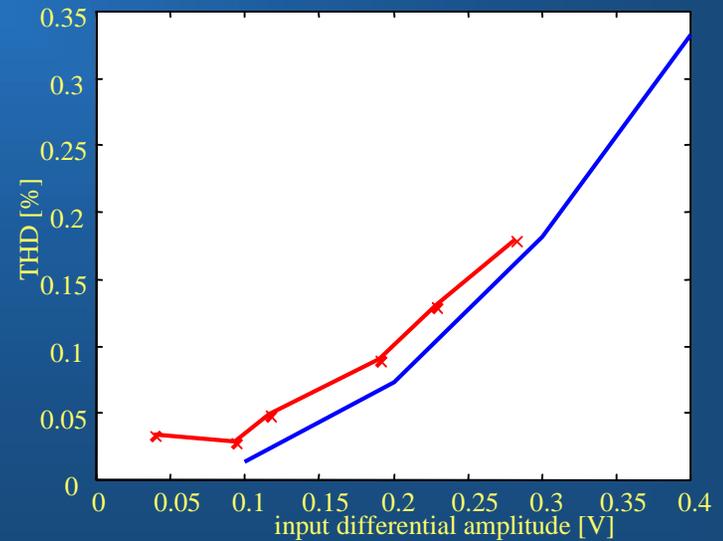
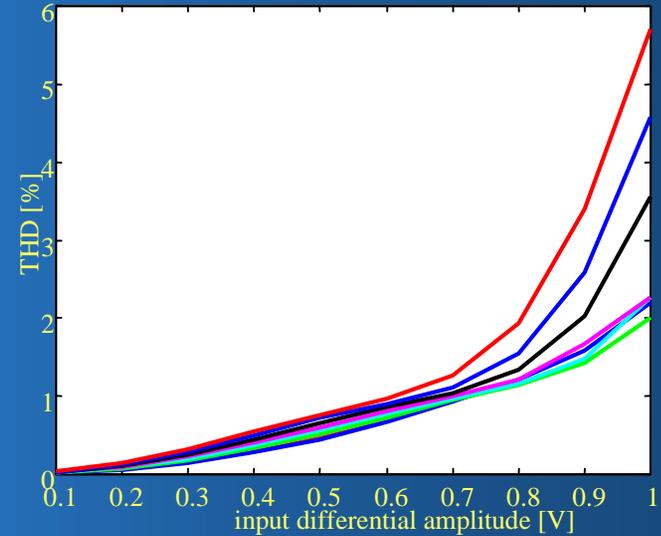


Simulated (continuous line) vs. measured (markers)



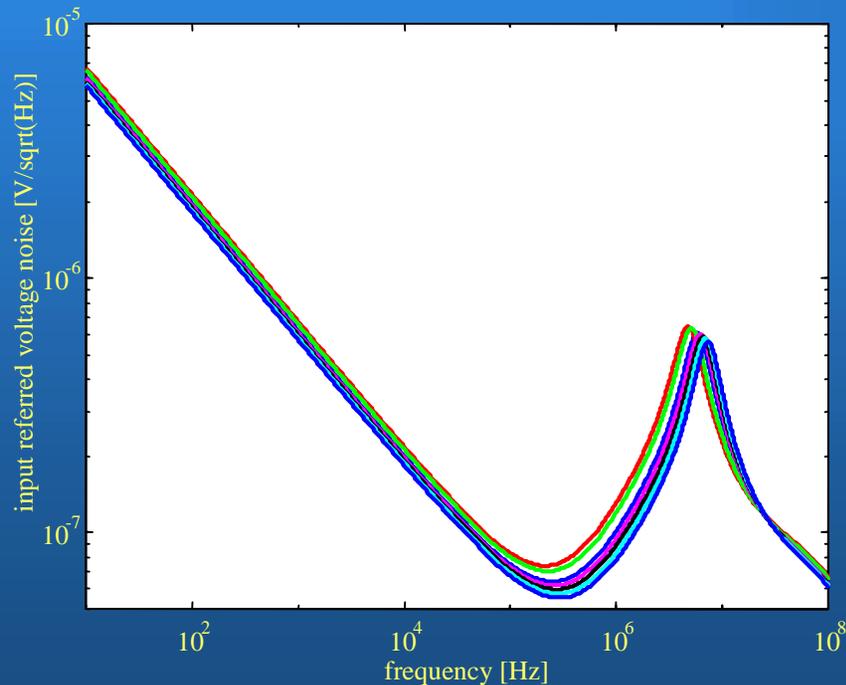
Distortions

- Simulated THD vs. input level for different tuning voltages (top right)
- Simulated and measured (markers) THD vs. input level (bottom right)
- Measured output spectrum for three different input levels (left bottom)

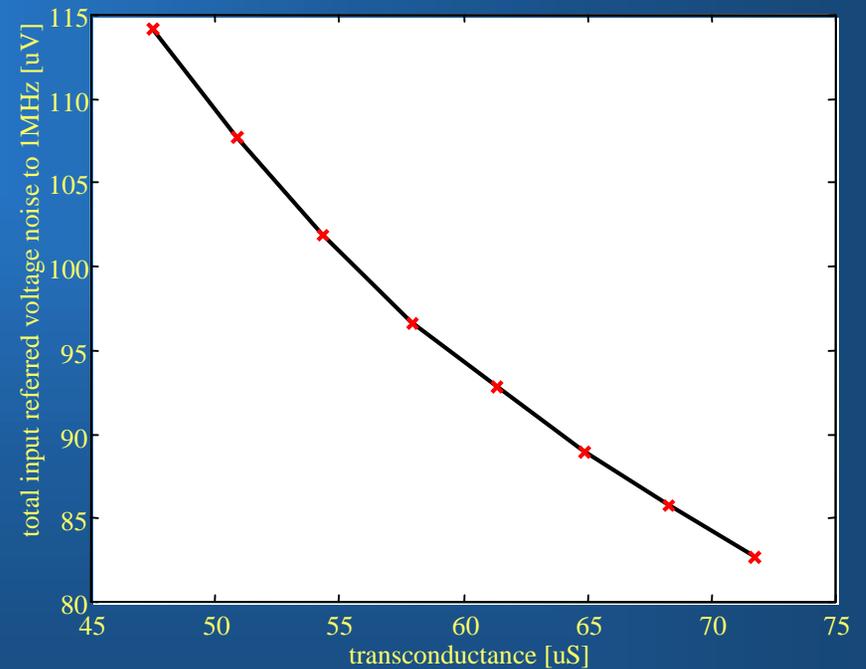


Noise simulation results

PSD of the input referred voltage noise for different tuning voltages



Total input referred voltage noise to 1MHz vs. tuned transconductance



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Resistor-based linear transconductors

- Transistor only transconductors can achieve at most 60dB linearity.
- Some applications require better linearity than achievable with transistor-only OTAs
- Solution: use resistor-based transconductors (Welland 1995, Chang 1997, Kimura 1998, Lee 2000, Chilakapati et al. 2000)
- The linearity of a differential pair with emitter/source resistive degeneration can be improved by making the output current independent of the base-to-emitter/gate-to-source voltages of the differential transistors.

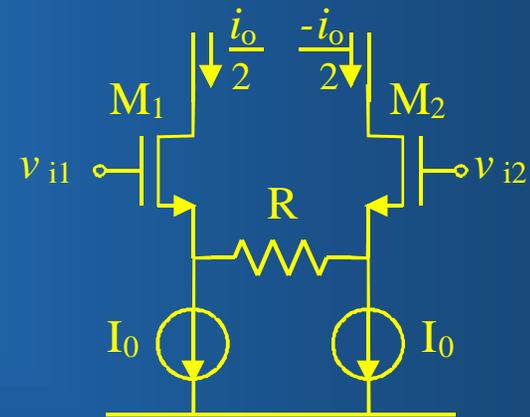
MOS differential pair with resistive source degeneration

$$v_i - R \frac{i_o}{2} = v_{GS1} - v_{GS2}$$

- If $v_{GS1} = v_{GS2}$, one has a linear transfer characteristic

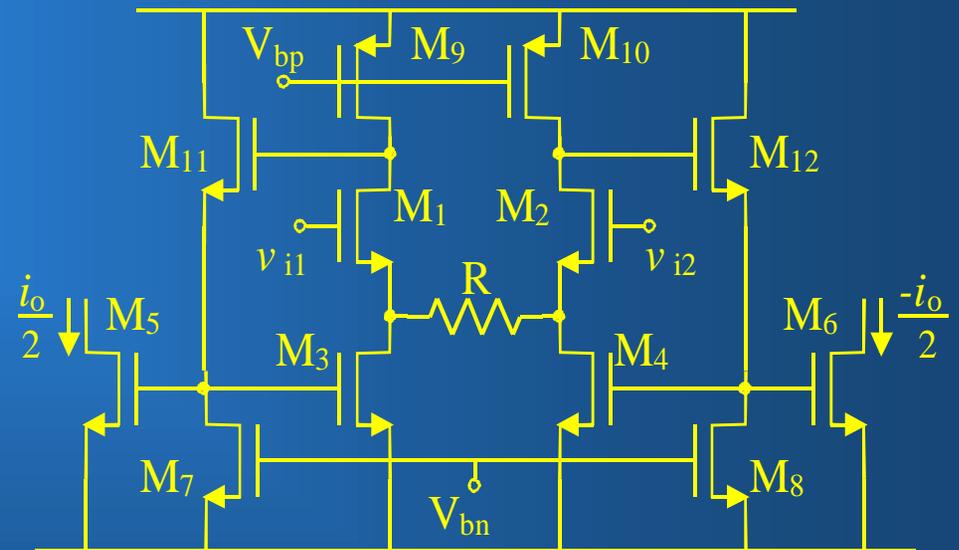
$$v_{GS} = \frac{2i_D}{\beta} = \frac{2I_D}{\beta} \sqrt{1 + \frac{i_d}{I_D}} = V_{GS\text{eff}} \sqrt{1 + \frac{i_d}{I_D}}$$

$$v_i - R \frac{i_o}{2} = V_{GS\text{eff}} \left(\sqrt{1 + \frac{i_o}{2I_0}} - \sqrt{1 - \frac{i_o}{2I_0}} \right)$$



Welland's CMOS transconductor

- Transistors M_1 - M_2 are biased at constant current by M_9 - M_{10} .
- The current through R is collected by M_3 - M_4 and reflected at the output by the current mirrors M_3 - M_5 and M_4 - M_6 .

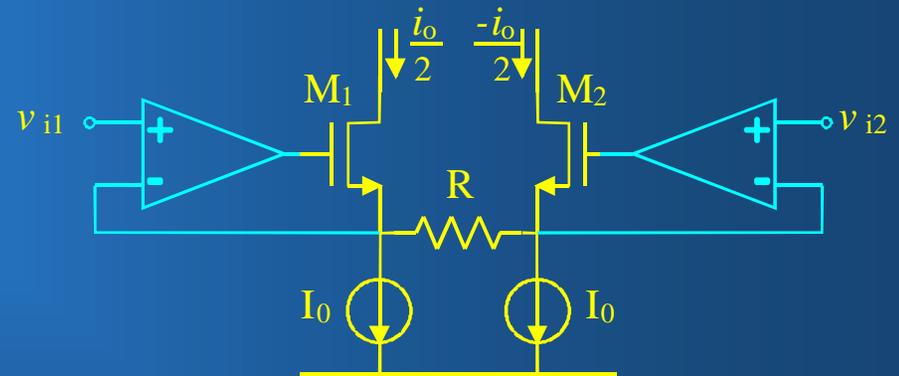


$$G_m = \frac{i_o}{v_{i1} - v_{i2}} = \frac{2}{R}$$

D. R. Welland, "Transconductance amplifiers and exponential variable gain amplifiers using the same", US Patent 5 451 901, Sept. 19, 1995.

Improving the linearity of the MOS differential pair with resistive source degeneration

- An extra pair of op-amps can be used to improve the linearity of the differential pair with resistive source degeneration.

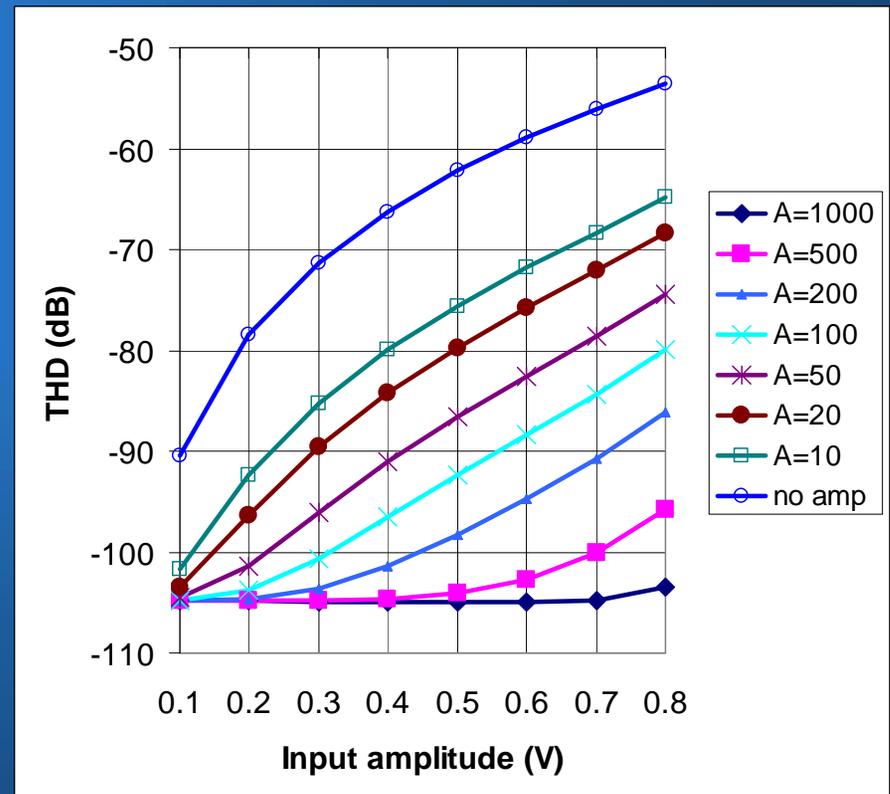


$$v_i - \frac{A+1}{A} R \frac{i_o}{2} = \frac{V_{GS_{eff}}}{A} \left(\sqrt{1 + \frac{i_o}{2I_0}} - \sqrt{1 - \frac{i_o}{2I_0}} \right)$$

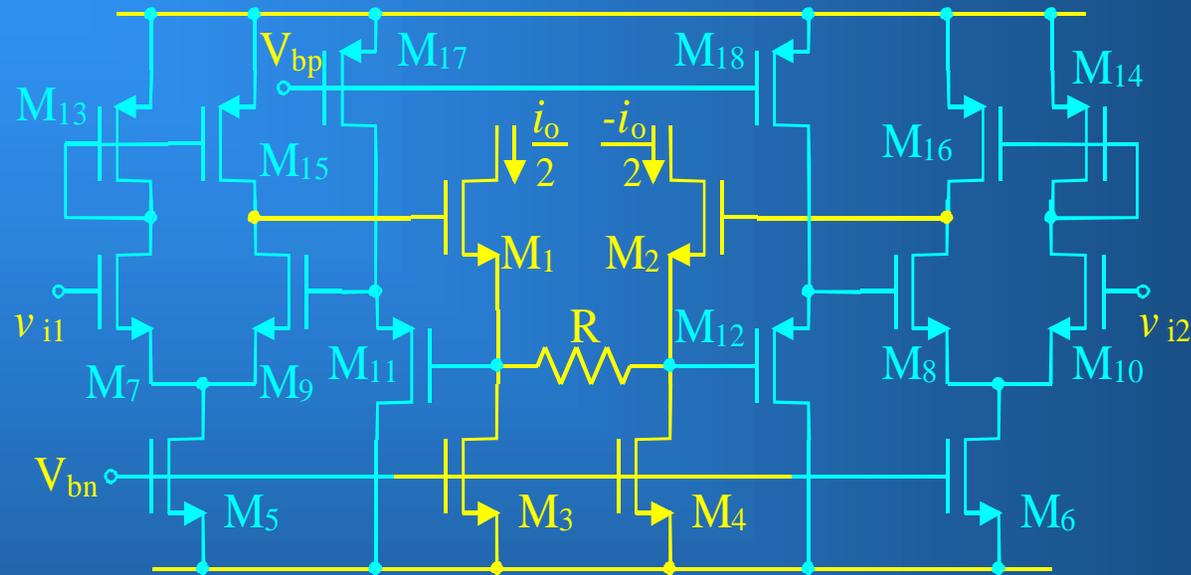
Z.Y. Chang, D. Haspelagh, and J. Verfaillie, "A highly linear CMOS G_m -C bandpass filter with on-chip automatic tuning," IEEE J. Solid-State Circuits, vol. SC-32, pp. 388-397, March 1997.

Achievable linearity

- Improvement in linearity of 25-30dB for $A=40\text{dB}$ compared to the no-amp case.
- Spice simulations:
 $A=40\text{dB} \Rightarrow \text{THD} < -80\text{dB}$,
 $V_{in} \leq 1.6V_{p-p}$
 $(R=4\text{k}\Omega, V_{GS\text{eff}}=50\text{mV}, I_0=250\mu\text{A})$.

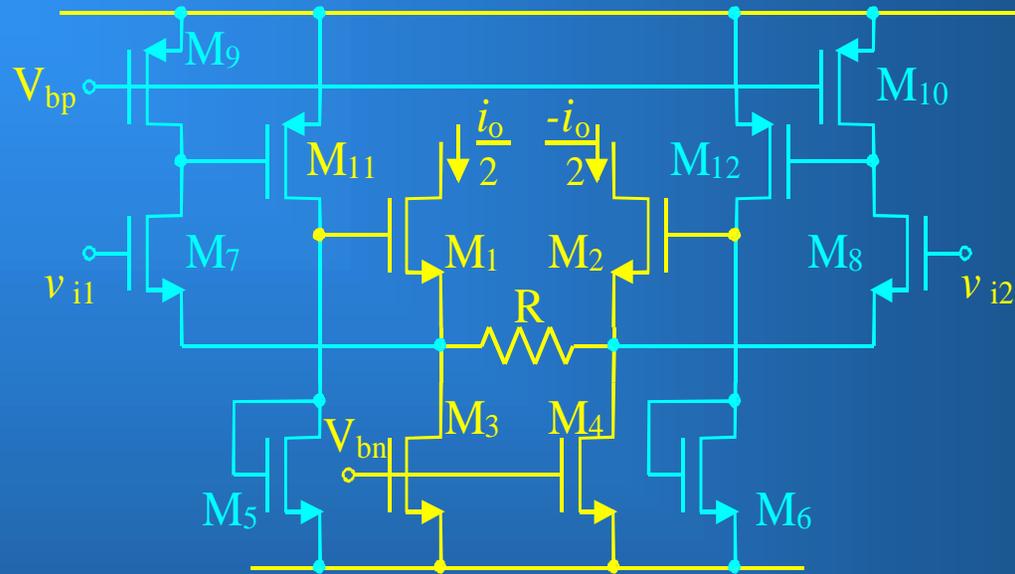


Proposed transconductor: structure I



- The amplifiers are realized as single-ended differential stages;
- Two voltage level shifters (M_{11} - M_{17} , M_{12} - M_{18}) ensure the low-voltage operation

Proposed transconductor: structure II

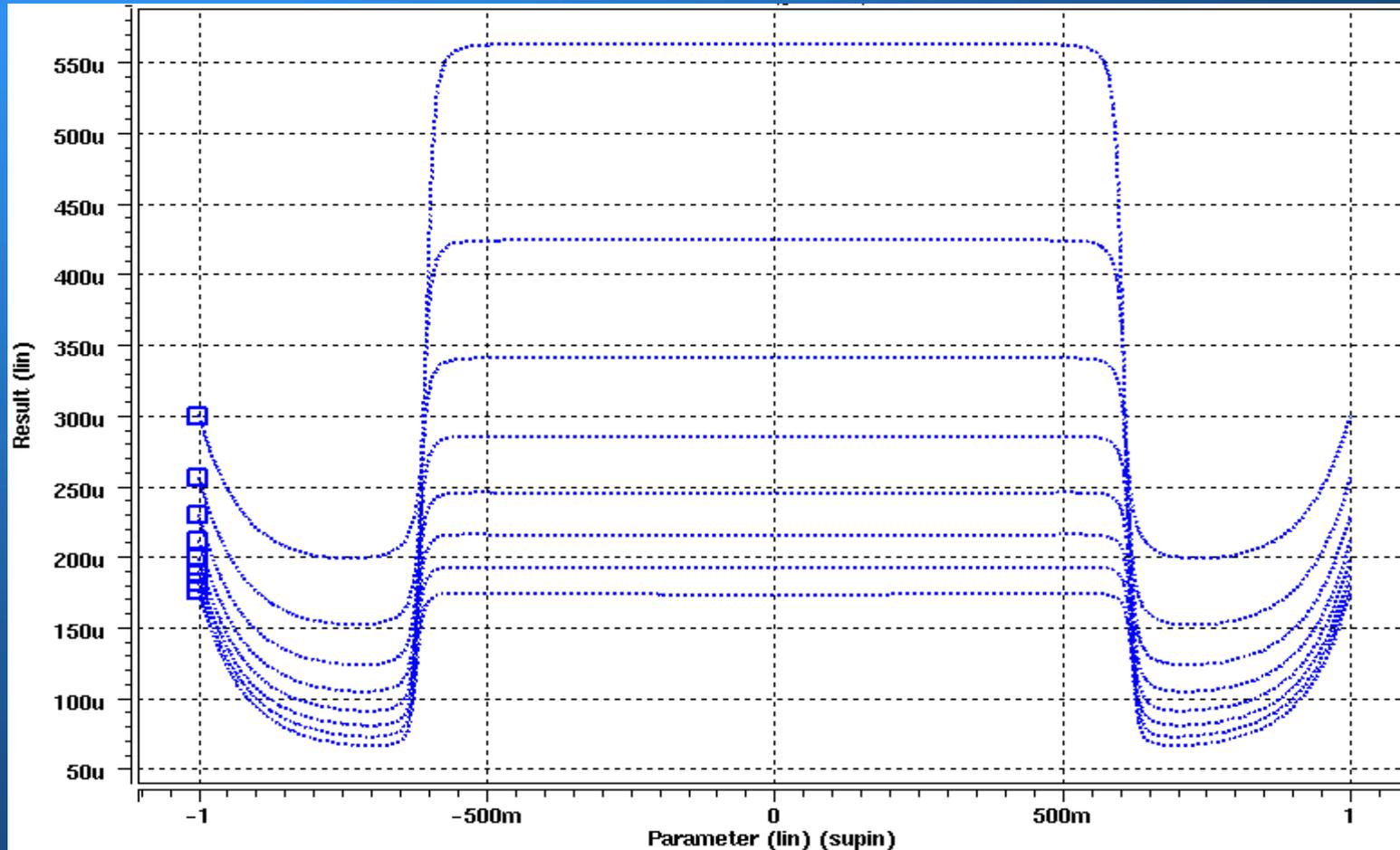


- A single stage (M₇-M₉, respectively M₈-M₁₀) is enough to realize the linearizing amplifier.
- A second inverting stage (M₁₁-M₅, respectively M₁₂-M₆) is needed to achieve negative feedback.

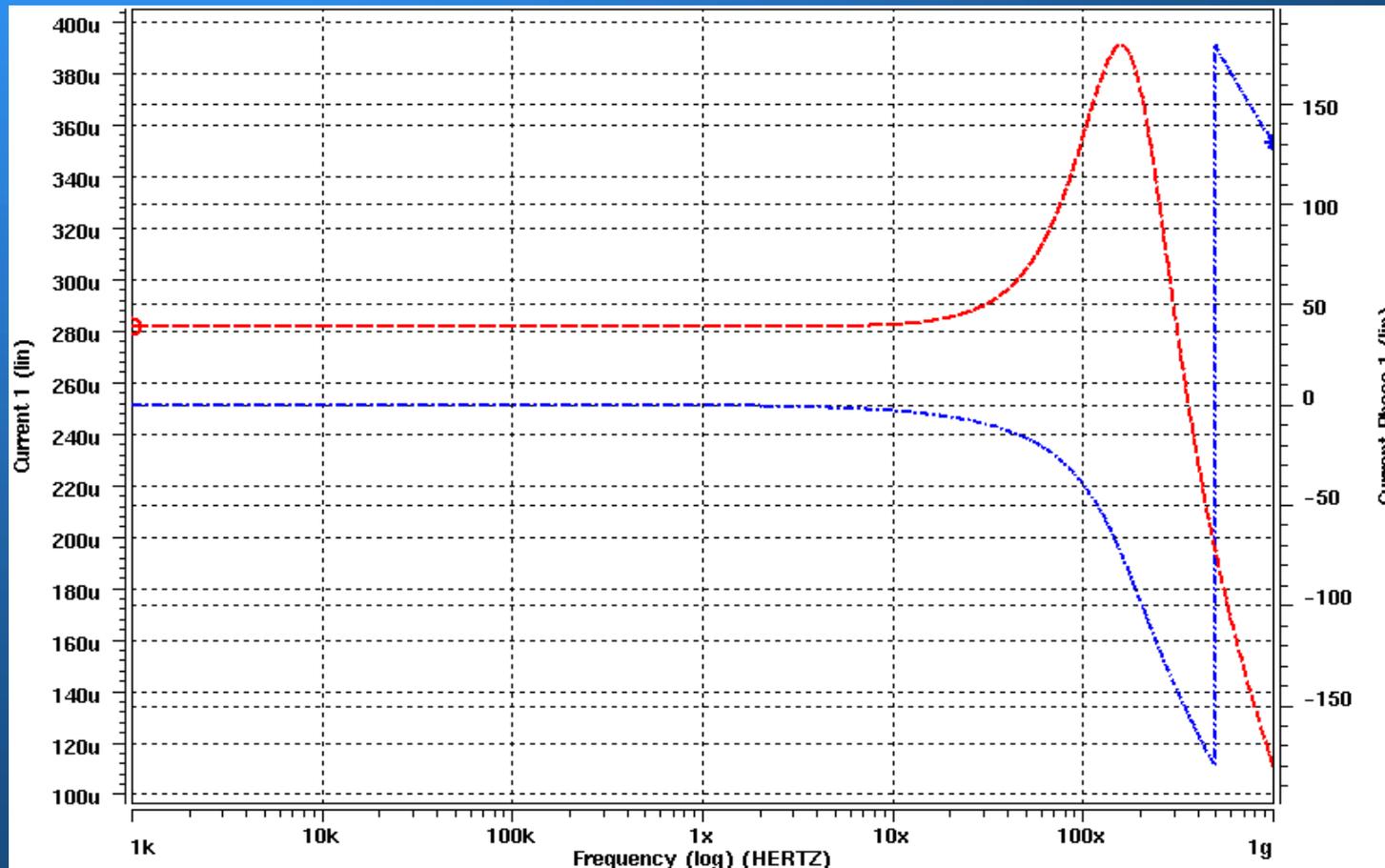
Simulation results (structure II)

- Linear range smaller than the predicted one:
 - dynamic range of amps
 - low supply voltage
- Bandwidth of linearizing amplifier sets the linearity bandwidth.
- Input NMOS transistors ensure better linearity/noise performance for the same power consumption
- Equal input and output common mode voltages of 1.2V for a supply voltage of 1.8V.

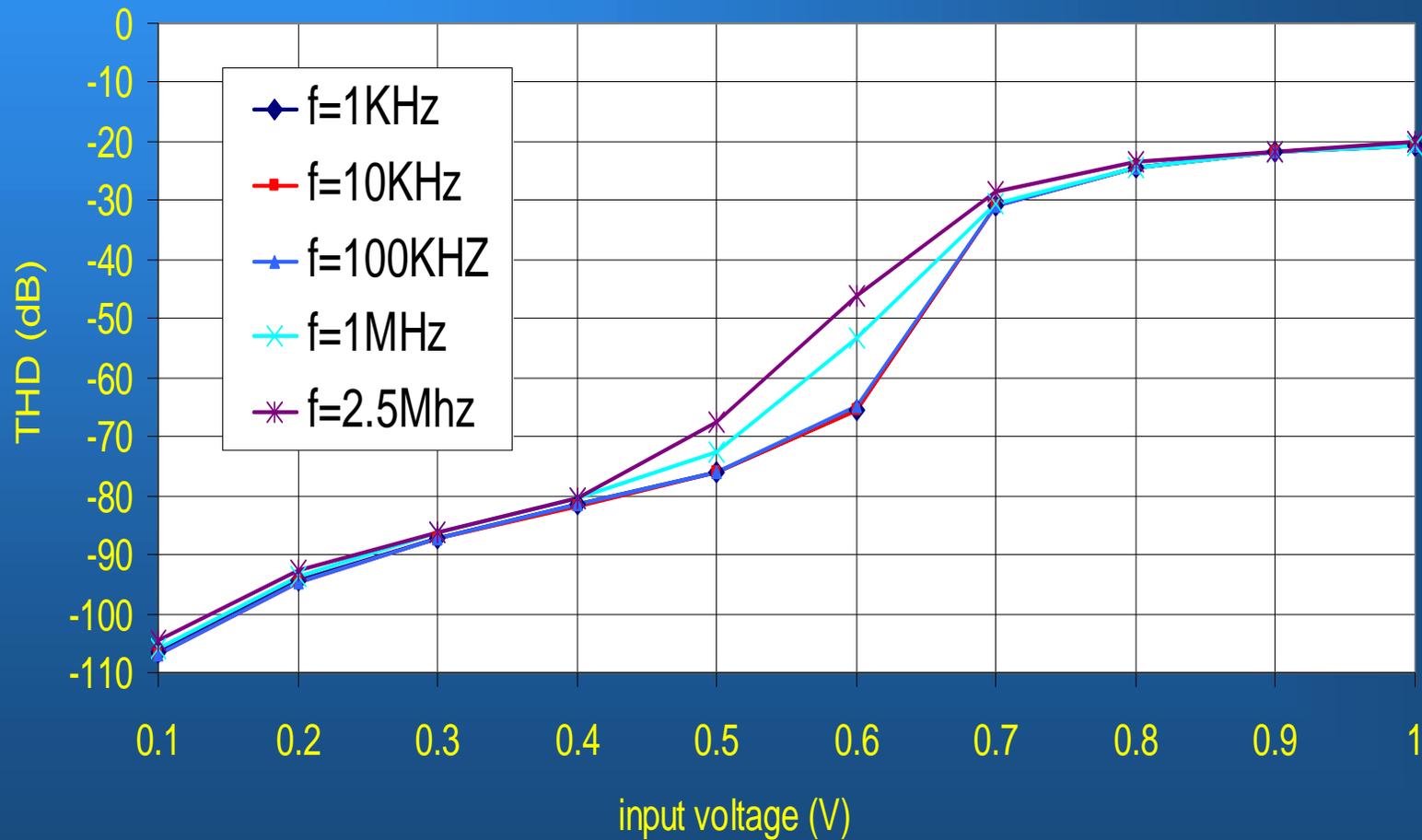
Transconductance



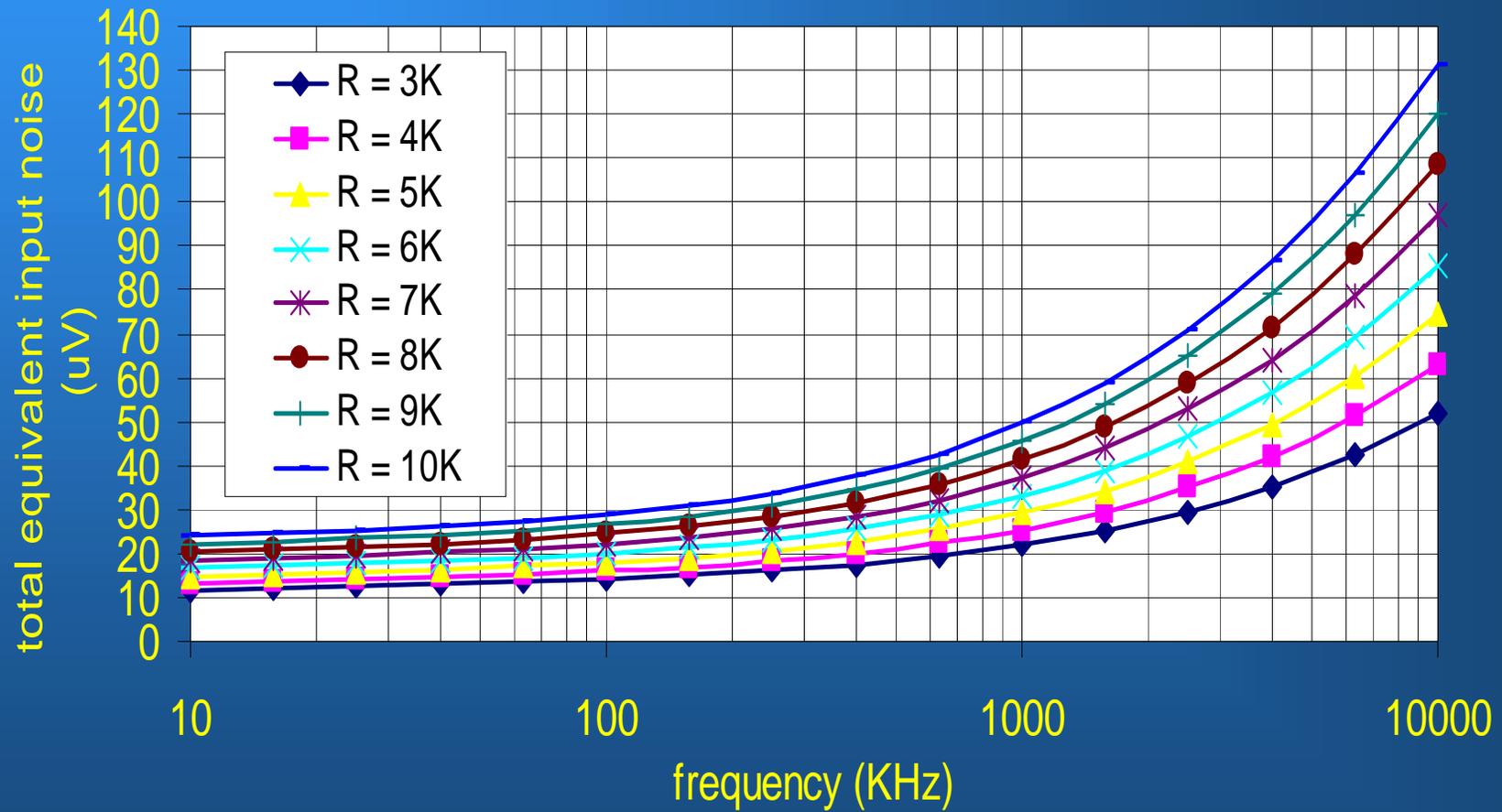
Frequency response



Total harmonic distortion



Noise simulations



Conclusions

- Transistor-only CMOS OTAs (transconductors) can achieve linearity up to approx. 50-60dB
- The linearity limitation of transistor-only transconductors is due to the non-perfect quadratic equation describing the i - v characteristic of MOSFETs
- Some applications (e.g. high SNR continuous-time Delta-Sigma modulators) require better linearity
- Resistor-based CMOS transconductors exhibit very good linearity, counter-balanced by some drawbacks:
 - more complex and/or coarse tunability
 - highly linear resistors not readily available in standard CMOS processes